Corvette-F1
User Manual

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Revision History

Rev.	Revision Date	Revised Content
1.4	2019/09/10	1. Remove V3 debugger to optional in section 2.1 & 2.4
1.3	2019/04/26	1. Add support N22 in section 1.1 & 2.1 2. Updated Figure 1 3. Update FPGA Pin Assign in section 2.12
1.2	2019/04/10	Change the wording of Corvette F1 to Corvette-F1
1.1	2018/06/14	1. Change title from AICE-MINI & V5 debugger to V3 & V5 debugger in section 2.4 2. Add WEEE directive information in Chapter 5 3. Updated Figure 2, Figure 3, Figure 4, Figure 7
1.0	2018/05/07	Initial release

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Typographical Convention Index

Document Element	Font	Font Style	Size	Color
Normal text	Georgia	Normal	12	Black
`Command line, source code or file paths`	`Lucida Console`	`Normal`	`11`	`Indigo`
`VARIABLES OR PARAMETERS IN COMMAND LINE, SOURCE CODE OR FILE PATHS`	**`LUCIDA CONSOLE`**	**`BOLD + ALL-CAPS`**	**`11`**	**`INDIGO`**
Note or warning	Georgia	Normal	12	Red
Hyperlink	Georgia	Underlined	12	Blue

1. Product Overview

1.1. Introduction

Corvette-F1 is a palm-sized, Arduino-compatible evaluation platform based on Xilinx Artix7 XC7A100T FPGA, which fully supports AndesCore N25 and AndeShape™ Platform AE250. Users can easily build the prototypes and applications of IoT devices under Arduino standard IDE and full-featured AndeSight™ IDE.

Warning: Corvette-F1 runs only at 3.3V. The maximum tolerate voltage of the I/O pins is 3.3V. Applying voltages higher than 3.3V to any I/O pin could damage the board.

2. Corvette-F1 Hardware Features

2.1. Features

- Easy to use
  - Xilinx Artix7 XC7A100T-1FTG256
  - Built-in V5 debugger for flash burner and program debugging functions
  - Built-in micro USB to UART bridge
  - Powered via the USB connector
- AndesCore and AndeShape Platform IP support
  - N25
  - AE250
- Wireless Support
  - Built-in Microchip ATWINC1510-MR210PB IoT Module
  - Support IEEE 802.11 b/g/n
- Peripheral Device
  - 4MB SPI Flash for user's program & data
  - 4 LEDs and 4 user buttons
  - GPIO
  - PWM
  - UART
  - I2C
  - SPI

2.2. Power

The Corvette-F1 can be powered via either on-board micro USB connectors (CON1 or CON2). The power source is selected automatically. When connect 2 USB cables to both of micro USB connectors, the maximum current draw can be up to 1A through 2 USB 2.0 ports.

2.3. Memory

Corvette-F1 has 2 SPI flash memory, U2 and U10. U2 is a 16MB for storing FPGA bitstream and U10 is 4MB for storing boot code and user's program and data.

2.4. V5 debugger

Corvette-F1 build in one set of debuggers to support AndesCore V5 family.
Users, they can get V5 debugging and UART functions by just connecting CON2 to an USB port of the host PC with a micro USB cable. This is significantly increasing the ease-of-use for software debugging and also can be used for an external SPI flash programmer.

2.5. System Block Diagram

The following Figure 1 shows the system diagram of Corvette-F1.

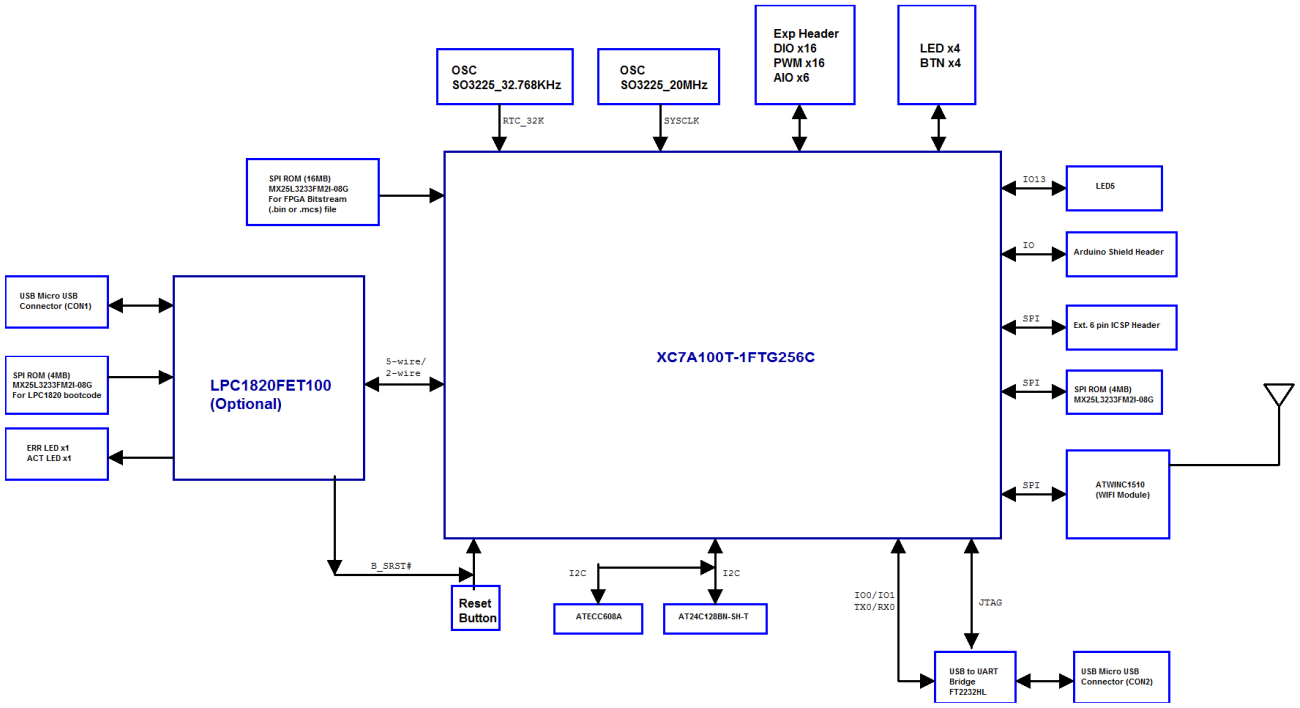

Figure 1. System Block Diagram

2.6. Corvette-F1 Physical View

The following Figure 2 is the picture of Corvette-F1

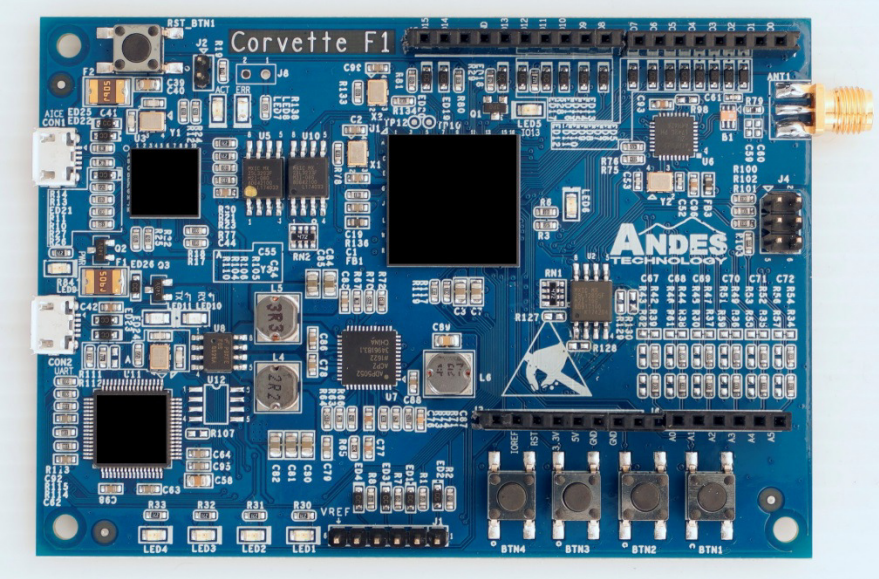

Figure 2. Picture of Corvette-F1

2.7. IO Connectors

The following Table 1 describes I/O connector function of Corvette-F1. Then the following Figure 3 describes the location of Corvette-F1 connectors.

Table 1. Corvette-F1 connector annotator and function

I/O annotator	Function	Remark
J1	Artix7 FPGA JTAG Download Connector	
J3	Arduino shield header	
J4	SPI Connector	
J5	Arduino shield header	
J6	Arduino shield header	
J7	Arduino shield header	
CON2	Micro USB Connector for V5 debugger and UART	
RST_BTN1	H/W Reset Button	
BTN1, BTN2, BTN3, BTN4	4 push buttons	
ANT1	SMA Connector	

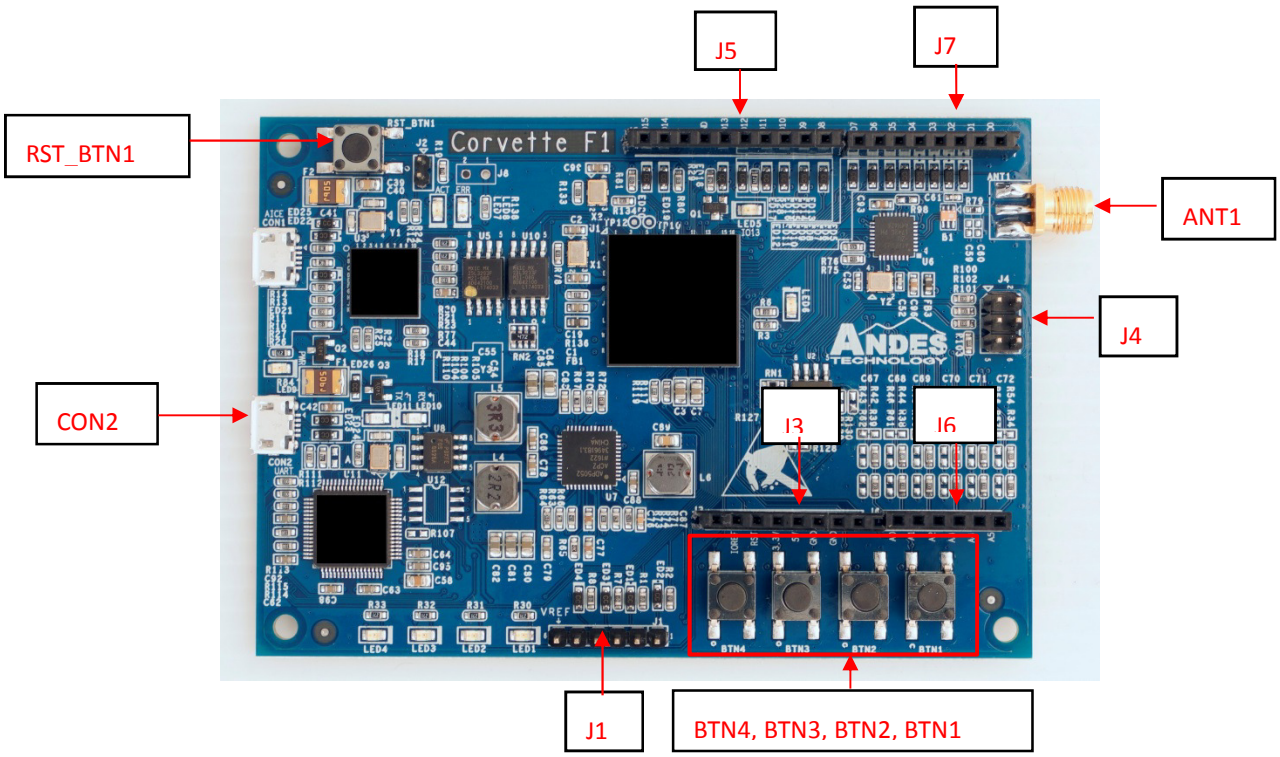

Figure 3. Location of Corvette-F1 connectors

2.8. Main Components and LEDs

The following Table 2 describes each main component and LED. Figure 4 will show the location of each main component and LED.

Table 2. Main Components and LEDs

Annotator	Function	Remark
LED1, LED2, LED3, LED4	4 indicator LEDs	
LED5	LED indicator for D13 pin	
LED6	LED indicator for Artix7 FPGA is done	
LED7	AICE is communicating with the target system , active LED	
LED8	Target system error (Timeout), error LED	
LED9	System power is on	
LED10	LED indicator for RX communication	
LED11	LED indicator for TX communication	
U1	ARTIX-7 FPGA (XC7A100T-1FTG256C)	
U2	16MB SPI Flash (MX25L3233FM2I-08G)	
U3	AICE MCU	
U6	AT86RF233 2.4GHz transceiver	
U7	ADP5052 power supply	
U10	4MB system SPI Flash (MX25L3233FM2I-08G)	
U11	FT2232HL USB to UART/FIFO	

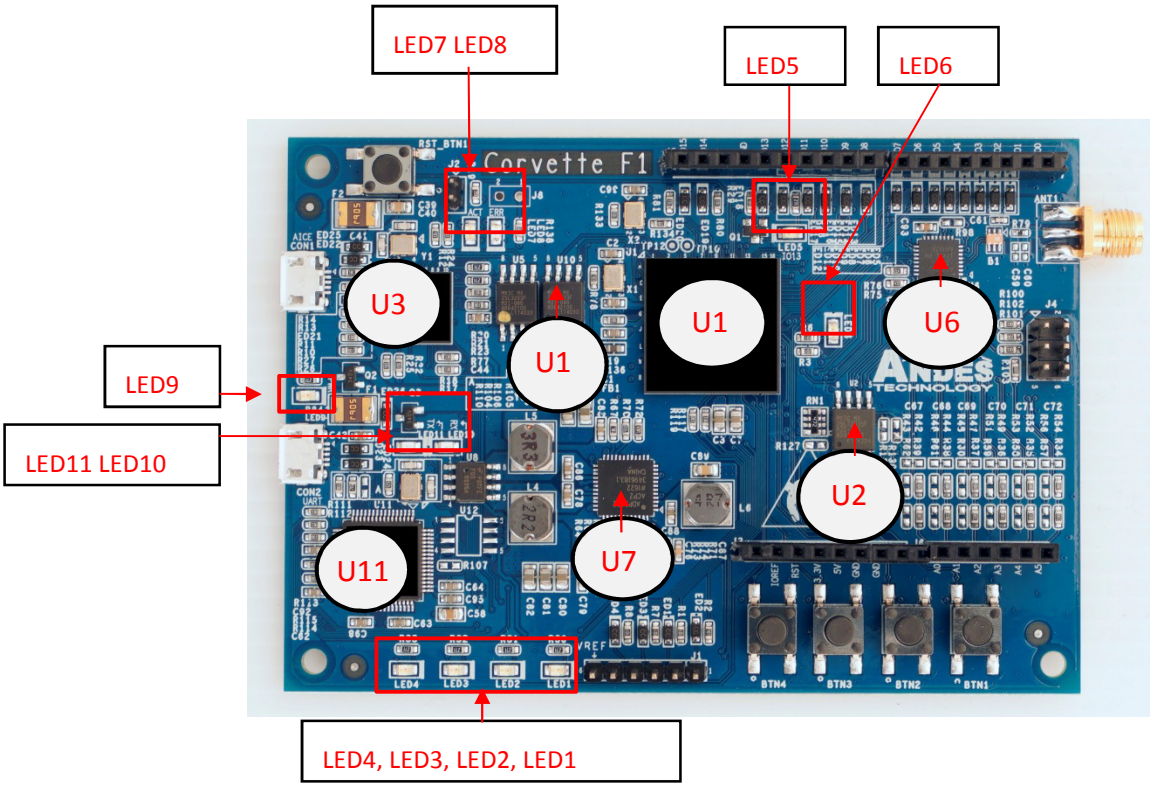

Figure 4. Component and LED placement

2.9. Connector Pin Define

2.9.1. ARTIX-7 JTAG Connector (J1)

Table 3 lists the pin definition of J1 connector.

Table 3. J1 Connector Pin Definition

Pin No.	Signal Name	Pin No.	Signal Name
1	A7_TMS	2	A7_TDI
3	A7_TDO	4	A7_TCK
5	GND	6	V_3V3

2.9.2. SPI Connector (J4)

Table 4 lists the pin definition of J4 connector.

Table 4. J4 Connector Pin Definition

Pin No.	Signal Name	Pin No.	Signal Name
1	SPI_MISO	2	V_5V
3	SPI_SCK	4	SPI_MOSI
5	RESET#	6	GND

2.10. Power Tree

Figure 5 shows the power tree of Corvette-F1. The CON1 and the CON2 can be the sources of V_5V individually or simultaneously, and then the V_5V is the input of U7 regulator to generate all needing DC outputs.

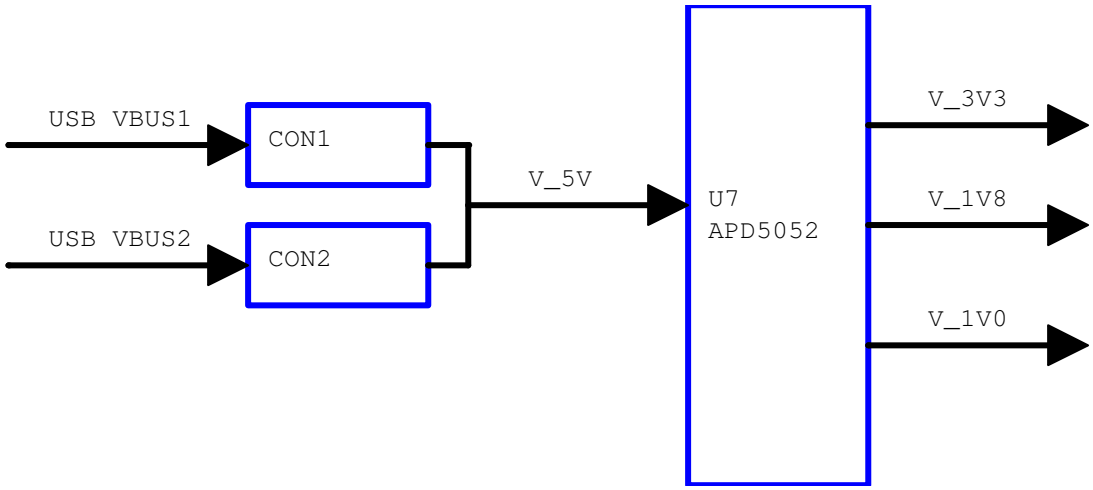

Figure 5. Power Tree of Corvette-F1

2.11. Clock Source

Figure 6 shows the clock sources of Corvette-F1.

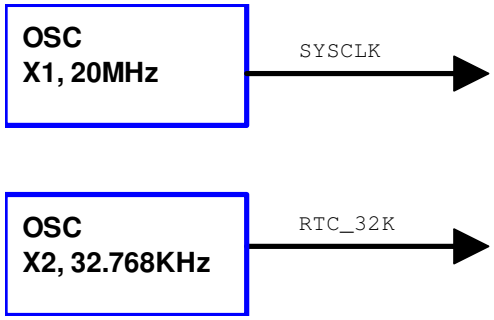

Figure 6. Clock Source of Corvette-F1

Table 5. Clock OSC function table

Domain	Annotator	Note
U1, XC7A100T-1FTG256C	X1	20MHz OSC. used for system main clock
	X2	32.768KHz OSC. used for RTC
U3, LPC1820	Y1	12MHz_CRY used for LPC1820 clock source
U6, AT86RF233	Y2	16MHz_CRY used for RF transceiver clock source
U11, FT2232HL	Y3	12MHz_CRY used for FT2232HL clock source

2.12. FPGA Pin Assignment

Bank	Pin	External Connector	External Link
0	H10	LED6	LED6.1 Ext Pu11 up (200R)
0	K8		
0	G7		
0	G8		
0	J8		
0	J7		
0	F8		
0	L7		
0	K7		
0	H7		
0	H8		
0	E8	U2	U2.6
0	M9		

Bank	Pin	External Connector	External Link
0	M10		
0	K10		Ext. Pu11 up (4.7KR)
0	N7	J1	J1.2
0	N8	J1	J1.3
0	M11		
0	E7		
0	L9		Ext. Pu11 up (4.7KR)
0	M7	J1	J1.1
14	K12		
14	J13	U2	U2.5
14	J14	U2	U2.1
14	K15	U2	U2.3
14	K16	U2	U2.7
14	L15		
14	M15	U6	U6.24
14	L14		
14	M14	U6	U6.19
14	K13		
14	L13		
14	L12	U2	U2.1
14	M12		
14	M16	U6	U6.11
14	N16	U6	U6.23
14	P15	BTN3	BTN3.1, BTN3.3
14	P16	BTN1	BTN1.1, BTN1.3
14	R15	U6	U6.22
14	R16	BTN2	BTN2.1, BTN2.3

Bank	Pin	External Connector	External Link
14	T14	U6	U6.20
14	T15	BTN4	BTN4.1, BTN4.3
14	N13	LED4	LED4.1
14	P13	LED3	LED3.1
14	N14	LED2	LED2.1
14	P14	LED1	LED1.1
14	N11	U11	U11.16
14	N12	U11	U11.18
14	P10	U11	U11.19
14	P11	U11	U11.17
14	R12		
14	T12		
14	R13		
14	T13		
14	R10		
14	R11		
14	N9		
14	P9		
14	M6		
14	N6		
14	P8		
14	R8		
14	T7		
14	T8		
14	T9		
14	T10		
14	R5		
14	T5		

Bank	Pin	External Connector	External Link
14	R6		
14	R7		
14	P6		
15	D10		
15	C8	J6	J6.1
15	C9		Ext. Pull down
15	A8	J5	J5.1
15	A9	J5	J5.2
15	B9	J6	J6.2
15	A10		Ext. Pull down
15	B10	J5	J5.5
15	B11	J5	J5.6
15	B12	J6	J6.5
15	A12		Ext. Pull down
15	D8		
15	D9		
15	A13	J6	J6.3
15	A14		Ext. Pull down
15	C14		
15	B14		
15	B15	J6	J6.4
15	A15		Ext. Pull down
15	C16	J6	J6.6
15	B16		Ext. Pull down
15	C11		
15	C12		
15	D13		

Bank	Pin	External Connector	External Link
15	C13		
15	E12	X2	X2.3
15	E13	U11	U11.26
15	E11	U11	U11.23
15	D11		
15	D14		
15	D15	J5	J5.7
15	F12		
15	F13	J4	J4.1
15	E16	J5	J5.10
15	D16	J5	J5.9
15	F15	J7	J7.1
15	E15	J5	J5.8
15	H11		
15	G12		
15	H12	J4	J4.4
15	H13	J4	J4.3
15	G14	J7	J7.7
15	F14		
15	H16	J7	J7.2
15	G16	J7	J7.4
15	J15	J7	J7.5
15	J16	J7	J7.8
15	H14	J7	J7.6
15	G15	J7	J7.3
15	G11		
34	L5		

Bank	Pin	External Connector	External Link
34	L4	U6	U6.8
34	M4		
34	M2		
34	M1		
34	N3		
34	N2		
34	N1		
34	P1		
34	P4		
34	P3		
34	M5		
34	N4		
34	R2		
34	R1		
34	R3		
34	T2		
34	T4		
34	T3		
34	P5		
35	E6		
35	B7		
35	A7		
35	B6		
35	B5		
35	A5		
35	A4		
35	B4		

Bank	Pin	External Connector	External Link
35	A3	U10	U10.7
35	C7		
35	C6		
35	D6		
35	D5		
35	C3	U10	U10.1
35	C2	U3, J3. J4, RST_BTN1	U3.H1, J3.3, J4.5, RST_BTN1.3
35	B2	U3	U3.E8
35	A2	U3	U3.G2
35	C1	U3	U3.H9
35	B1	U3	U3.G1
35	E2	U10	U10.5
35	D1		
35	E3	U10	U10.3
35	D3	U10	U10.2
35	D4	U10	U10.6
35	C4		
35	F5	X1	X1.3
35	E5		
35	F4	U3	U3.K8
35	F3		
35	F2		
35	E1		
35	G5		
35	G4		
35	G2		
35	G1		
35	H5		

Bank	Pin	External Connector	External Link
35	H4		
35	J5		
35	J4		
35	H2		
35	H1		
35	J3		
35	H3		
35	K1		
35	J1		
35	L3		
35	L2		
35	K3		
35	K2		
35	K5		

3. Programming FPGA of Corvette-F1

This section describes the sequence of programming the FPGA bitstream file (.mcs or .bin file) to the SPI flash of Corvette-F1 with Xilinx Vivado Design Suit.

3.1. Host PC Requirements

- Xilinx Vivado Design Suit 2017.2 or latter
- Corvette-F1 programming package, including the following files:
  - For V5 users: ae250_chip.mcs or ae250_chip.bin
- Xilinx Platform Cable USB or Platform Cable USB II

■ Warning Notices: The system power must be turned off before plug/unplug Xilinx Platform Cable to Corvette-F1 main board.

3.2. Programming Steps

- Connect Xilinx Platform Cable to a USB port of Host PC and JTAG port (J1) on Corvette-F1 as Figure 7.
- Supply 5V power from Host PC by USB cable. The Power LED (LED9) should be lighted on as Figure 7.
- Make sure the green LED on the Xilinx Platform Cable is lighting up.

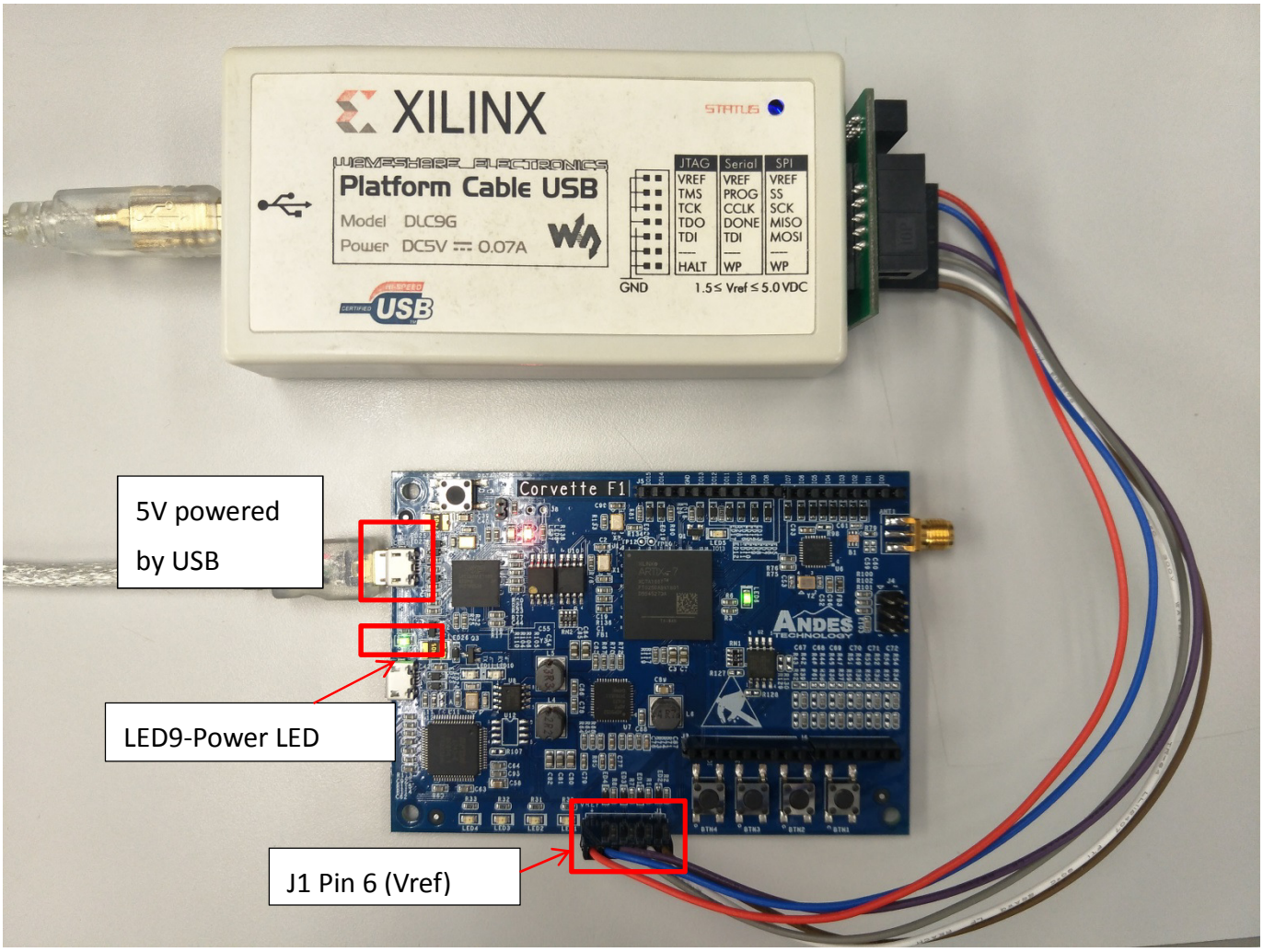

Figure 7. Platform Setup up

- Launch Vivado IDE
- Click on Open Hardware Manager icon.

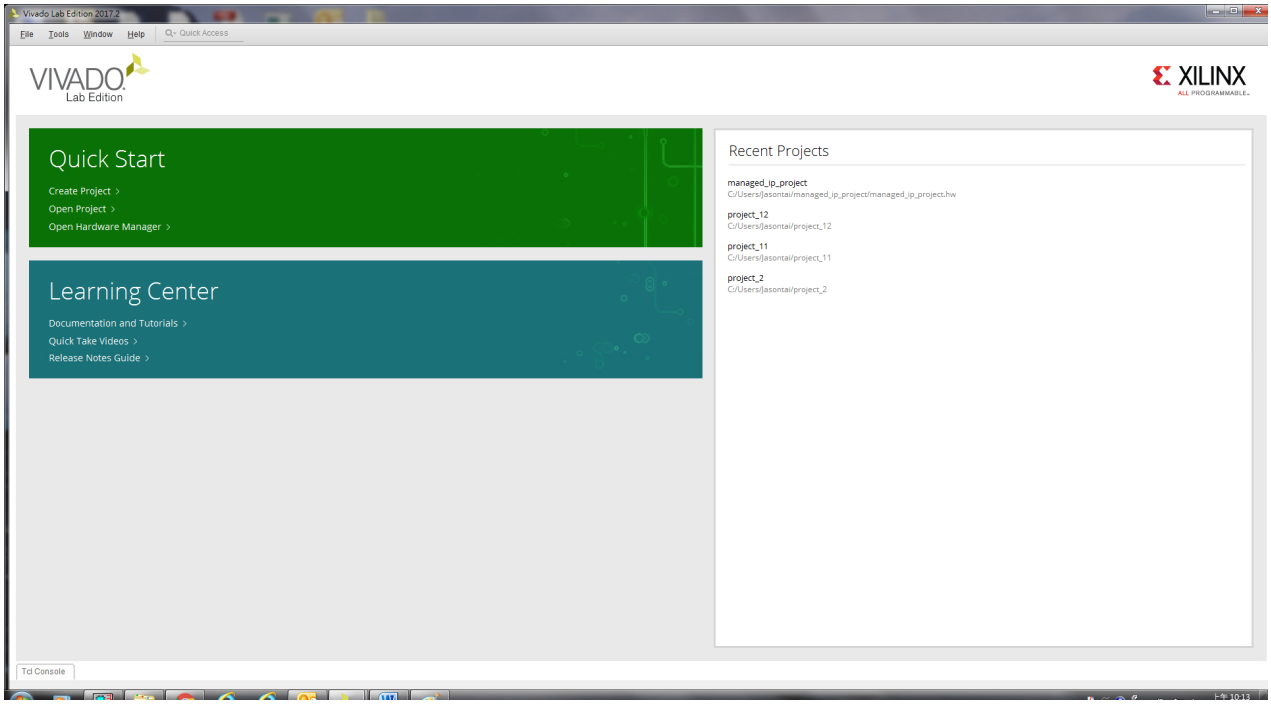

Figure 8. Open Hardware Manager icon

❖ Click on “Tools→ Auto Connect” as Figure 9.

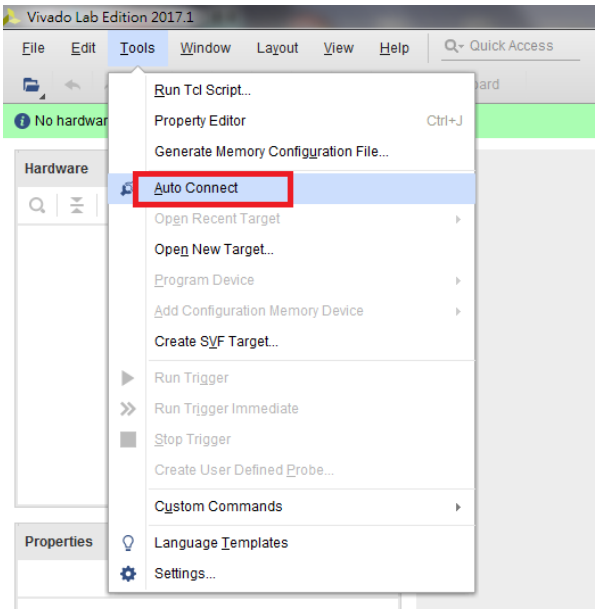

Figure 9. Auto Connect

❖ Right click on “xc7a100t_0 “ and select “Add Configuration Memory Device” as Figure 10.

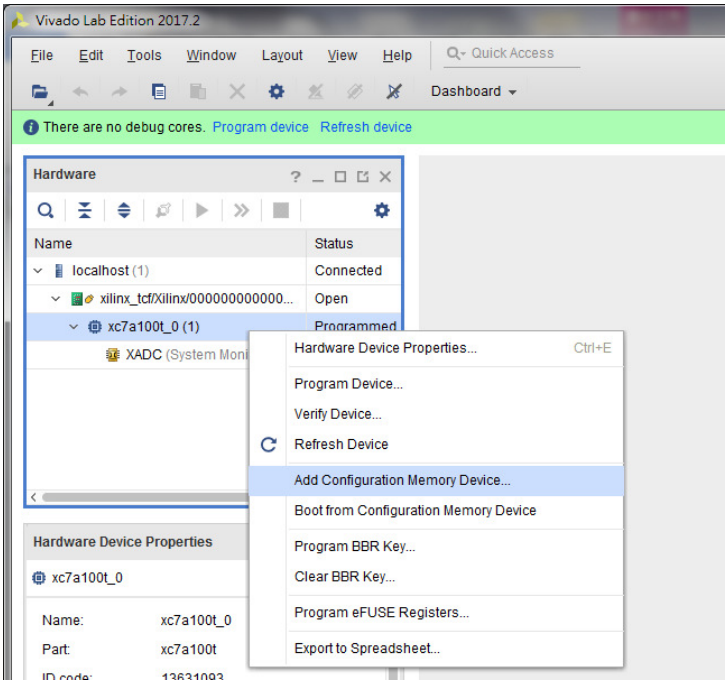

Figure 10. Add Configuration Memory Device

❖ Type “mx25l12845g-spi-x1_x2_x4” into Search field and select the device then click on “OK” as Figure 11.

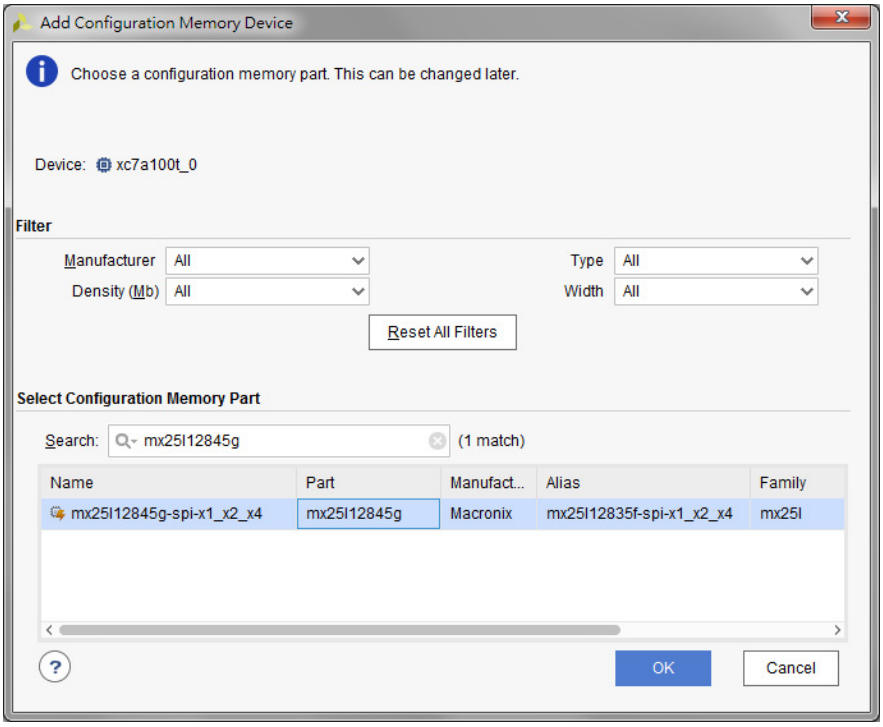

Figure 11. Select “mx25l12845g-spi-x1_x2_x4” memory

❖ Click “OK” to confirm “Add Configuration Memory Device Completed” as Figure 12.

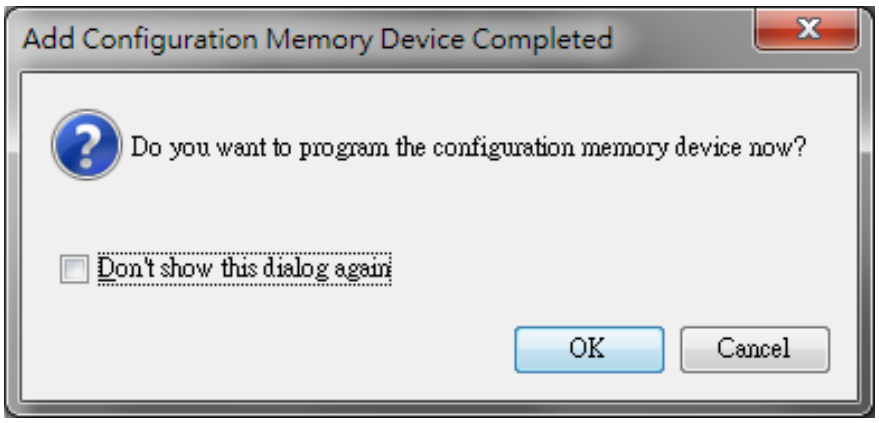

Figure 12. Confirm “Add Configuration Device Completed”

- Select “ae210_chip.mcs” or “ae210_chip.bin” from working directory and then click “OK” as Figure 13.

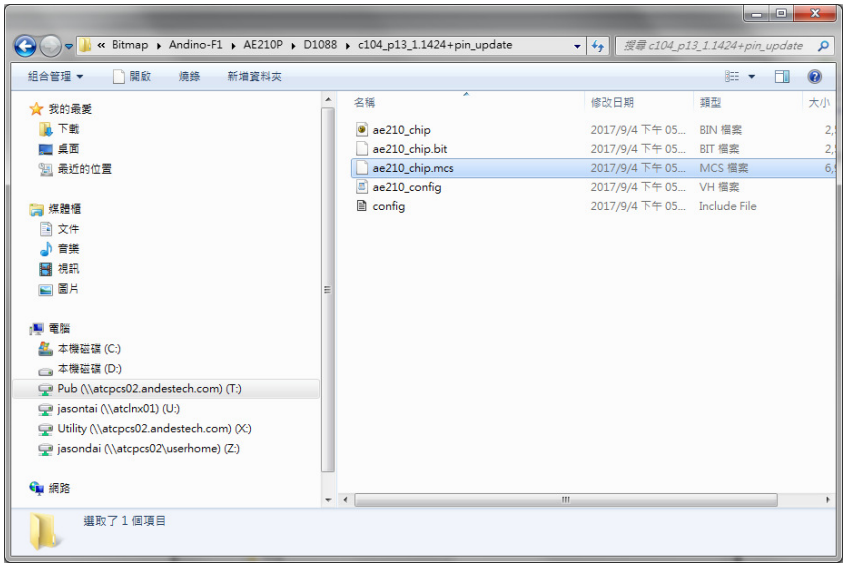

Figure 13. Specify the bitsream file for FPGA configuration

- Click “OK” in Program Configuration Memory Device page as Figure 14.

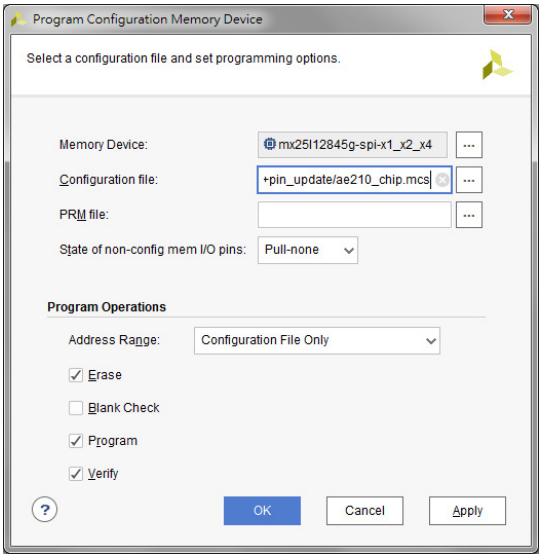

Figure 14. Program Configuration Memory Device

❖ Performing program operation as Figure 15.

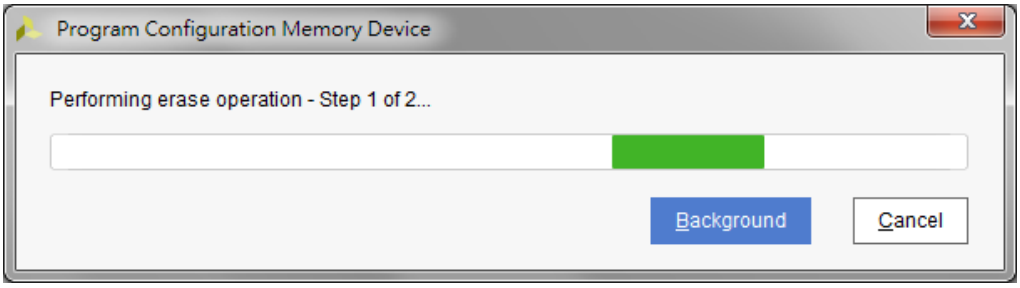

Figure 15. Performing program operation

❖ Wait a few minutes for showing the message “Flash programming completed successfully” as Figure 16.

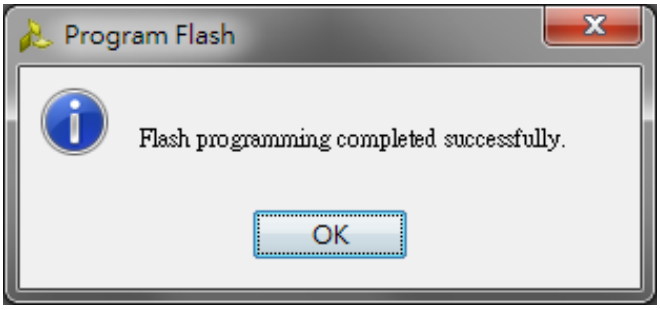

Figure 16. Flash programming completed successfully

❖ Remove USB and JTAG download cables and the programming procedure is completed.

4. Pin Definition of Shield Connector

Table 6. Pin and function name of Shield connector

Pin Name	Function Name	Description
IO15	SCL	I2C clock
IO14	SDA	I2C data
NC	--	Not connected
GND	Ground	Ground Connected to the ground plane
IO13	GPIO 13	General purpose I/O pin
IO12	GPIO12	General purpose I/O pin
IO11	GPIO11	General purpose I/O pin
IO10	GPIO10	General purpose I/O pin
IO9	GPIO9	General purpose I/O pin
IO8	GPIO8	General purpose I/O pin
IO7	GPIO7	General purpose I/O pin
IO6	GPIO6	General purpose I/O pin
IO5	GPIO5	General purpose I/O pin
IO4	GPIO4	General purpose I/O pin
IO3	GPIO3	General purpose I/O pin
IO2	GPIO2	General purpose I/O pin
IO1	TXD	UART Transmit data pin
IO0	RXD	UART Receive data pin
NC	--	Not connected
IOREF	Digital I/O voltage reference	Connect to 3.3V power rail
RST#	Hardware Reset of Shield	Connect to the “RST_BTN1”

Pin Name	Function Name	Description
		button and a digital I/O pin of the FPGA (active low)
3V3	3.3V power rail	Connected to 3.3V power rail
V_5V	5.0V power rail	Connected to 5.0V power rail
GND	Ground	Ground Connected to the ground plane
GND	Ground	Ground Connected to the ground plane
NC	--	Not connected
A0	PWM0	PWM channel 0
A1	PWM1	PWM channel 1
A2	PWM2	PWM channel 2
A3	PWM3	PWM channel 3
A4	N/A	Not applicable
A5	N/A	Not applicable
MISO	SPI bus master input / slave output	
SCLK	SPI clock	
RST#	Hardware Reset shield	Connected to the "RST_BTN1" button and a digital I/O pin of the FPGA (active low)
V_5V	5.0V power rail	Connected to 5.0V power rail
MOSI	SPI bus master output / slave input	
GND	Ground	Ground Connected to the ground plane

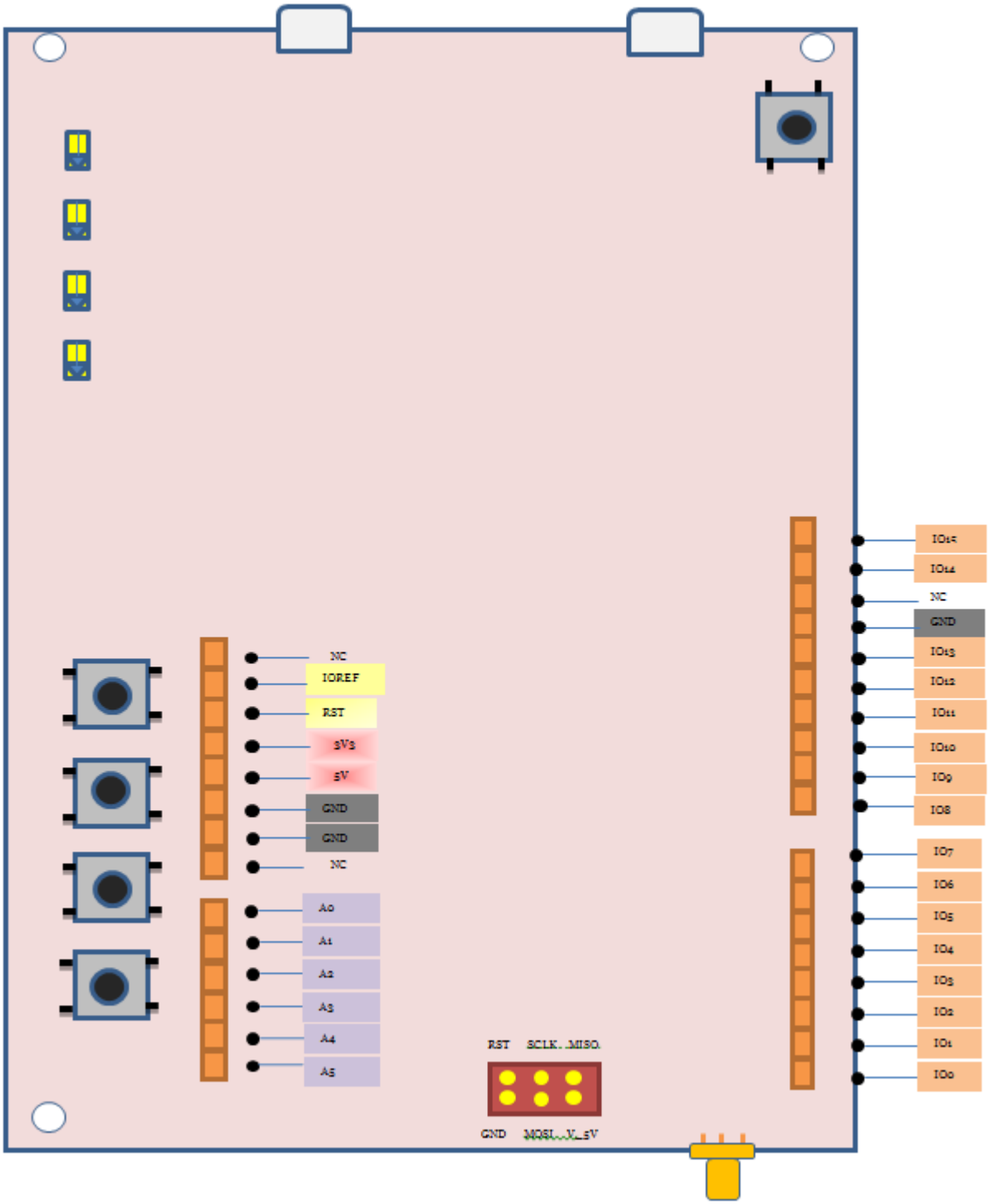

Figure 17. Location of Shield connectors

5. WEEE Directive

For support of EU WEEE directive, Andes encourage European customers to recycle on-hand scrapped Andes board products. You can contact weee@andestech.com for further information.