TaaviSalum / **Digital-electronics-1**

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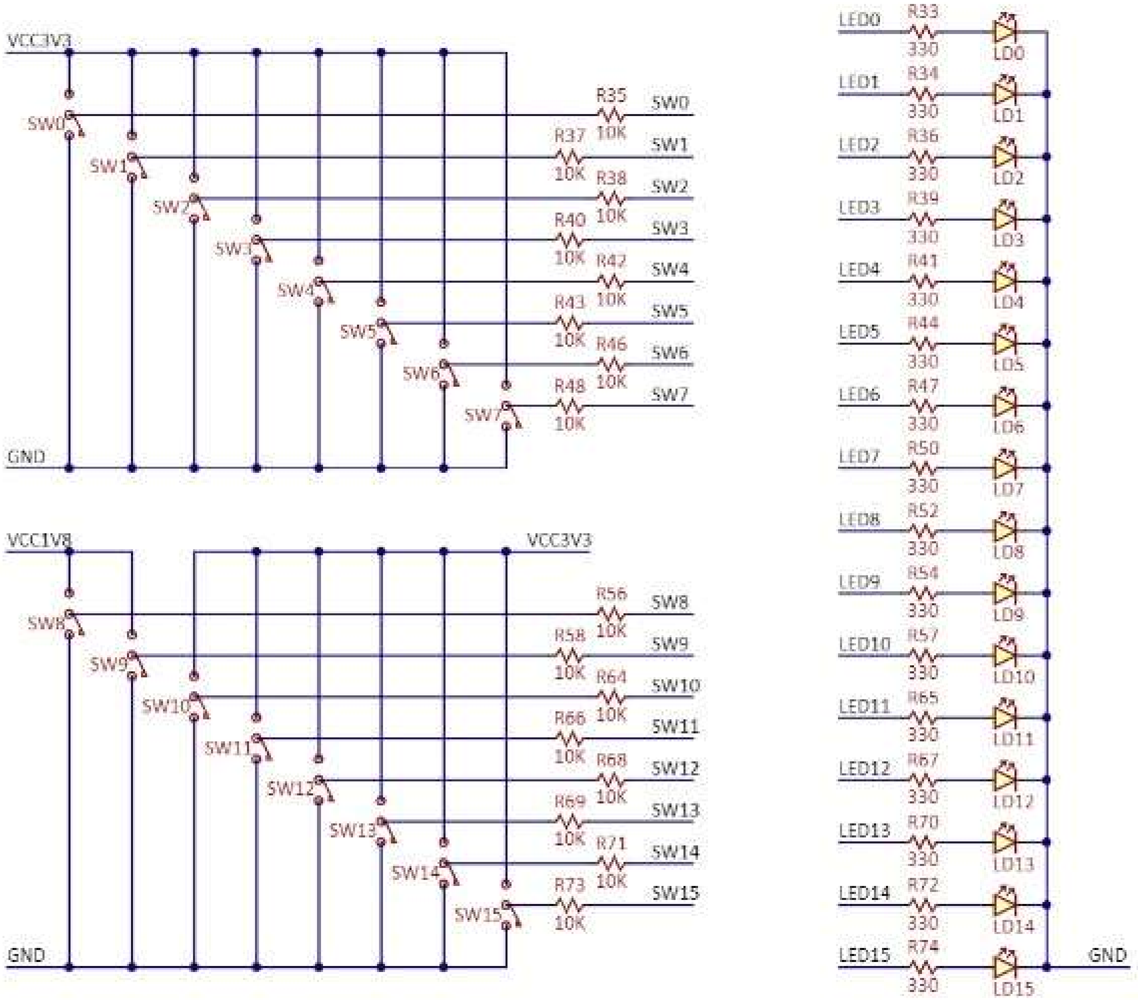
README.md

Digital-electronics-1

Laboratory #3

Exercise 1: Preparation tasks

Connection of 16 slide switches and 16 LEDs on Nexys A7 board



Exercise 2: 2-bit wide 4-to-1 multiplexer

VHDL architecture:

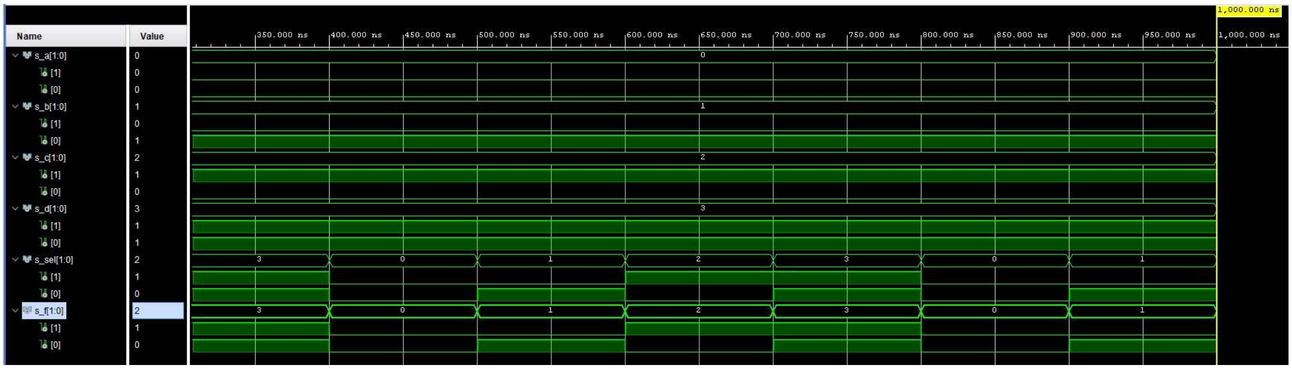
```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity mux_2bit_4to1 is
    port(
        a_i     : in  std_logic_vector(2 - 1 downto 0);
        b_i     : in  std_logic_vector(2 - 1 downto 0);
        c_i     : in  std_logic_vector(2 - 1 downto 0);
        d_i     : in  std_logic_vector(2 - 1 downto 0);
        sel_i   : in  std_logic_vector(2 - 1 downto 0);
        f_o     : out std_logic_vector(2 - 1 downto 0)
    );
end mux_2bit_4to1;
```

```
architecture Behavioral of mux_2bit_4to1 is
begin
    f_o <= a_i when (sel_i = "00") else
           b_i when (sel_i = "01") else
           c_i when (sel_i = "10") else
           d_i;

end architecture Behavioral;
```

VHDL testbench:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity tb_mux_2bit_4to1 is
    -- Entity of testbench is always empty
end tb_mux_2bit_4to1;

architecture Behavioral of tb_mux_2bit_4to1 is

    -- Local signals
    signal s_a      : std_logic_vector(2 - 1 downto 0);
    signal s_b      : std_logic_vector(2 - 1 downto 0);
    signal s_c      : std_logic_vector(2 - 1 downto 0);
    signal s_d      : std_logic_vector(2 - 1 downto 0);
    signal s_sel    : std_logic_vector(2 - 1 downto 0);
    signal s_f      : std_logic_vector(2 - 1 downto 0);

begin

    uut_mux_2bit_4tol : entity work.mux_2bit_4to1
        port map(
            a_i   => s_a,
            b_i   => s_b,
            c_i   => s_c,
            d_i   => s_d,
            sel_i => s_sel,
            f_o   => s_f
        );

    p_stimulus : process
    begin

        report "Stimulus process started" severity note;

        s_d <= "11"; s_c <= "10"; s_b <= "01"; s_a <= "00";
        s_sel <= "00"; wait for 100 ns;
        s_sel <= "01"; wait for 100 ns;
        s_sel <= "10"; wait for 100 ns;
        s_sel <= "11"; wait for 100 ns;
    end process p_stimulus;

end architecture Behavioral;
```

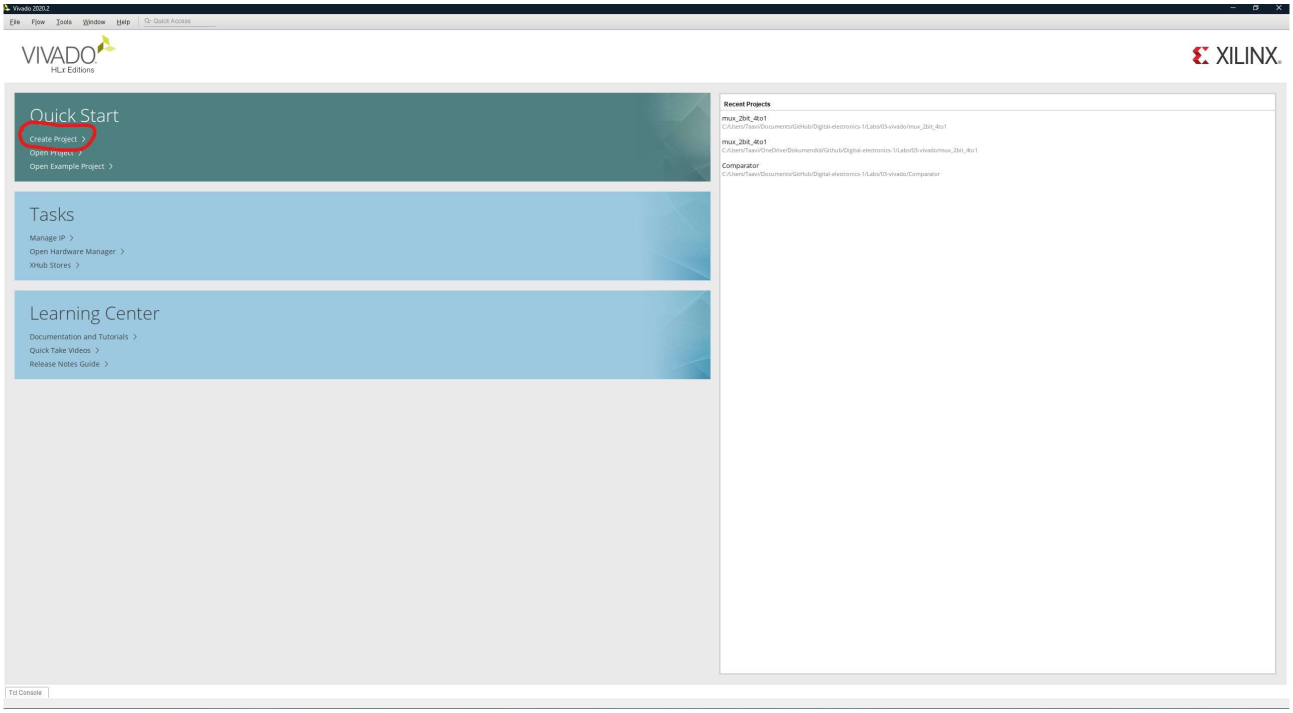
Simulator console output



Exercise 3: A Vivado tutorial

Quick tutorial for Vivado design flow: how to create new project, how to add source file, testbench file and XDC constraints file and how to run simulation

Step 1: Click "Create Project"



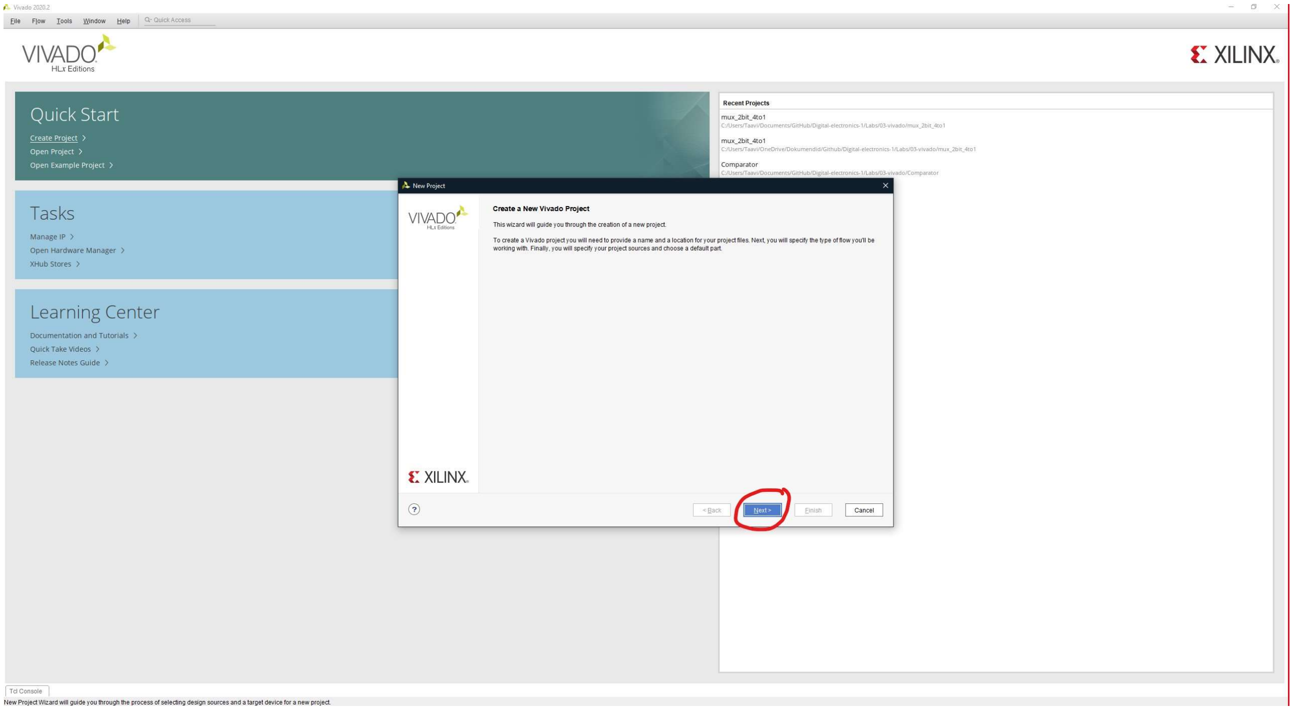
Recent Projects

mux_2bit_4to1
C:/Users/Taavi/Documents/GitHub/Digital-electronics-1/Labs/03-vivado/mux_2bit_4to1

mux_2bit_4to1
C:/Users/Taavi/OneDrive/Dokumendid/Github/Digital-electronics-1/Labs/03-vivado/mux_2bit_4to1

Comparator
C:/Users/Taavi/Documents/GitHub/Digital-electronics-1/Labs/03-vivado/Comparator

Step 2: Click "Next"



mux_2bit_4to1
C:/Users/Taavi/Documents/GitHub/Digital-electronics-1/Labs/03-vivado/mux_2bit_4to1

mux_2bit_4to1
C:/Users/Taavi/OneDrive/Dokumendid/Github/Digital-electronics-1/Labs/03-vivado/mux_2bit_4to1

Comparator
C:/Users/Taavi/Documents/GitHub/Digital-electronics-1/Labs/03-vivado/Comparator

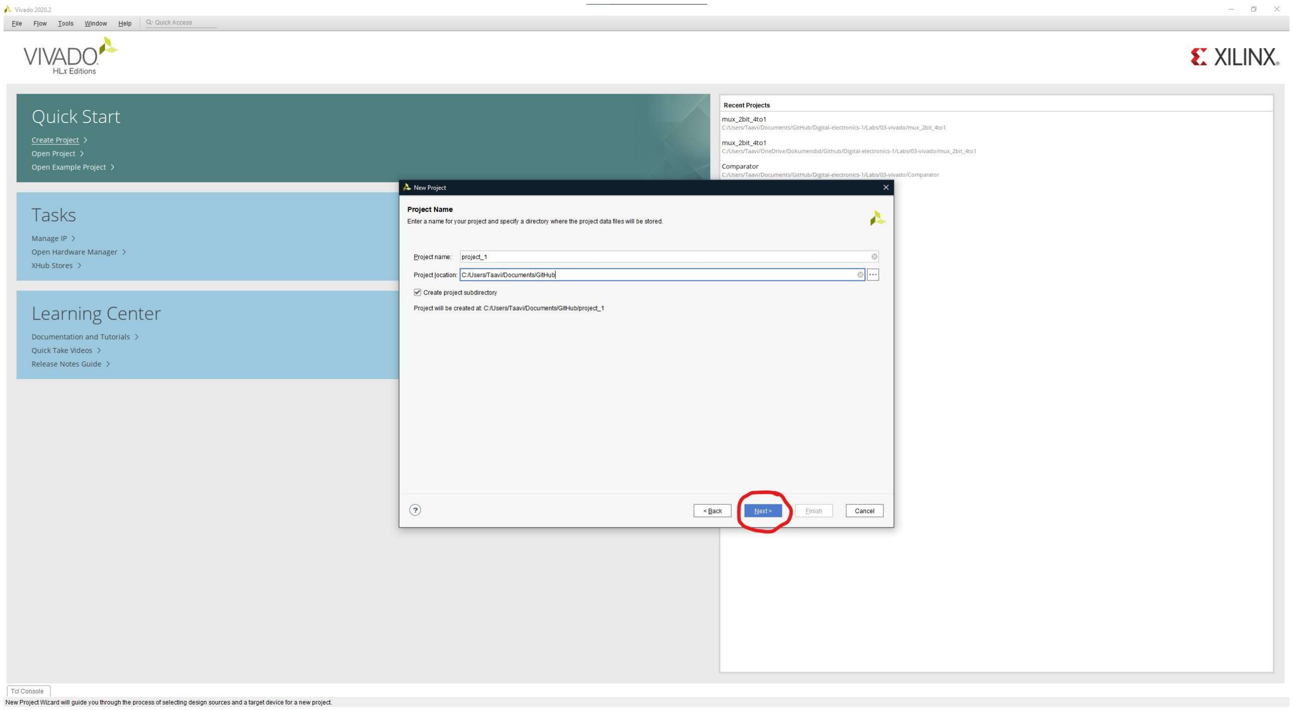
Create a New Vivado Project

This wizard will guide you through the creation of a new project.

To create a Vivado project you will need to provide a name and a location for your project files. Next, you will specify the type of flow you'll be working with. Finally, you will specify your project sources and choose a default part.

New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

Step 3: Decide where do you want to save the project and click "Next"



mux_2bit_4to1
C:/Users/Taavi/Documents/GitHub/Digital-electronics-1/Labs/03-vivado/mux_2bit_4to1

mux_2bit_4to1
C:/Users/Taavi/OneDrive/Dokumendid/Github/Digital-electronics-1/Labs/03-vivado/mux_2bit_4to1

Comparator
C:/Users/Taavi/Documents/GitHub/Digital-electronics-1/Labs/03-vivado/Comparator

Project Name

Enter a name for your project and specify a directory where the project data files will be stored.

Project name: project_1

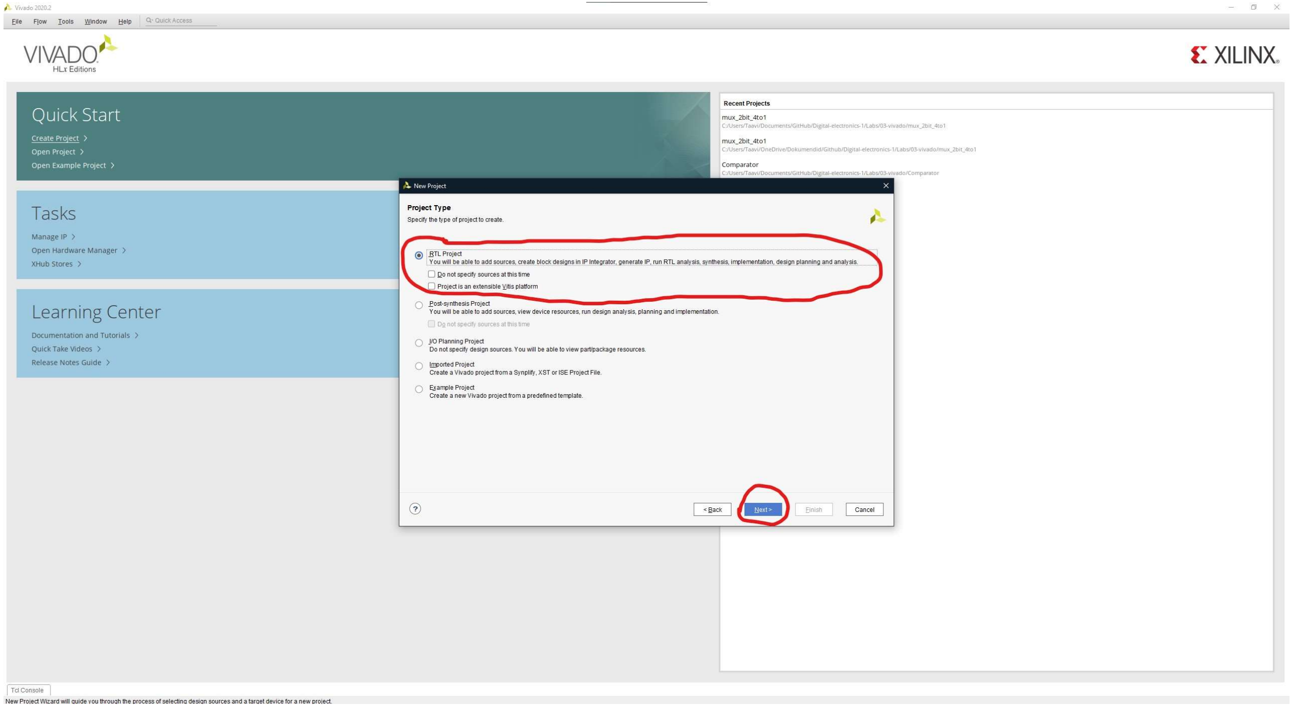
Project location: C:/Users/Taavi/Documents/GitHub

☑ Create project subdirectory

Project will be created at: C:/Users/Taavi/Documents/GitHub/project_1

New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

Step 4: Make sure the project is a "RTL Project" and click "Next"



Project Type

Specify the type of project to create.

● RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
□ Do not specify sources at this time
□ Project is an extensible Vitis platform

○ Post-synthesis Project
You will be able to add sources, view device resources, run design analysis, planning and implementation.
□ Do not specify sources at this time

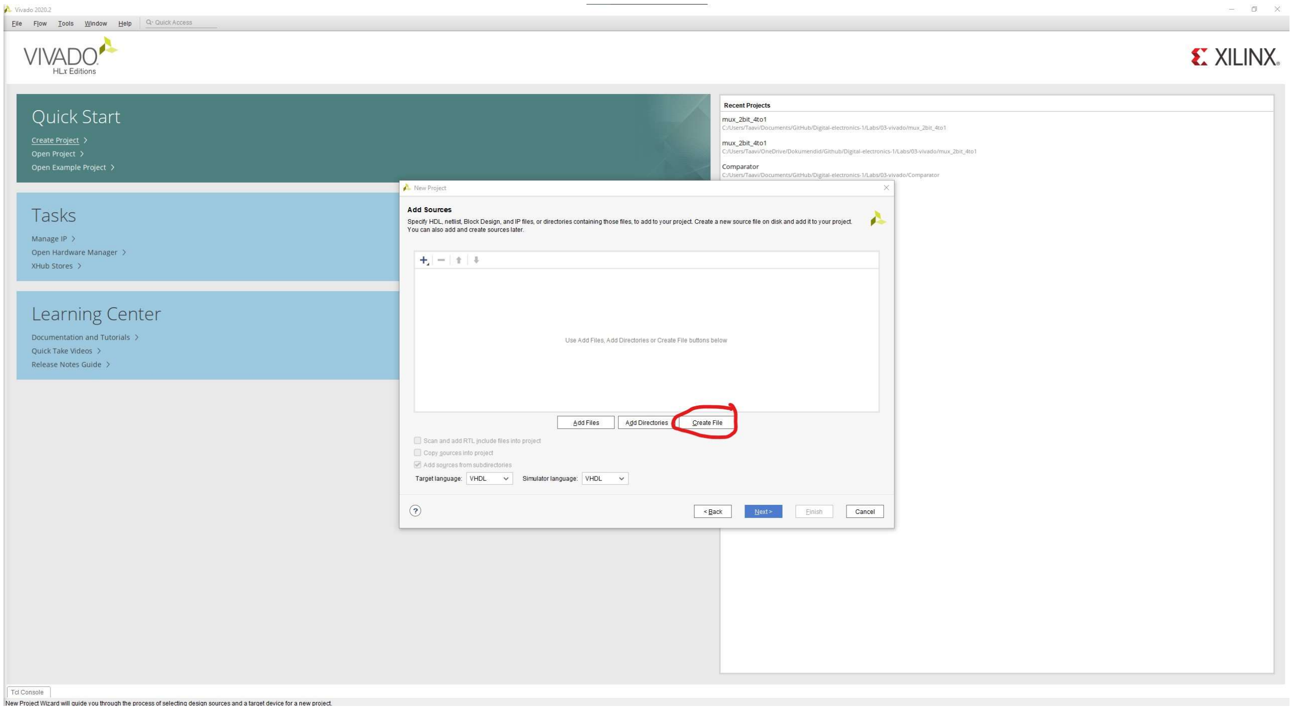
○ I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.

○ Imported Project
Create a Vivado project from a Synplify, XST or ISE Project File.

○ Example Project
Create a new Vivado project from a predefined template.

New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

Step 5: To add source files click on one of the options but to make a new one click on "Create File"



Add Sources

Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.

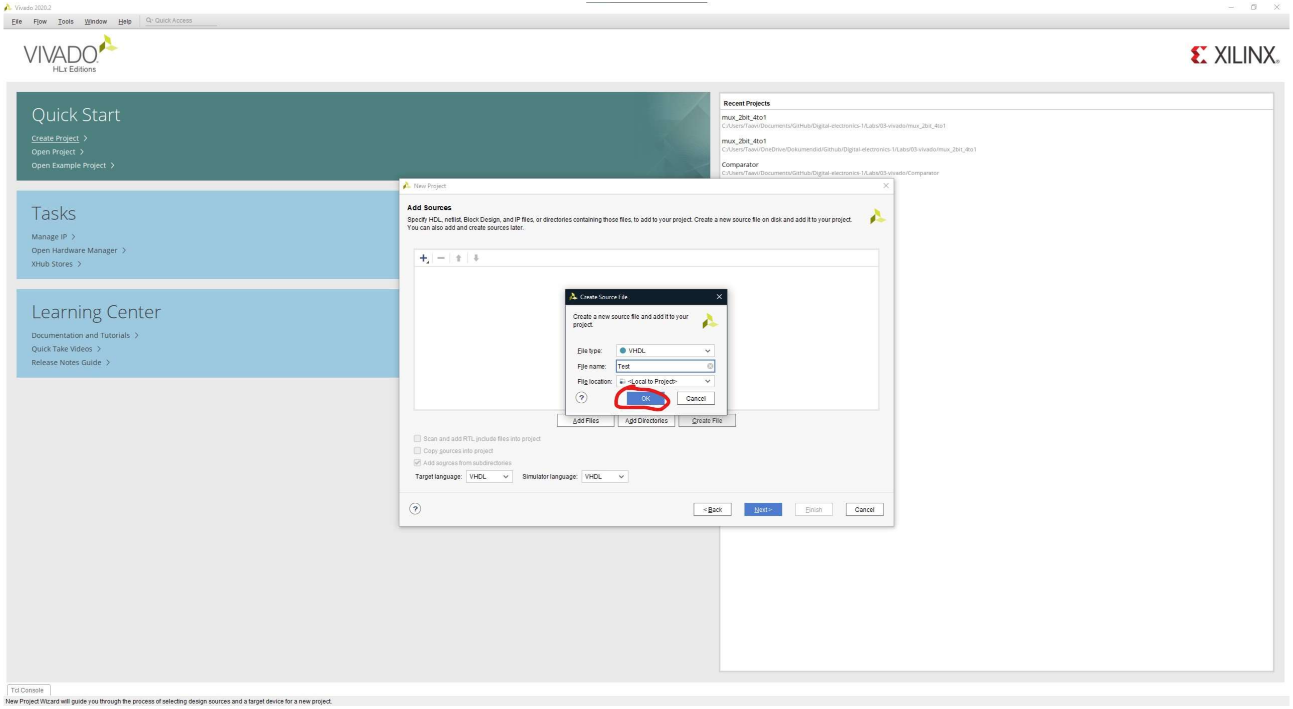
Use Add Files, Add Directories or Create File buttons below

□ Scan and add RTL include files into project
□ Copy sources into project
☑ Add sources from subdirectories

Target language: VHDL Simulator language: VHDL

New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

Step 6: Make sure the file type is "VHDL" then name the source file and click "OK"



Recent Projects

mux_2bit_4to1
C:/Users/Taavi/Documents/GitHub/Digital-electronics-1/Labs/03-vivado/mux_2bit_4to1

mux_2bit_4to1
C:/Users/Taavi/OneDrive/Dokumendid/Github/Digital-electronics-1/Labs/03-vivado/mux_2bit_4to1

Comparator
C:/Users/Taavi/Documents/GitHub/Digital-electronics-1/Labs/03-vivado/Comparator

New Project

Add Sources

Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.

Create Source File

Create a new source file and add it to your project.

File type: VHDL

File name: Test

File location: <Local to Project>

OK Cancel

Add Files | Add Directories | Create File

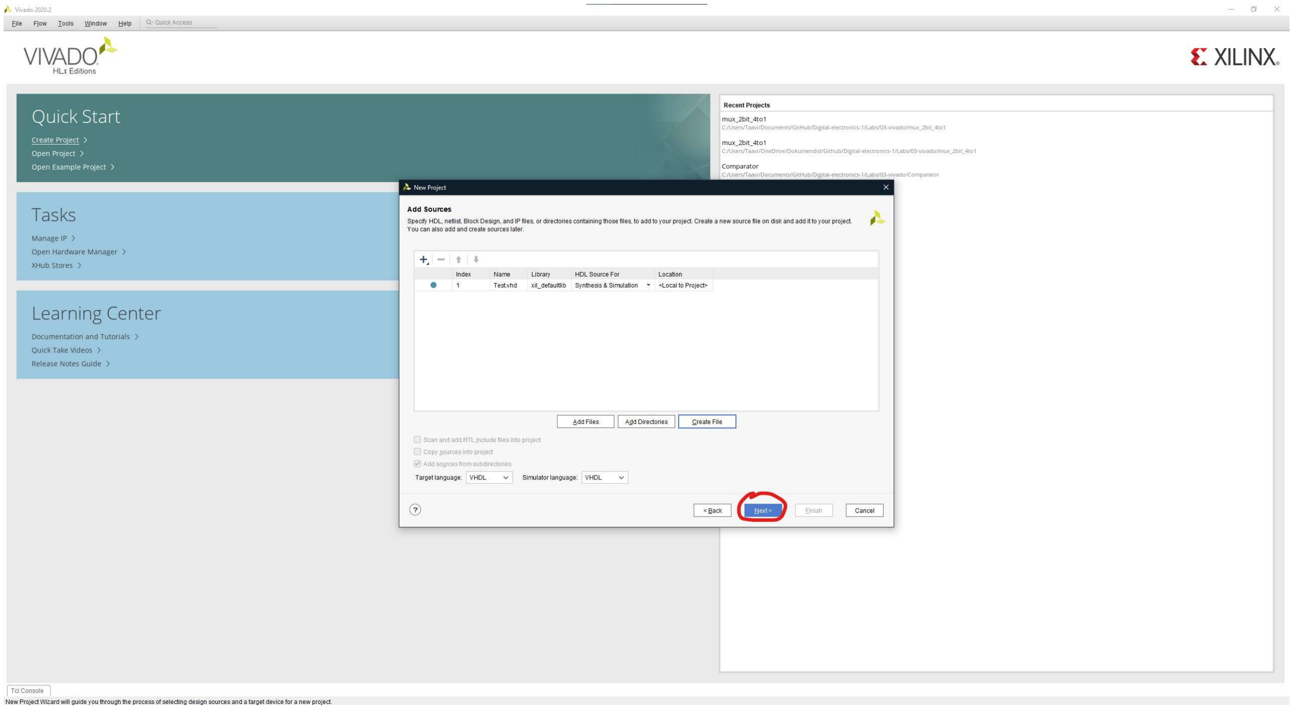
☐ Scan and add RTL include files into project
☐ Copy sources into project
☑ Add sources from subdirectories

Target language: VHDL Simulator language: VHDL

< Back | Next > | Finish | Cancel

New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

Step 7: Once all of the source files have been added click "Next"



Recent Projects

mux_2bit_4to1
C:/Users/Taavi/Documents/GitHub/Digital-electronics-1/Labs/03-vivado/mux_2bit_4to1

mux_2bit_4to1
C:/Users/Taavi/OneDrive/Dokumendid/Github/Digital-electronics-1/Labs/03-vivado/mux_2bit_4to1

Comparator
C:/Users/Taavi/Documents/GitHub/Digital-electronics-1/Labs/03-vivado/Comparator

New Project

Add Sources

Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.

	Index	Name	Library	HDL Source For	Location
●	1	Test.vhd	xil_defaultlib	Synthesis & Simulation	<Local to Project>

Add Files | Add Directories | Create File

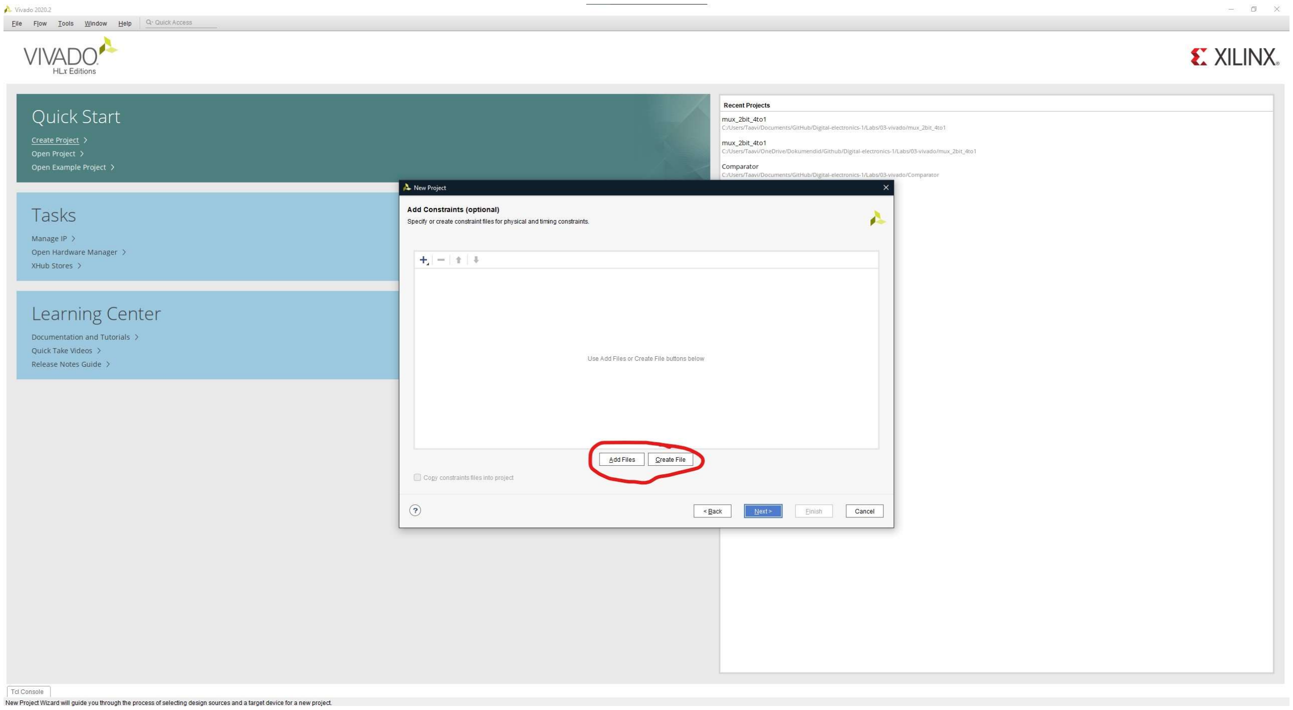
☐ Scan and add RTL include files into project
☐ Copy sources into project
☑ Add sources from subdirectories

Target language: VHDL Simulator language: VHDL

< Back | Next > | Finish | Cancel

New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

Step 8: To add XDC constraint files click on of the options but to make a new one click on "Create File"



mux_2bit_4to1
C:/Users/Taavi/Documents/GitHub/Digital-electronics-1/Labs/03-vivado/mux_2bit_4to1

mux_2bit_4to1
C:/Users/Taavi/OneDrive/Dokumendid/Github/Digital-electronics-1/Labs/03-vivado/mux_2bit_4to1

Comparator
C:/Users/Taavi/Documents/GitHub/Digital-electronics-1/Labs/03-vivado/Comparator

Add Constraints (optional)

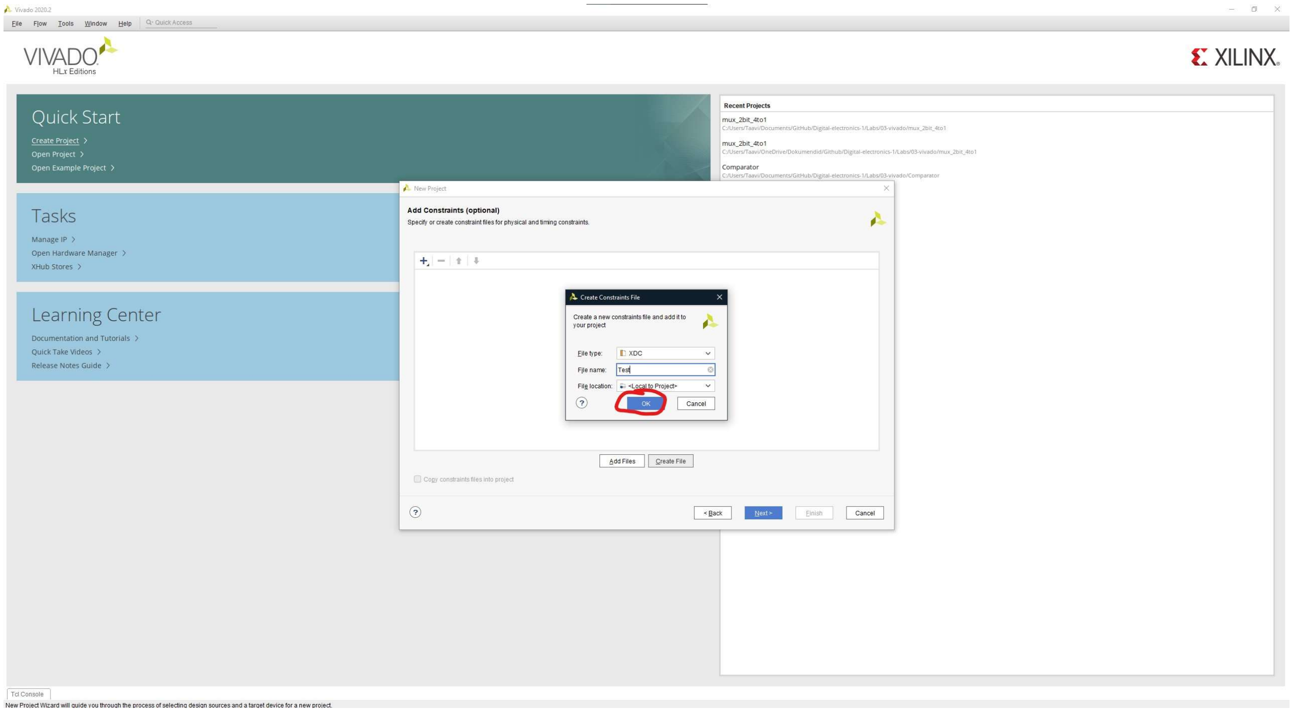
Specify or create constraint files for physical and timing constraints.

Use Add Files or Create File buttons below

□ Copy constraints files into project

New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

Step 9: Make sure the file type is "XDC" then name the XDC constraint file and click "OK"



mux_2bit_4to1
C:/Users/Taavi/Documents/GitHub/Digital-electronics-1/Labs/03-vivado/mux_2bit_4to1

mux_2bit_4to1
C:/Users/Taavi/OneDrive/Dokumendid/Github/Digital-electronics-1/Labs/03-vivado/mux_2bit_4to1

Comparator
C:/Users/Taavi/Documents/GitHub/Digital-electronics-1/Labs/03-vivado/Comparator

Add Constraints (optional)

Specify or create constraint files for physical and timing constraints.

Create a new constraints file and add it to your project

File type: XDC

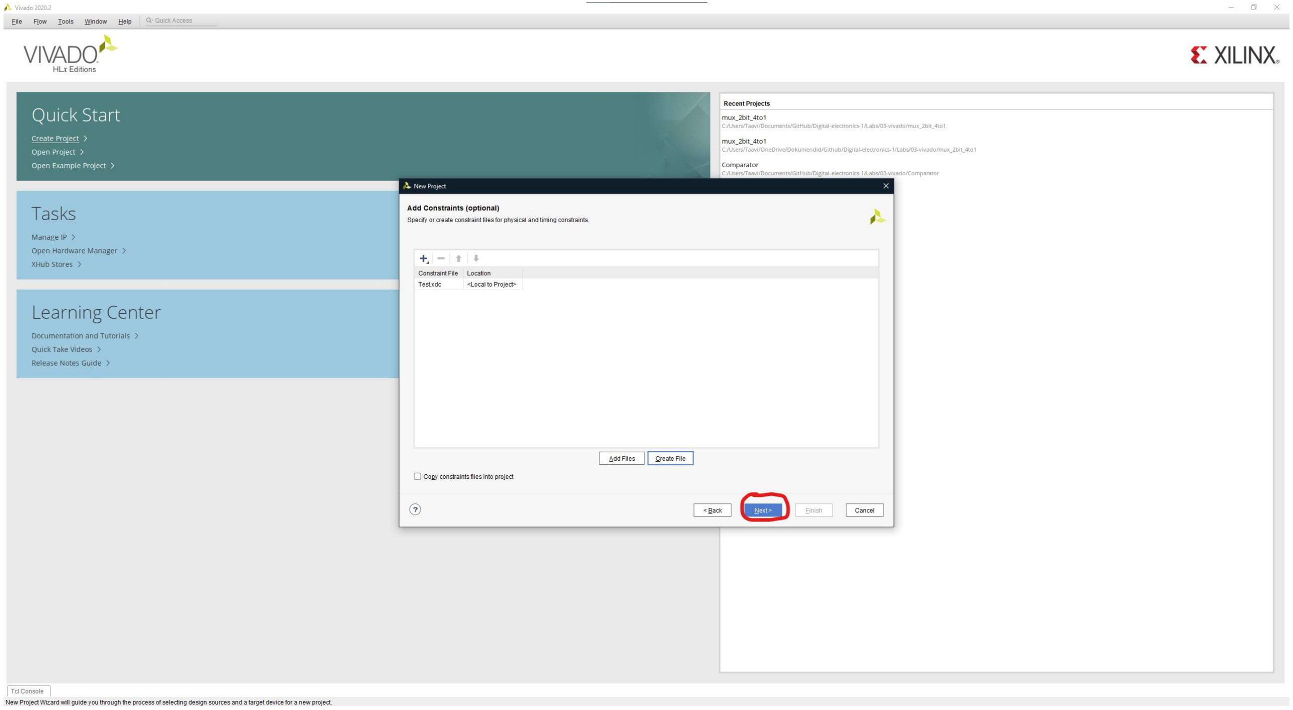
File name: Test

File location: <Local to Project>

□ Copy constraints files into project

New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

Step 10: Once all of the XDC constraint files have been added click "Next"



mux_2bit_4to1
C:/Users/Taavi/Documents/GitHub/Digital-electronics-1/Labs/03-vivado/mux_2bit_4to1

mux_2bit_4to1
C:/Users/Taavi/OneDrive/Dokumendid/Github/Digital-electronics-1/Labs/03-vivado/mux_2bit_4to1

Comparator
C:/Users/Taavi/Documents/GitHub/Digital-electronics-1/Labs/03-vivado/Comparator

New Project

Add Constraints (optional)

Specify or create constraint files for physical and timing constraints.

Constraint File	Location
Test.xdc	<Local to Project>

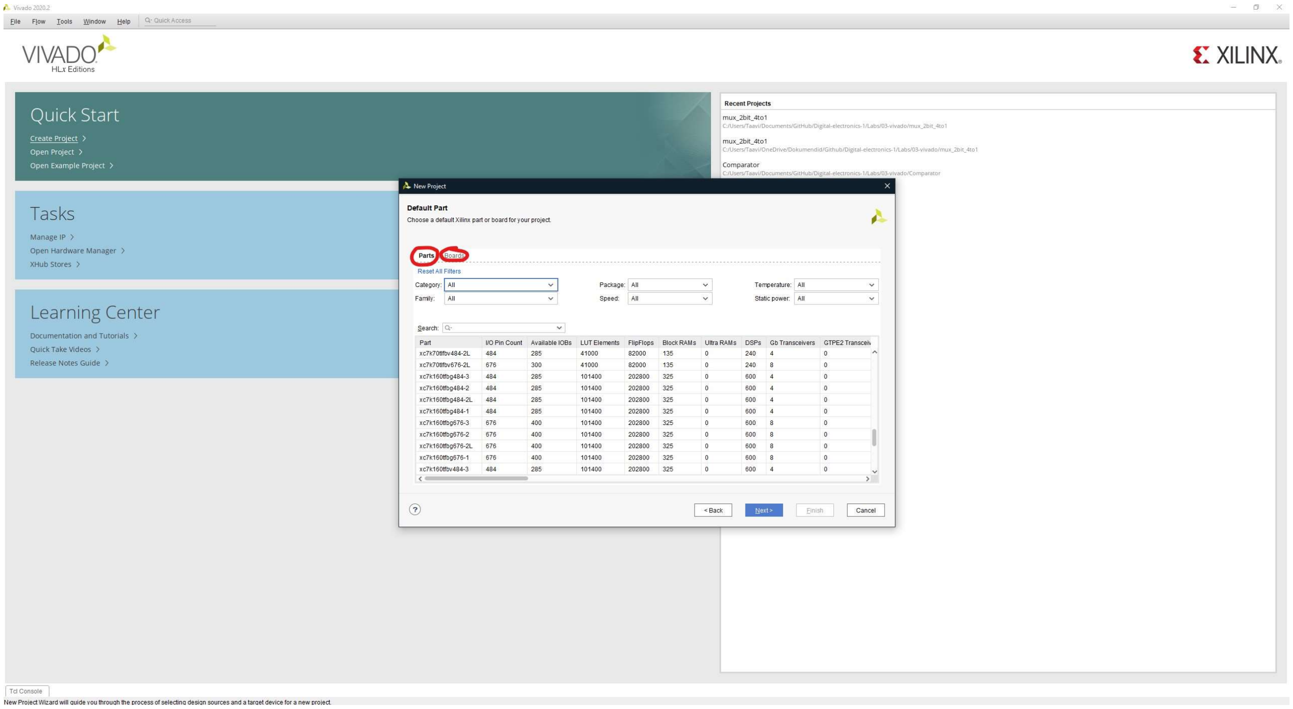
Add Files | Create File

□ Copy constraints files into project

< Back | Next > | Finish | Cancel

New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

Step 11: Find the FPGA you are using under "Parts" or "Boards"



mux_2bit_4to1
C:/Users/Taavi/Documents/GitHub/Digital-electronics-1/Labs/03-vivado/mux_2bit_4to1

mux_2bit_4to1
C:/Users/Taavi/OneDrive/Dokumendid/Github/Digital-electronics-1/Labs/03-vivado/mux_2bit_4to1

Comparator
C:/Users/Taavi/Documents/GitHub/Digital-electronics-1/Labs/03-vivado/Comparator

New Project

Default Part

Choose a default Xilinx part or board for your project.

Parts | Boards

Reset All Filters

Category: All
Family: All
Package: All
Speed: All
Temperature: All
Static power: All

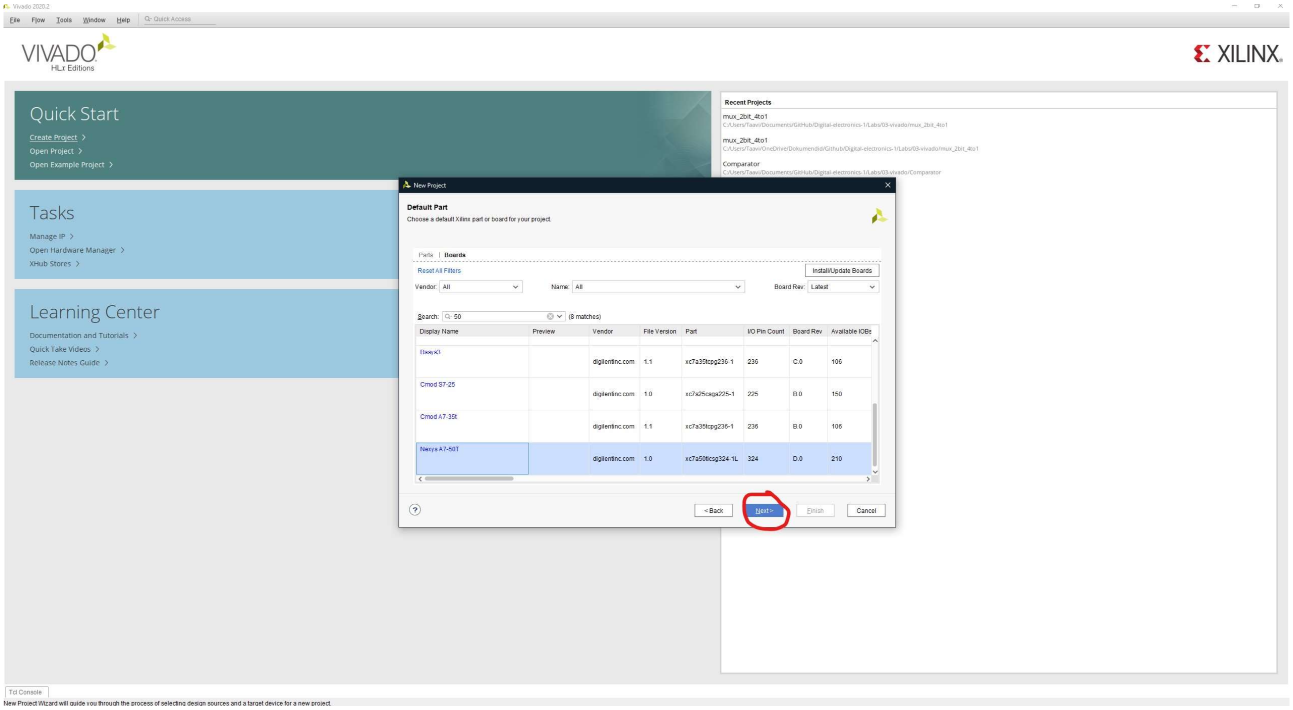
Search:

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs	Gb Transceivers	GTPE2 Transceiv
xc7k70tfbv484-2L	484	285	41000	82000	135	0	240	4	0
xc7k70tfbv676-2L	676	300	41000	82000	135	0	240	8	0
xc7k160tfbg484-3	484	285	101400	202800	325	0	600	4	0
xc7k160tfbg484-2	484	285	101400	202800	325	0	600	4	0
xc7k160tfbg484-2L	484	285	101400	202800	325	0	600	4	0
xc7k160tfbg484-1	484	285	101400	202800	325	0	600	4	0
xc7k160tfbg676-3	676	400	101400	202800	325	0	600	8	0
xc7k160tfbg676-2	676	400	101400	202800	325	0	600	8	0
xc7k160tfbg676-2L	676	400	101400	202800	325	0	600	8	0
xc7k160tfbg676-1	676	400	101400	202800	325	0	600	8	0
xc7k160tfbv484-3	484	285	101400	202800	325	0	600	4	0

< Back | Next > | Finish | Cancel

New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

Step 12: Once you have find it, select it and click "Next"



Recent Projects

mux_2bit_4to1
C:/Users/Taavi/Documents/GitHub/Digital-electronics-1/Labs/03-vivado/mux_2bit_4to1

mux_2bit_4to1
C:/Users/Taavi/OneDrive/Dokumendid/Github/Digital-electronics-1/Labs/03-vivado/mux_2bit_4to1

Comparator
C:/Users/Taavi/Documents/GitHub/Digital-electronics-1/Labs/03-vivado/Comparator

Default Part

Choose a default Xilinx part or board for your project.

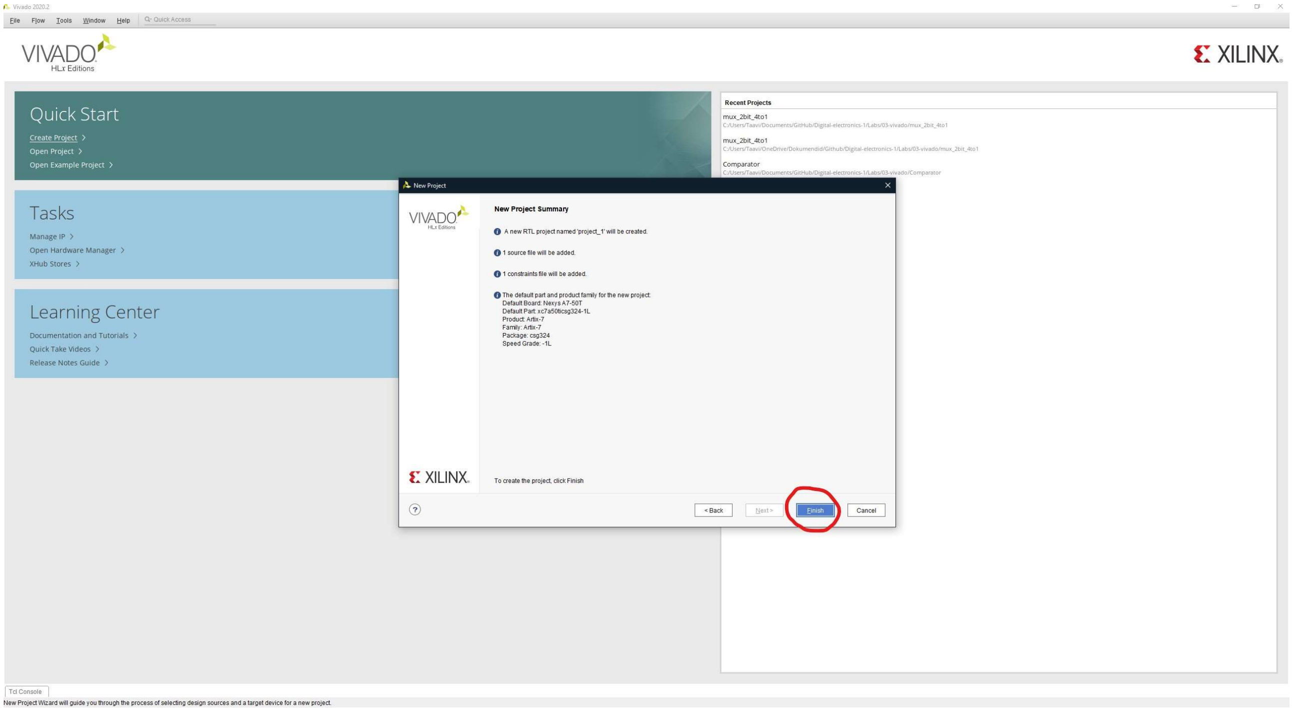
Vendor: All Name: All Board Rev: Latest

Search: 50 (8 matches)

Display Name	Preview	Vendor	File Version	Part	I/O Pin Count	Board Rev	Available IOBs
Basys3		digilentinc.com	1.1	xc7a35tcpg236-1	236	C.0	106
Cmod S7-25		digilentinc.com	1.0	xc7s25csga225-1	225	B.0	150
Cmod A7-35t		digilentinc.com	1.1	xc7a35tcpg236-1	236	B.0	106
Nexys A7-50T		digilentinc.com	1.0	xc7a50ticsg324-1L	324	D.0	210

New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

Step 13: Have a quick overview of the project and once everything is correct click "Finish"



Recent Projects

mux_2bit_4to1
C:/Users/Taavi/Documents/GitHub/Digital-electronics-1/Labs/03-vivado/mux_2bit_4to1

mux_2bit_4to1
C:/Users/Taavi/OneDrive/Dokumendid/Github/Digital-electronics-1/Labs/03-vivado/mux_2bit_4to1

Comparator
C:/Users/Taavi/Documents/GitHub/Digital-electronics-1/Labs/03-vivado/Comparator

New Project Summary

A new RTL project named 'project_1' will be created.

1 source file will be added.

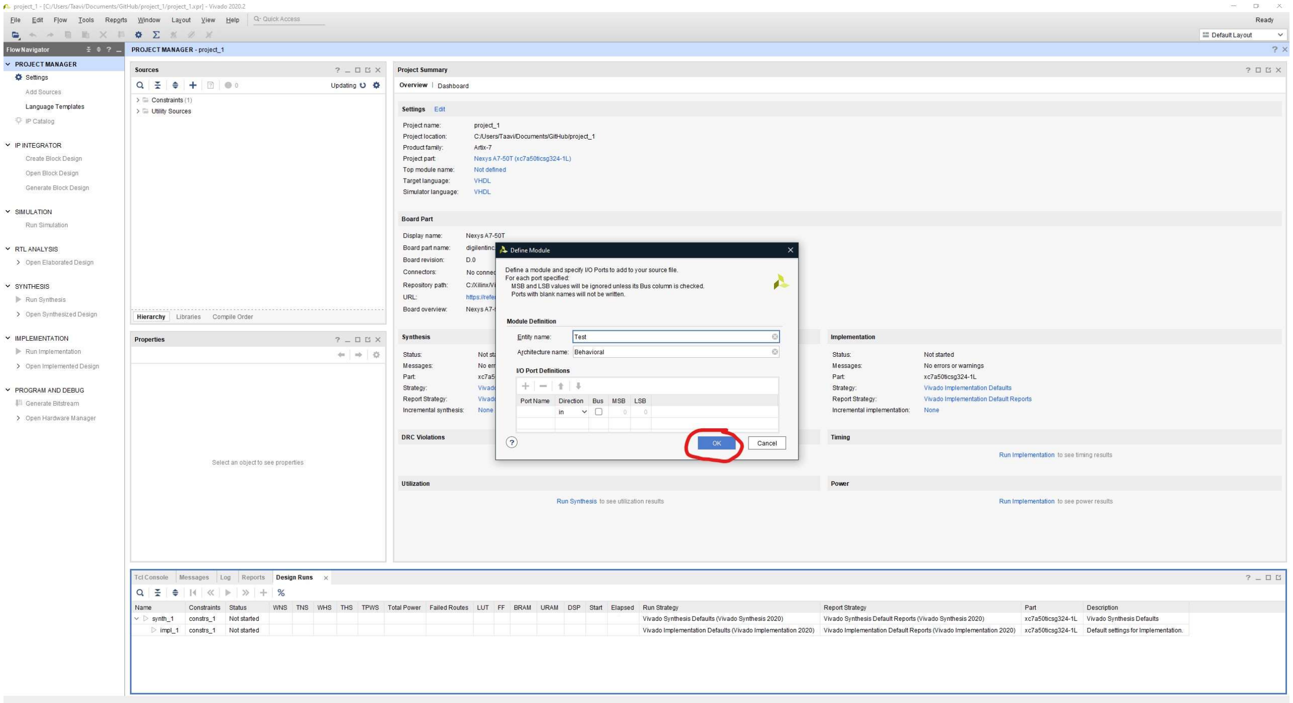
1 constraints file will be added.

The default part and product family for the new project:
Default Board: Nexys A7-50T
Default Part: xc7a50ticsg324-1L
Product: Artix-7
Family: Artix-7
Package: csg324
Speed Grade: -1L

To create the project, click Finish

New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

Step 14: A window will pop-up and there you can add the testbench file and once everything is correct click "OK"



Define Module

Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.

Module Definition

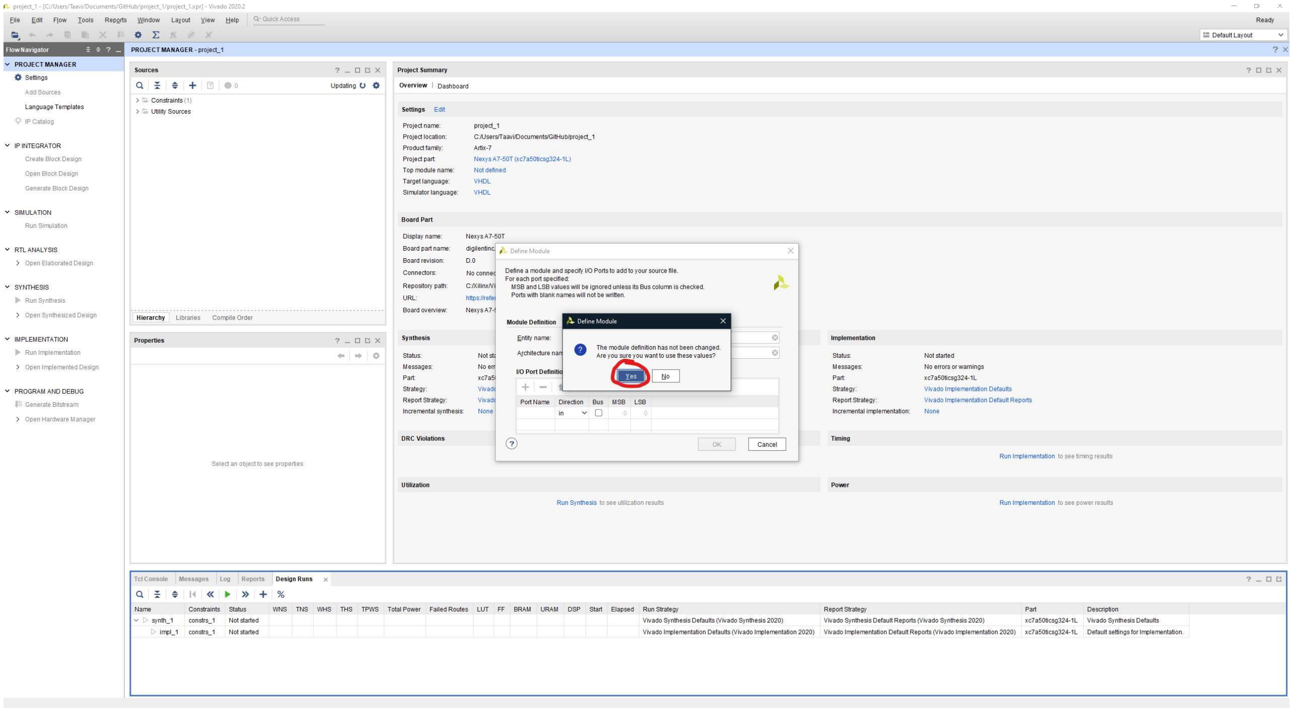
Entity name: Test

Architecture name: Behavioral

I/O Port Definitions

Port Name	Direction	Bus	MSB	LSB
	in	□	0	0

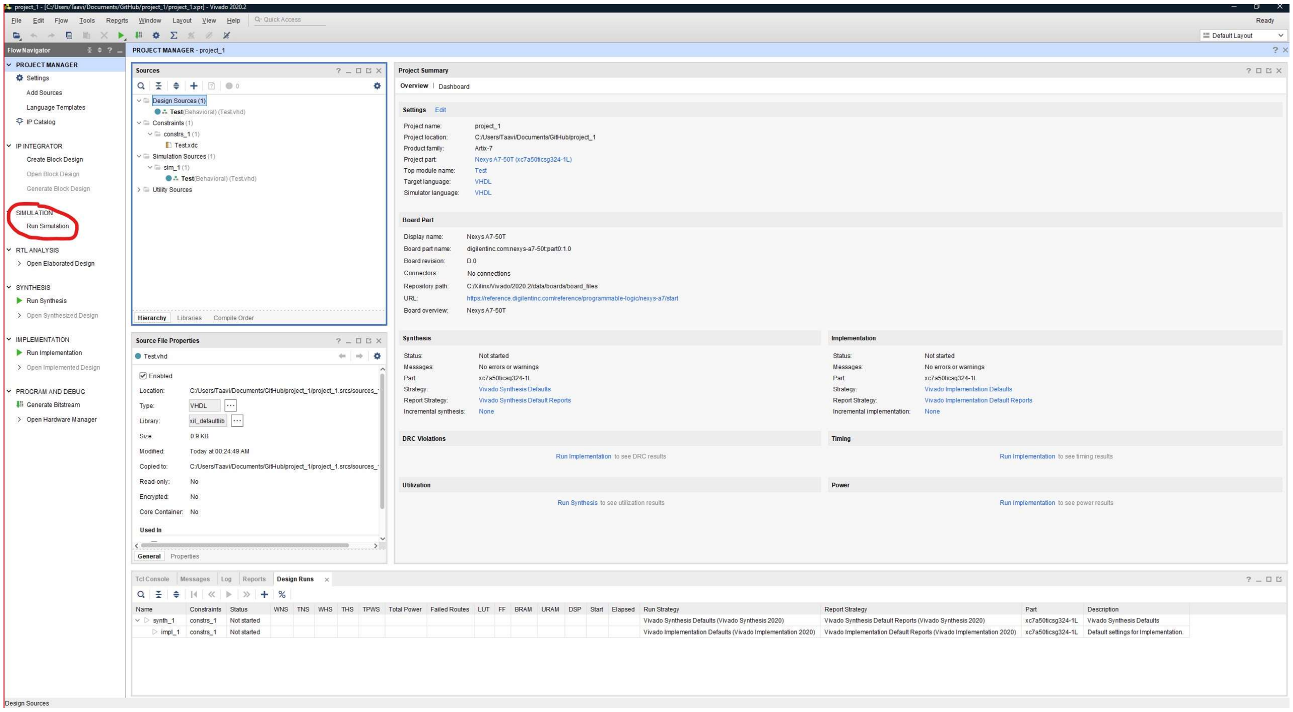
Step 15: Click "Yes"



Define Module

The module definition has not been changed.
Are you sure you want to use these values?

Step 16: To run the simulation click "Run Simulation



Source File Properties: Test.vhd

☑ Enabled

Location: C:/Users/Taavi/Documents/GitHub/project_1/project_1.srcs/sources_

Type: VHDL

Library: xil_defaultlib

Size: 0.9 KB

Modified: Today at 00:24:49 AM

Copied to: C:/Users/Taavi/Documents/GitHub/project_1/project_1.srcs/sources_

Read-only: No

Encrypted: No

Core Container: No

Used In

Project Summary

Settings Edit

Project name: project_1
Project location: C:/Users/Taavi/Documents/GitHub/project_1
Product family: Artix-7
Project part: Nexys A7-50T (xc7a50ticsg324-1L)
Top module name: Test
Target language: VHDL
Simulator language: VHDL

Board Part

Display name: Nexys A7-50T
Board part name: digilentinc.com:nexys-a7-50t:part0:1.0
Board revision: D.0
Connectors: No connections
Repository path: C:/Xilinx/Vivado/2020.2/data/boards/board_files
URL: https://reference.digilentinc.com/reference/programmable-logic/nexys-a7/start
Board overview: Nexys A7-50T

Synthesis

Status: Not started
Messages: No errors or warnings
Part: xc7a50ticsg324-1L
Strategy: Vivado Synthesis Defaults
Report Strategy: Vivado Synthesis Default Reports
Incremental synthesis: None

Implementation

Status: Not started
Messages: No errors or warnings
Part: xc7a50ticsg324-1L
Strategy: Vivado Implementation Defaults
Report Strategy: Vivado Implementation Default Reports
Incremental implementation: None

DRC Violations

Run Implementation to see DRC results

Timing

Run Implementation to see timing results

Utilization

Run Synthesis to see utilization results

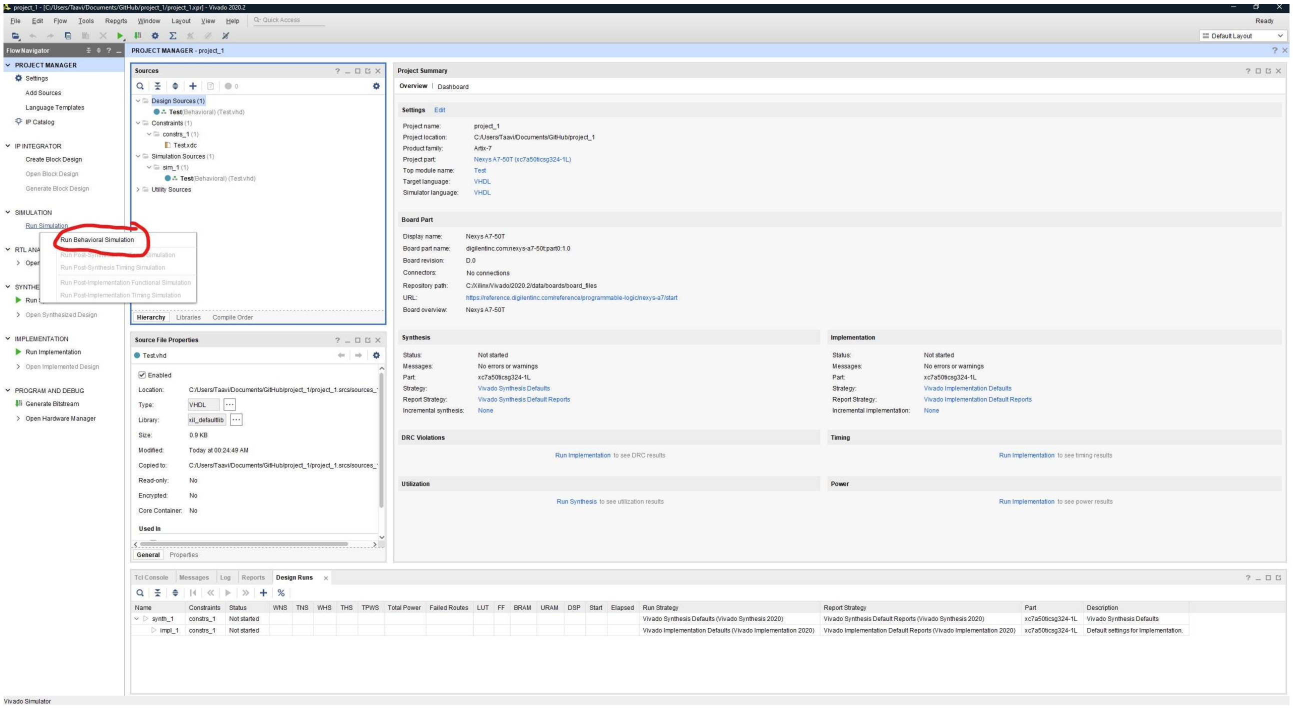
Power

Run Implementation to see power results

Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy	Part	Description
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2020)	Vivado Synthesis Default Reports (Vivado Synthesis 2020)	xc7a50ticsg324-1L	Vivado Synthesis Defaults
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2020)	Vivado Implementation Default Reports (Vivado Implementation 2020)	xc7a50ticsg324-1L	Default settings for Implementation.

Step 17: Click "Run Behavioral Simulation"



☑ Enabled

Location: C:/Users/Taavi/Documents/GitHub/project_1/project_1.srcs/sources_

Type: VHDL

Library: xil_defaultlib

Size: 0.9 KB

Modified: Today at 00:24:49 AM

Copied to: C:/Users/Taavi/Documents/GitHub/project_1/project_1.srcs/sources_

Read-only: No

Encrypted: No

Core Container: No

Used In

Settings Edit

Project name: project_1
Project location: C:/Users/Taavi/Documents/GitHub/project_1
Product family: Artix-7
Project part: Nexys A7-50T (xc7a50ticsg324-1L)
Top module name: Test
Target language: VHDL
Simulator language: VHDL

Board Part

Display name: Nexys A7-50T
Board part name: digilentinc.com:nexys-a7-50t:part0:1.0
Board revision: D.0
Connectors: No connections
Repository path: C:/Xilinx/Vivado/2020.2/data/boards/board_files
URL: https://reference.digilentinc.com/reference/programmable-logic/nexys-a7/start
Board overview: Nexys A7-50T

Synthesis

Status: Not started
Messages: No errors or warnings
Part: xc7a50ticsg324-1L
Strategy: Vivado Synthesis Defaults
Report Strategy: Vivado Synthesis Default Reports
Incremental synthesis: None

Implementation

Status: Not started
Messages: No errors or warnings
Part: xc7a50ticsg324-1L
Strategy: Vivado Implementation Defaults
Report Strategy: Vivado Implementation Default Reports
Incremental implementation: None

DRC Violations

Run Implementation to see DRC results

Timing

Run Implementation to see timing results

Utilization

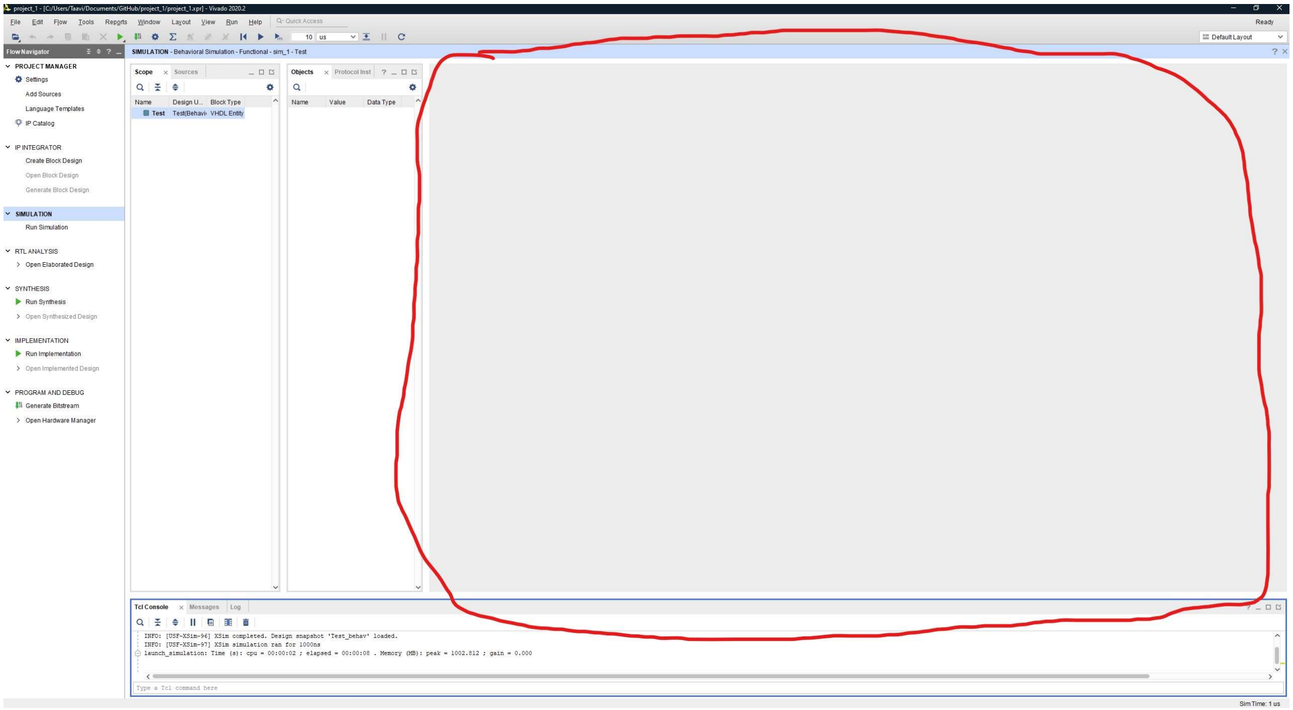
Run Synthesis to see utilization results

Power

Run Implementation to see power results

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy	Part	Description
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2020)	Vivado Synthesis Default Reports (Vivado Synthesis 2020)	xc7a50ticsg324-1L	Vivado Synthesis Defaults
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2020)	Vivado Implementation Default Reports (Vivado Implementation 2020)	xc7a50ticsg324-1L	Default settings for Implementation.

Step 18: Simulated time waveforms will appear on the right window *(For current tutorial there is no simulated time waveform)*



```
INFO: [USF-XSim-96] XSim completed. Design snapshot 'Test_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:02 ; elapsed = 00:00:08 . Memory (MB): peak = 1002.812 ; gain = 0.000
```