LABORATORY MANUAL

Course Code/Title: EEF360 – Systems Simulation and PCB Design

Lab Exercise 6

Title: FLIP-FLOP USING PROTEUS

Aim: To analyze flip-flop circuits with emphasis on JK flip-flop using Proteus ISIS

Objectives:

- To understand the working principles of flip-flops
- To understand the difference between level and edge triggering.
- To understand the simulation procedure of rising edge trigger JK flip-flop using Proteus ISIS.
- To better appreciate the analytical knowledge on flip-flops.

INTRODUCTION

A flip-flop is a bistable circuit. Both of its output states are stable. The circuit remains in a particular output state indefinitely until something is done to change that output status. There are different types of flip-flop such as; R-S, J-K, Master Slave, Toggle and D-Flip- flops, each with its particularities. For this lab-Session, we shall focus on simulating J-K flip- flop.

J-K Flip-Flop

A J-K flip-flop behaves in the same fashion as an R-S flip-flop except for one of the entries in the function table. In the case of an R-S flip-flop, the input combination S = R = 1 (in the case of a flip-flop with active HIGH inputs) and the input combination S = R = 0 (in the case of a flip-flop with active LOW inputs) are prohibited.

In the case of a J-K flip-flop with active HIGH inputs, the output of the flip-flop toggles, that is, it goes to the other state, for J = K = 1 . The output toggles for J = K = 0 in the case of the flip-flop having active LOW inputs. Thus, a J-K flip-flop overcomes the problem of a forbidden input combination of the R-S flip-flop.

J-K Flip-Flop with PRESET and CLEAR Inputs

It is often necessary to clear a flip-flop to a logic ‘0’ state (Qn = 0) or preset it to a logic ‘1’ state (Qn = 1). The flip-flop is cleared (that is, Qn = 0) whenever the CLEAR input is ‘0’ and the PRESET input is ‘1’. The flip-flop is preset to the logic ‘1’ state whenever the PRESET input is ‘0’ and the CLEAR input is ‘1’. Figure 1 shows the circuit symbol of this presettable, clearable clocked J-K flip-flop with active LOW CLEAR and PRESET inputs. Figure 2 shows the function table of such a flip-flop. It is evident from the function table that, whenever the PRESET input is active, the output goes to the ‘1’ state irrespective of the status of the clock, J and K inputs. Similarly, when the flip-flop is cleared, that is, the CLEAR input is active, the output goes to the ‘0’ state irrespective of the status of the clock, J and K inputs. In a flip-flop of this type, both PRESET and CLEAR inputs should not be made active at the same time.

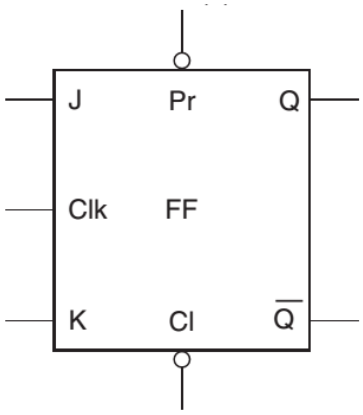

Figure 1. Circuit symbol of J-K flip-flop with PRESET and CLEAR inputs.

PR	CL	CLK	J	K	Q_{n+1}	$\overline{Q_{n+1}}$
0	1	X	X	X	1	0
1	0	X	X	X	0	1
0	0	X	X	X	---	---
1	1	1	0	0	Q_n	$\overline{Q_n}$
1	1	1	1	0	1	0
1	1	1	0	1	0	1
1	1	1	1	1	Toggle	
1	1	0	X	X	Q_n	$\overline{Q_n}$

Figure 2. Function Table of J-K flip-flop with PRESET and CLEAR inputs.

PART I: PRE-LAB

1) With the help of a sketch, explain the difference between a level trigger and an edge trigger R-S flip flop (avoid forbidden conditions in choosing your inputs).
2) What is the difference between an active high and active low Toggle flip flop (illustrate)
3) Given the characteristic tables for J-K flip-flop with active HIGH and active LOW J and K inputs as shown in Figure 3 a and b respectively;

Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

a

Q_n	J	K	Q_{n+1}
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

b

figure 3. Characteristic tables of JK Flip Flops; a) active HIGH b) active LOW

i. Draw the Karnaugh map for each
ii. Derive the characteristic equations from the Karnaugh map
iii. Draw the waveform of each

PART II: LAB. SIMULATION

The simulation is based strictly on the circuit of figure 4 below

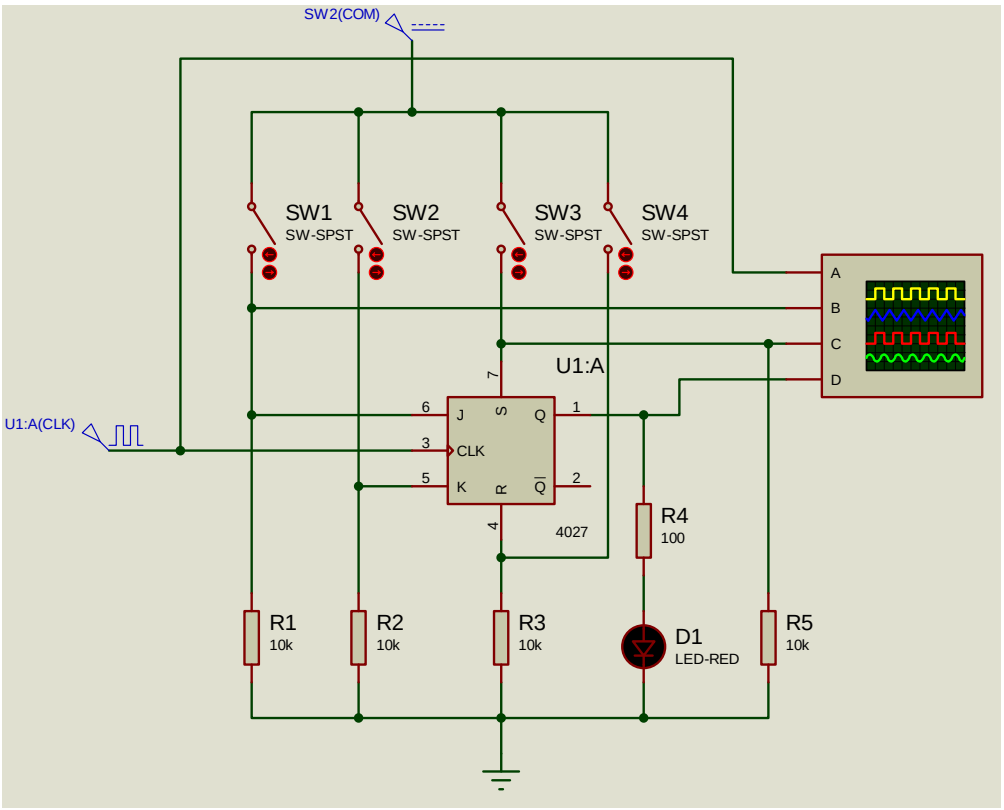

Figure 4. Proteus simulation circuit for a J-K flip flop.

Components required

Lot	Component name	Component Specification	Number of Components Required
1	JK Flip Flop	4027	1
2	Resistor	10k	4
3	Resistor	100	1
4	LED	LED-RED	1
5	Switch	SW-SPST	4
6	Clock	DCLOCK	1
7	Ground	GND	1
8	Source	DC	1

Simulation Procedure using Proteus

1. Using the right components from the parts library, enter the circuit of figure 4 in the Proteus ISIS design window.
2. Point to Generator Mode from the icons at the left of your screen and select DCLOCK, then place it appropriately as depicted in the figure. Repeat the process for DC source.
3. Set the DC source to 5 volts and clock frequency and period to 1.
4. Set J=1 and K=0(SW1 close, SW2 open), and observe the output.
5. Next set J=0 and K=0(SW1 open, SW2 open). What happens to the output?
6. Set J=0 and K=1
7. Set J=1 and K=1
8. When the output is 1 (LED ON), set Reset to 1(SW4 pressed) and observe.
9. Set all switches to zero except SW3 and observe.
10. Editing the properties of the oscilloscope
    - Right click on the Oscilloscope and select edit properties.
    - Run simulation
    - Set all 4 channels and Trigger to DC
    - Using the switches, emulate questions 4-downto-9 and observe this time the waveforms (show waveforms).
11. conclude