In the name of God

Computer Architecture: Assignment #4

Due on Friday, March 4, 2016

Dr. Zarandi 10:45 am

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Contents

Problem 1

Computer A:$T_{access} = t_1 * h_1 + (1 - h_1) * (t_1 + t_2) = 0.98 * 2 + 0.02 * 20 = 2.36ns$
Computer B:$T_{access} = t_1 * h_1 + (1 - h_1) * (t_1 + t_2) = 0.90 * 1.2 + 0.1 * 20 = 3.08ns$

Problem 2

(a)

0	1	...	63	64
x	x	x	x	x
x	✓	✓	✓	x
x	✓	✓	✓	x

hit rate= 42/65 = 64.61%

(b)

With LRU replacement policy you the hit rate will be the zero because the in the second round all of the requiered addresses will be filled sequentially and none of the address will be hitted.
hit rate will be zero.

Problem 3

Memory size = 64*8 word=512 words.
Block size = 3 bits.
Cache set index = 2 bits.
Tag = 9-2-3 = 4 bits.
Number of bits for addressing a word = 9 bits.
Word size = 4 bytes.
Number of bits for finding relational position of a word = 3 bits.

Problem 4

(a)

3	3	3	0	0	0	4	4	4	4	4	4
null	2	2	2	3	3	3	3	3	1	1	1
null	null	1	1	1	2	2	2	2	2	0	0
miss	miss	miss	miss	miss	miss	miss	hit	hit	miss	miss	hit

miss rate=9/12=0.75

Problem 4 continued on next page...

(b)

3	3	3	3	3	3	4	4	4	4	0	0
null	2	2	2	2	2	2	3	3	3	3	4
null	null	1	1	1	1	1	1	2	2	2	2
null	null	null	0	0	0	0	0	0	1	1	1
miss	miss	miss	miss	hit	hit	miss	miss	miss	miss	miss	miss

miss rate = 10 / 12 = 0.833333

The problem is the wrong replacement policy because the data which has been added first isn't always the data that must be deleted. The replacement policy must be replaced with LRU so that the hit rate increases.