1.

(a) $64k = 2^{16}$

6 bit tag	8 bit index	2 bit relational position

number of bits for block = 2 bits = 4 position.
number of bits for index = size of cache (block form) = 8 bits.
number of bits for tag = 6 bits.

(b) 16 bits.

(c) $2^{10}/4 = 2^8 = 256$ blocks.

(d) $T_{access} = 100(h_1) + (1 - h_1)(1200) \leq 120 \rightarrow 1080 \leq 1100h_1$
$\rightarrow 1 \geq h_1 \geq 0.981818$

2. size of the cache is 16 blocks.

requested address	block-number	tag	hit 1	hit 2	hit 3
0	0	0	x	✓	✓
21	5	1	x	✓	✓
23	7	1	✓	✓	✓
35	3	2	x	✓	✓
76	1	4	x	✓	✓
1	1	0	✓	✓	✓
66	2	4	✓	✓	✓
80	0	5	x	✓	✓
54	6	3	x	✓	✓
36	4	2	✓	✓	✓
24	8	1	✓	✓	✓
23	7	1	✓	✓	✓
75	11	4	✓	✓	✓

In the second and the third round all of the addresses are hitted because all of the requested addresses are less than 256.
Miss ratio = 6/42 = 1/7