1.

(a) $64k = 2^{16}$

6 bit tag	8 bit index	2 bit relational position

number of bits for block = 2 bits = 4 position.
number of bits for index = size of cache (block form) = 8 bits.
number of bits for tag = 6 bits.

(b) 16 bits.

(c) $2^{10}/4 = 2^8 = 256$ blocks.

(d) $T_{access} = 100(h_1) + (1 - h_1)(1200) \leq 120 \rightarrow 1080 \leq 1100h_1$
$\rightarrow 1 \geq h_1 \geq 0.981818$

2. size of the cache is 16 blocks.

requested address	tag	hit 1	hit 2	hit 3
0	0	x	✓	✓
21	1	x	✓	✓
23	1	✓	✓	✓
35	2	x	✓	✓
76	4	x	✓	✓
1	0	✓	✓	✓
66	4	✓	✓	✓
80	5	x	✓	✓
54	3	x	✓	✓
36	2	✓	✓	✓
24	1	✓	✓	✓
23	1	✓	✓	✓
75	4	✓	✓	✓

In the second and the third round all of the addresses are hitted because all of the requested addresses are less than 256.
Miss ratio = 6/42 = 1/7

3.

(a)

requested addresses	tag	hit	number of fulled	row
0	0	x	1	0
1	0	✓	1	0
15	3	x	2	0
14	3	✓	2	0
14	3	✓	2	0
15	3	✓	2	0
16	4	x	1	1
2	0	✓	2	0
23	5	x	2	1
27	6	x	3	1
16	4	✓	3	1
2	0	✓	2	0
23	5	✓	3	1
27	6	✓	3	1
16	4	✓	3	1
14	3	✓	2	0
1	0	✓	2	0
21	5	✓	3	1
22	5	✓	3	1
23	5	✓	3	1
22	5	✓	3	1
10	2	x	3	0
18	4	✓	3	1
15	3	✓	3	1
1	0	✓	3	0
0	0	✓	3	0
14	3	✓	3	0
28	7	x	4	1
25	7	✓	4	1

Hit ratio is equal to 0.72.

(b,c) These two states are the same.

requested address	tag	hit
0	0	x
1	0	✓
15	7	x
14	7	✓
14	7	✓
15	7	✓
16	8	x
2	1	x
23	11	x
27	13	x
16	8	✓
2	1	✓
23	11	✓
27	13	✓
16	8	✓
14	7	✓
1	0	✓
21	10	x
22	11	✓
23	11	✓
22	11	✓
10	5	x
18	8	✓
15	7	✓
1	0	✓
0	0	✓
14	7	✓
28	14	x
25	12	x