1.

(a) 
$$64k = 2^{16}$$

6 bit tag

umber of bits	for block	= 2  bits =	4 position.	

2 bit relational position

8 bit index

number of bits for block = 2 bits = 4 position. number of bits for index = size of cache (block form) = 8 bits. number of bits for tag = 6 bits.

- (b) 16 bits.
- (c)  $2^{10}/4 = 2^8 = 256$  blocks.
- (d)  $T_{access} = 100(h_1) + (1 h_1)(1200 + 100) \le 0.2 * 1200 \rightarrow 1060 \le 1200h_1$  $\rightarrow 1 \ge h_1 \ge 0.883333$
- 2. size of the cache is 16 blocks.

requested address	tag	hit 1	hit 2	hit 3
0	0	X	✓	✓
21	1	X	✓	✓
23	1	$\checkmark$	$\checkmark$	$\checkmark$
35	2	X	✓	<b>√</b>
76	4	X	✓	✓
1	0	$\checkmark$	✓	<b>√</b>
66	4	✓	✓	✓
80	5	X	✓	✓
54	3	X	✓	✓
36	2	✓	✓	✓
24	1	✓	✓	✓
23	1	✓	✓	✓
75	4	✓	✓	✓

In the second and the third round all of the addresses are hitted because all of the requested addresses are less than 256.

Miss ratio = 6/42 = 1/7

3.

(a)

requested addresses	tag	hit	number of fulled	row
0	0	X	1	0
1	0	<b>√</b>	1	0
15	3	Х	2	0
14	3	<b>√</b>	2	0
14	3	<b>√</b>	2	0
15	3	<b>√</b>	2	0
16	4	X	1	1
2	0	<b>√</b>	2	0
23	5	X	2	1
27	6	X	3	1
16	4	<b>√</b>	3	1
14	3	<b>√</b>	2	0
1	0	<b>√</b>	2	0
21	5	$\checkmark$	3	1
22	5	<b>√</b>	3	1
23	5	<b>√</b>	3	1
22	5	<b>√</b>	3	1
10	2	X	3	0
18	4	<b>√</b>	3	1
15	3	<b>√</b>	3	1
1	0	<b>√</b>	3	0
0	0	<b>√</b>	3	0
14	3	<b>√</b>	3	0
28	7	X	4	1
25	6	<b>√</b>	4	1

Hit ratio is equal to 0.72. Final state of cache:

0	1	2	3	null	null	null	null	8	9	10	11	12	13	14	15
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

(b,c) These two states are the same.

requested address	tag	hit
0	0	X
1	0	X 🗸
15	7	X 🗸
14	7	<b>√</b>
14		<b>√</b>
15	7	<b>√</b>
16	8	X
2	1	X
23	11	X
27	13	X ✓ ✓
16	8	<b>√</b>
14	7	$\checkmark$
1	0	<b>√</b>
21	10	X ✓
22	11	<b>√</b>
23	11	<b>√</b>
22	11	$\checkmark$
10	5	X
18	8	$\checkmark$
15	7	✓ ✓
1	0	✓ ✓
0	0	<b>√</b>
14	7	<b>√</b>
28	14	X
25	12	X

The hit ratio is equal to 0.56

4. Time of not finding requested data in cache = 70ns.  $T_{access} = 0.95*10 + 0.05*(60+10) = 13.0ns$