Digital Systems - Homework 02 - Group 5

Group members

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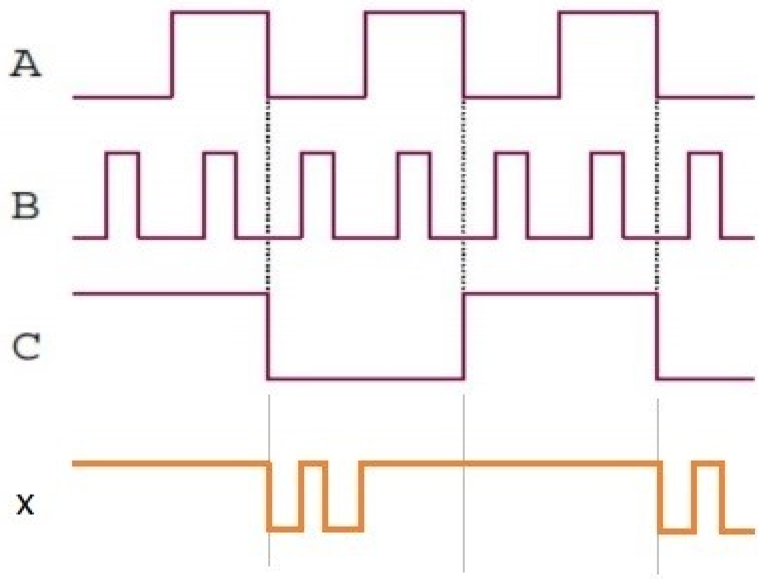
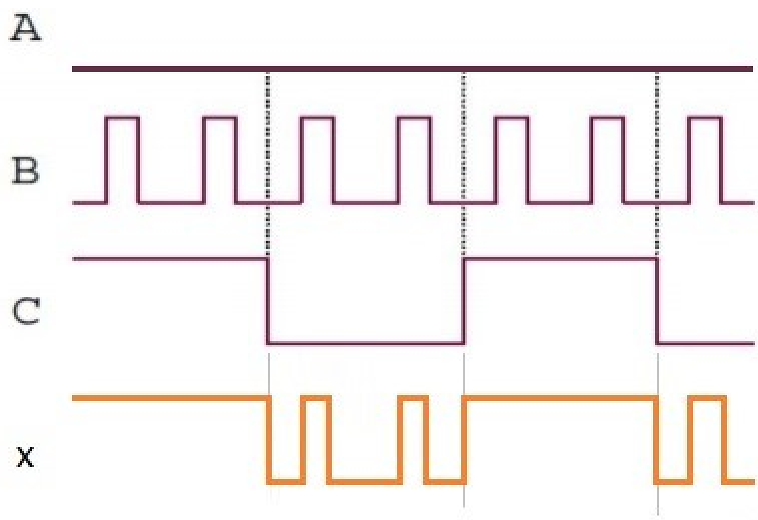
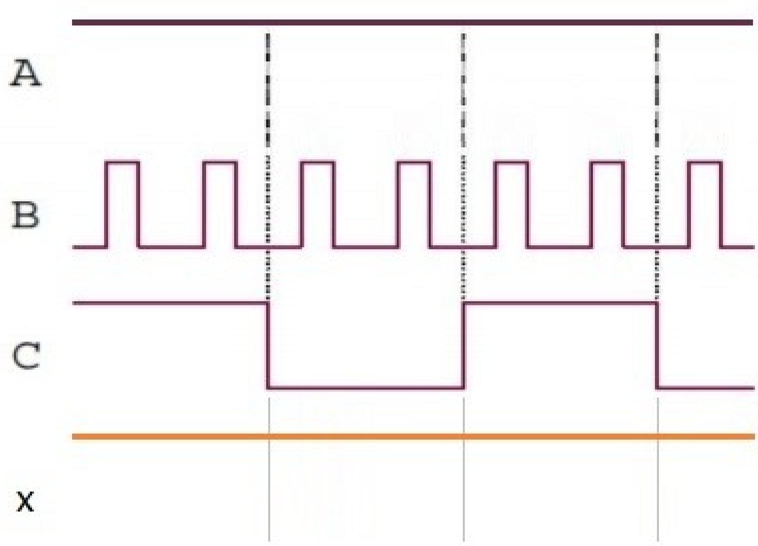
Problem 1.



Problem 2.

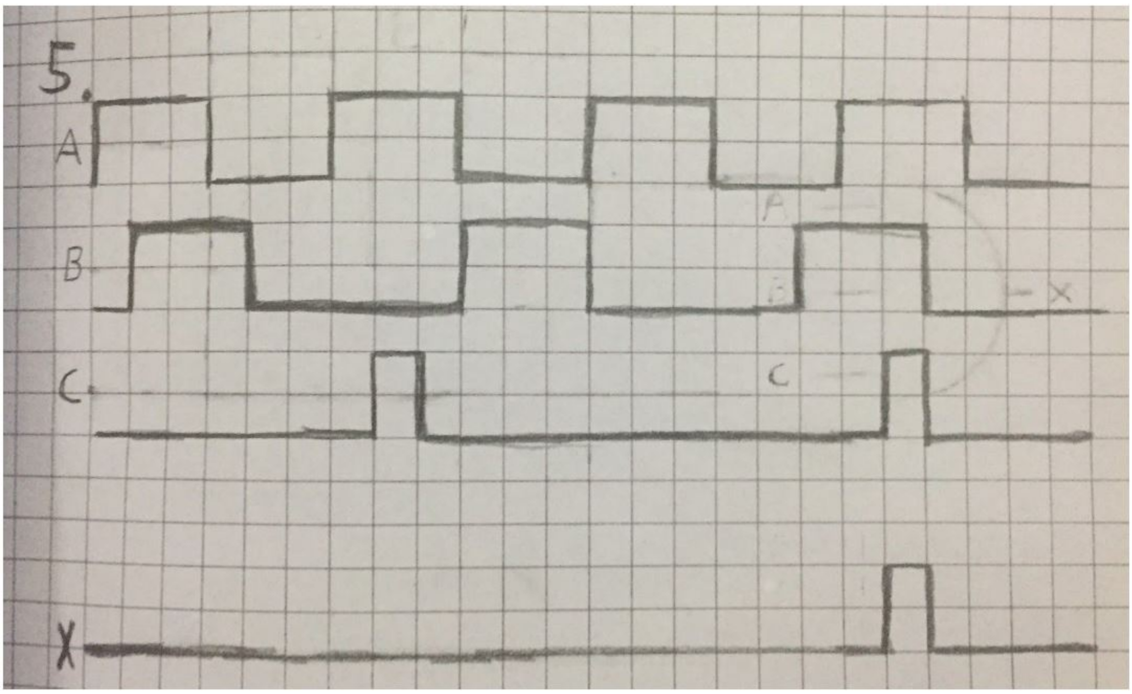


Problem 3.

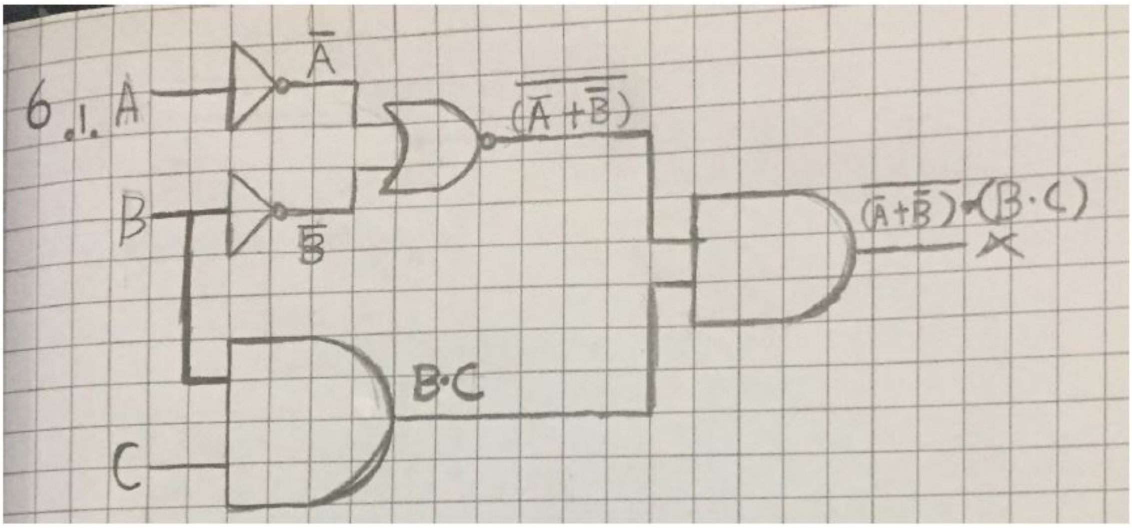


Problem 4. The number of entries corresponds to the number of inputs. So, there are $2^5 = 32$ entries in 5 input table. Also, in general, the output of an OR gate is HIGH whenever one or more inputs are HIGH. Therefore, $2^5 - 1 = 31$ entries.

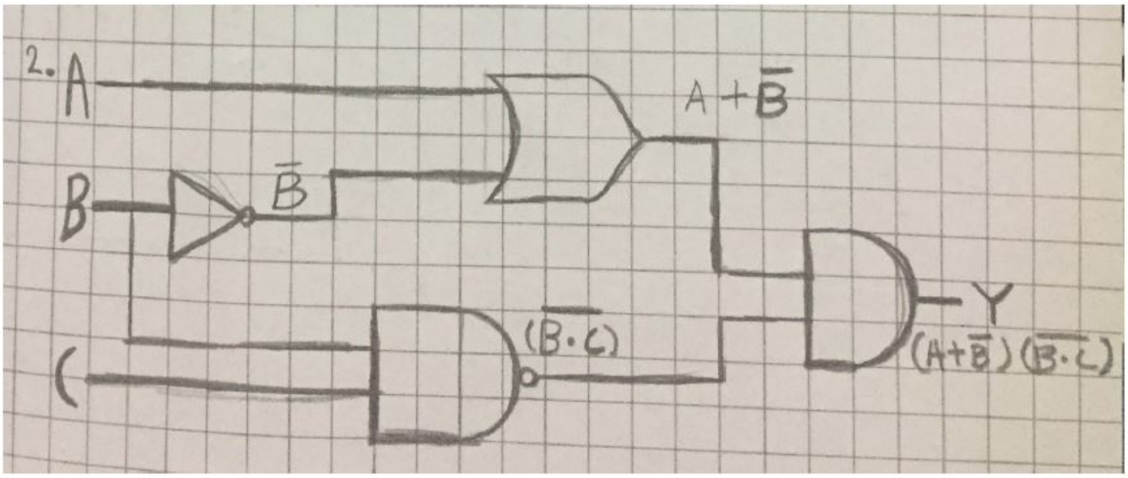
Problem 5.



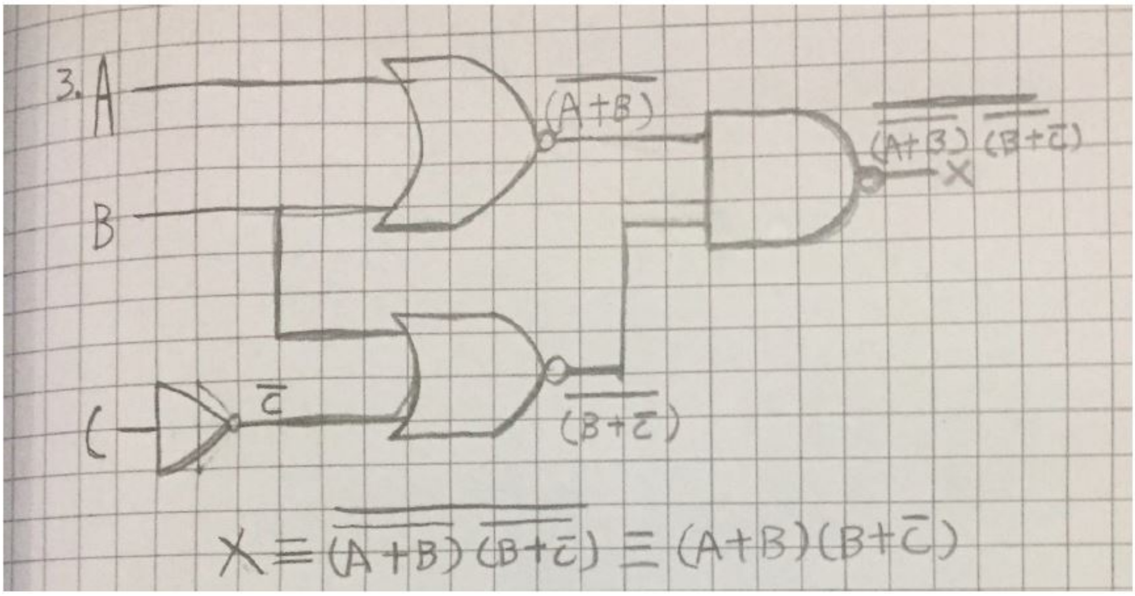
Problem 6.



A	B	C	X
1	1	1	1
1	0	0	0
0	1	0	0
0	0	1	0
1	1	0	0
1	0	1	0
0	1	1	0
0	0	0	0



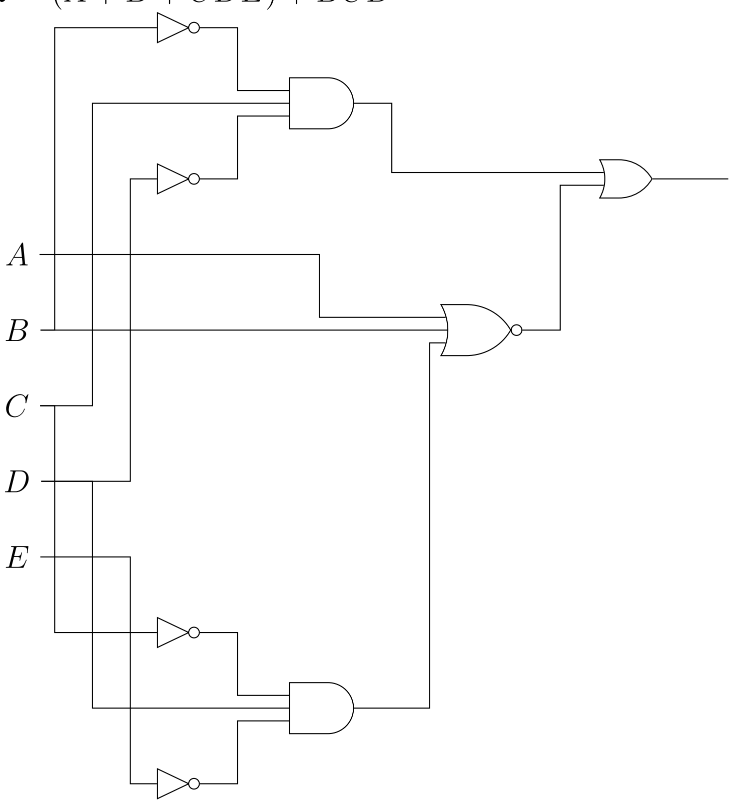
A	B	C	Y
1	1	1	0
1	0	0	1
0	1	0	0
0	0	1	1
1	1	0	0
1	0	1	1
0	1	1	0
0	0	0	1



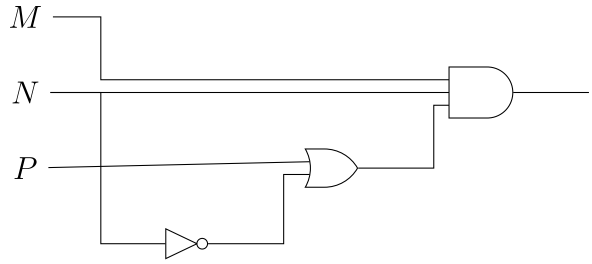
A	B	C	X
1	1	1	1
1	0	0	1
0	1	0	1
0	0	1	0
1	1	0	1
1	0	1	0
0	1	1	1
0	0	0	0

Problem 7.

1. $z = (\overline{A + B + \bar{C}D\bar{E}}) + \bar{B}C\bar{D}$



2. $x = MN(P + \bar{N})$



Problem 8. Simplify the following expressions using De Morgans theorem:

a)

$X = \overline{A * \overline{\overline{B + \overline{C}}} * D}$
$= \overline{A} + B + \overline{C} + \overline{D}$

b)

$Y = \overline{\overline{\overline{A * B} * C} * D}$
$= \overline{A * B} * C + \overline{D}$
$= (\overline{A} + \overline{B}) * C + \overline{D}$

Problem 9. Simplify the following expressions:

a)

$X = \overline{A}*B*C*D + A*\overline{B}*\overline{C}*\overline{D} + A*\overline{B}*(\overline{\overline{C} + D}) + A(\overline{B + C})*D + A*(\overline{B + \overline{C} + \overline{\overline{D}}} + B*\overline{C}) + ABC$
$= \overline{A}*B*C*D + (A*\overline{B}*\overline{C}*\overline{D} + A*\overline{B}*C*\overline{D}) + (A*\overline{B}*\overline{C}*D + A*\overline{B}*C*D) + (A*B*\overline{C} + A*B*C)$
$= \overline{A} * B * C * D + (A * \overline{B} * \overline{D} + A * \overline{B} * D) + A * B$
$= \overline{A} * B * C * D + (A * \overline{B} + AB)$
$= \overline{A} * B * C * D + A$

$= A + BCD$

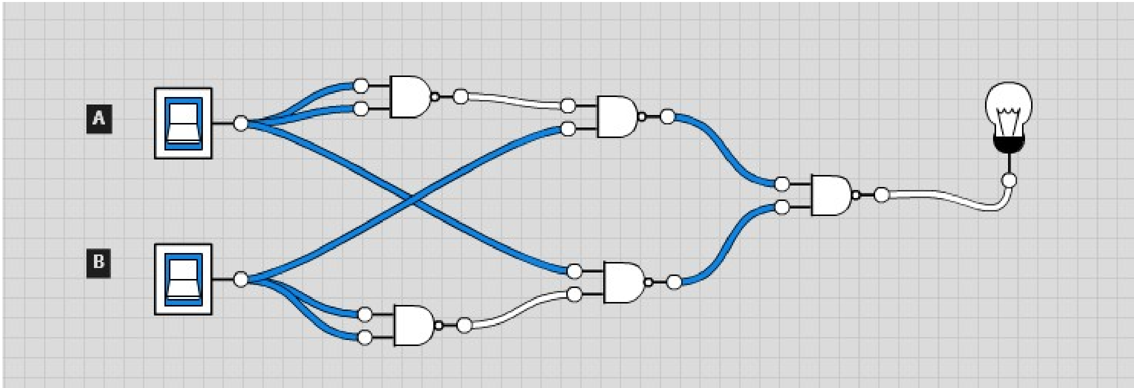
b)

$Y = \overline{A} * C * \overline{D} + A * \overline{B} * \overline{C} + (\overline{C + D}) + \overline{A} * \overline{B} * C * D + (\overline{\overline{A} + \overline{C}}) * \overline{D}$
$= \overline{A} * C * \overline{D} + A * \overline{B} * \overline{C} + \overline{C} * \overline{D} + \overline{A} * \overline{B} * C * D + A * C * \overline{D}$
$= (\overline{A} * C * \overline{D} + A * C * \overline{D}) + \overline{C} * \overline{D} + A * \overline{B} * \overline{C} + \overline{A} * \overline{B} * C * D$
$= (C * \overline{D} + \overline{C} * \overline{D}) + A * \overline{B} * \overline{C} + \overline{A} * \overline{B} * C * D$
$= (\overline{D} + \overline{A} * \overline{B} * C * D) + A * \overline{B} * \overline{C}$
$= \overline{D} + \overline{A} * \overline{B} * C + \overline{A} * \overline{B} * C$
$= \overline{B} * (A * \overline{C} + \overline{A} * C) + \overline{D}$

Problem 10.

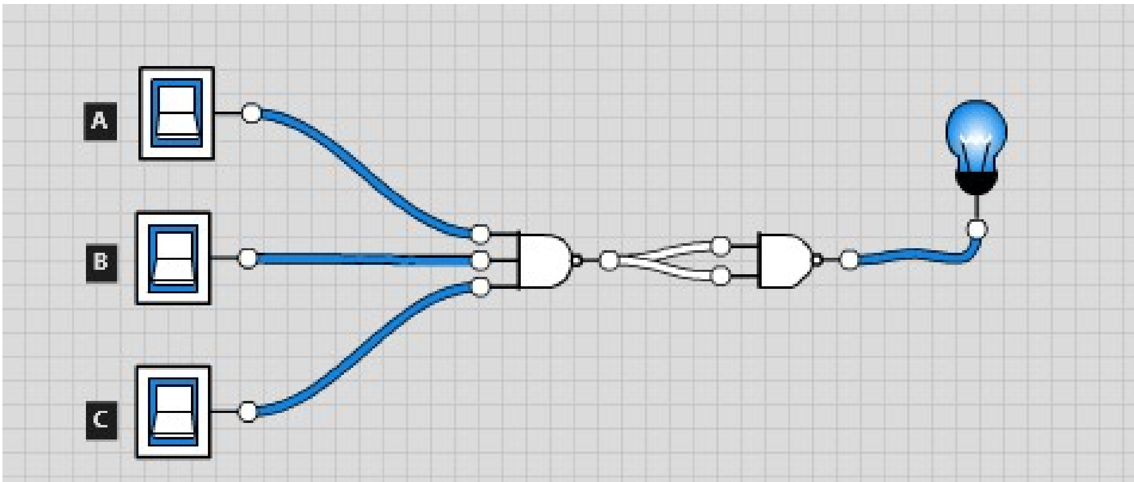
- Transforming $X = AB + BA$ into NAND only:

$$\rightarrow X = ((A'B)'.(B'A)')'$$



- Transforming $X = (A' + B')'.BC$ into NAND only:

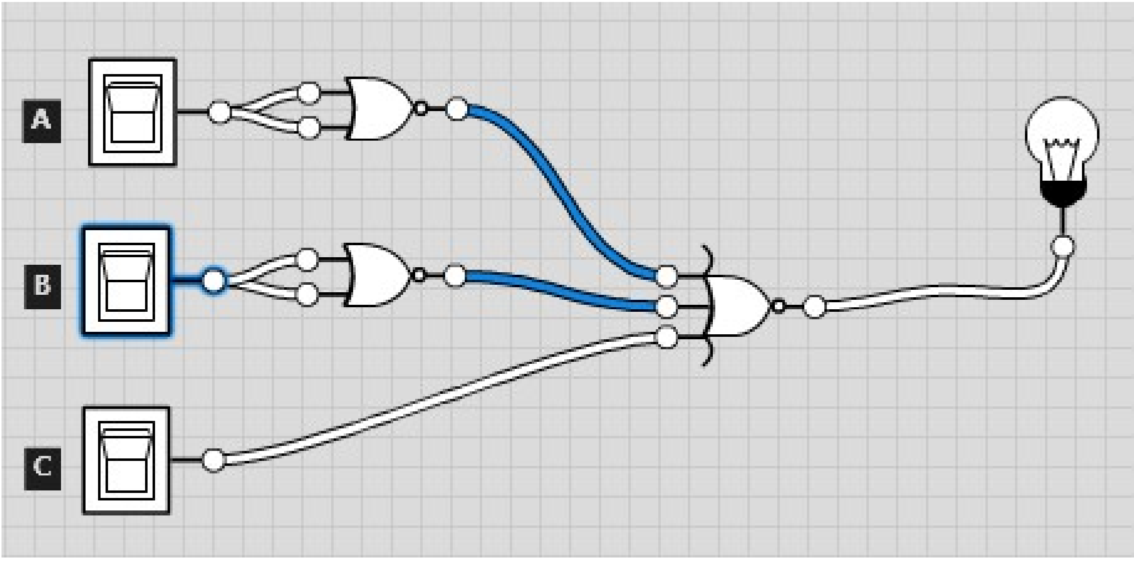
$$\rightarrow X = ((ABC)')'$$



Problem 11.

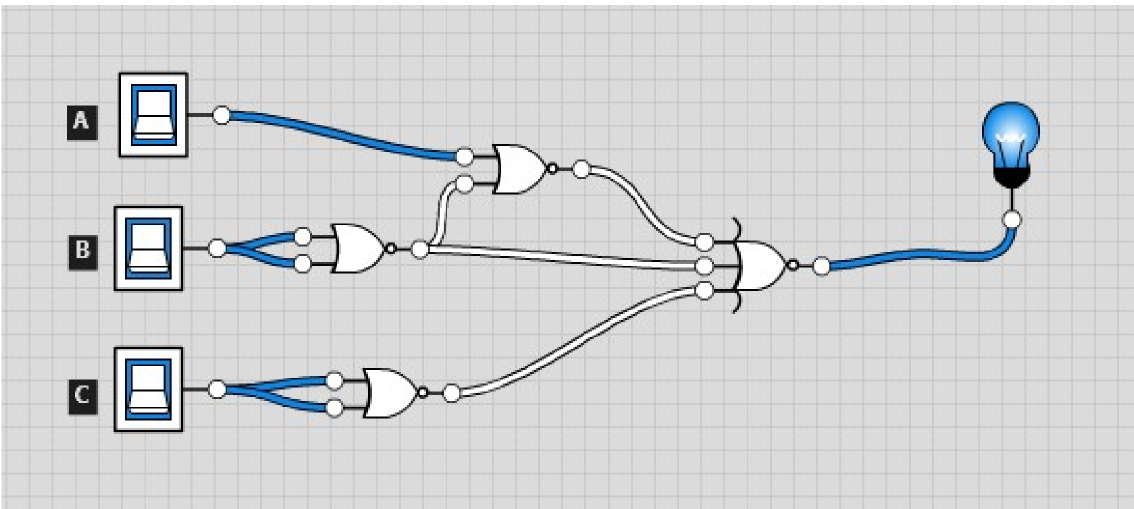
- Transforming $X = AB.(B' + C)'$ into NOR only:

$$\rightarrow X = (A' + B' + C)'$$



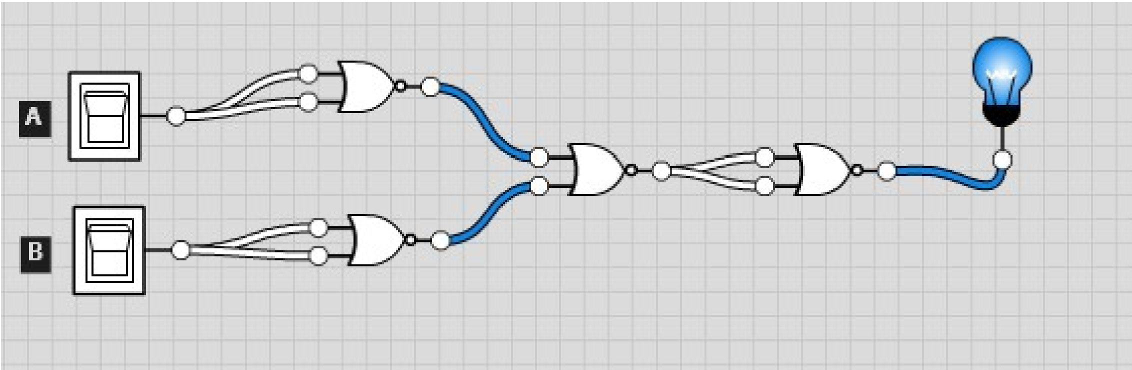
- Transforming $X = (A + B).BC$ into NOR only:

$$\rightarrow X = ((A + B')' + B' + C')'$$

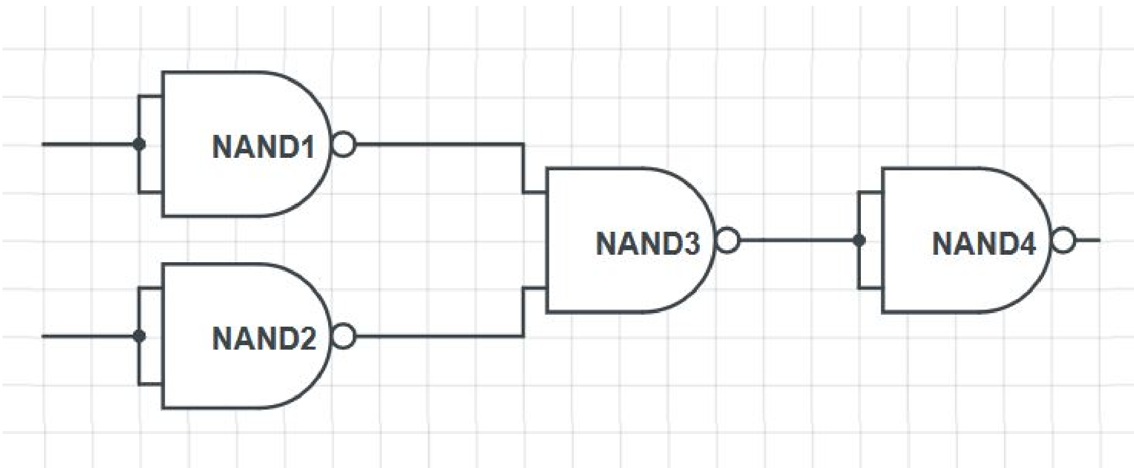


Problem 12. Build a 2-input NAND gate using only 2-input NOR gates

$$(AB)' = ((A' + B')')'$$

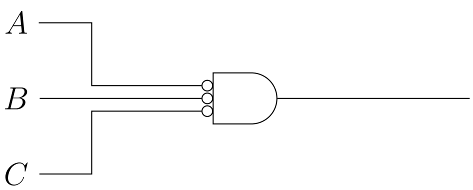


Problem 13. Build a 2-input NOR gate using only 2-input NAND gates

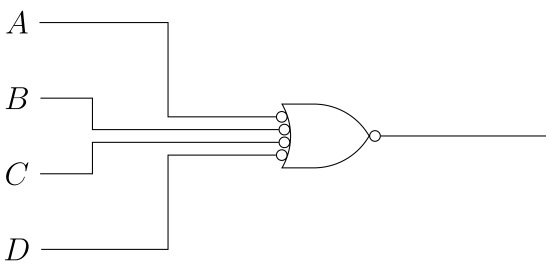


Problem 14. Draw the appropriate gate symbols for the following statements

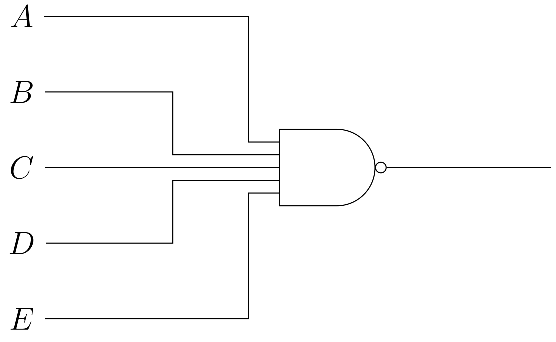
1. The output is HIGH (1) when all three inputs are LOW (0).



2. The output is LOW when any of the four inputs is LOW.



3. The output is LOW when all 5 inputs are HIGH.



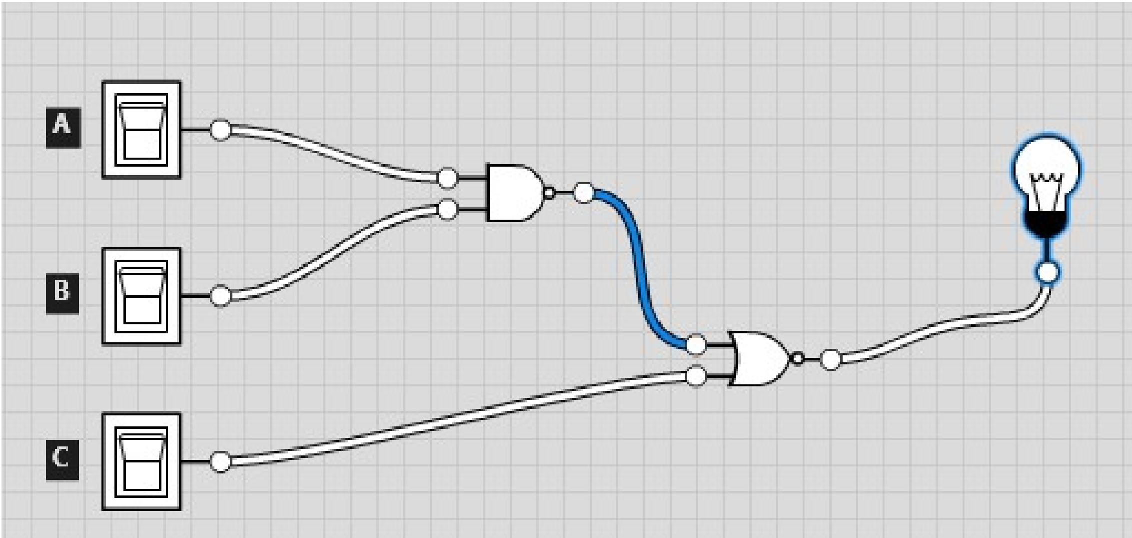
Problem 15.
According to the De Morgan's theorem, we can change the OR (2) gate to a NAND gate.

Problem 16.
For the LED to be ON, the final output needs to be LOW, either:

- E is high
- C is low and D is high
- B is low, and A is low or D is high

Problem 17. Implement $X = ABC'$ using only 1 2-input NOR gate and 1 2-input NAND gate

$$\rightarrow X = ((AB)' + C)'$$



Problem 18. Implement $Y = ABCD$ uses only 2-input NAND gates.

$$\rightarrow Y = ((((AB)')'.((CD)')')')'$$