BOOLEAN ALGEBRA & LOGIC GATES

Basic

1. Draw the timing diagram for the output signal x of the OR gate.

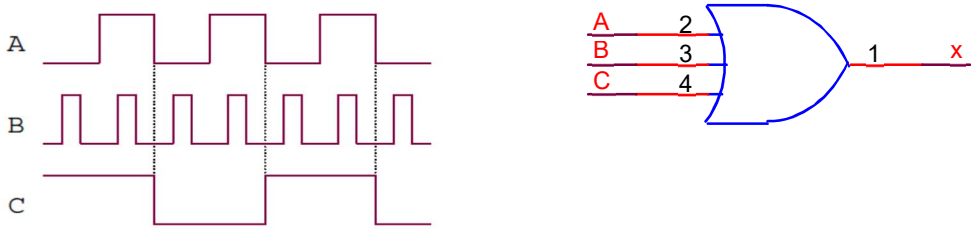

Figure 1

2. Suppose signal A in Figure 1 is grounded - GND (A = 0). Draw the timing diagram for the OR signal of the gate.

3. Suppose signal A in Figure 1 is +5V – VCC (A = 1). Draw the timing diagram for the OR signal of the gate.

4. With 5-inputs OR gate, how many input entries allow for high output (HIGH or 1)?

5. Draw the timing diagram for the output signal x of the AND gate.

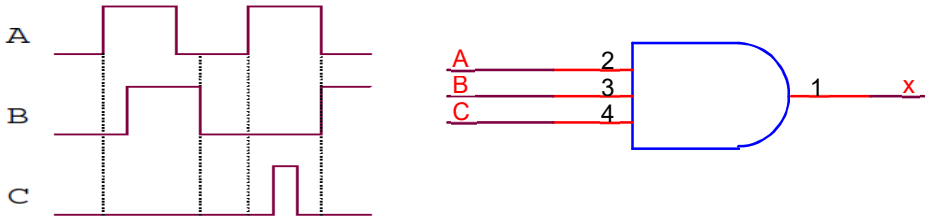

Figure 2

6. Write the Boolean expresion and truth table for the outputs of the circuits below

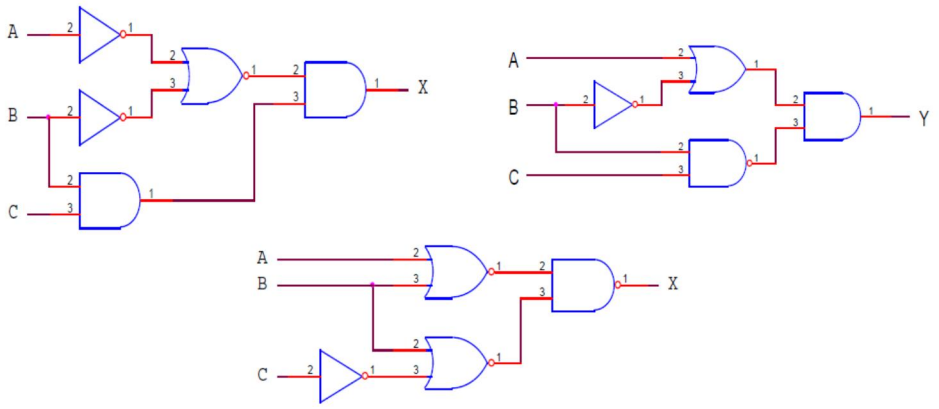

Figure 3

7. Draw logic circuits corresponding to the following Boolean expressions:

(a) $z = \overline{(A + B + \bar{C}D\bar{E})} + \bar{B}C\bar{D}$

(b) $x = MN(P + \bar{N})$

8. Simplify the following expressions using DeMorgan's theorem:

(a) $X = \overline{A\overline{(B + \bar{C})}D}$

(b) $Y = \overline{\overline{A\bar{B}C}D}$

9. Simplify the following expressions:

(a) $X = \bar{A}BCD + A\bar{B}\bar{C}\bar{D} + A\bar{B}\overline{(\bar{C} + D)} + A\overline{(B + C)}D + A\overline{(B + \bar{C} + \bar{D} + B\bar{C})} + ABC$

(b) $Y = \bar{A}C\bar{D} + A\bar{B}\bar{C} + \overline{(C + D)} + \bar{A}\bar{B}CD + \overline{(\bar{A} + \bar{C})}\bar{D}$

10. Transform the following circuits using only NAND gates

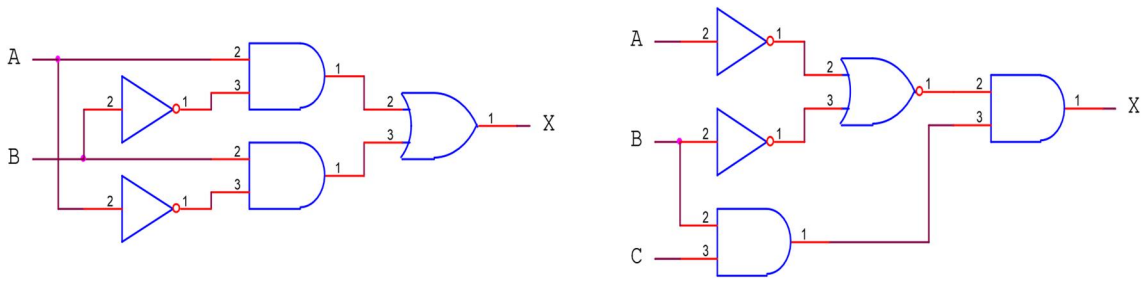

Figure 4

11. Transform the following circuits using only NOR gates

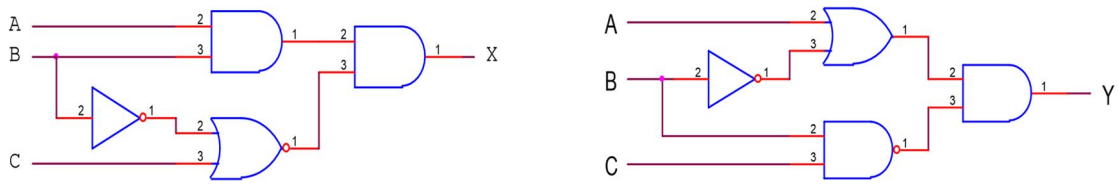

Figure 5

12. Build a 2-input NAND gate using only 2-input NOR gates.

13. Build a 2-input NOR gate using only 2-input NAND gates.

14. Draw the appropriate gate symbols for the following statements:

(a) The output is HIGH (1) when all three inputs are LOW (0).

(b) The output is LOW when any of the four inputs is LOW.

(c) The output is LOW when all 5 inputs are HIGH.

15. The logic circuit in Figure 6 is being used to activate an alarm when its output f goes LOW. Modify the circuit diagram so that it represents the circuit operation more effectively.

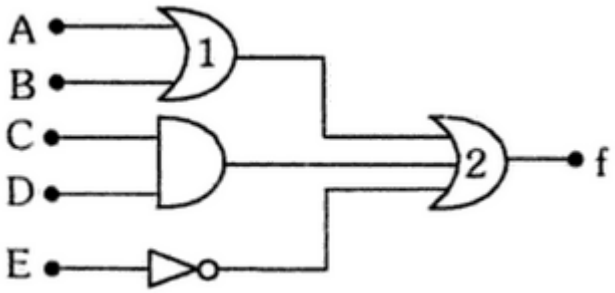

Figure 6

16. Determine the input conditions necessary to activate LED on.

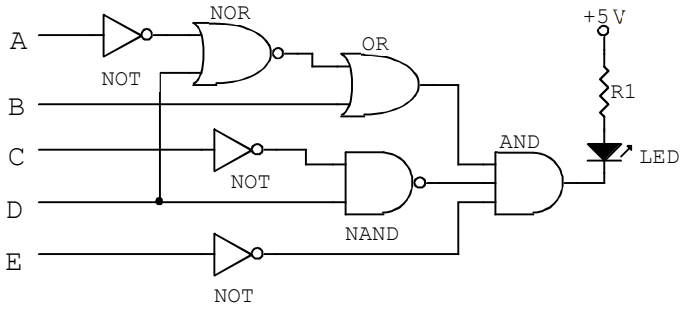

Figure 7

Advance

17. Implement $x = AB\bar{C}$ uses only 1 2-input NOR gate and 1 2-input NAND gate.

18. Implement *y=ABCD* uses only 2-input NAND gates.