Tutorial 2

1 Introduction

1.1 Target

- Practice design using RTL model, the structure model, and behavior model.
- Arithmetic and MSI circuit.
- Use Quartus software to describe ICs, simulation and check the operation in the DE2i-150 board.

1.2 Requirement

- Revise the Chapter 5 about Arithmetic.
- Read the tutorial and finish all requirement before going to class.
- Do all exercises in Part 3 and take more practice (from books or Internet) after class.

1.3 Content

- Design and implement arithmetic and MSI circuit.
- Implement the ICs: 7447, 74138, 74151 and 7490 in Verilog using RTL, structure and behavior model.
- Simulation the ICs implemented in Quartus software.
- Using implemented ICs to design some simple circuit.
- Install the designed to the DE2i-150 board (optional).

2 Background

2.1 Design with Module - RTL model

There are different ways to describe a module using:

- Structure model: Connect primitives and modules.
- **RTL** model: Continuous assignment.
- Behavior model: initial and always block.

Example in using the RTL model for **majority** circuit:

```
module majority (major, V1, V2, V3) ;

output major ;
input V1, V2, V3 ;

assign major = V1 & V2
             | V2 & V3
             | V1 & V3;
endmodule
```

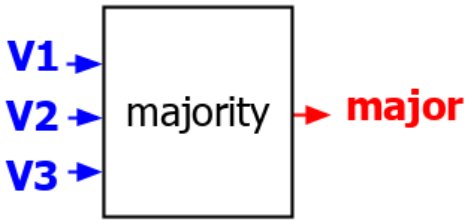


Figure 1: Majority with RTL model

Similarly to majorrity, implement the Full-Adder using RTL model in Figure 2:

```
module fa_rtl (A, B, CI, S, CO) ;

input A, B, CI ;
output S, CO ;

// use continuous assignments
assign S =
assign C0 =

endmodule
```

Figure 2: Full-Adder with RTL model

2.2 IC7447 and LED 7-seg

The construction of 7-segment LED:

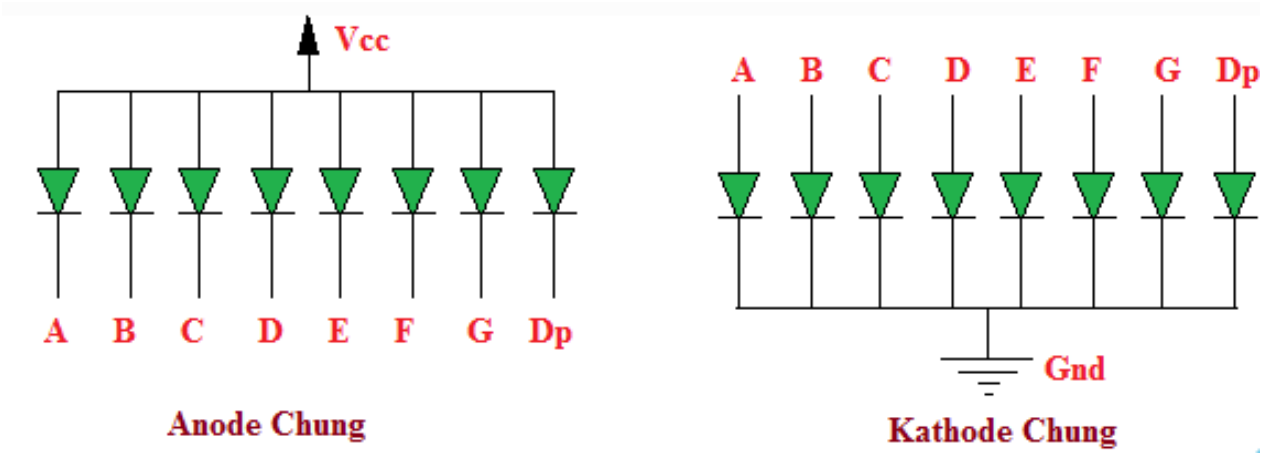


Figure 3: Two types in connection of LED 7-seg.

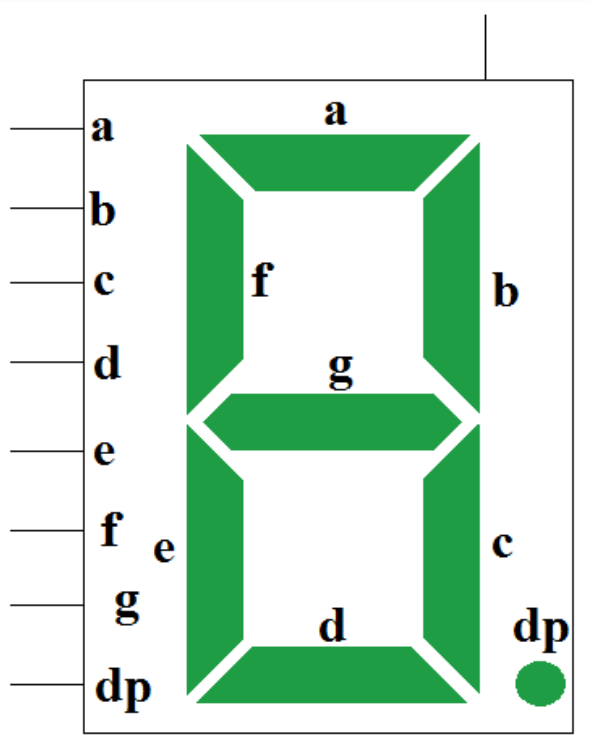


Figure 4: 7-Segment with dot.

The code for LED 7-seg with Common Anode is provided as Figure 5 below. What is the code for LED 7-seg with Common Cathode?

Số	Số nhị phân								HEX
	7	6	5	4	3	2	1	0	
	dp	g	f	e	d	c	b	a	
0	1	1	0	0	0	0	0	0	C0
1	1	1	1	1	1	0	0	1	F9
2	1	0	1	0	0	1	0	0	A4
3	1	0	1	1	0	0	0	0	B0
4	1	0	0	1	1	0	0	1	99
5	1	0	0	1	0	0	1	0	92
6	1	0	0	0	0	0	1	0	82
7	1	1	1	1	1	0	0	0	8F
8	1	0	0	0	0	0	0	0	80
9	1	0	0	1	0	0	0	0	90
A	1	0	0	0	1	0	0	0	88
B	1	0	0	0	0	0	1	1	83
C	1	1	0	0	0	1	1	0	C6
D	1	0	1	0	0	0	0	1	A1
E	1	0	0	0	0	1	1	0	86
F	1	0	0	0	1	1	1	0	8E

Figure 5: Common Anode.

2.3 IC 74LS90 Decade Counter

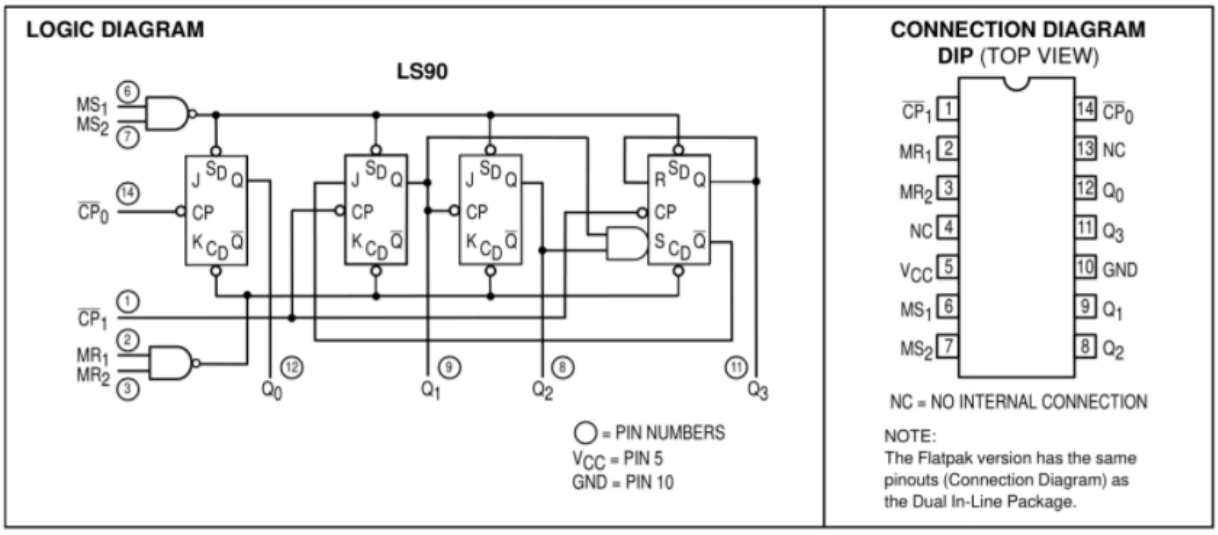


Figure 6: 74LS90 Pin.

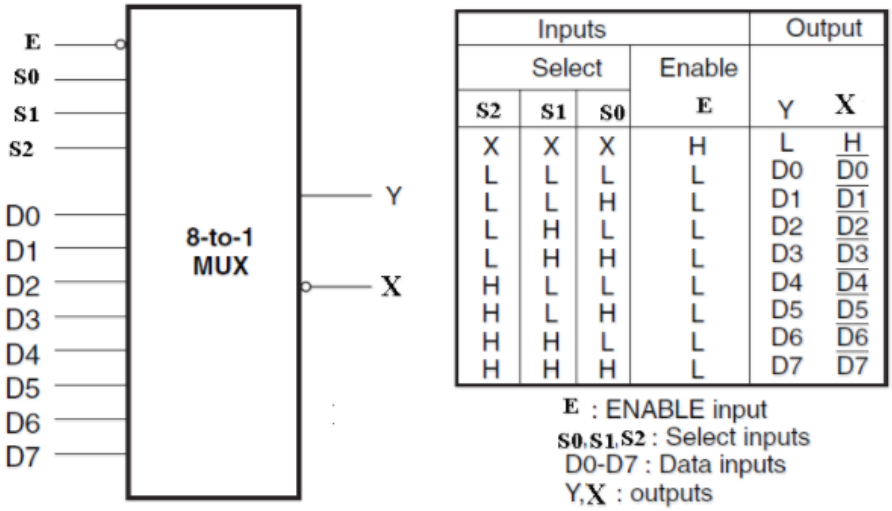
LS90
MODE SELECTION

RESET/SET INPUTS				OUTPUTS			
MR_1	MR_2	MS_1	MS_2	Q_0	Q_1	Q_2	Q_3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	Count			
X	L	X	L	Count			
L	X	X	L	Count			
X	L	L	X	Count			

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Figure 7: 74LS90 Truth Table.

2.4 IC 74LS151 - Multiplexer



Inputs				Output	
Select			Enable		
S2	S1	S0	E	Y	X
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

E : ENABLE input
S0,S1,S2 : Select inputs
D0-D7 : Data inputs
Y,X : outputs

Figure 8: 74LS151 Truth Table.

2.5 IC 74LS138 - Decoder

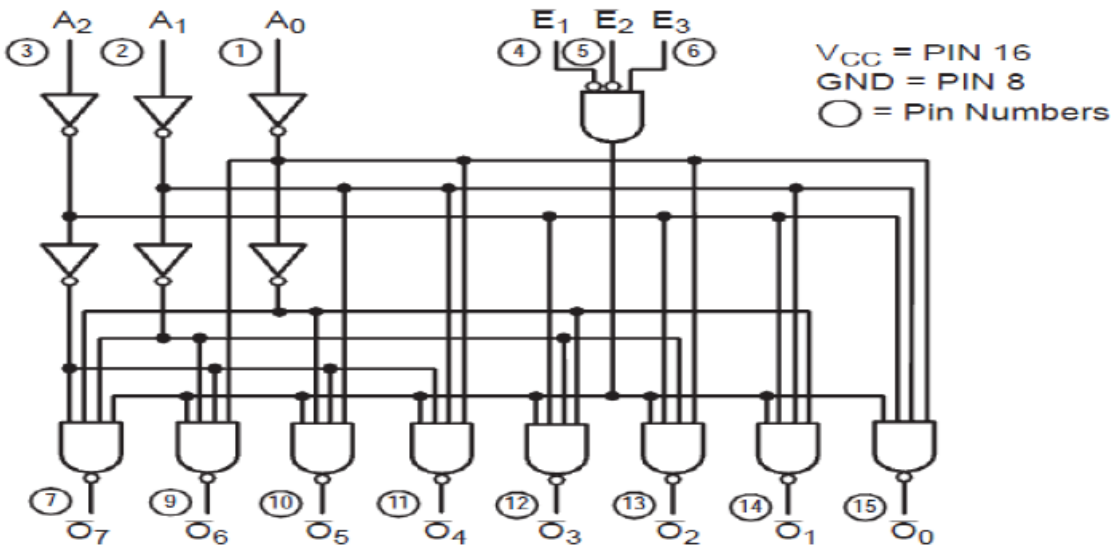


Figure 9: 74LS138.

TRUTH TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Figure 10: 74LS138 Truth Table.

3 Exercise

Report Requirement:

- Present the design in step by step, truth table and K-map (if needed for design)
- The RTL result generated from Quartus software.
- Waveform result (Take 1 or 2 picture that include some main cases).

Note that, all the design must run simulation (waveform) before compilation or install to the DE2i-150 board.

Exercise 1: (0.5p) Implement a circuit with functional **similar to** IC 7447 using **RTL model** with interfaces:

- Input: 5 signals: A, B, C, D and reset. Therein, ABCD (A is MSB) is the BCD code input, reset signal is active low (0).
- Output: 7 signals: a, b, c, d, e, f and g. Therein, 7 signals is the 7 segments of LED 7-seg. When reset signal active, Led 7-seg should turn off, in contrast, reset the 7 signals output will depend on the input ABCD.

Suggestion:

- You should read the DE2i-150 manual to find the LED 7-seg in the DE2i-150 is Common Anode or Common Cathode.
- We only use one reset signal in this design.
- The RTL model could be helpful.

Exercise 2: (1p) Implement IC 74LS90 in Quartus, run the simulation then use this IC to design a MOD 9 counter (0-¿8).

Exercise 3: (1p) Creating Parallel 4 bits Full Adder with Register Designing a 4-bit Adder using a Full Adder component. This one requires the circuit can add 4-bits in parallel. Furthermore, this practice expects the student to include LOAD, CLEAR and TRANSFER signal in the design.

Exercise 4: (1p) Two's complement Circuit Design the logic circuit that receives input and transfers it into two's complement value. The two's complement operation is simply a one's complement which inverts all the input bits followed by the addition of "1" value to the result.

Exercise 5: (1.5p) Implement a Multiplexer which is **similar to** IC 74151, with interfaces:

- Input: 12 signals include:
  - 3 Select signals S_{0-2}.
  - 1 active low enable E signal.
  - 8 Data signals I_{0-7}
- Output: 2 signals Z and $\bar{Z}$.

Requirements: You should implement in two following ways:

- From truth table, use the K-map or Boolean expression to simplify Output signal. Then use the RTL model (continuous assignment) to implement the Oputput signal.
- Using both RTL and structure model by implement the 2-to-1 multiplexer using RTL (Figure 11). Then connect those 2-to-1 muxs into 8-to-1 mux (Hình 12).

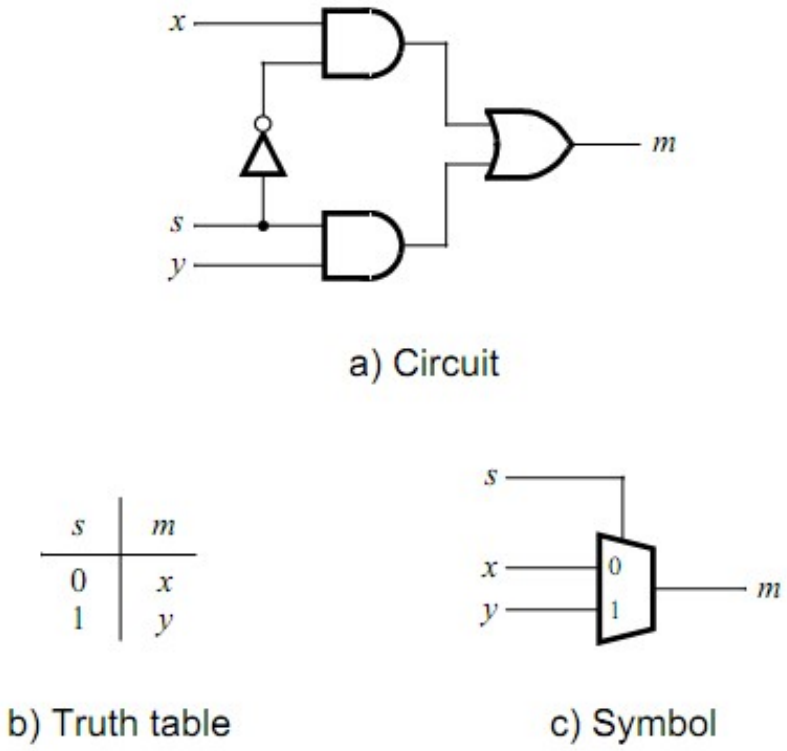


Figure 11: 2-to-1 multiplexer.

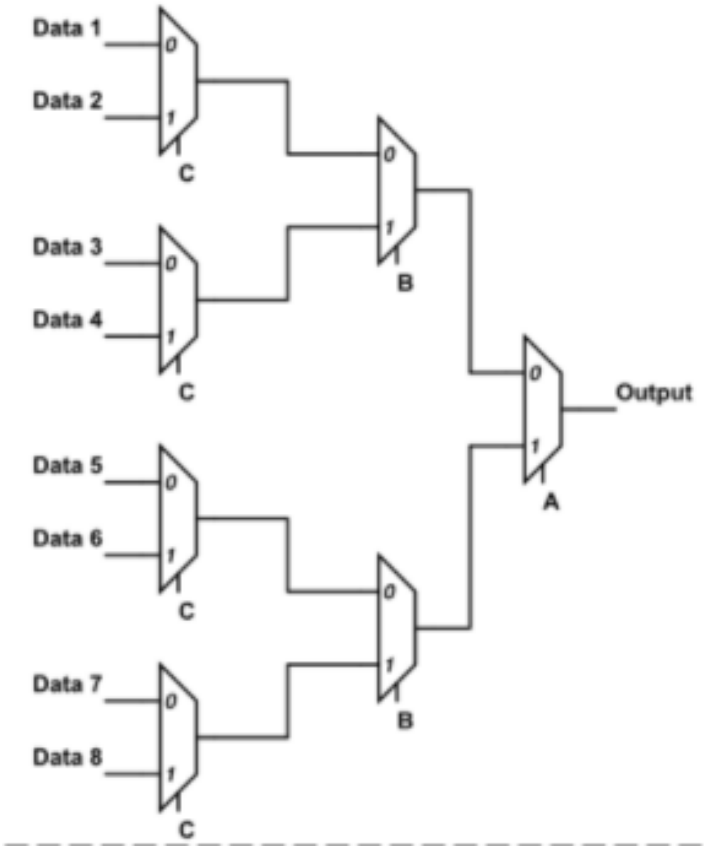


Figure 12: 8-to-1 from 2-to-1 multiplexer.

Exercise 6: (1p) Implement the Demultiplexer which is **similar to** IC 74138, with interfaces:

- Input: 6 signals include:
  - 3 Address signals A_{0-2}.
  - 3 Enable signals E_0 active high, E_1 and E_2 active low.
- Output: 8 active low signals O_{0-7} .

Exercise 7: (1p) Design circuit use implemented Multiplexer from the previous exercise with functionality:

- $F(A, B, C, D) = \sum(1, 5, 9, 13)$
- $F(A, B, C, D) = \sum(2, 3, 8, 11)$

Exercise 8: (1p) Design circuit use implemented Demultiplexer from previous exercise with functionality:

- $F(A, B, C, D) = \sum(1, 5, 9, 13)$
- $F(A, B, C, D, E) = \sum(1, 9, 17, 21)$

Exercise 9: (2p) For good report!