Review Midterm

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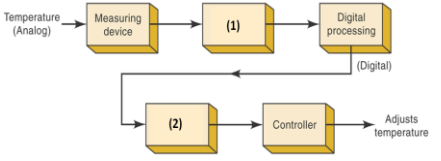
Overview

1. Choose the right answer to complete the diagram for a precision temperature regulation system.



A. (2) Digital-to-analog converter – (1) Analog-to-digital converter
B. (2) Analog-to-analog converter – (1) Digital-to-digital converter
C. (2) Digital-to-analog converter – (1) Analog-to-digital converter
D. (2) Analog-to-analog converter – (1) Digital-to-digital converter

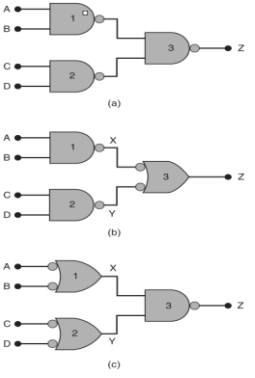
2. Which of the following is the most widely used alphanumeric code for computer input and output?

- A. Gray B. BCD C. Parity D. ASCII

Boolean

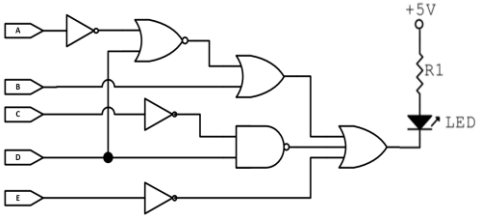
1. Which images is suitable the most with this description: “Output Z will go LOW only when A or B is LOW and C or D is LOW”.

A. a
B. b
C. c
D. All of them



Boolean

2. Define the combination of inputs for the circuit to make LED ON:



A. LED ON when B = 0 and C = 0 and D = 1 and E = 1
B. LED ON when A = 1 and B = 0 and C = 0 and D = 0 and E = 1
C. LED ON when A = 0 and B = 0 and C = 0 and D = 1 and E = 0
D. LED ON when A = 1 and B = 0 and C = 1 and D = 0 and E = 0

Kmap

- Find the minimum Boolean function F(ABC) in SOP form from the following k-map:
-

		BC			
		00	01	11	10
A	0	x	1	0	x
	1	1	x	x	1

- a. F = AC'+B'
- b. F = A+B
- c. F = B'+C'
- d. Both b and c are true

Flip-flop

1. The circuit that is primarily responsible for certain flip-flops to be designated as edge-triggered is the:
   A. NAND latch.
   B. NOR latch.
   C. pulse-steering circuit.
   D. edge-detection circuit.

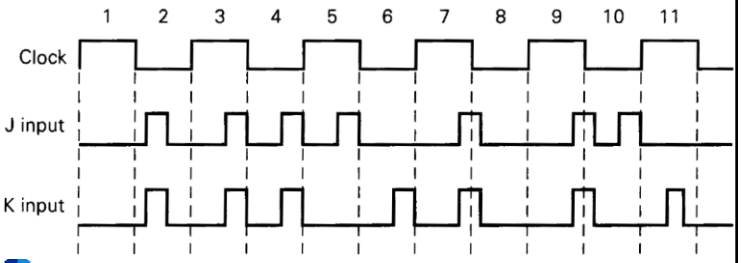
2. As a general rule for stable flip-flop triggering, the clock pulse rise and fall times must be:
   A. at a maximum value to enable the input control signals to stabilize.
   B. very long.
   C. of no consequence as long as the levels are within the determinate range of value.
   D. very short.

Flip-flop

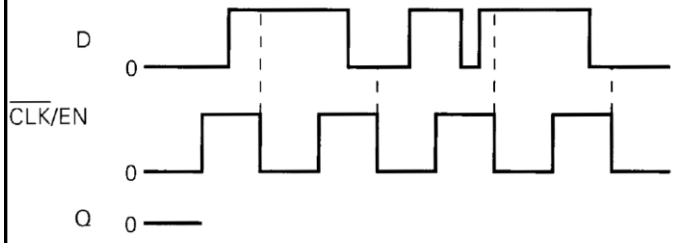
1. Edge-triggered flip-flops must have:
   A. active-low inputs and complemented outputs.
   B. a pulse transition or edge detector circuit.
   C. very fast response times.
   D. at least two inputs to handle rising and falling edges.

2. What is one disadvantage of an S-R flip-flop?
   A. It has only a single output.
   B. It has no CLOCK input.
   C. It has no Enable input.
   D. It has an invalid state.

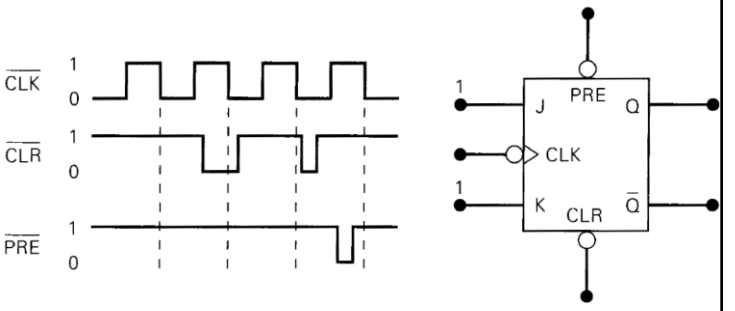
Problem: The waveforms below are to be applied to two different FF's. Draw Q for (a) positive edge-triggered (b) negative edge-triggered.



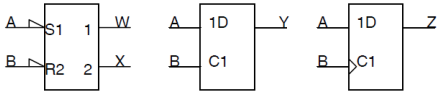
Problem: Compare the operation of the D latch with the negative edge-triggered D FF using the following waveforms.

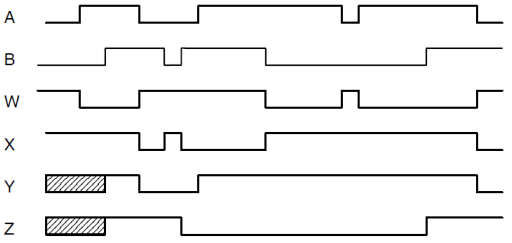


Problem:Determine the Q output



The signals A and B are applied to the inputs of an SR flip-flop (or Set-Clear FF), a transparent latch and a D-type flip-flop. Sketch the waveforms at W, X, Y and Z.





The circuit below is made from two D-type flip-flops with an asynchronous RESET input. Assume that Q0 and Q1 are both low initially and sketch a timing diagram showing the waveforms of CLOCK, Q0 and Q1 for the next six clock pulses.