COUNTERS & REGISTERS

1. Design a ripple counter, MOD-4, up counter, using J-K Flip-Flop and D Flip-Flop.

2. Design a ripple counter, MOD-12, up counter, using J-K Flip-Flop and D Flip-Flop.

3. (a) Design a ripple counter, MOD-16, down counter, using J-K Flip-Flop and D Flip-Flop.

(b) Suppose the counter is in state 0110, determines the state of the counter after the next 27 clock cycles.

4. Design a ripple counter, MOD-5, down counter, using J-K Flip-Flop and D Flip-Flop..

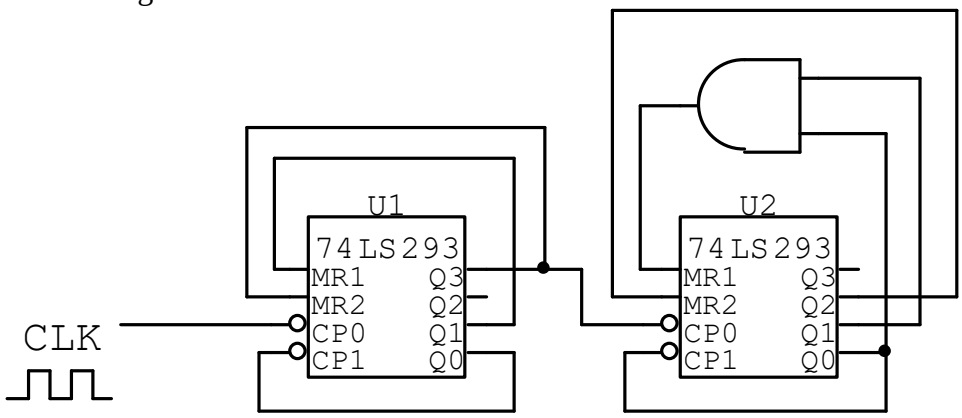
5. Use J-K Flip-Flop and D Flip-Flop to design an asynchronous counter as follows:

$$4 \rightarrow 5 \rightarrow 6 \rightarrow 7 \rightarrow 4 \rightarrow ...$$

6. Use J-K Flip-Flop and D Flip-Flop to design an asynchronous down counter as follows

$$6 \rightarrow 5 \rightarrow 4 \rightarrow 3 \rightarrow 2 \rightarrow 1 \rightarrow 6 \rightarrow ...$$

7. Given the following counter circuit:



With the frequency of the clock signal $\mathbf{f_{CLK} = 35\ KHz}$

(a) What is the MOD of the counter?

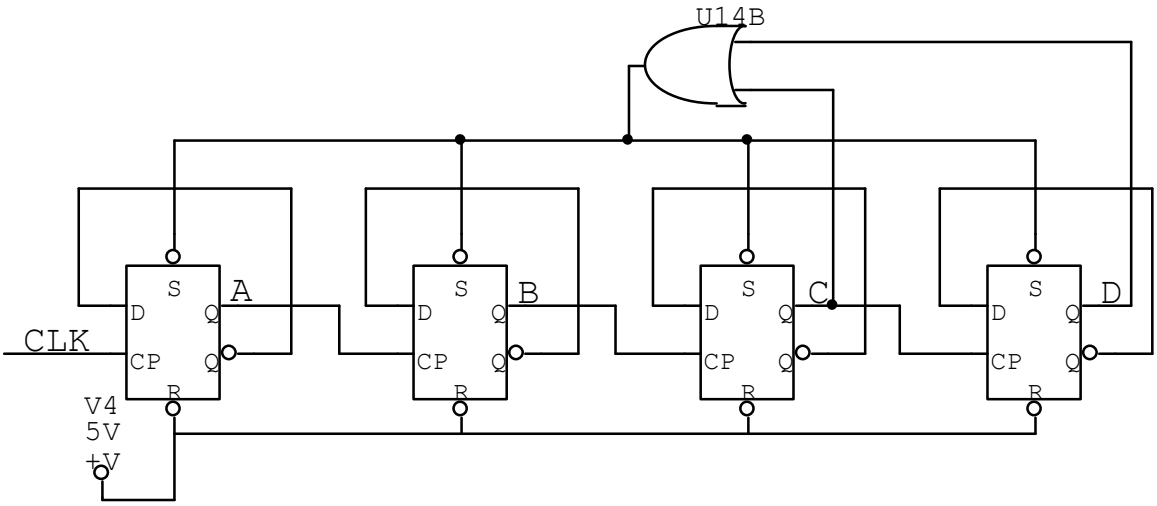
(b) Determine the frequency of Q3 of U1?

(c) Determine the frequency of Q2 of U2?

(d) In the Q3, Q2, Q1, Q0 signals of U1 and U2, which signals are glitches?

(e) Determine duty cycle of Q2 of U2?

8. Given the following counter circuit:



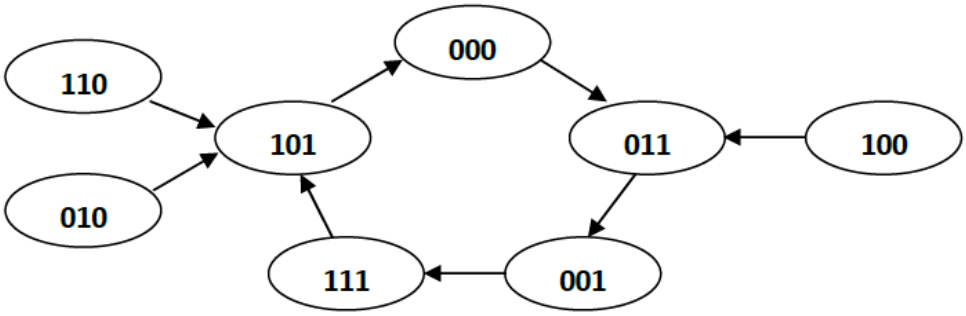
(a) What is the MOD of the counter?

(b) In the A, B, C, D signals, which signals are glitches?

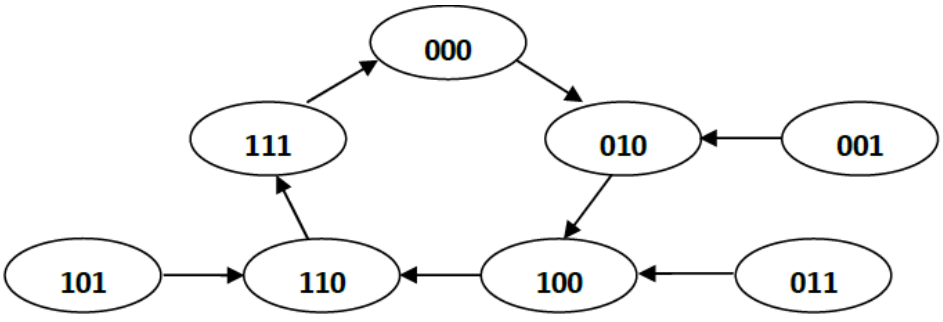
(c) What is the frequency of output B as compared with the frequency of CLK?

(d) What is the frequency of output D as compared with the frequency of CLK?

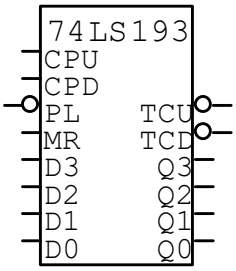
9. Use J-K Flip-Flop to design a synchronous counter circuits according to the following transition diagram:



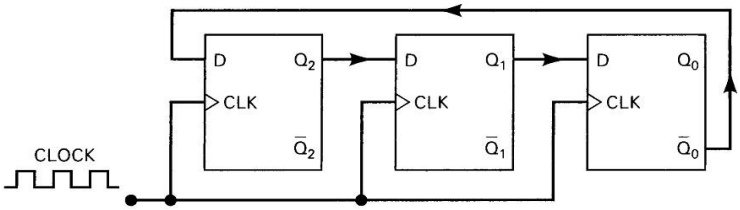
10. Use D-FlipFlop to design a synchronous counter circuits according to the following transition diagram:



11. Use 74LS193 and 74LS32 ICs to design a down counter from 12 → 5

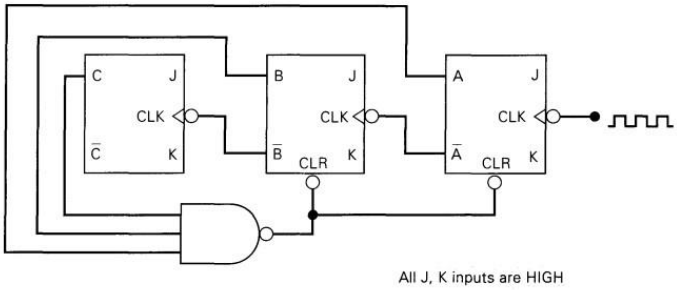


12. Given the following counter circuit:



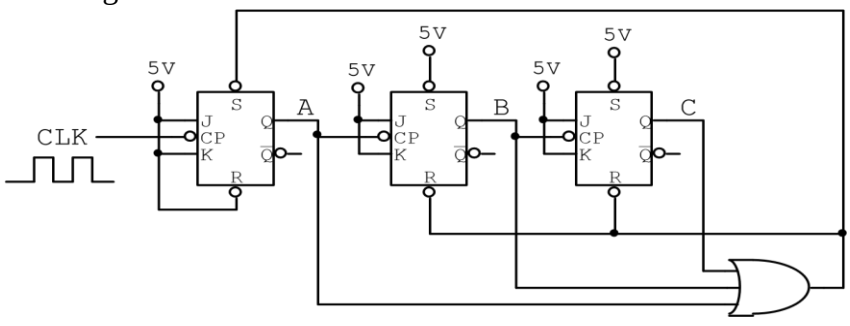
Assume the initial state of the counter $Q_2Q_1Q_0 = 000$, determine the sequence of the counter.

13. Given the following counter circuit



Assume the initial state of the counter CBA = 010, determine the sequence of the counter.

14. Given the following counter circuit:



Assume the initial state of the counter CBA = 010, determine the sequence of the counter.