ELEX 7660: Digital System Design

Lab 1

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2 Source code of the module

```
1   module decode2 (input logic [1:0] digit, output logic [3:0] ct) ;
2
3         always_comb begin
4            case(digit)
5               2'b00 : ct = 4'b1110;
6               2'b01 : ct = 4'b1101;
7               2'b10 : ct = 4'b1011;
8               2'b11 : ct = 4'b0111;
9            endcase
10        end
11
12  endmodule
13
```

Figure 4 – Source code of the decode2 module

```
1  module decode7 (input logic [3:0] num, output logic [7:0] leds) ;
2
3          always_comb begin
4             case(num)
5                4'h00 : leds = 8'h3F;       // display 0
6                4'h01 : leds = 8'h06;       // display 1
7                4'h02 : leds = 8'h5B;       // display 2
8                4'h03 : leds = 8'h4F;       // display 3
9                4'h04 : leds = 8'h66;       // display 4
10               4'h05 : leds = 8'h6D;       // display 5
11               4'h06 : leds = 8'h7D;       // display 6
12               4'h07 : leds = 8'h07;       // display 7
13               4'h08 : leds = 8'h7F;       // display 8
14               4'h09 : leds = 8'h67;       // display 9
15               4'h0A : leds = 8'h77;       // display A
16               4'h0B : leds = 8'h7C;       // display b
17               4'h0C : leds = 8'h39;       // display C
18               4'h0D : leds = 8'h5E;       // display d
19               4'h0E : leds = 8'h79;       // display E
20               4'h0F : leds = 8'h71;       // display F
21            endcase
22         end
23   endmodule
24
```

Figure 5 - Source code of the decode7 module

```
1  module bcitid (input logic [1:0] digit, output logic [3:0] idnum);
2
3     always_comb begin
4        case (digit)
5           2'b11: idnum = 4'h4; // Leftmost digit
6           2'b10: idnum = 4'h7; // Third digit
7           2'b01: idnum = 4'h6; // Second digit
8           2'b00: idnum = 4'h3; // Rightmost digit
9        endcase
10    end
11
12 endmodule
```

Figure 6 - Source code of the bcitid module

3 RTL Netlist

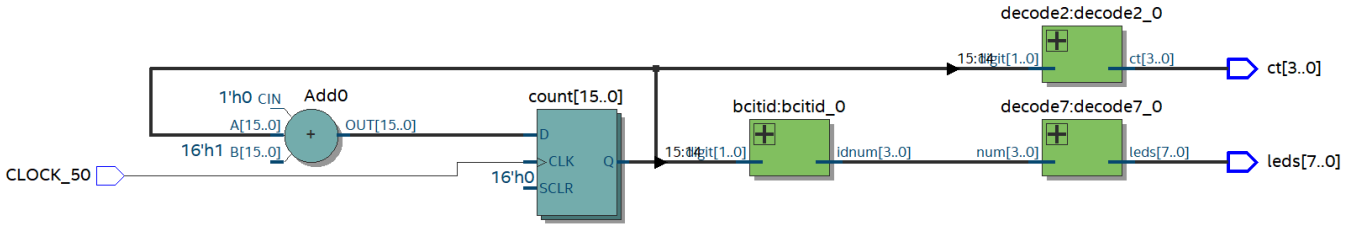

Figure 7 – Final RTL Netlist