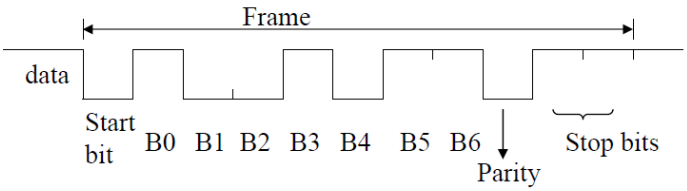
Spring 2024: Digital System Design

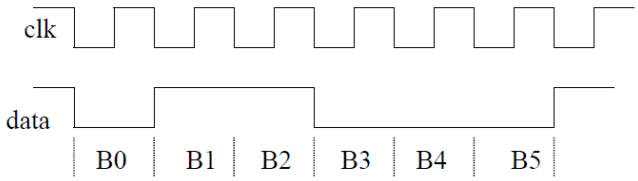
Lab 8. Implementation of UART controller

UART vs. USART

- UART does not require clock signal. However, it transfers extra bits (start bits and stop bits) during data communication.
- USART does not transfer extra bits. However, it requires clock signal.



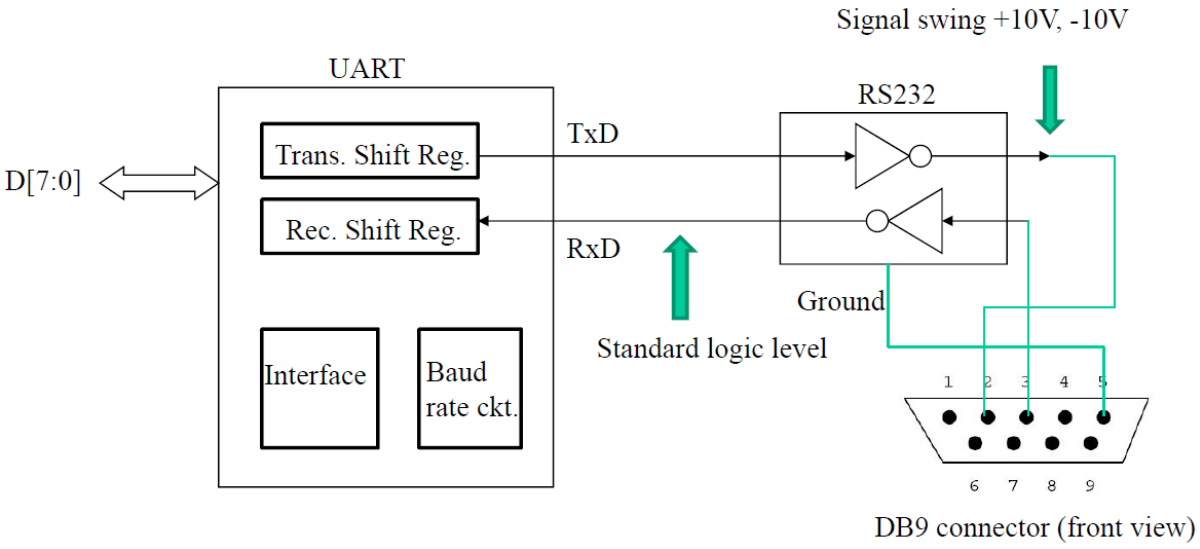
UART



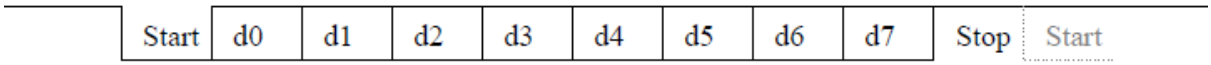
USART

In this lab, we use an asynchronous transfer method (UART).

Overview of UART and RS-232



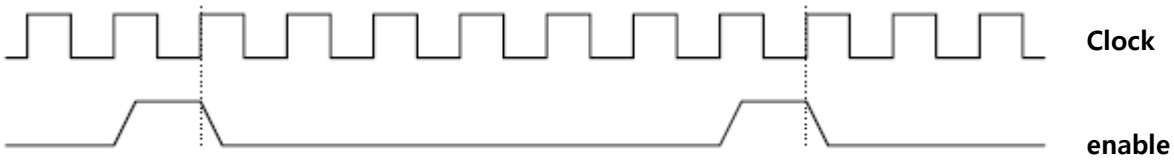
UART Operation



- Signal is logic '1' when the system is idle.
- The data is transmitted serially LSB first at a given bit rate (BAUD rate).
- We can use an ASCII code to represent numbers or characters.

BAUD rate

- Number of bits per second



- In this figure, 1-bit data is transmitted during 7 clock cycles.
- e.g.) 1 clock period is 10us, BAUD rate is 14286bps.
- Frequently used baud rate: 9600, 19200, 115200 ...

1. Design an UART **transmitter** using RTL Verilog
   - 8-data bits
   - 1-stop bit
   - No parity
   - Baud rate : 19200
2. Implement your UART_tx controller on FPGA
3. Take input from the up-down switches and send the data when you push the push button.
4. Transmit the data to Terminal on your x86 from FPGA via serial cable.
5. Specific character should be printed out on Terminal.
6. You have to show your state diagram, microarchitecture, and testbench.

10진수	16진수	2진수	ASCII	10진수	16진수	2진수	ASCII
0	0×00	00000000	NULL	64	0×40	01000000	@
1	0×01	00000001	SOH	65	0×41	01000001	A
2	0×02	00000010	STX	66	0×42	01000010	B
3	0×03	00000011	ETX	67	0×43	01000011	C
4	0×04	00000100	EOT	68	0×44	01000100	D
5	0×05	00000101	ENQ	69	0×45	01000101	E
6	0×06	00000110	ACK	70	0×46	01000110	F
7	0×07	00000111	BEL	71	0×47	01000111	G
8	0×08	00001000	BS	72	0×48	01001000	H
9	0×09	00001001	HT	73	0×49	01001001	I
10	0×0A	00001010	LF	74	0×4A	01001010	J
11	0×0B	00001011	VT	75	0×4B	01001011	K
12	0×0C	00001100	FF	76	0×4C	01001100	L
13	0×0D	00001101	CR	77	0×4D	01001101	M
14	0×0E	00001110	SO	78	0×4E	01001110	N
15	0×0F	00001111	SI	79	0×4F	01001111	O
16	0×10	00010000	DLE	80	0×50	01010000	P
17	0×11	00010001	DC1	81	0×51	01010001	Q
18	0×12	00010010	SC2	82	0×52	01010010	R
19	0×13	00010011	SC3	83	0×53	01010011	S
20	0×14	00010100	SC4	84	0×54	01010100	T
21	0×15	00010101	NAK	85	0×55	01010101	U
22	0×16	00010110	SYN	86	0×56	01010110	V
23	0×17	00010111	ETB	87	0×57	01010111	W
24	0×18	00011000	CAN	88	0×58	01011000	X
25	0×19	00011001	EM	89	0×59	01011001	Y
26	0×1A	00011010	SUB	90	0×5A	01011010	Z
27	0×1B	00011011	ESC	91	0×5B	01011011	[
28	0×1C	00011100	FS	92	0×5C	01011100	₩
29	0×1D	00011101	GS	93	0×5D	01011101	]
30	0×1E	00011110	RS	94	0×5E	01011110	^
31	0×1F	00011111	US	95	0×5F	01011111	_

10진수	16진수	2진수	ASCII	10진수	16진수	2진수	ASCII
32	0×20	00100000	SP	96	0×60	01100000	`
33	0×21	00100001	!	97	0×61	01100001	a
34	0×22	00100010	"	98	0×62	01100010	b
35	0×23	00100011	#	99	0×63	01100011	c
36	0×24	00100100	$	100	0×64	01100100	d
37	0×25	00100101	%	101	0×65	01100101	e
38	0×26	00100110	&	102	0×66	01100110	f
39	0×27	00100111	'	103	0×67	01100111	g
40	0×28	00101000	(	104	0×68	01101000	h
41	0×29	00101001	)	105	0×69	01101001	i
42	0×2A	00101010	*	106	0×6A	01101010	j
43	0×2B	00101011	+	107	0×6B	01101011	k
44	0×2C	00101100	,	108	0×6C	01101100	l
45	0×2D	00101101	-	109	0×6D	01101101	m
46	0×2E	00101110	.	110	0×6E	01101110	n
47	0×2F	00101111	/	111	0×6F	01101111	o
48	0×30	00110000	0	112	0×70	01110000	p
49	0×31	00110001	1	113	0×71	01110001	q
50	0×32	00110010	2	114	0×72	01110010	r
51	0×33	00110011	3	115	0×73	01110011	s
52	0×34	00110100	4	116	0×74	01110100	t
53	0×35	00110101	5	117	0×75	01110101	u
54	0×36	00110110	6	118	0×76	01110110	v
55	0×37	00110111	7	119	0×77	01110111	w
56	0×38	00111000	8	120	0×78	01111000	x
57	0×39	00111001	9	121	0×79	01111001	y
58	0×3A	00111010	:	122	0×7A	01111010	z
59	0×3B	00111011	;	123	0×7B	01111011	{
60	0×3C	00111100	<	124	0×7C	01111100	|
61	0×3D	00111101	=	125	0×7D	01111101	}
62	0×3E	00111110	>	126	0×7E	01111110	~
63	0×3F	00111111	?	127	0×7F	01111111	DEL

1. CAL-200 (Max 10)

SW00	PIN_132
SW01	PIN_131
SW02	PIN_130
SW03	PIN_127
SW04	PIN_120
SW05	PIN_119
SW06	PIN_118
SW07	PIN_114
SW08	PIN_113
SW09	PIN_111
SW10	PIN_110
SW11	PIN_106
SW12	PIN_105
SW13	PIN_102
SW14	PIN_101
SW15	PIN_100

CAL-200 Slide Switch Pin Mapping

BTN3	PIN_134
BTN2	PIN_135
BTN1	PIN_140
BTN0	PIN_141
BTN_Reset	PIN_54

CAL-200 Button Pin Mapping

UART0_Rx	PIN_47
UART0_Tx	PIN_50
UART1_Rx	PIN_52
UART1_Tx	PIN_55

CAL-200 UART Pin Mapping

2. SPL-LAB100 (Cyclone III)

Signal Name	FPGA PIN	Description	I/O Standard
SW[15]	PIN_21	Slide Switch[15]	3.3V
SW[14]	PIN_37	Slide Switch[14]	3.3V
SW[13]	PIN_39	Slide Switch[13]	3.3V
SW[12]	PIN_43	Slide Switch[12]	3.3V
SW[11]	PIN_45	Slide Switch[11]	3.3V
SW[10]	PIN_50	Slide Switch[10]	3.3V
SW[9]	PIN_52	Slide Switch[9]	3.3V
SW[8]	PIN_56	Slide Switch[8]	3.3V
SW[7]	PIN_84	Slide Switch[7]	3.3V
SW[6]	PIN_88	Slide Switch[6]	3.3V
SW[5]	PIN_94	Slide Switch[5]	3.3V
SW[4]	PIN_98	Slide Switch[4]	3.3V
SW[3]	PIN_100	Slide Switch[3]	3.3V
SW[2]	PIN_106	Slide Switch[2]	3.3V
SW[1]	PIN_109	Slide Switch[1]	3.3V
SW[0]	PIN_111	Slide Switch[0]	3.3V

Pin Assignments for Slide Switches

Signal Name	FPGA PIN	Description	I/O Standard
BTN[3]	PIN_112	Push-Button[3]	3.3V
BTN[2]	PIN_113	Push-Button[2]	3.3V
BTN[1]	PIN_114	Push-Button[1]	3.3V
BTN[0]	PIN_117	Push-Button[0]	3.3V

Pin Assignments for Push-buttons

Signal Name	FPGA PIN	Description	I/O Standard
tx0	PIN_5	UART Transmitter 0	3.3V
tx1	PIN_6	UART Transmitter 1	3.3V
rx0	PIN_4	UART Receiver 0	3.3V
rx1	PIN_9	UART Receiver 1	3.3V

RS-232 Pin Assignments