Respond to Input Request on Hardware Requirement/Block Diagrams for Oct-19 SAFEPOWER Follow-up Meeting

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1 System Block Diagram

The main elements of the system are switches connected in a 2x2 mesh topology and interfaced to processing nodes through network interfaces (NI). A block diagram illustrating the system can be seen in Fig. 1. The figure depicts four resources or nodes which are either microblaze systems or dual cortex A9 processor, connected to a structure of switches array each is denoted by Sxx via network interfaces (NI).

2 Hardware Requirements

Table 1: Resource Utilisation

	Microblaze	64KB Microblaze Memory	NoC
6-inputs LUTs	1115	7	2768
Registers	2272	13	6723
BlockRAM	0	16	8

- The NoC part of the MPSoC system would require minimal Look-up tables (LUT)s and registers resources on the programmable logic of the Zynq device as shown in the last column of Table 1.
- Since the next release would be slightly different, a 50% increase in the required resources can be taken into consideration as design margins.

- Minimal on-chip memory requirements for the NoC part of the MPSoC would depend on the maximum size of packets or messages in Bytes expected to be sent and received at any moment of time. This is because, the packets to be sent or received are stored in the network interface which is considered a part of the NoC. The 8 Block RAM in Table 1 corresponds to 2KB of send buffer and 2 KB or receive buffer for four nodes.

- Table 1 (Column 1 and 2) shows a minimal requirements on the soft-processor systems (Microblaze, on-chip memory). The application derived from the relevant use-cases (avionics+public) would potentially override/re-define the requirement on the soft-processing systems and possibly the required logic resources for the NoC.

- For potential Dynamic Frequency Scaling (DFS), four Programmable Clock signals (3 to be fed to the soft-processor systems and 1 for the NoC block) from Processing System Clock Generator Module can be allocated. Alternatively, four Clocking Management Tiles can be allocated.

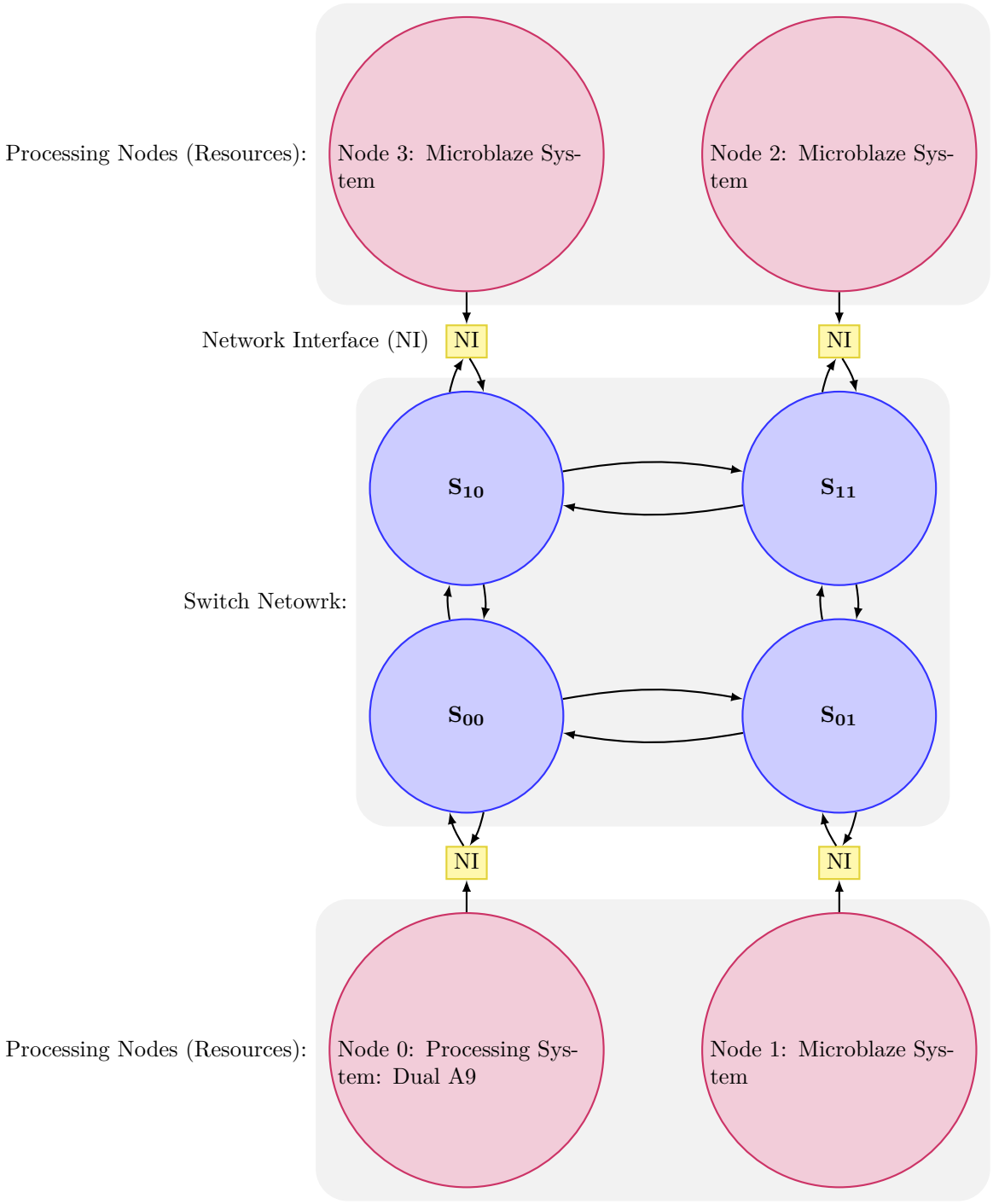

Figure 1: Block Diagram of Network-on-Chip Based MPSoC Depicting Network Interfaces and Switch Network for 2x2 Mesh Type Nostrum NoC and Processing Nodes