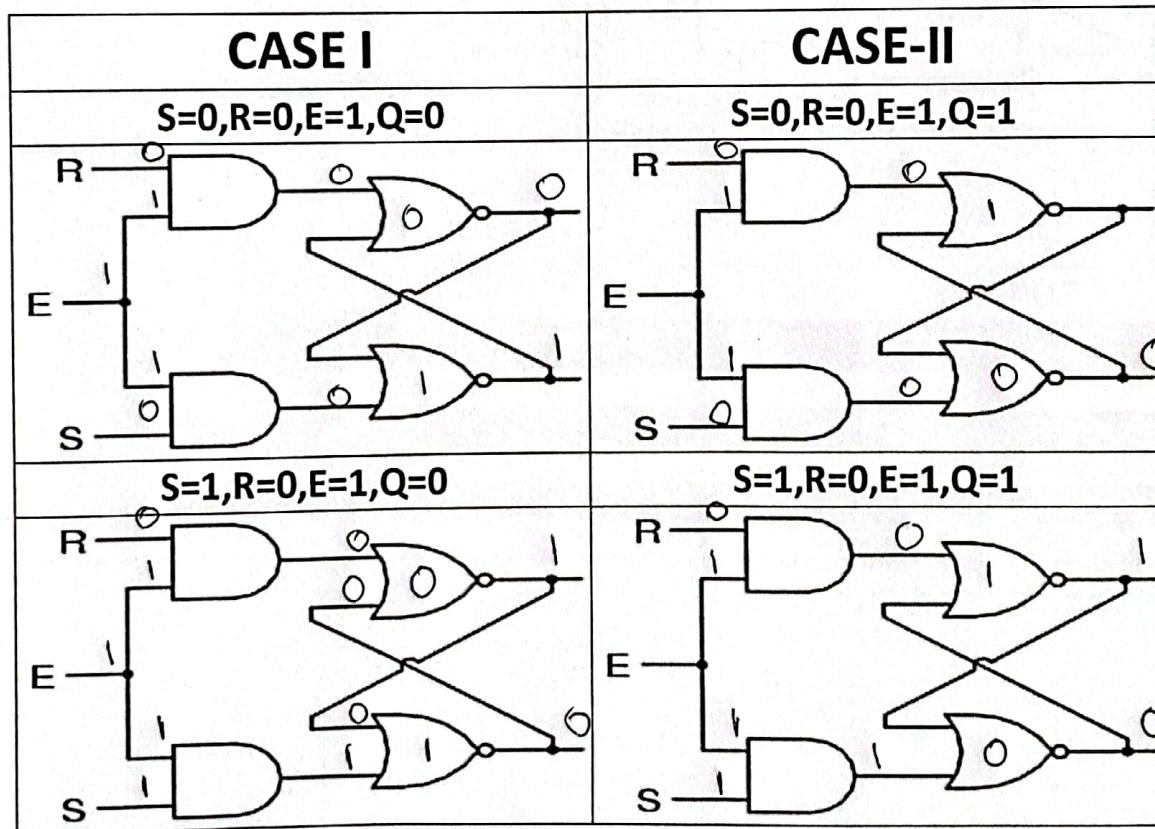
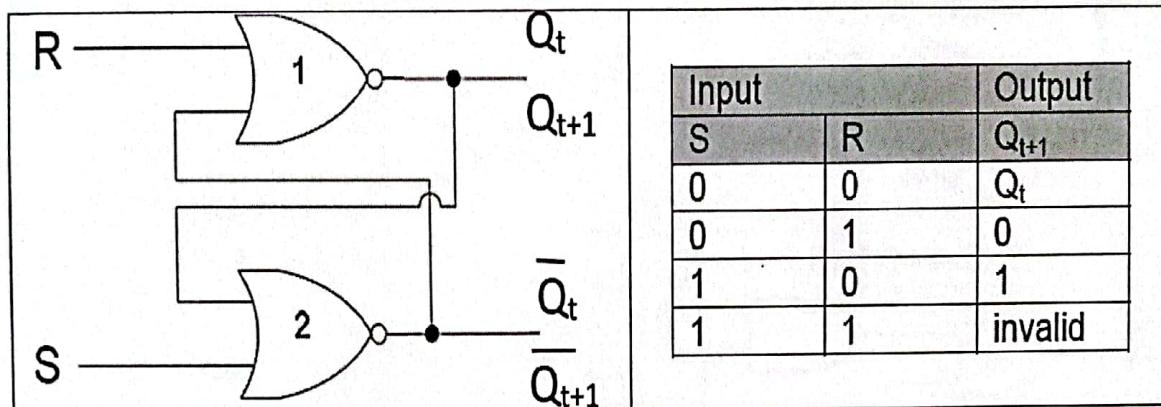


1. Following is the table for NOR BASED S-R Latch? Use the table to process all 8 possible cases for the GATED S_R Latch?

NOTE: Process each & every gate in all 8 cases



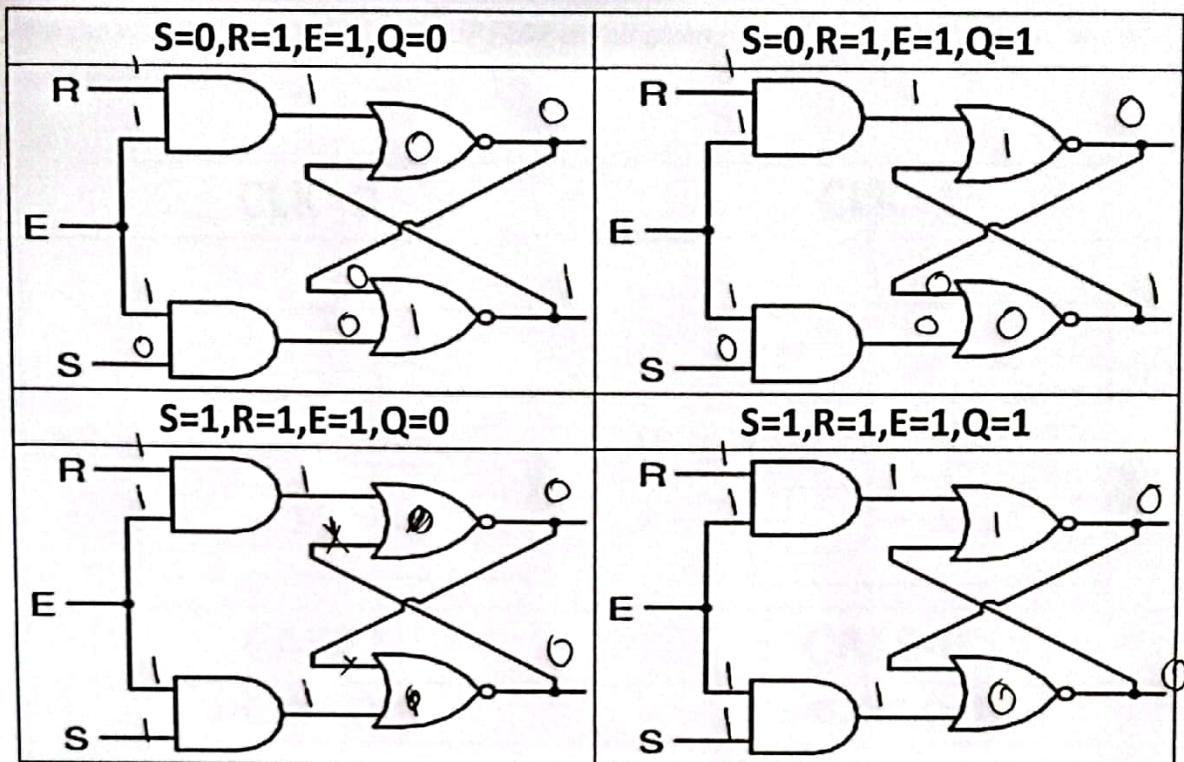


TABLE:

INPUT			OUTPUT
E	S	R	Q_{t+1}
0	X	X	Q_t
1	0	0	Q_t
1	0	1	Reset (0)
1	1	0	Set (1)
1	1	1	Invalid

Process the POSITIVE CLOCK EDGE JK FLIP FLOP circuit given below for all possible cases and fill the table accordingly?

$0 \rightarrow 1$

CIRCUIT:

CLK=0	CLK=1
CASE I	CASE-II
J=0,K=0,Q=0	J=0,K=0,Q=1
J=0,K=1,Q=0	J=0,K=1,Q=1

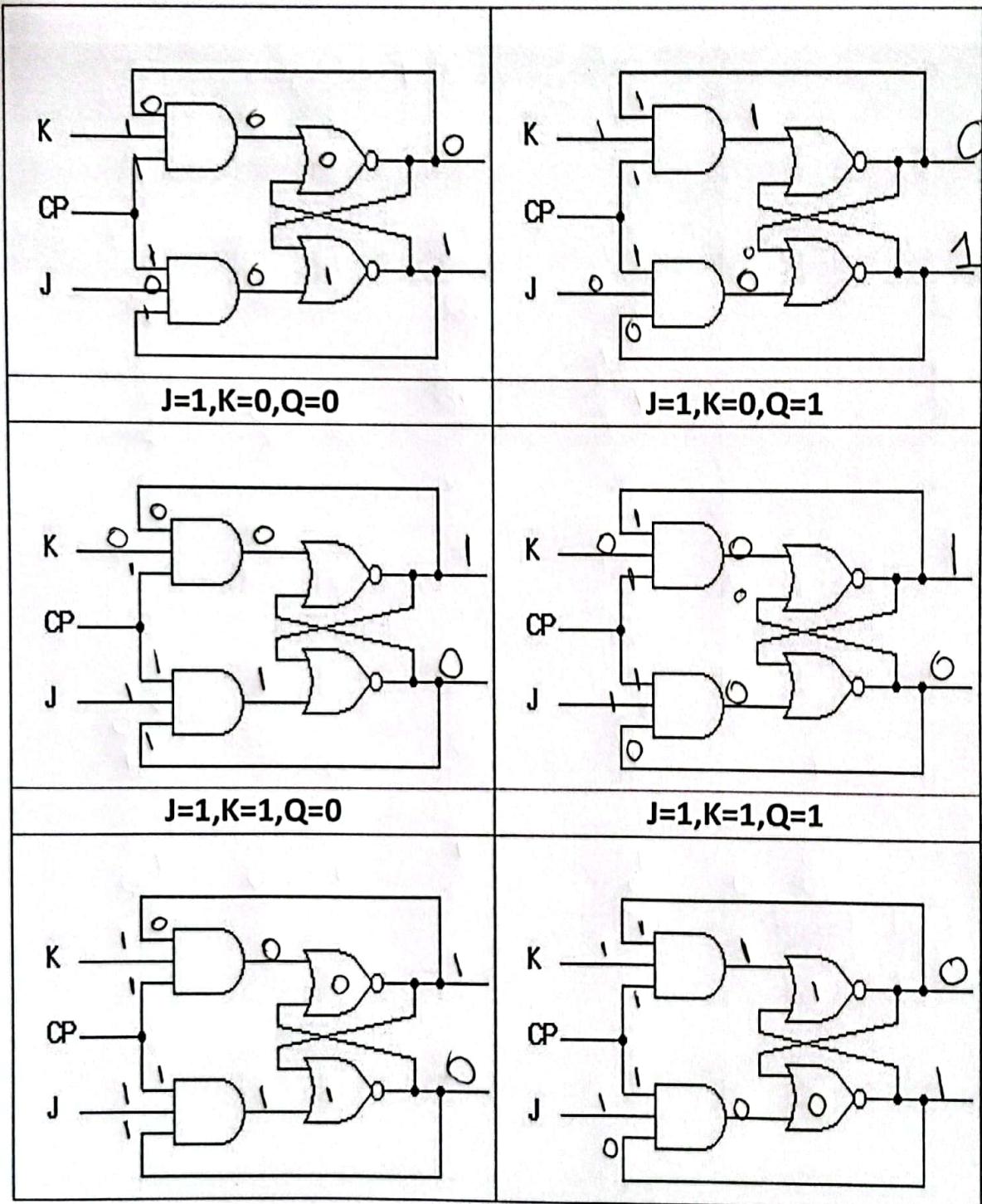


TABLE:

CLK	J	K	Q_{t+1}	\bar{Q}_{t+1}
0	X	X	Q_t	\bar{Q}_t
1	X	X	Q_t	\bar{Q}_t
\uparrow	0	0	Q_t	\bar{Q}_t
\uparrow	0	1	Reset (0)	1
\uparrow	1	0	Set (1)	0
\uparrow	1	1	\bar{Q}_t	Q_t

Modify given circuit to introduce Asynchronous CLEAR and SET inputs fill table?

HINT: For reference kindly read Section 7-2 of DIGITAL FUNDAMENTAL by Thomas Floyd, 10th Edition

CIRCUIT:

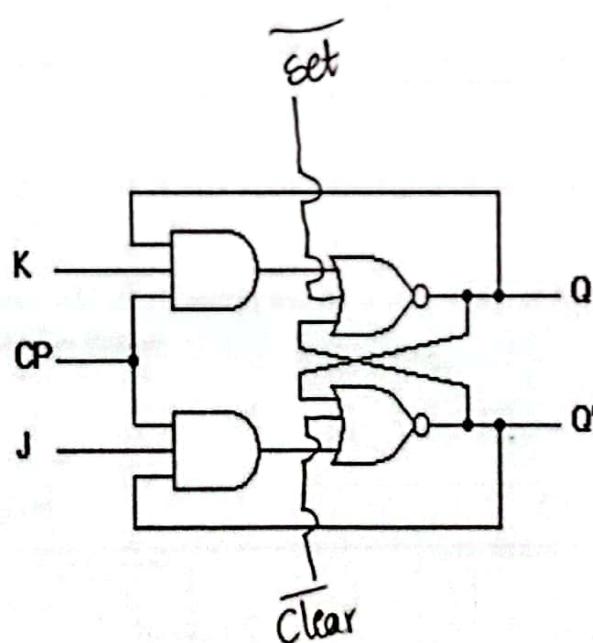


TABLE:

SET	CLEAR	Q_{t+1}	\bar{Q}_{t+1}
0	0	Q_t Invalid	\bar{Q}_t Invalid
0	1	0	1
1	0	1	0
1	1	Set Invalid	Set Invalid

2. Following is the table for NAND BASED S-R Latch? Use the table to process all 8 possible cases for the GATED S_R Latch?
- NOTE: Process each & every gate in all 8 cases

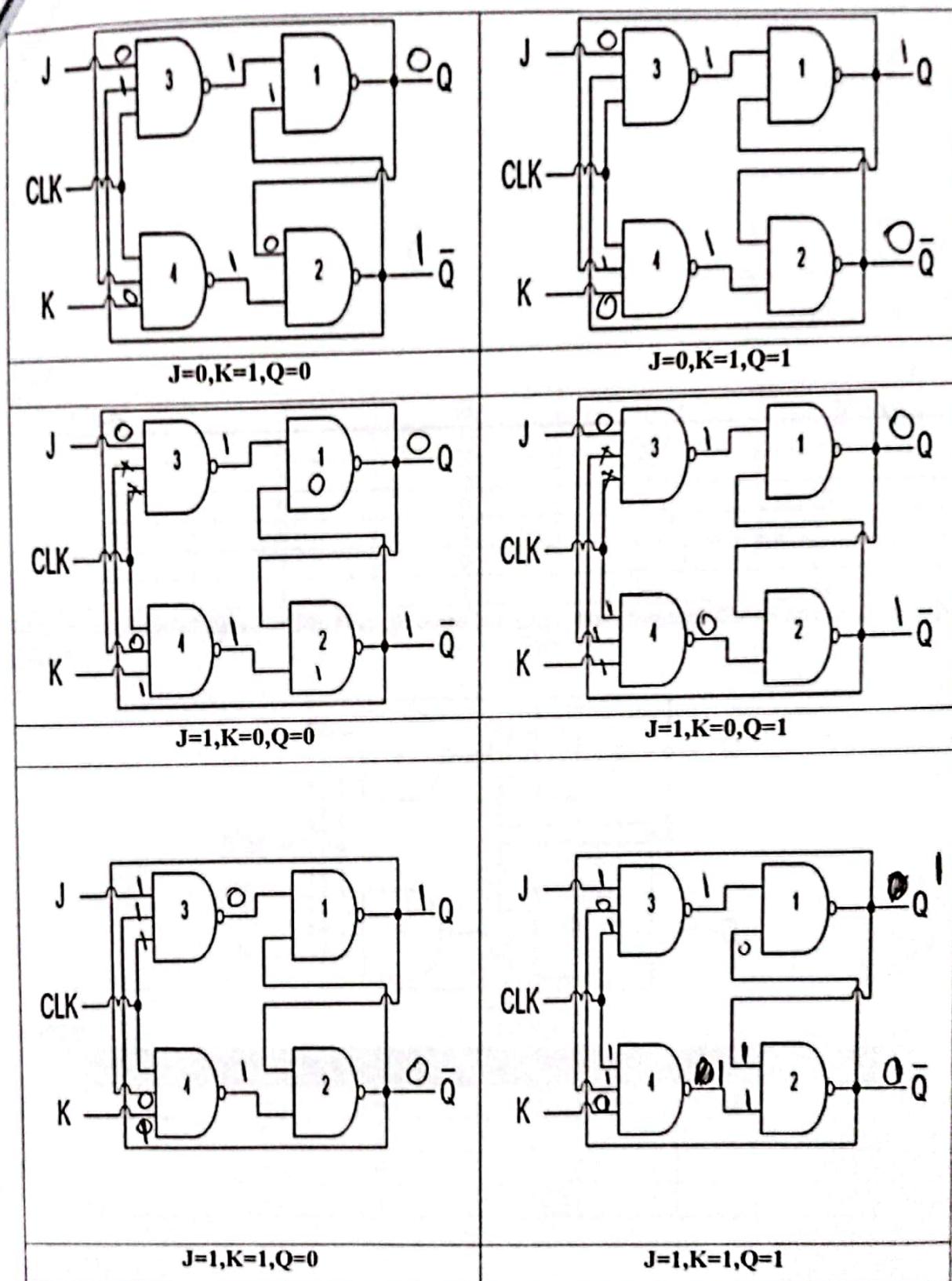
INPUT		OUTPUT	
S	R	Q_{t+1}	\bar{Q}_{t+1}
0	0	Invalid	Invalid
0	1	1	0
1	0	0	1
1	1	old state	old state

- Process the POSITIVE CLOCK EDGE JK FLIP FLOP circuit given below for all possible cases and fill the table accordingly?

NOTE: Process each and every block no marks will be given for direct answer. No need to process NAND LATCH use table filled in Part A

CIRCUIT:

CLK=0	CLK=1
<p>CASE I $J=0, K=0, Q=0$</p>	<p>CASE-II $J=0, K=0, Q=1$</p>



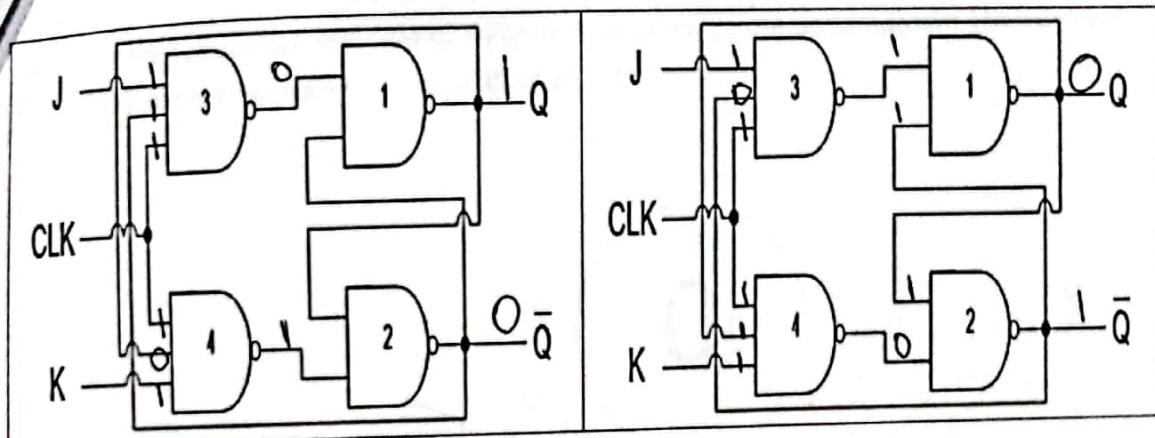


TABLE:

CLK	J	K	Q_{t+1}	\bar{Q}_{t+1}
0	X	X	Q_t	\bar{Q}_t
1	X	X	Q_t	\bar{Q}_t
↑	0	0	Q_t	\bar{Q}_t
↑	0	1	0	1
↑	1	0	1	0
↑	1	1	\bar{Q}_t	Q_t

Modify given NAND Based JK Flip Flop circuit to introduce Asynchronous CLEAR and SET inputs fill table?

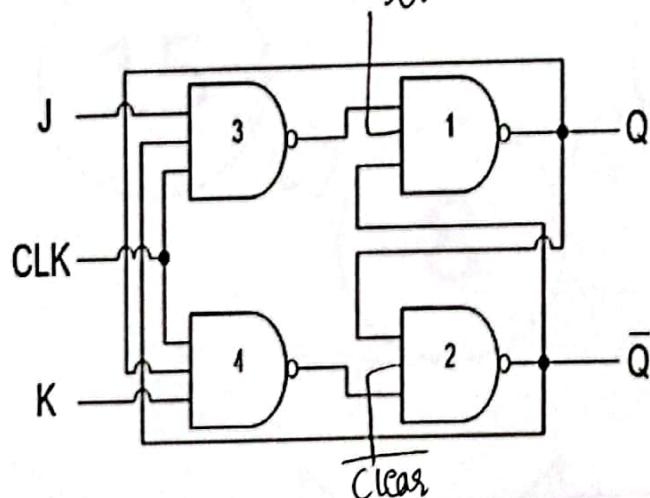
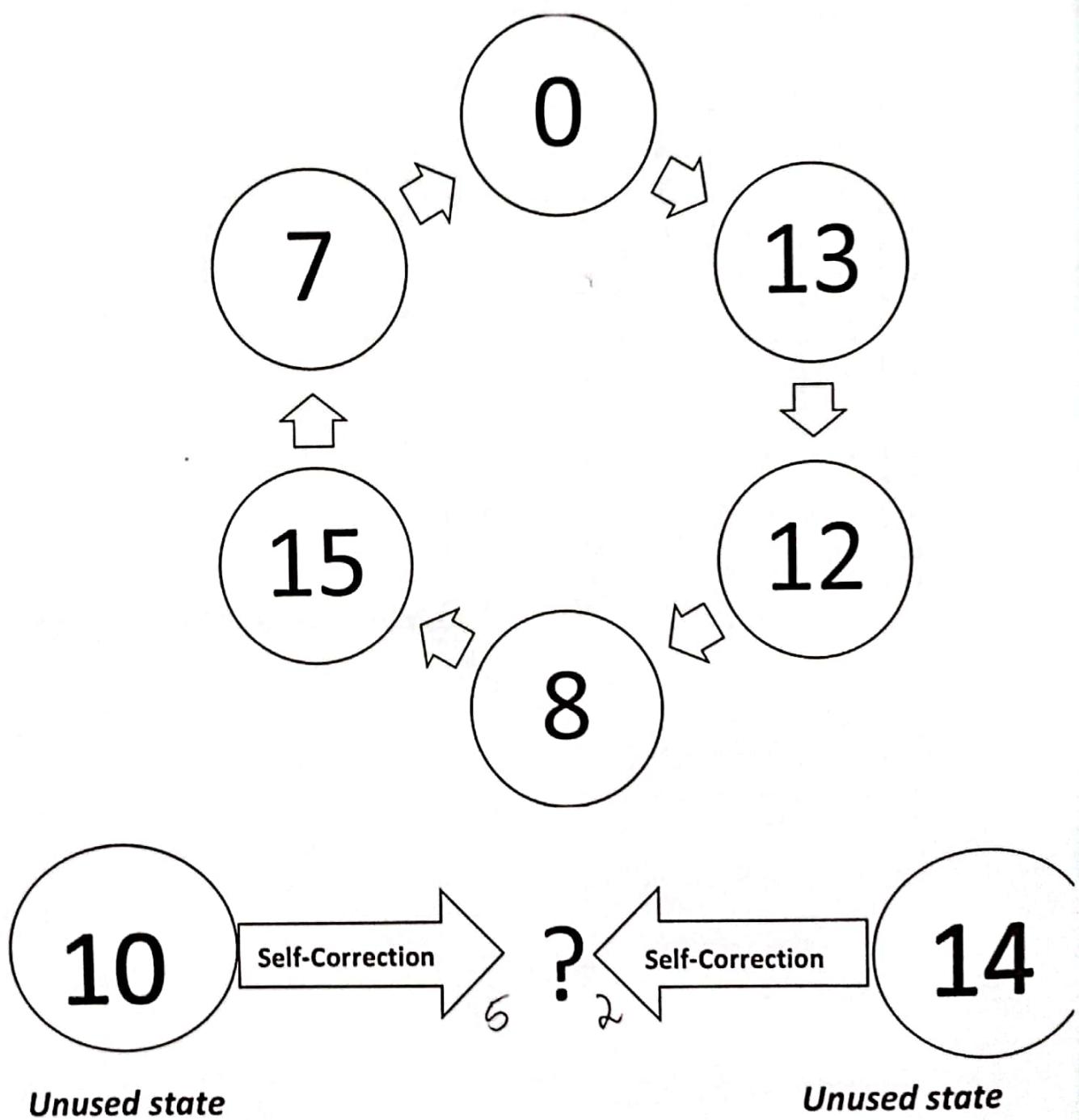


TABLE:

SET	CLEAR	Q_{t+1}	\bar{Q}_{t+1}
0	0	InValid	InValid
0	1	1	0
1	0	0	1
1	1	Q_t	\bar{Q}_t

3. Design the sequential circuit using T-Flip-flop specified by the state diagram given below?
find self-correcting state for unused state 10, 14?



State Table

A	B	C	D	T _A	T _B	T _C	T _D	A+	B+	C+	D+	
0	0	0	0	1	1	0	1	1	1	0	1	0
0	0	0	1	X	X	X	X	X	X	X	X	1
0	0	1	0	X	X	X	X	X	X	X	X	2
0	0	1	1	X	X	X	X	X	X	X	X	3
0	1	0	0	X	X	X	X	X	X	X	X	4
0	1	0	1	X	X	X	X	X	X	X	X	5
0	1	1	0	X	X	X	X	X	X	X	X	6
0	1	1	1	0	1	1	1	0	0	0	0	7
1	0	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	X	X	X	X	X	X	X	X	9
1	0	1	0	X	X	X	X	X	X	X	X	10
1	0	1	1	X	X	X	X	X	X	X	X	11
1	1	0	0	0	1	0	0	1	0	0	0	12
1	1	0	1	0	0	0	1	1	1	0	0	13
1	1	1	0	X	X	X	X	X	X	X	X	14
				0	0	0	0	1	1	1	1	15

SIMPLIFICATION & EXPRESSIONST_A

AB	CD	00	01	11	10
00	00	1	X	X	X
00	01	X	X	0	X
01	00			1	X
11	00	0	0	1	X
10	01	0	X	X	X

$$= \bar{A}\bar{C} + AC = A \odot C$$

T_B

AB	CD	00	01	11	10
00	00	1	X	X	X
00	01	X		1	X
01	00		X	X	X
11	11	1	0	0	X
10	10	1	X	X	X

$$T_B = \bar{C}\bar{D} + \bar{A}\bar{B}$$

T_C

$$T_C = \bar{A}B + \bar{A}\bar{B}$$

AB	CD	00	01	11	10
00	00	0	X	X	X
01	00	X	X	1	X
11	00	0	0	0	X
10	01	1	X	X	X

T_D

AB	CD	00	01	11	10
00	00	1	X	X	X
01	00	X	X	1	X
11	00	0	1	0	X
10	01	1	X	X	X

$$T_D = \bar{B} + \bar{A} + \bar{C}\bar{D}$$

For 14:

P.S	T	N.S
1	1	0
1	1	0
1	0	1
0	0	0

 $\Rightarrow 0010$

2

Next state
for 14

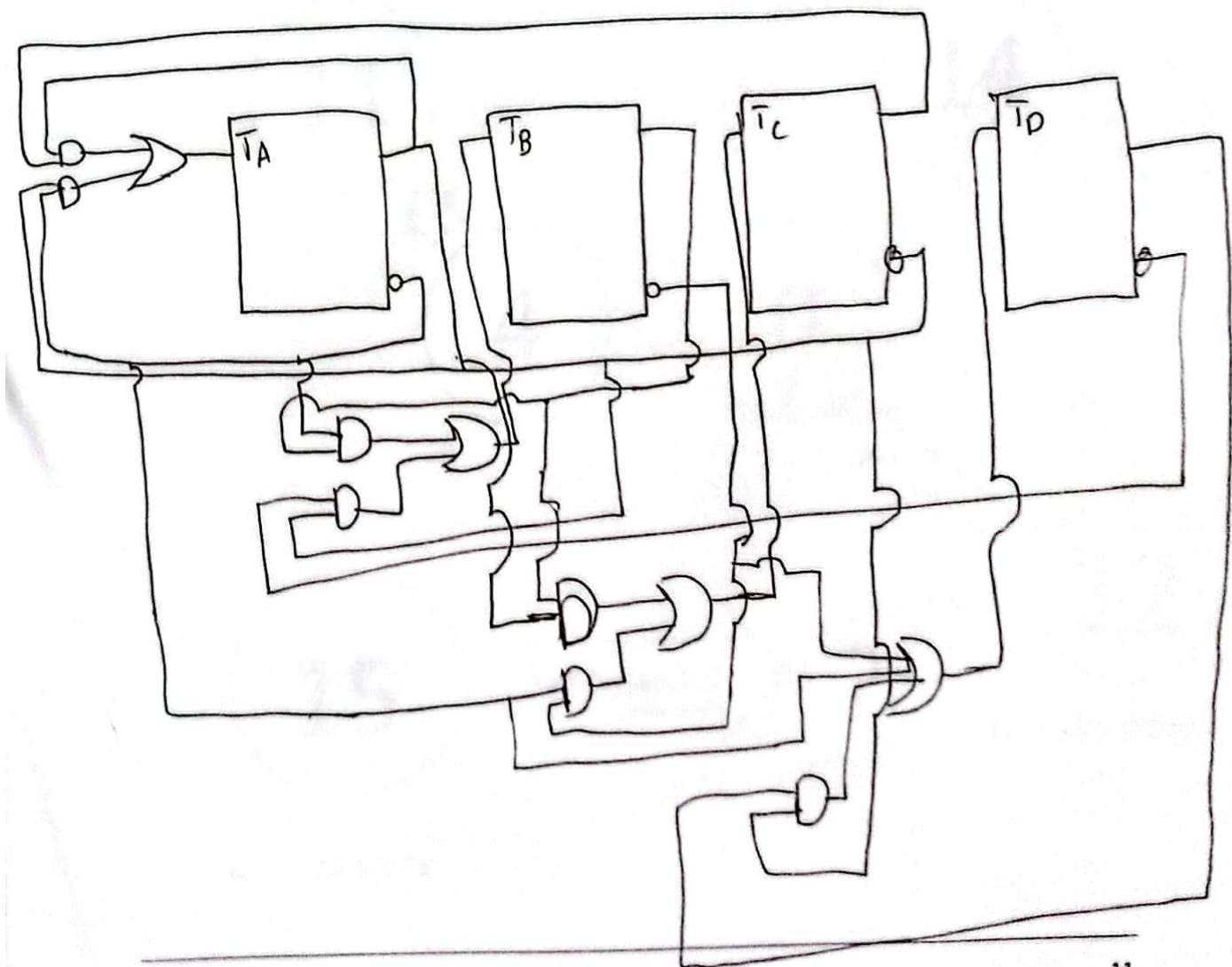
For 10:

P.S	T
1	1
0	1
1	1
0	1

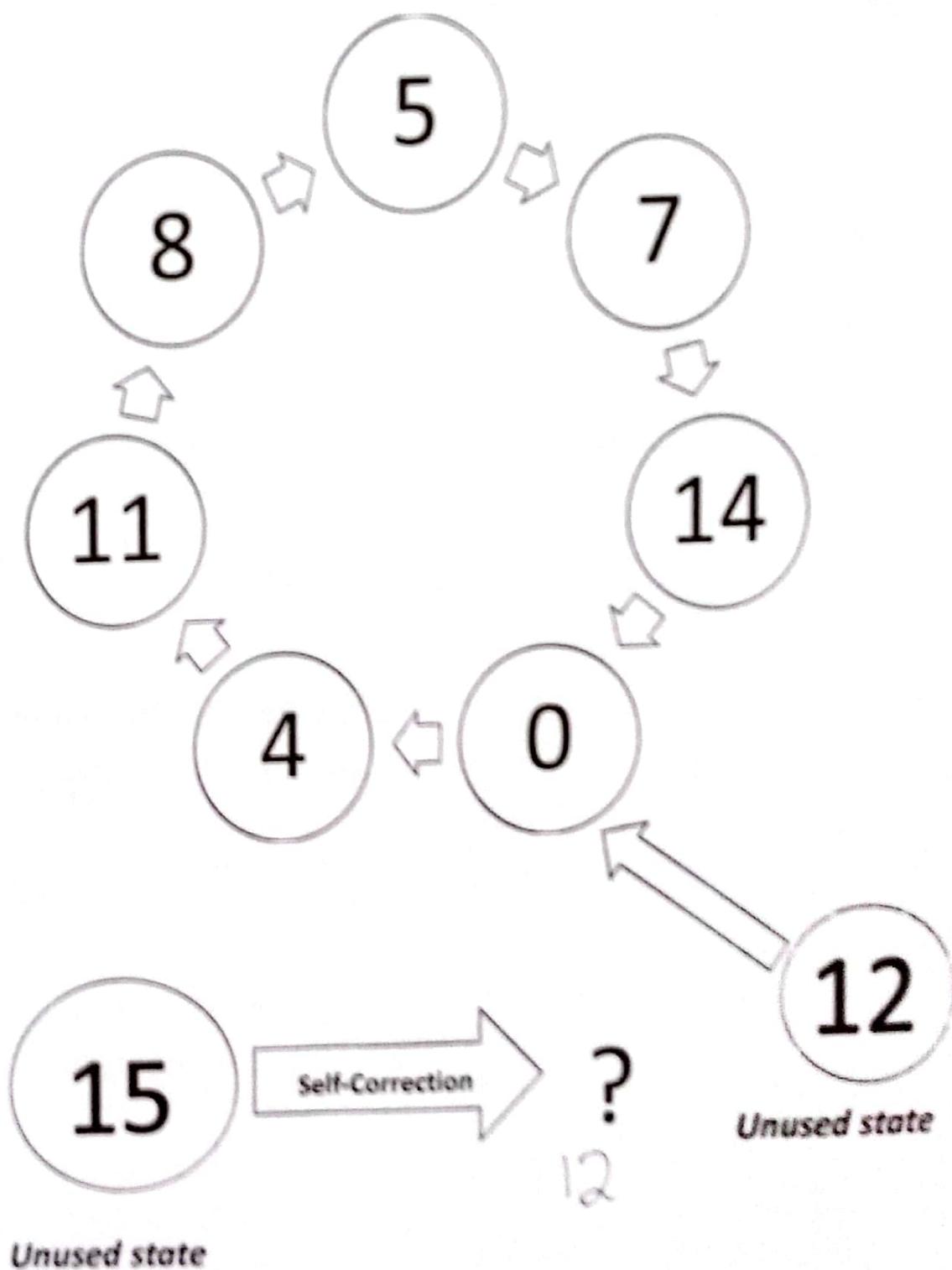
N.S
0
1
0
1

 $\Rightarrow 0101$

5

Next state
for 10

4. Design the sequential circuit using JK-Flip-flop specified by the state diagram given below?
find self-correcting state for unused state 15?



State Table

State No	Previous State				Next State				J_A	K_A	J_B	K_B	J_C	K_C	J_D	K_D
	A	B	C	D	A+	B+	C+	D+	J _A	K _A	J _B	K _B	J _C	K _C	J _D	K _D
5	0	1	0	1	0	1	1	1	0	X	0	1	X	0	1	0
7	0	1	1	1	1	1	1	0	1	1	X	0	X	0	1	1
14	1	1	1	0	0	0	0	0	X	1	X	1	X	1	0	X
0	0	0	0	0	0	1	0	0	0	X	1	X	0	X	0	X
4	0	1	0	0	1	0	1	1	1	X	X	1	1	X	1	X
11	1	0	1	1	1	0	0	0	X	0	0	X	X	1	1	X
8	1	0	0	0	1	0	1	X	1	1	X	0	X	1	0	X
12	1	1	0	0	0	0	0	0	X	1	X	1	0	X	0	X
15	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X

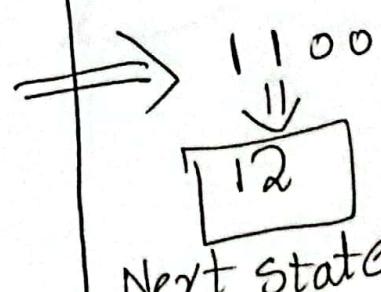
SIMPLIFICATION & EXPRESSIONS

$\text{J}_A = C + B\bar{D}$ $K_A = \bar{D}$ $\bar{J}_B = \bar{C}$ $K_B = \bar{D}$
 $\bar{J}_C = \bar{A}\bar{B}$ $K_C = A$ $J_D = A \oplus B$ $K_D = C$

For 1111 JK values:

$$\begin{aligned}
 \bar{J}_A &= 1 & K_A &= 0 \\
 \bar{J}_B &= 0 & K_B &= 0 \\
 \bar{J}_C &= 0 & K_C &= 1 \\
 J_D &= 0 & K_D &= 1
 \end{aligned}$$

PS	J	K	N.S
1	1	0	1
1	0	0	1
1	0	1	a
0	1	0	

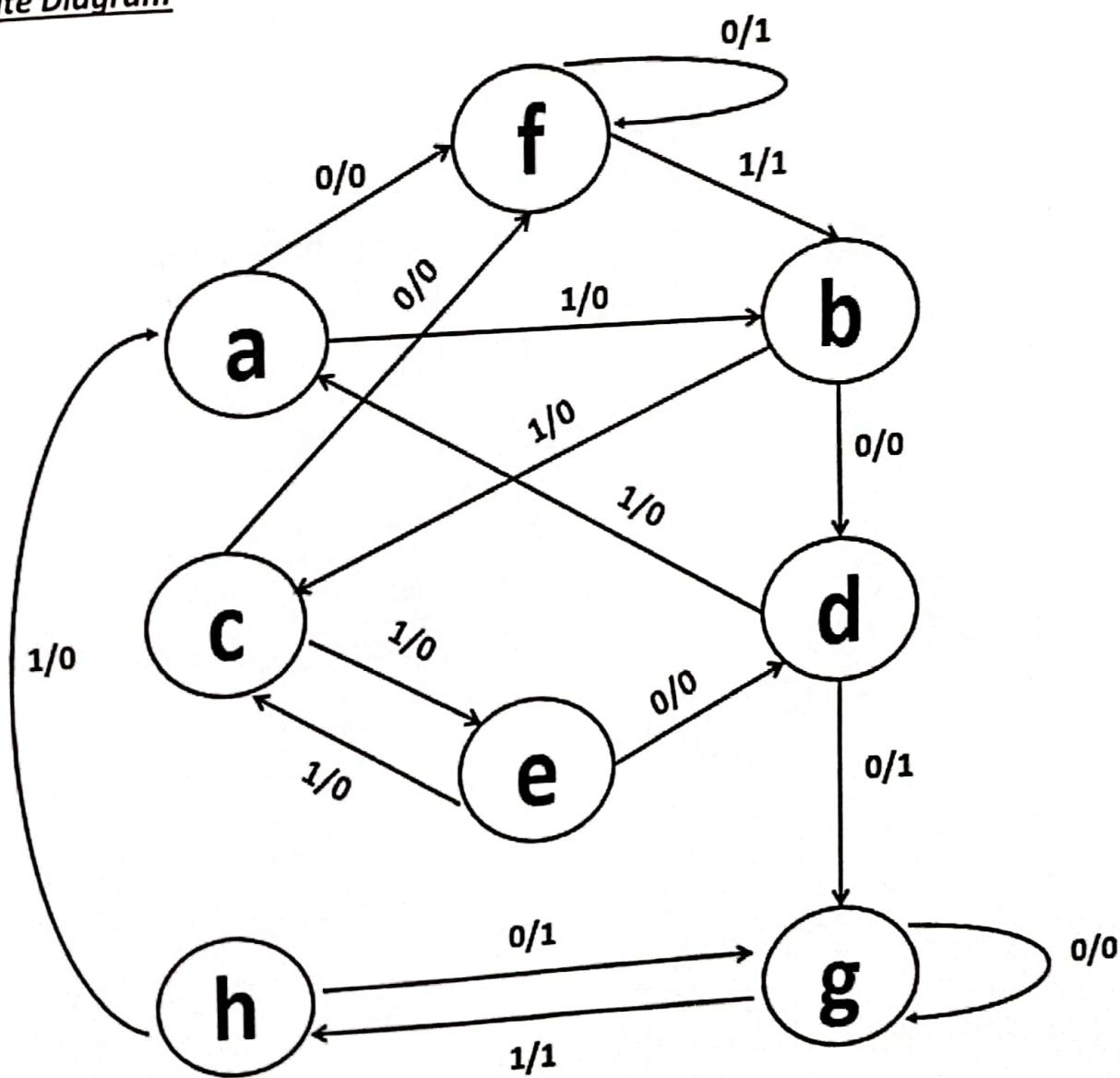


Next State

of 15_{13}
is $12(1100)$

5. For STATE DIAGRAM given below determine output where input sequence is 01110010011
where starting state is **a**

INPUT	0	1	1	1	0	0	1	0	0	1	1	0	1
STATE	a	f	b	c	e	d	g	h	g	g	h	a	f
OUTPUT	0	1	0	0	0	1	1	1	0	1	0	0	1

State Diagram

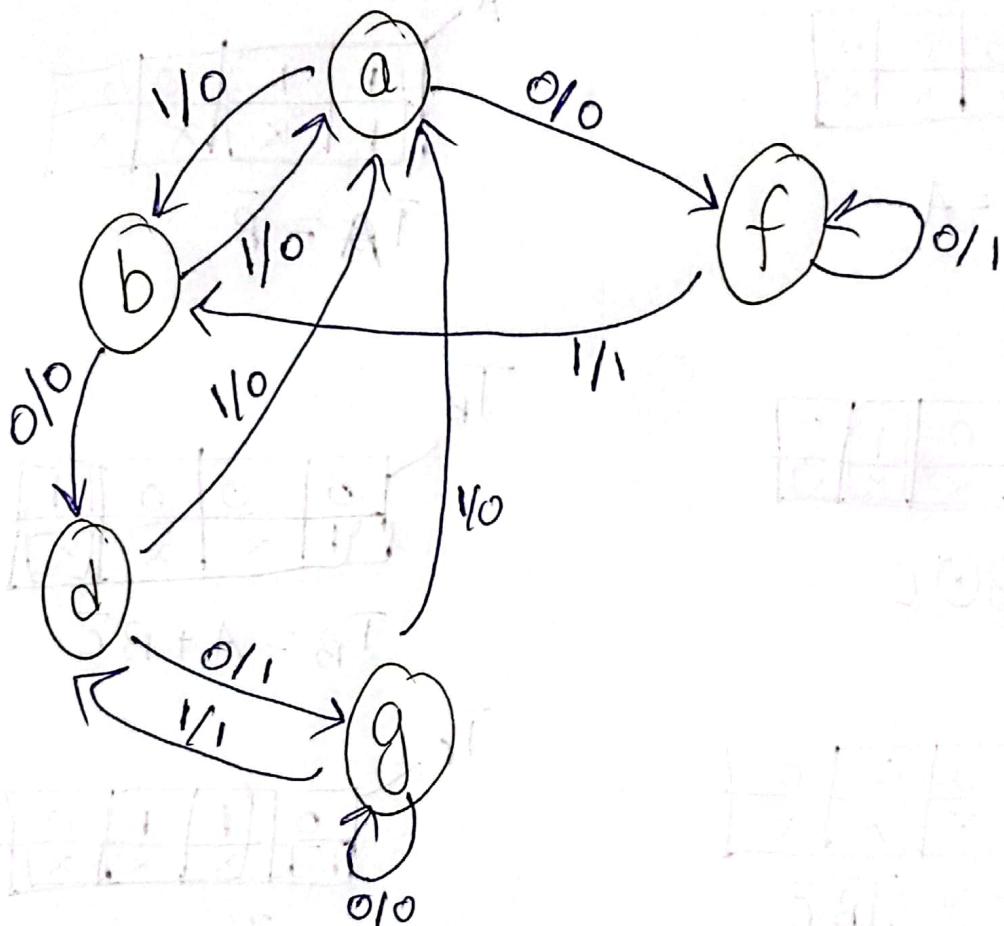
P. S	Next state $x=0$	Next state $x=1$
a	f	b
b	d	c
c	f	e
d	g	a
e	d	c
f	f	b
g	g	h
h	g	a

OUTPVT	$x=0$	$x=1$
0	0	0
0	0	0
0	1	0
0	0	0
1	1	1
0	0	0
1	1	0

Generate Reduced State Table

P. S	Next state $x=0$	Next state $x=1$	OUTPVT $x=0$	OUTPVT $x=1$
a	f	b	0	0
b	d	a	0	0
d	g	a	1	0
f	f	b	1	1
g	g	d	0	1

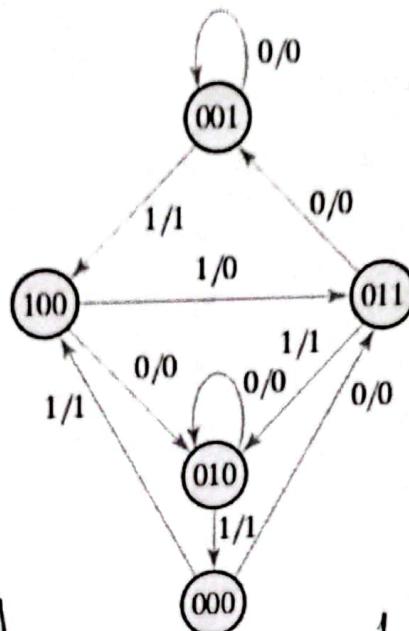
Assignment 4
Produce Reduced State Diagram



For Reduced State Diagram produced in part d, determine output where input sequence is 01110010011 where starting state is a

INPUT	0	1	1	1	0	0	1	0	0	1	1	0	1
STATE	a	f	b	a	b	a	f	b	d	g	d	a	f
OUTPUT	0	1	0	0	0	0	1	0	1	1	0	0	1

6. A sequential circuit has three flip-flops A, B, C; one input 'x'; and one output 'y'. The state diagram is shown below. The circuit is to be designed by treating the unused states as don't-care conditions. Where 101 is an unused state find self-correction for $x=0$ & $x=1$. Use T flip-flops to the circuit design.



x	A	B	C	A_t	B_t	C_t	T_A	T_B	T_C	y
0	0	0	0	0	1	1	0	1	1	0
0	0	0	1	0	0	1	0	0	0	0
0	0	1	0	0	1	0	0	0	0	0
0	0	1	1	0	0	1	0	1	0	0
0	1	0	0	0	1	0	1	1	0	0
0	1	0	1	x	x	x	x	x	x	x
0	1	1	0	x	x	x	x	x	x	x
0	1	1	1	x	x	x	x	x	x	x
1	0	0	0	1	0	0	1	0	0	1
1	0	0	1	1	0	0	1	0	0	1
1	0	1	0	0	0	0	0	0	1	1
1	0	1	Φ	0	1	1	1	1	1	0
1	01	0	0	0	1	1	x	x	x	x
1	1	0	01	x	x	x	x	x	x	x
1	1	01	0	x	x	x	x	x	x	x
1	1	1	1	x	x	x	x	x	x	x



$$\chi = 0$$

T_A

0	0	0	0
1	x	x	x

$$T_A = A$$

$$\chi = 1$$

T_A

1	1	0	0
1	x	x	x

$$T_A = \bar{B}$$

T_B

1	0	1	0
1	x	x	x

$$T_B = B \odot C$$

T_C

1	0	0	0
0	x	x	x

$$T_C = \bar{A} \bar{B} \bar{C}$$

T_B

0	0	0	1
1	x	x	x

$$T_B = A + BC$$

T_C

0	1	1	0
1	x	x	x

$$T_C = A + C$$

101 \rightarrow When $\chi=0$

$$T_A = A = 1$$

$$T_B = B \odot C = 0 \odot 1 = 0$$

$$T_C = \bar{A} \bar{B} \bar{C} = \bar{1} \bar{0} \bar{1} = 0$$

101 \rightarrow When $\chi=1$

$$T_A = \bar{B} = 1$$

$$T_B = A + BC = 1$$

$$T_C = A + C = 1$$

No	T_A	T_B	N.S N.S.	
			$\chi=0$	$\chi=1$
1	1	1	0	0
0	0	1	0	1
1	0	1	1	0

1) When $\chi=0$ 101 next state is 001

2) When $\chi=1$ 101 next state is 010.

Segment T
e. A sequential
state don't
change

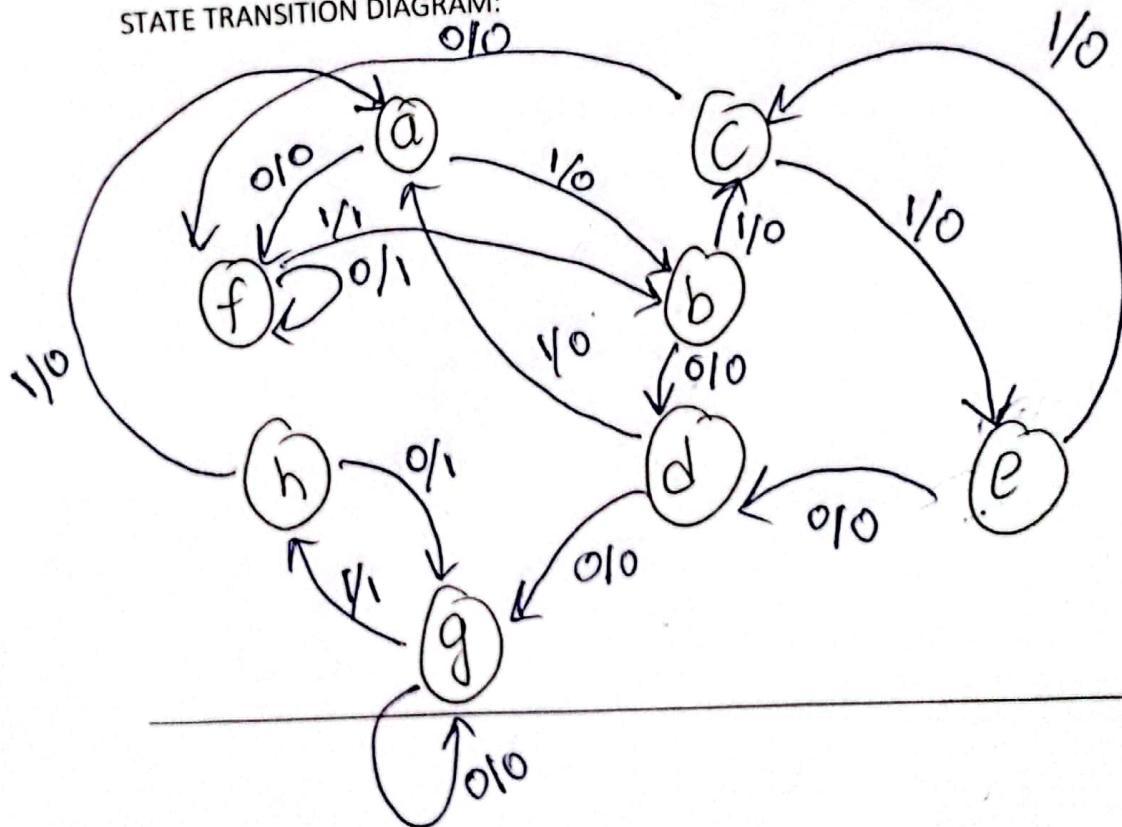
Assignment 4

8. For the given state table perform all of the following.
- Draw the corresponding state diagram
 - Draw Reduced State Table
 - Draw Reduced State Diagram

TABLE:

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

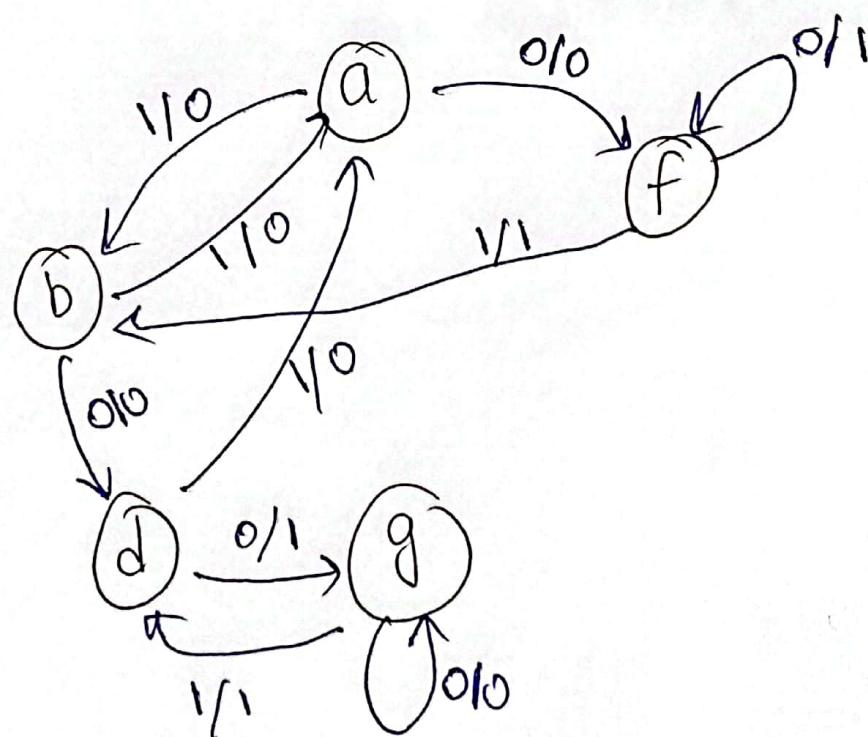
STATE TRANSITION DIAGRAM:



REDUCED STATE TABLE:

PRESENT STATE	NEXT STATE		OUTPUT	
	X=0	X=1	X=0	X=1
a	f	b	0	0
b	d	a	0	0
d	g	a	1	1
f	f	b	0	1
g	g	d	1	1

REDUCED STATE DIAGRAM:



For STATE DIAGRAMS given below convert your university id to binary and determine Output and NEXT State

ACTUAL STATE DIAGRAM

0680

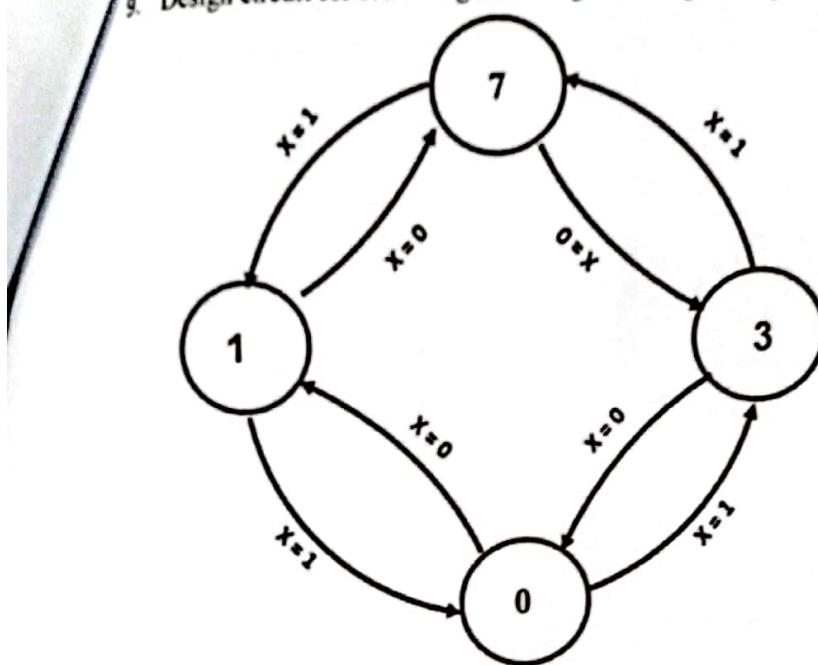
1010101000

REDUCED STATE DIAGRAM

1010101000
abda^fbda^f
0001000101010101000
abda^fbda^f
000100010

Same

9. Design circuit for following state diagram using JK flip Flop?



$$\bar{J}_A = \bar{X} \bar{B}$$

$$K_A = X \oplus C$$

$$\bar{J}_B = 1$$

$$K_B = \bar{X} \bar{A} + X \bar{C}$$

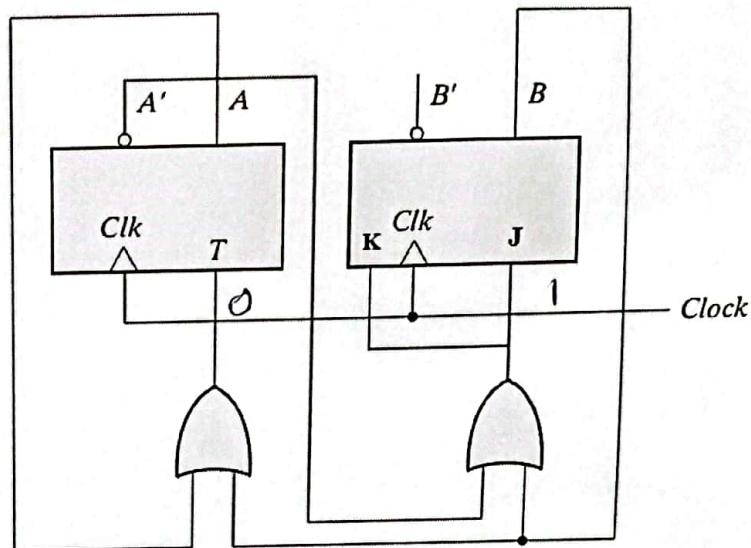
$$\bar{J}_C = \bar{X} B$$

$$K_C = X \odot A$$

TABLE, SIMPLIFICATION & EXPRESSIONS

X	A	B	C	\bar{J}_A	K_A	\bar{J}_B	K_B	\bar{J}_C	K_C	A+	B+	C+	
000	0	0	0	1	X	1	X	0	X	1	1	X	0
000	0	0	1	X	X	X	X	X	X	X	0	X	0
000	0	1	0	X	0	X	X	X	X	X	X	1	1
000	1	0	0	X	X	X	X	X	X	X	X	1	1
000	1	0	1	X	X	X	X	X	X	X	0	1	1
000	0	1	0	X	X	X	X	X	X	X	0	1	1
000	0	1	1	X	X	X	X	X	X	X	0	1	1
000	1	1	0	X	X	X	X	X	X	X	1	1	1
000	1	1	1	X	X	X	X	X	X	X	1	1	1
001	0	0	0	1	X	1	X	0	X	1	0	X	0
001	0	0	1	X	X	X	X	X	X	X	1	1	1
001	0	1	0	X	0	X	X	X	X	X	0	1	1
001	0	1	1	X	X	X	X	X	X	X	1	1	1
001	1	0	0	X	X	X	X	X	X	X	0	0	1
001	1	0	1	X	X	X	X	X	X	X	1	1	1
001	1	1	0	X	X	X	X	X	X	X	1	1	1
001	1	1	1	X	X	X	X	X	X	X	1	1	1
010	0	0	0	1	X	1	X	1	X	0	0	X	0
010	0	0	1	X	X	X	X	X	X	X	1	1	1
010	0	1	0	X	0	X	X	X	X	X	0	1	1
010	0	1	1	X	X	X	X	X	X	X	1	1	1
010	1	0	0	X	X	X	X	X	X	X	0	0	1
010	1	0	1	X	X	X	X	X	X	X	1	1	1
010	1	1	0	X	X	X	X	X	X	X	1	1	1
010	1	1	1	X	X	X	X	X	X	X	1	1	1
011	0	0	0	1	X	0	X	0	X	1	1	X	0
011	0	0	1	X	X	X	X	X	X	X	0	0	1
011	0	1	0	X	0	X	X	X	X	X	1	1	1
011	0	1	1	X	X	X	X	X	X	X	0	1	1
011	1	0	0	X	X	X	X	X	X	X	1	1	1
011	1	0	1	X	X	X	X	X	X	X	0	0	1
011	1	1	0	X	X	X	X	X	X	X	1	1	1
011	1	1	1	X	X	X	X	X	X	X	1	1	1
100	0	0	0	1	X	1	X	1	X	0	0	X	0
100	0	0	1	X	X	X	X	X	X	X	1	1	1
100	0	1	0	X	0	X	X	X	X	X	0	1	1
100	0	1	1	X	X	X	X	X	X	X	1	1	1
100	1	0	0	X	X	X	X	X	X	X	0	0	1
100	1	0	1	X	X	X	X	X	X	X	1	1	1
100	1	1	0	X	X	X	X	X	X	X	1	1	1
100	1	1	1	X	X	X	X	X	X	X	1	1	1
101	0	0	0	1	X	0	X	0	X	1	1	X	0
101	0	0	1	X	X	X	X	X	X	X	0	0	1
101	0	1	0	X	0	X	X	X	X	X	1	1	1
101	0	1	1	X	X	X	X	X	X	X	0	1	1
101	1	0	0	X	X	X	X	X	X	X	1	1	1
101	1	0	1	X	X	X	X	X	X	X	0	0	1
101	1	1	0	X	X	X	X	X	X	X	1	1	1
101	1	1	1	X	X	X	X	X	X	X	1	1	1
110	0	0	0	1	X	1	X	1	X	0	0	X	0
110	0	0	1	X	X	X	X	X	X	X	1	1	1
110	0	1	0	X	0	X	X	X	X	X	0	1	1
110	0	1	1	X	X	X	X	X	X	X	1	1	1
110	1	0	0	X	X	X	X	X	X	X	0	0	1
110	1	0	1	X	X	X	X	X	X	X	1	1	1
110	1	1	0	X	X	X	X	X	X	X	0	1	1
110	1	1	1	X	X	X	X	X	X	X	1	1	1
111	0	0	0	1	X	0	X	0	X	1	1	X	0
111	0	0	1	X	X	X	X	X	X	X	0	0	1
111	0	1	0	X	0	X	X	X	X	X	1	1	1
111	0	1	1	X	X	X	X	X	X	X	0	1	1
111	1	0	0	X	X	X	X	X	X	X	1	1	1
111	1	0	1	X	X	X	X	X	X	X	0	0	1
111	1	1	0	X	X	X	X	X	X	X	1	1	1
111	1	1	1	X	X	X	X	X	X	X	1	1	1

10. Derive the state table and the state diagram of the sequential circuit shown in the given figure. Regenerate equivalent circuit using just D Flip Flop

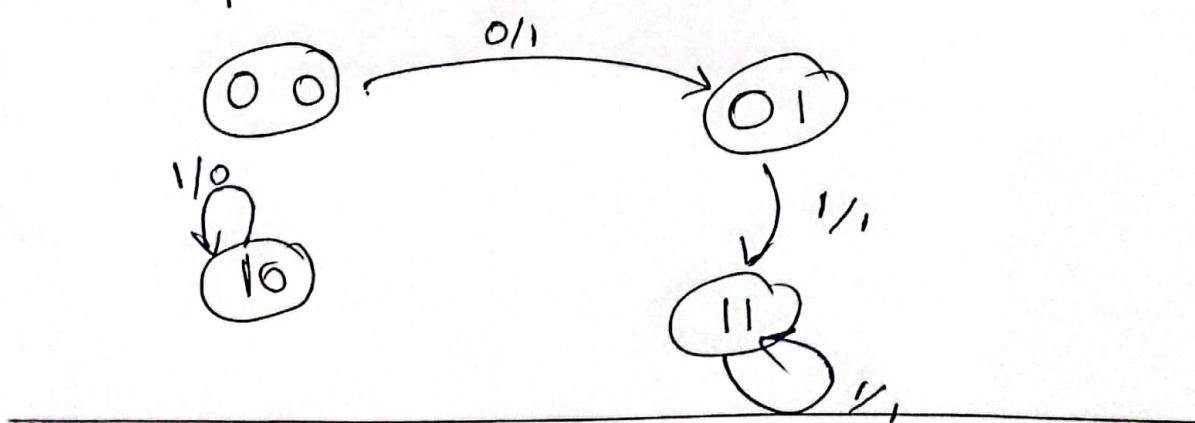


$$T = A + B$$

$$J = \bar{A} + B$$

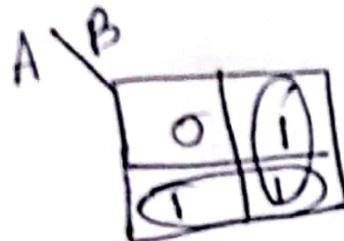
$$K = \bar{A} + B$$

A	B	T	J	K	D ₀	D ₁	A + B +
0	0	0	1	1	0	1	0 1
0	1	1	0	0	1	1	1 1
1	0	0	0	0	1	0	1 0
1	1	0	0	0	1	1	1 1

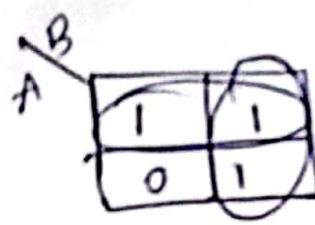


Element 4

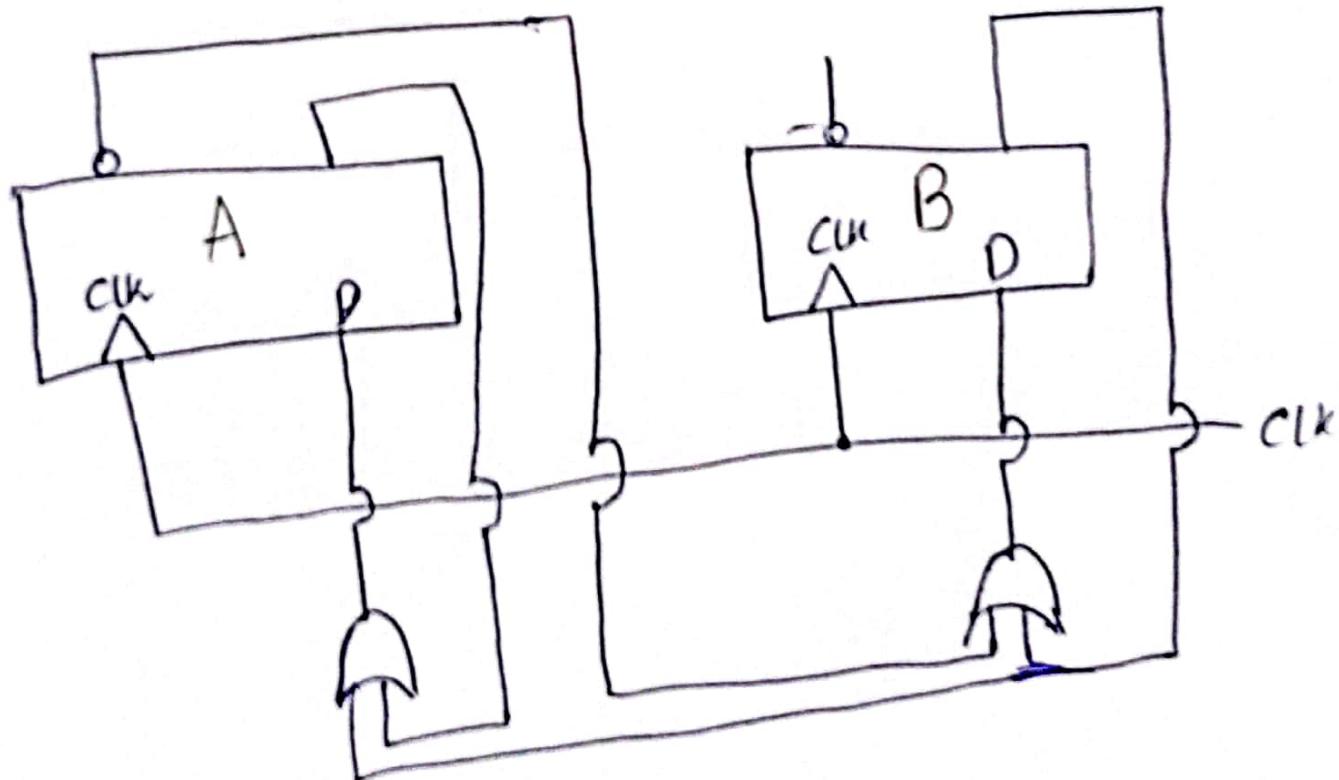
b



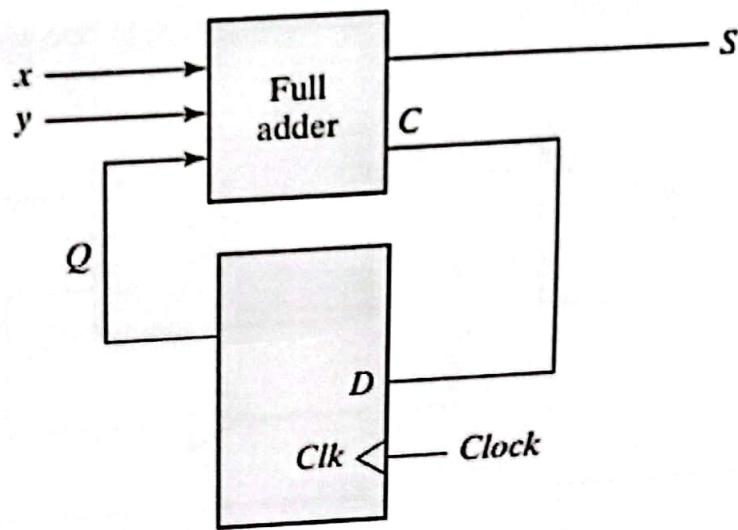
$$= A + B$$

 D_1 

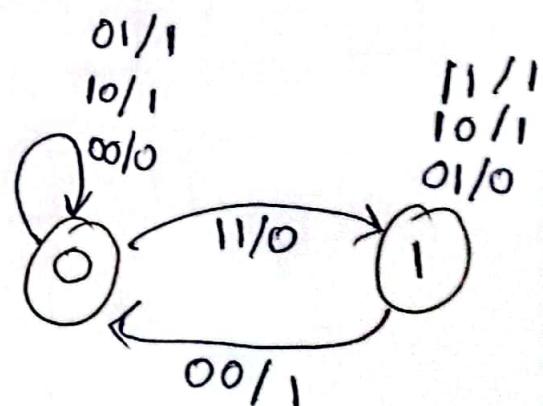
$$= \bar{A} + B$$



1. A sequential circuit has one flip-flop Q , two inputs x and y , and one output S . It consists of a full-adder circuit connected to a D flip-flop, as shown in Fig. Derive the state table and state diagram of the sequential circuit.



Q	x	y	Q_{t+1}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
0	0	1	1	0
1	0	0	1	0
1	1	1	1	1



Complete the timing diagram for the output \overline{CLK} , Y and Q by considering that you are applying given CLK and D as an input to the circuit given below where En is active high enable

Note: Highlight the part of your timing diagram that indicates that it's a Master SlaveFlip flop

