Management Data Input/Output

Management Data Input/Output (**MDIO**), also known as **Serial Management Interface** (**SMI**) or **Media Independent Interface Management** (**MIIM**), is a serial bus defined for the Ethernet family of IEEE 802.3 standards for the Media Independent Interface, or **MII**. The MII connects media access control (MAC) devices with Ethernet physical layer (PHY) circuits. The MAC device controlling the MDIO is called the Station Management Entity (SME).

Relationship to MII

MII has two signal interfaces:

- A Data interface to the Ethernet MAC, for sending and receiving Ethernet frame data.
- A PHY management interface, MDIO, used to read and write the control and status registers of the PHY in order to configure each PHY before operation, and to monitor link status during operation.

Electrical specification

The MDIO interface is implemented by two signals:

- MDIO Interface Clock (MDC): clock driven by the MAC device to the PHY.
- MDIO data: bidirectional, the PHY drives it to provide register data at the end of a read operation.

The bus only supports a single MAC as the master, and can have up to 32 PHY slaves.

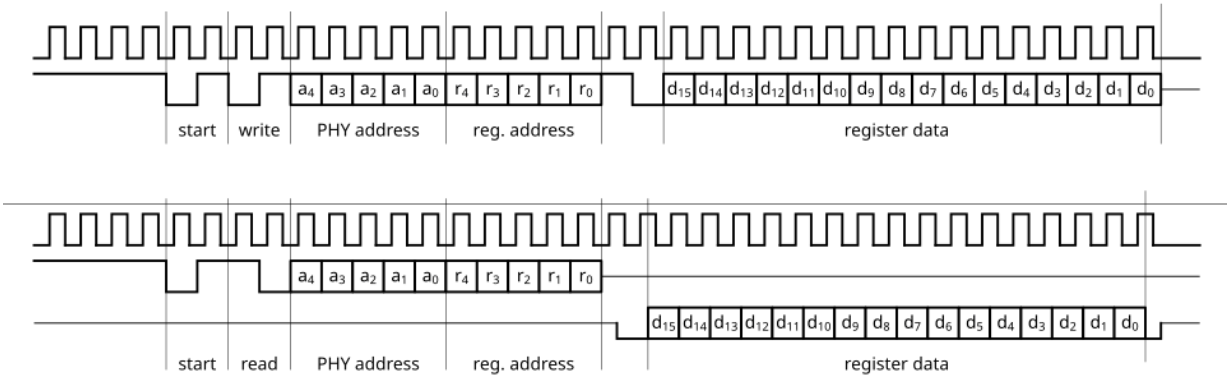
The MDC can be periodic, with a minimum period of 400 ns, which corresponds to a maximum frequency of 2.5 MHz. Newer chips, however, allow faster accesses. For example, the DP83640 supports a 25 MHz maximum clock rate for MDC.

The MDIO requires a specific pull-up resistor of 1.5 kΩ to 10 kΩ, taking into account the total worst-case leakage current of 32 PHYs and one MAC.

Bus timing (clause 22)

Before a register access, PHY devices generally require a preamble of 32 ones to be sent by the MAC on the MDIO line. The access consists of 16 control bits, followed by 16 data bits. The control bits consist of 2 start bits, 2 access type bits (read or write), the PHY address (5 bits), the register address (5 bits), and 2 "turnaround" bits.

During a write command, the MAC provides address and data. For a read command, the PHY takes over the MDIO line during the turnaround bit times, supplies the MAC with the register data requested, then releases the MDIO line.



When the MAC drives the MDIO line, it has to guarantee a stable value 10 ns (setup time) before the rising edge of the clock MDC. Further, MDIO has to remain stable 10 ns (hold time) after the rising edge of MDC.

When the PHY drives the MDIO line, the PHY has to provide the MDIO signal between 0 and 300 ns after the rising edge of the clock.[1] Hence, with a minimum clock period of 400 ns (2.5 MHz maximum clock rate) the MAC can safely sample MDIO during the second half of the low cycle of the clock.

MDIO Packet Format (clause 22)

	MDIO Packet Format																															
Bit:	**0**	**1**	**2**	**3**	**4**				**8**	**9**				**13**	**14**	**15**	**16**															**31**
0	PRE_32																															
32	ST		OP		PA5					RA5					TA		D16															

PRE_32

The first field in the MDIO header is the Preamble. During the preamble, the MAC sends 32 bits, all '1', on the MDIO line.

ST

The Start field consists of 2 bits and always contains the combination '01'.

OP

The Opcode consists of 2 bits. There are two possible opcodes, read '10' or write '01'.

PA5

5 bits, PHY address.

RA5

The Register Address field indicates the register to be written to or read from. It is 5 bits long.

TA

The turn-around field is 2 bits long. When data is being written to the PHY, the MAC writes '10' to the MDIO line. When data is being read, the MAC releases the MDIO line.

D16

16 bits, data. This can be sent by either the SME or the PHY, depending on the value of the OP field.

Z

Tristate MDIO.

Commands

IEEE 802.3 Part 3[1] use different opcodes and start sequences. Opcodes 00(set address) and 11(read)/01(write)/10(read increment) are used as two serial transactions to read and write registers.

References

1. *IEEE 802.3 Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) access method and Physical Layer specification*. IEEE. doi:10.1109/IEEESTD.2018.8457469 (https://doi.org/10.1109%2FIEEESTD.2018.8457469). ISBN 978-1-5044-5090-4.

External links

- Clause 22 Access to Clause 45 Registers (http://www.ieee802.org/3/efm/public/nov02/oam/pannell_oam_1_1102.pdf)