GPIO Application

CSE 3105 – Computer Interfacing & Embedded System

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- ☐ The software initialization involves **two** key steps:
 - First, it enables the clock of the GPIO port B via the RCC module.
 - Second, it configures pin 2 of GPIO port B as a general-purpose output pin, with the output type as **push-pull**.
 - To light up the red LED, we need to output logic "1" to pin 2.

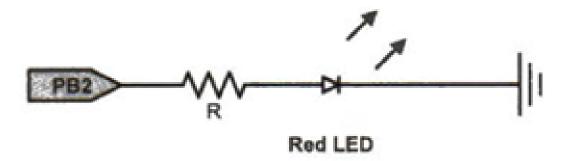


Figure: Connection diagram between a processor pin and LED

- ☐ In assembly, a load-modify-store sequence is required to change the register value stored in memory.
- Also, we can use "EQU" directive to create symbols for the GPIO B base address and ODR register offset, which make the assembly program more readable and self-documenting.
- \Box The following is an example:

```
GPIOB_BASE EQU 0x48000400 ; Base memory address
```

GPIO_ODR EQU 20 ; Byte offset of ODR from the base

LDR r7, =GPIOB BASE ; Load GPIO port B base address

LDR rl, [r7, #GPIO ODR]; Read GPIOB->ODR

ORR rl, rl, #(1«6) ; Set bit 6

STR rl, [r7, #GPIO_ODR] ; Write to GPIOB->ODR

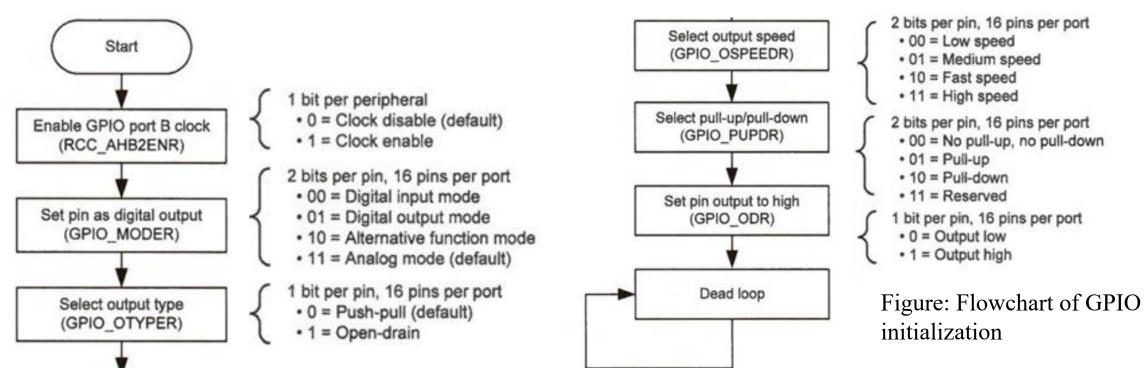
☐ We need to enable the clock of GPIO port B. ☐ To save energy, every peripheral's clock is turned off by default. ☐ We can enable the clock of a peripheral by setting the corresponding bit of the clock control register defined in the reset and clock control (RCC) structure. // Reset and clock control typedef struct { _ IO uint32_t CR; // Clock control register IO uint32 t ICSCR; // Internal clock sources calibration register IO uint32 t CFGR; // Clock configuration register _ IO uint32_t AHBlENR; // AHB 1 peripheral clocks enable register IO uint32 tAHB2ENR; // AHB 2 peripheral clocks enable register IO uint32 t AHB3ENR; // AHB 3 peripheral clocks enable register } RCC TypeDef; #define RCC ((RCC_TypeDef *) 0x40021000))

Field	Full Name	Purpose
CR	Clock Control Register	Enables/disables oscillators (HSI, HSE, PLL), and system reset flags.
ICSCR	Internal Clock Sources Calibration Register	Calibrates internal oscillators (like HSI or MSI). Improves accuracy.
CFGR	Clock Configuration Register	Selects system clock source and sets prescalers for AHB, APB buses.
AHB1ENR	AHB1 Clock Enable Register	Enables/disables clocks to peripherals on the AHB1 bus (e.g., GPIOA, DMA1).
AHB2ENR	AHB2 Clock Enable Register	Enables clocks for AHB2 peripherals (e.g., GPIOB, USB, RNG).
AHB3ENR	AHB3 Clock Enable Register	Enables clocks for peripherals on AHB3 (e.g., external memory controller).

☐ The following C statements enable the clock of GPIO port B.

#define RCC_AHB2ENR_GPIOBEN (0x00000002)
RCC->AHB2ENR |= RCC_AHB2ENR_GPIOBEN;

☐ The flowchart of initializing a GPIO pin as digital output with push pull can be designed as:



- When we change the value of specific bits in a register, we need to preserve the value of the other bits in this register to avoid creating unexpected negative impacts. For example, if we want to set the least significant bit in register R, " $\mathbf{R} = \mathbf{0}\mathbf{x}\mathbf{1}$;" is incorrect because it also clears all the other bits. Instead, we should use a bitwise logical OR operation " $\mathbf{R} \models \mathbf{0}\mathbf{x}\mathbf{1}$;"
- When we change the value of multiple bits, it is a good practice to reset these bits before updating them. For example, if we want to set the least significant four bits b3b2b1b0 in register R to 1001, we need to clear these four bits first by running " $\mathbf{R} \& = \sim 0 \mathbf{x} \mathbf{F}$; $\mathbf{R} = 0 \mathbf{x} 9$;"
- ☐ If we do not clear these four bits first, we may fail to set the register correctly if their initial values are not **0**. For example, if the value of b3b2b1b0 is 0111 initially, " $\mathbf{R} \models \mathbf{0}\mathbf{x}\mathbf{9}$;" will lead a binary result of 1111.

- □ Each GPIO port has a *data output register* (ODR) and a *data input register* (IDR).
- □ Each bit in ODR controls the output of a corresponding GPIO pin in this port. In a push-pull setting, if the bit value is 1, the output voltage on its corresponding GPIO pin is high; if the bit value is 0, the output voltage then is low.
- ☐ The IDR register records the input of all pins of a GPIO port.

☐ The following C program demonstrates how to set up a GPIO pin and light up an LED in detail. Suppose we use the GPIO pin PB 2 to drive a red LED.

```
// Red LED is connected PB 2 (GPIO port B pin 2)
void GPIO_Clock_Enable(){
    // Enable the clock to GPIO port B
    RCC->AHB2ENR |= RCC_AHB2ENR_GPIOBEN;
}
```

☐ The following C program demonstrates how to set up a GPIO pin and light up an LED in detail. Suppose we use the GPIO pin PB 2 to drive a red LED.

```
// Set output type of pin 2 as push-pull
// 0 = push-pull (default)
// 1 = open-drain
GPIOB->OTYPER &= ~(1<<2);
// Set output speed of pin 2 as Low
// 00 = Low speed, 01 = Medium speed
// 10 = Fast speed, 11 = High speed
GPIOB->OSPEEDR &= ~(3UL<<4); // Clear speed bits
// Set pin 2 as no pull-up, no pull-down
// 00 = no pull-up, no pull-down 01 = pull-up
// 10 = pull-down,
GPIOB->PUPDR &= ~(3UL<<4);
// no pull-up, no pull-down</pre>
```

☐ The following C program demonstrates how to set up a GPIO pin and light up an LED in detail. Suppose we use the GPIO pin PB 2 to drive a red LED.

- ☐ The implementation in assembly is like the above C program. In the program,
 - ❖ GPIOB_BASE and RCC_BASE are pre-defined memory addresses
 - * GPIO_MODER, GPIO_OTYPER, GPIO_OSPEEDR, GPIO_PUPDR, and GPIO_ODR are byte offset of its corresponding variable in the data structure GPIO_ TypeDef defined previously.

```
; Constants defined in file stm32L476xx constants.s
; Memory addresses of GPIO port B and RCC (reset and clock control) data
; structure. These addresses are predefined by the chip manufacturer.
GPIOB BASE
                   EQU
                         0x48000400
RCC BASE
            EQU
                         0x40021000
; Byte offset of each variable in the GPIO_TypeDef structure
GPIO MODER
                   EQU
                         0x00
GPIO OTYPER
                   EQU
                         0x04
GPIO RESERVEDO
                   EQU
                         0x06
GPIO OSPEEDR
                   EQU
                         0x08
                   EQU
                         0x0C
GPIO PUPDR
GPIO IDR
                   EQU
                         0x10
GPIO RESERVED1
                         0x12
GPIO ODR
                         0x14
```

```
GPIO RESERVED2
                   EQU
                         0x16
GPIO BSRRL
                   EQU
                         0x18
GPIO BSRRH
                         0x1A
GPIO LCKR
                         0x1C
GPIO AFR0
                         0x20
                                  AFR[0]
GPIO AFR1
                         0x24
                               ; AFR[1]
GPIO AFRL
                         0x20
GPIO_AFRH
                         0x24
                   EQU
; Byte offset of variable AHB2ENR in the RCC_TypeDef structure
RCC AHB2ENR
                         0x4C
                   EQU
```

☐ The implementation in assembly is like the above C program.

```
INCLUDE stm321476xx_constants.s
AREA main, CODE, READONLY
        __main ; make __main visible to linker
EXPORT
ENTRY
main PROC
; Enable the clock to GPIO port B
; Load address of reset and clock control (RCC)
LDR r2, =RCC_BASE ; Pseduo instruction
LDR r1, [r2, \#RCC\_AHB2ENR] ; r1 = RCC->AHB2ENR
              ; Set bit 2 of AHB2ENR
ORR r1, r1, #2
STR r1, [r2, #RCC_AHB2ENR] ; GPIO port B clock enable
; Load GPIO port B base address
LDR r3, =GPIOB_BASE ; Pseudo instruction
```

☐ The implementation in assembly is like the above C program.

```
; Set pin 2 I/O mode as general-purpose output
LDR r1, [r3, #GPIO_MODER] ; Read the mode register
BIC r1, r1, \#(3 << 4) ; Direction mask pin 6, clear bits 5 and 4 ORR r1, r1, \#(1 << 4) ; Set mode as digital output (mode = 01)
STR r1, [r3, #GPIO_MODER] ; Save to the mode register
; Set pin 2 the push-pull mode for the output type
LDR r1, [r3, #GPIO_OTYPER] ; Read the output type register
BIC r1, r1, #(1<<2) ; Push-pull(0), open-drain (1)
STR r1, [r3, #GPIO_OTYPER] ; Save to the output type register
; Set I/O output speed value as Low
LDR r1, [r3, #GPIO_OSPEEDR] ; Read the output speed register
BIC r1, r1, #(3<<4) ; Low(00), Medium(01), Fast(01), High(11)
STR r1, [r3, #GPIO_OSPEEDR] ; Save to the output speed register
```

☐ The implementation in assembly is like the above C program.

```
; Set I/O output speed value as Low
 LDR r1, [r3, #GPIO_OSPEEDR] ; Read the output speed register
 BIC r1, r1, #(3<<4) ; Low(00), Medium(01), Fast(01), High(11)
 STR r1, [r3, #GPIO_OSPEEDR] ; Save to the output speed register
 ; Set I/O as no pull-up, no pull-down
 LDR r1, [r3, #GPIO_PUPDR] ; r1 = GPIOB -> PUPDR
 BIC r1, r1, #(3<<4) ; No PUPD(00), PU(01), PD(10), Reserved(11)
STR r1, [r3, #GPIO_PUPDR] ; Save pull-up and pull-down setting
 ; Light up LED
 LDR r1, [r3, #GPIO_ODR] ; Read the output data register
 ORR r1, r1, #(1<<2) ; Set bit 2
 STR r1, [r3, #GPIO_ODR] ; Save to the output data register
stop
 B stop ; dead Loop & program hangs here
 ENDP
  END
```

Self Study

- □ Article 14.8 (Pushbutton) and 14.9 (Keypad Scan)
- Ref. Book: Embedded Systems with ARM Cortex-M Microcontrollers in Assembly Language and C 3rd Ed Yifeng Zhu Eman (2018) [Chapter 14]

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