VLSI Project Report

1. **Schematic/Figure** of your design.

   Design 1:

   Implementing priority inversion on hardware level.

   Design 2,3,4:

   Sensors[5:0] are the signals coming from the sensors, current represent current state
   If(sensors == 0):
   Next state = idle;
   Out = 0;
   Else if(sensors[i] == 1 && i > current)
   Assign next state is the state of the minimum i that satisfy condition;
   Else
   Iterate from sensors[0] to sensors[current] and assign next state to the first match

   Output = 1<<next state;

   Design 5:

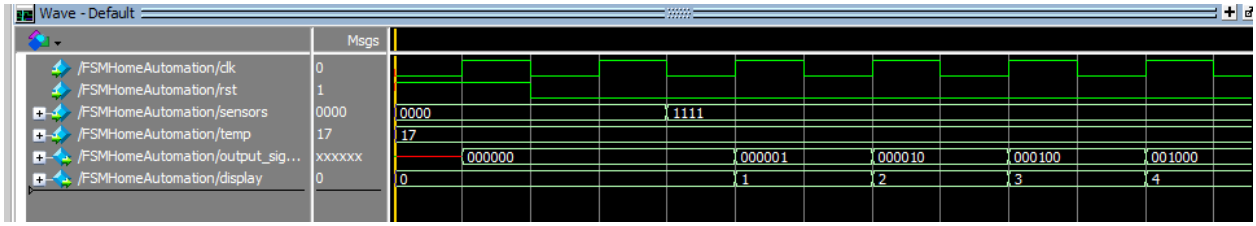
   Sensors[5:0] are the signals coming from the sensors, current represent current state
   If(sensors == 0):
   Next state = idle;
   Out = 0;
   Else if(sensors[i] == 1 && i > current)
   Assign next state is the state of the minimum i that satisfy condition;
   Else
   Iterate from sensors[0] to sensors[current] and assign next state to the first match

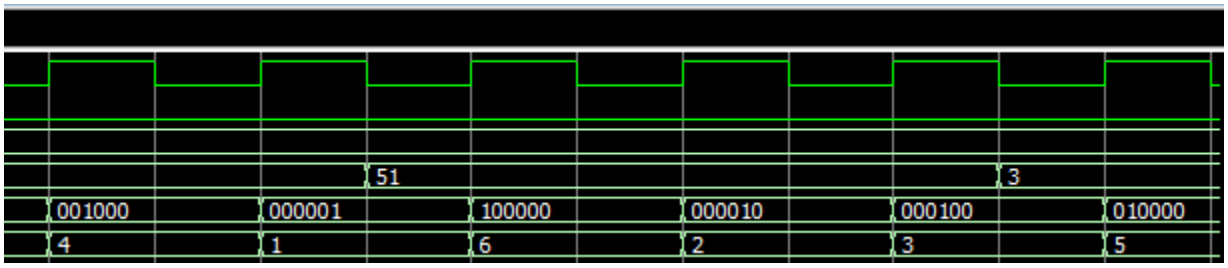
   Output = 1<<current;

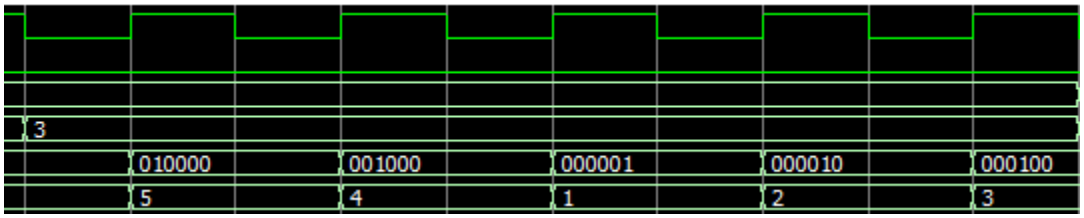
2. Any **screenshot** required above (from 1-11).

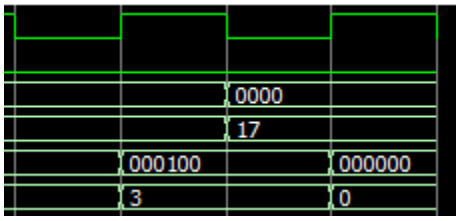
a. Design 1

i. Pre-synthesis simulation

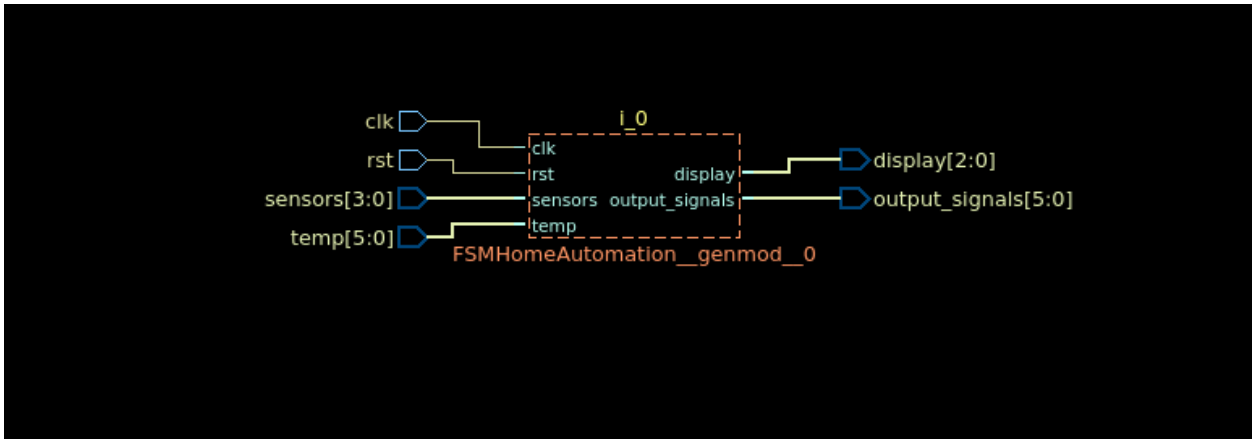


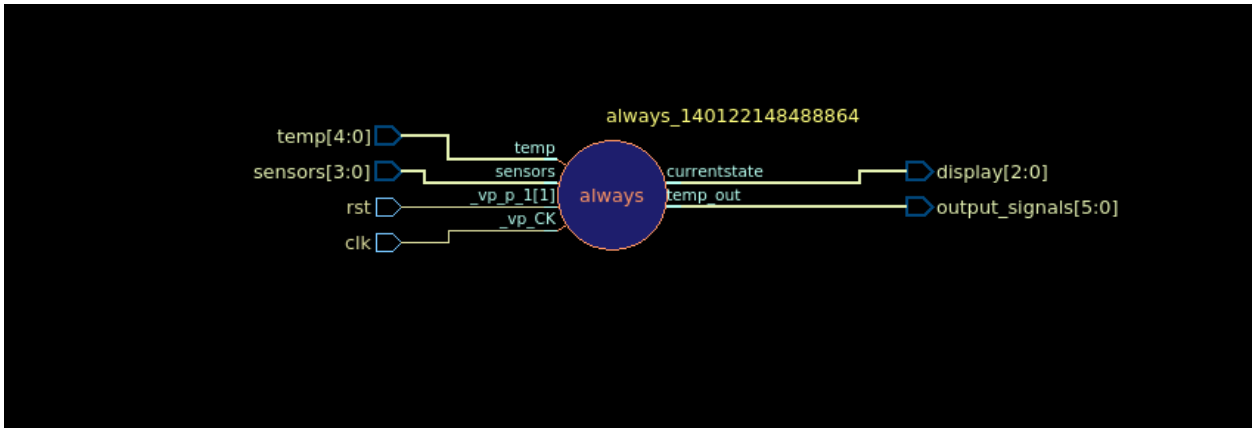


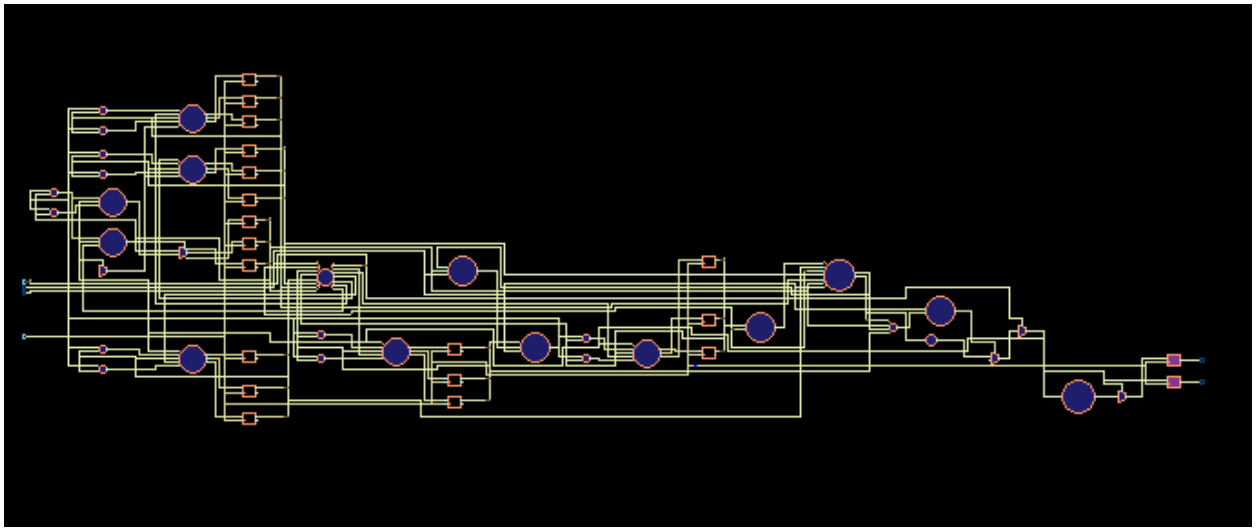




ii. Synthesis schematic







iii. Reports (**design, path and power**.)

Design:

Report Physical info:

		Area (squm)	Leakage (uW)
Design Name	FSMHomeAutomation		
Total Instances	1296	1178	25.216
Macros	0	0	0.000
Pads	0	0	0.000
Phys	0	0	0.000
Blackboxes	0	0	0.000
Cells	1296	1178	25.216
Buffers	0	0	0.000
Inverters	337	179	4.837
Clock-Gates	0	0	0.000
Combinational	932	876	18.171
Latches	0	0	0.000
FlipFlops	27	123	2.208
Single-Bit FF	27	123	2.208
Multi-Bit FF	0	0	0.000
Clock-Gated	0		
Bits	27	123	2.208
Load-Enabled	0		
Clock-Gated	0		
Tristate Pin Count	0		
Physical Info	Placed		
Chip Size (mm x mm)	0.104 x 0.104	10882	
Fixed Cell Area		0	
Phys Only	0	0	
Placeable Area		1921	
Movable Cell Area		1178	
Utilization (%)	61		
Chip Utilization (%)	61		
Total Wire Length (mm)	1.041		
Longest Wire (mm)	0.053		
Average Wire (mm)	0.052		

Path:

Report Path Groups:

	Path Group	Weight	Critical Range(ps)	Worst Slack(ps)
1	default	1.000	0.0	569.5
2	I2R	1.000	0.0	25.6
3	I2O	1.000	0.0	<ill>
4	R2O	1.000	0.0	80.3

Power:

Report Power (instances with prefix '*' are included in total) :

	Instance	Internal Power(uw)	Switching Power(uw)	Leakage Power(uw)	Total Power(uw)
1	*currentstate_reg[2]	1.721545	2.044160	0.079112	3.844817
2	*currentstate_reg[1]	2.485642	2.949635	0.079112	5.514390
3	*currentstate_reg[0]	1.680164	1.989510	0.079112	3.748787
4	*temp_out_reg[5]	0.525816	0.625695	0.079112	1.230623
5	*temp_out_reg[4]	0.249505	0.296898	0.079112	0.625515
6	*temp_out_reg[3]	1.043621	1.241146	0.079112	2.363879
7	*temp_out_reg[2]	0.506999	0.602935	0.079112	1.189046
8	*temp_out_reg[1]	1.906625	2.262533	0.079112	4.248271
9	*temp_out_reg[0]	1.008644	1.197663	0.079112	2.285419
.					
.					
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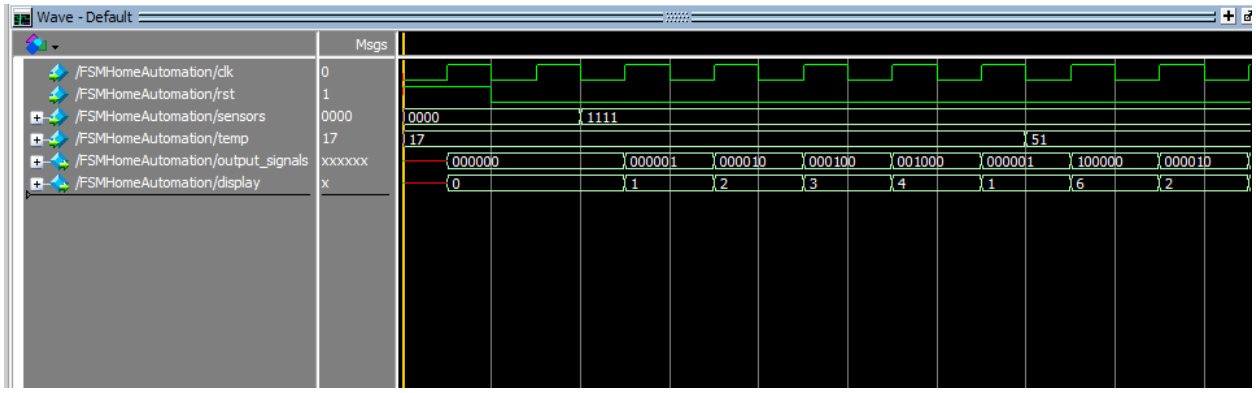
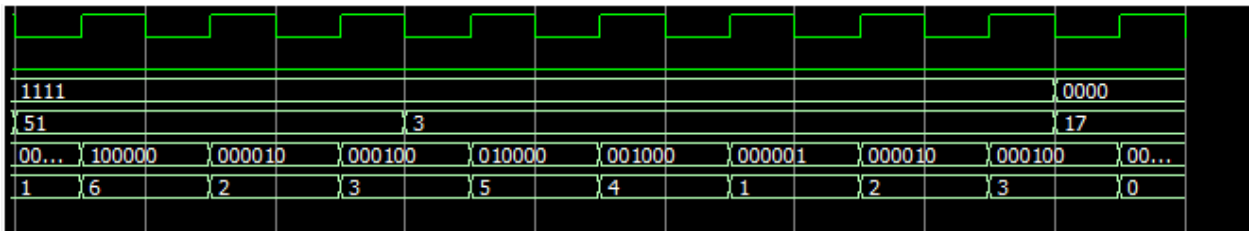
.					
1185	*i_0_1_714	0.263221	0.098619	0.014353	0.376193
1186	*i_0_1_715	0.167825	0.538445	0.017393	0.723664
1187	*i_0_1_716	8.901238	19.840952	0.014353	28.756544
1188	*i_0_1_717	0.272092	12.767406	0.014353	13.053851
1189	*i_0_1_718	0.293748	1.725352	0.014353	2.033453
1190	*i_0_1_719	0.249436	13.310367	0.014353	13.574156
1191	*i_0_1_720	0.272658	1.402829	0.017393	1.692880
1192	*i_0_1_721	0.253269	2.260654	0.014353	2.528275
1193	*i_0_1_722	0.370018	7.161611	0.017393	7.549022
1194	*i_0_1_723	0.304095	16.192986	0.014353	16.511435
1195	*i_0_1_724	0.272897	17.889002	0.014353	18.176254
1196	*i_0_1_725	0.142723	0.210101	0.022619	0.375444
1197	*i_0_1_726	0.098629	0.143797	0.018105	0.260531
1198					
1199	*TOTAL	961.778076	2711.337891	25.216120	3698.332275

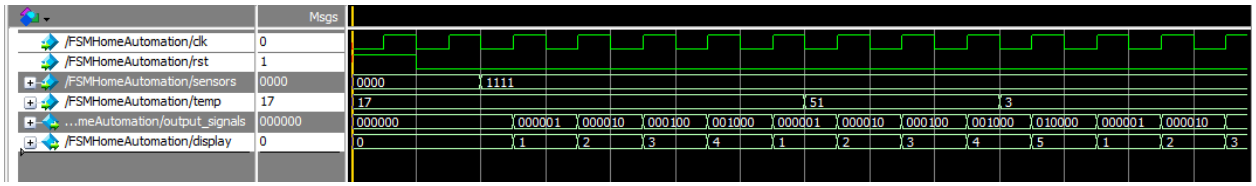
iv. Post-synthesis simulation

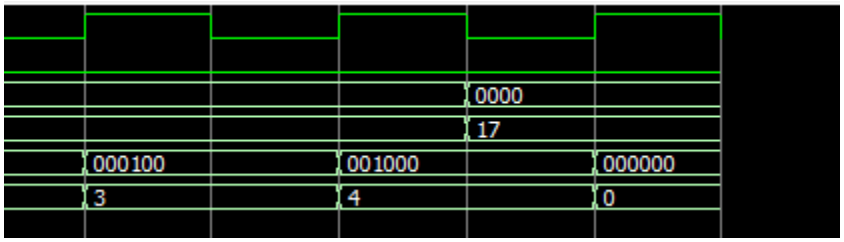




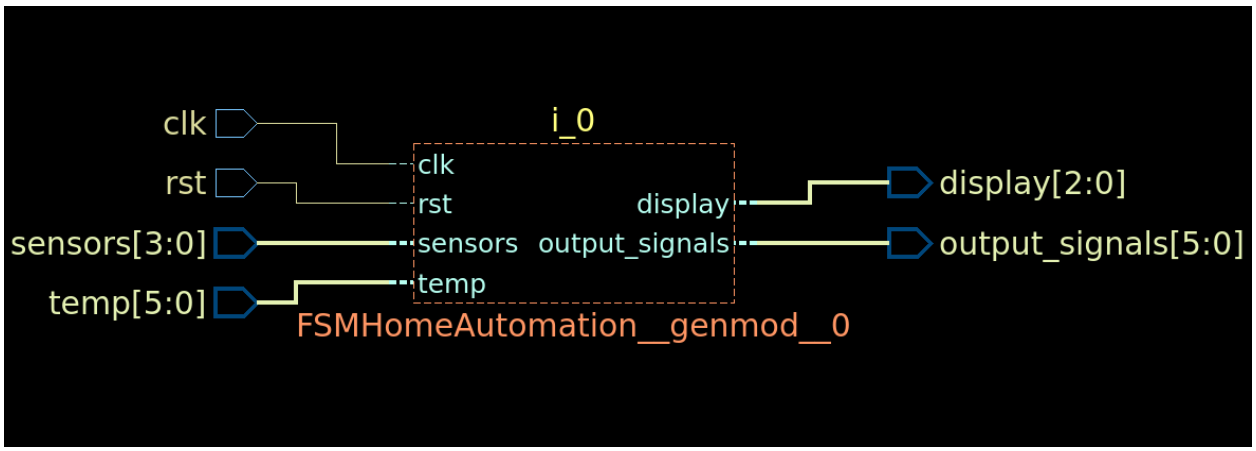
b. Design 2

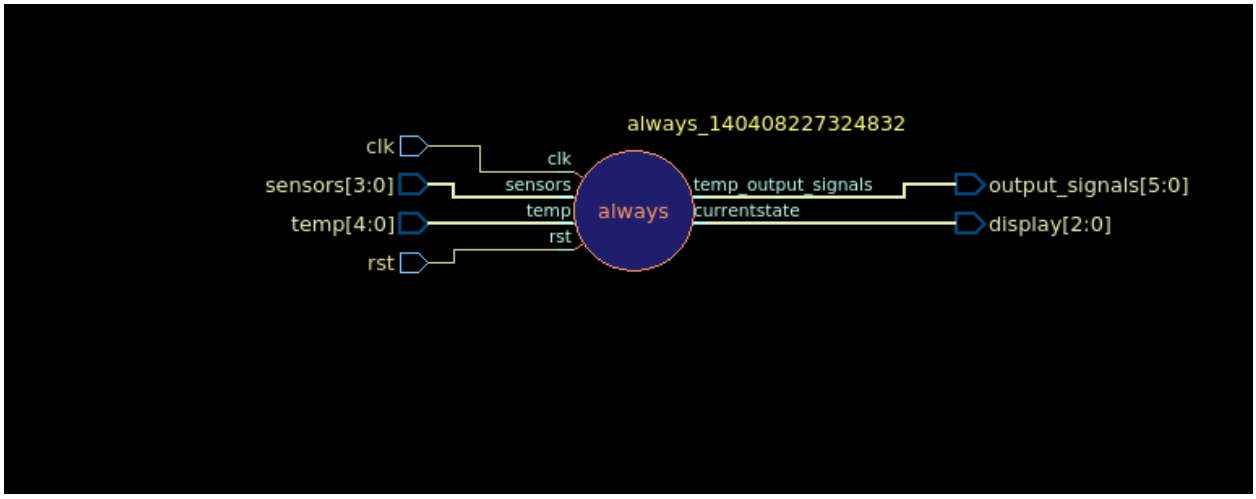
i. Pre-synthesis simulation

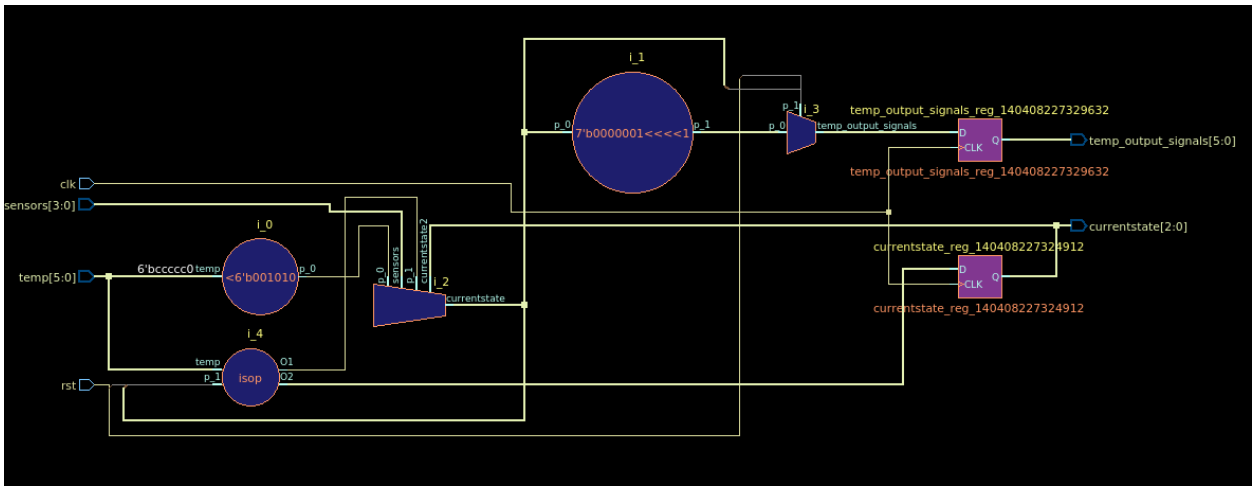


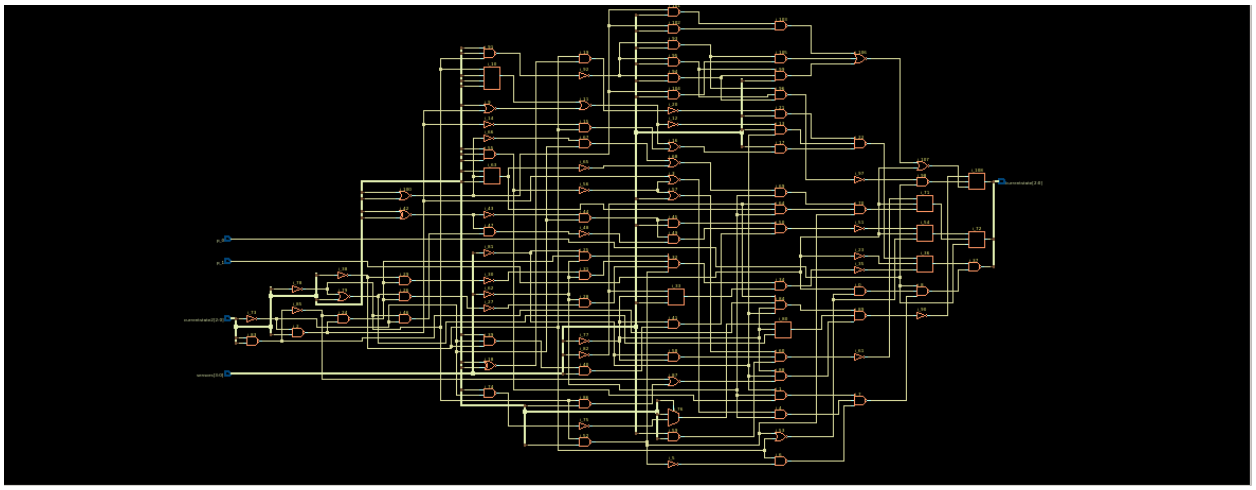


ii. Synthesis schematic









iii. Reports (**design, path and power**.)

Design:

```
Report Physical info:
-----------------------+-----------------+----------+------------
                       |                 |Area (squm)|Leakage (uW)
-----------------------+-----------------+----------+------------
Design Name            |FSMHomeAutomation|          |
  Total Instances      |              156|       164|       3.502
    Macros             |                0|         0|       0.000
    Pads               |                0|         0|       0.000
    Phys               |                0|         0|       0.000
    Blackboxes         |                0|         0|       0.000
    Cells              |              156|       164|       3.502
      Buffers          |                0|         0|       0.000
      Inverters        |               38|        20|       0.545
      Clock-Gates      |                0|         0|       0.000
      Combinational    |              109|       103|       2.208
      Latches          |                0|         0|       0.000
      FlipFlops        |                9|        41|       0.748
       Single-Bit FF   |                9|        41|       0.748
       Multi-Bit FF    |                0|         0|       0.000
       Clock-Gated     |                0|          |
       Bits            |                9|        41|       0.748
         Load-Enabled  |                0|          |
         Clock-Gated   |                0|          |
  Tristate Pin Count   |                0|          |
Physical Info          |Placed           |          |
  Chip Size (mm x mm)  |0.077 x 0.077    |      5858|
  Fixed Cell Area      |                 |         0|
    Phys Only          |                0|         0|
  Placeable Area       |                 |       255|
  Movable Cell Area    |                 |       164|
  Utilization (%)      |               64|          |
  Chip Utilization (%) |               64|          |
  Total Wire Length (mm)|            0.769|          |
  Longest Wire (mm)    |            0.039|          |
  Average Wire (mm)    |            0.038|          |
-----------------------+-----------------+----------+------------
```

Path:

Report Path Groups:

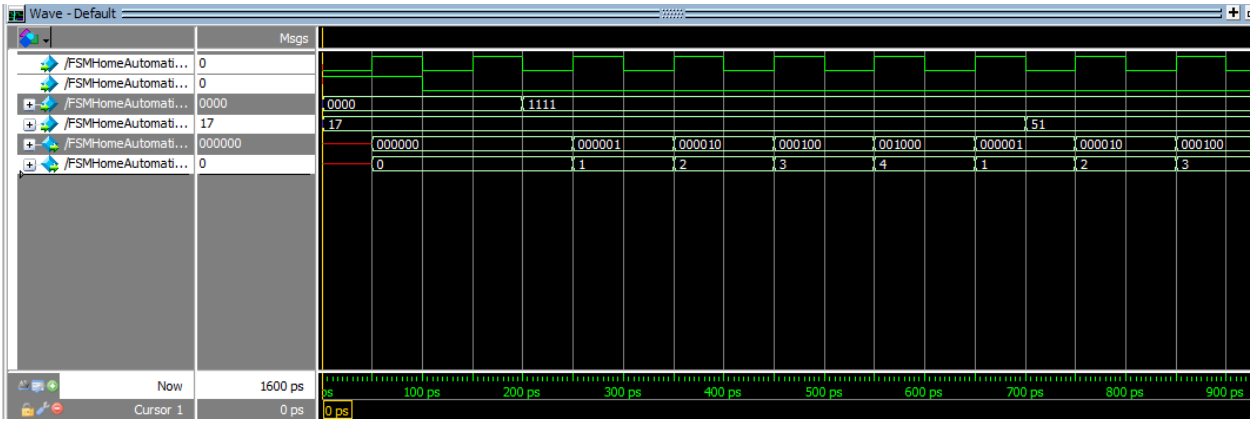
	Path Group	Weight	Critical Range(ps)	Worst Slack(ps)
1	default	1.000	0.0	464.9
2	I2R	1.000	0.0	0.1
3	I2O	1.000	0.0	<ill>
4	R2O	1.000	0.0	533.5

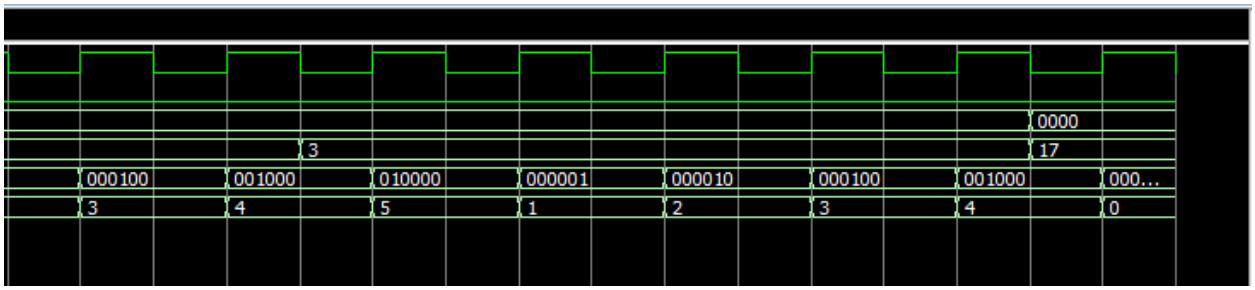
Power:

Report Power (instances with prefix '*' are included in total) :

	Instance	Internal Power(uw)	Switching Power(uw)	Leakage Power(uw)	Total Power(uw)
1	*currentstate_reg[2]	2.802215	15.063667	0.079112	17.944994
2	*currentstate_reg[1]	3.678111	22.444254	0.079112	26.201475
3	*currentstate_reg[0]	2.671433	16.464357	0.079112	19.214905
4	*i_0_0_0	2.054896	2.241766	0.014353	4.311016
5	*i_0_0_1	1.379093	4.150906	0.017393	5.547392
6	*i_0_0_2	2.884940	1.022788	0.014353	3.922082
7	*i_0_0_3	2.024328	5.903510	0.017393	7.945232
8	*i_0_0_4	9.629982	1.363718	0.014353	11.008053
9	*i_0_0_5	9.637429	1.316520	0.014353	10.968302
.					
.					
.					
.					
.					
140	*temp_output_signals_reg[1]	1.553417	1.652364	0.079112	3.284893
141	*temp_output_signals_reg[5]	1.130431	1.205290	0.079112	2.414833
142	*temp_output_signals_reg[3]	0.694582	0.738480	0.079112	1.512174
143	*temp_output_signals_reg[4]	0.446858	0.474818	0.079112	1.000788
144	*temp_output_signals_reg[0]	0.627183	0.666679	0.079112	1.372974
145					
146	*TOTAL	310.441315	400.082214	3.501752	714.025269

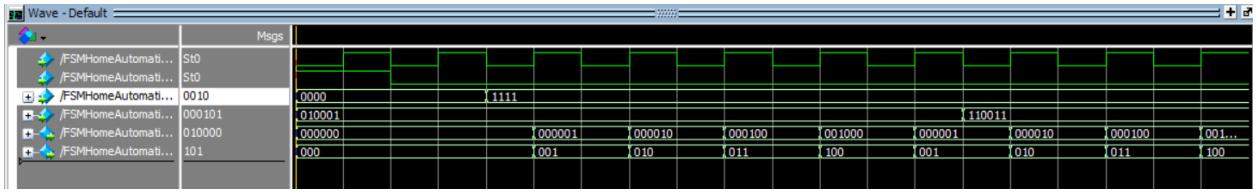
iv. Post-synthesis simulation

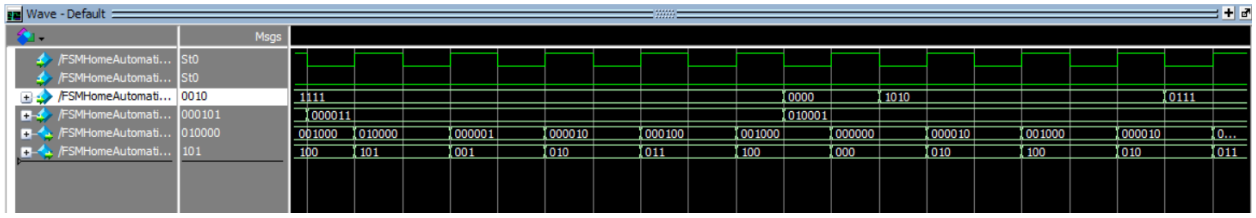


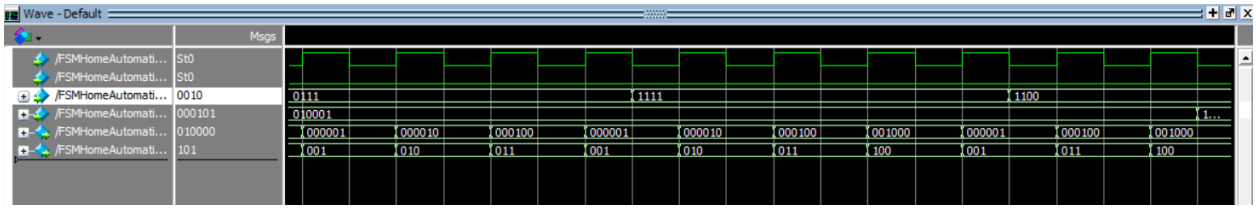


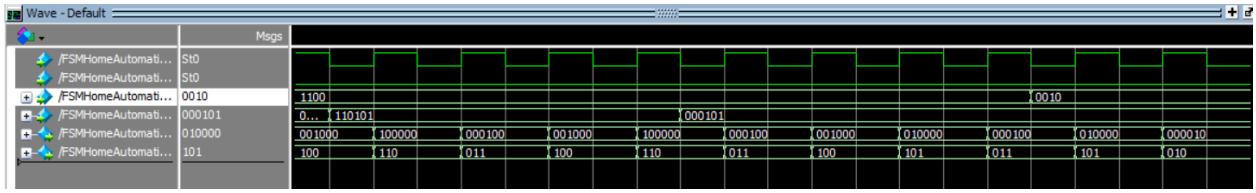
c. Design 3

i. Pre-synthesis simulation

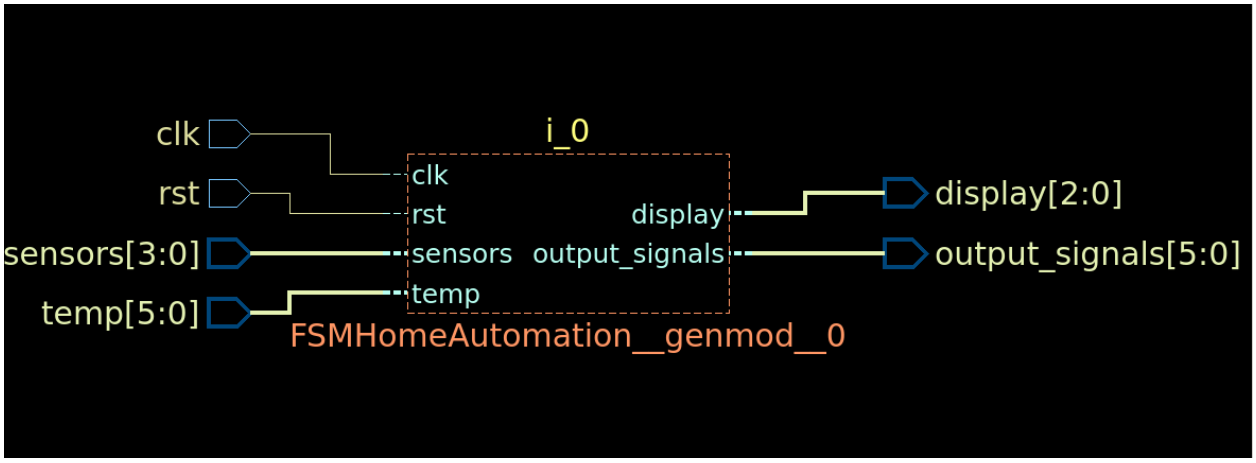


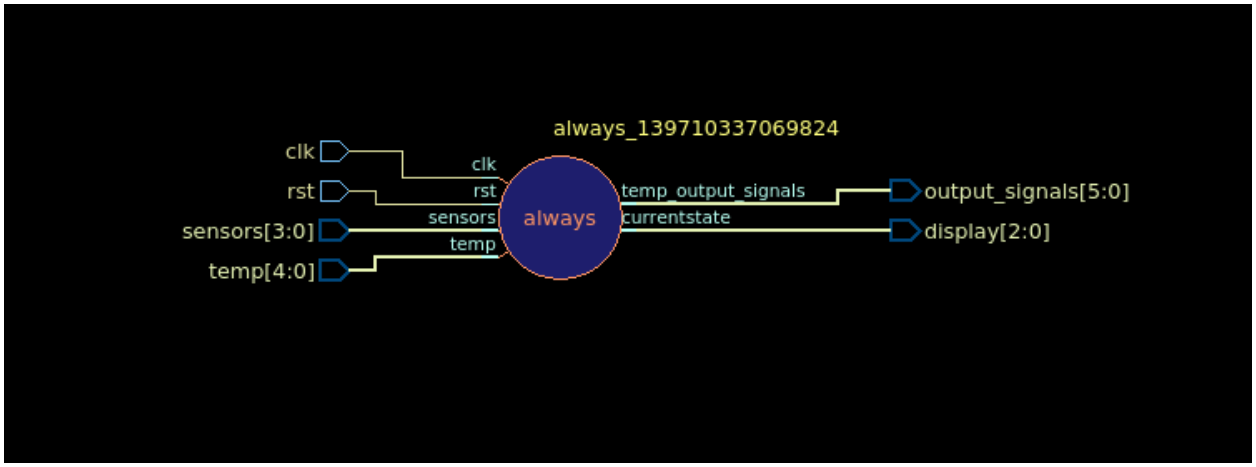


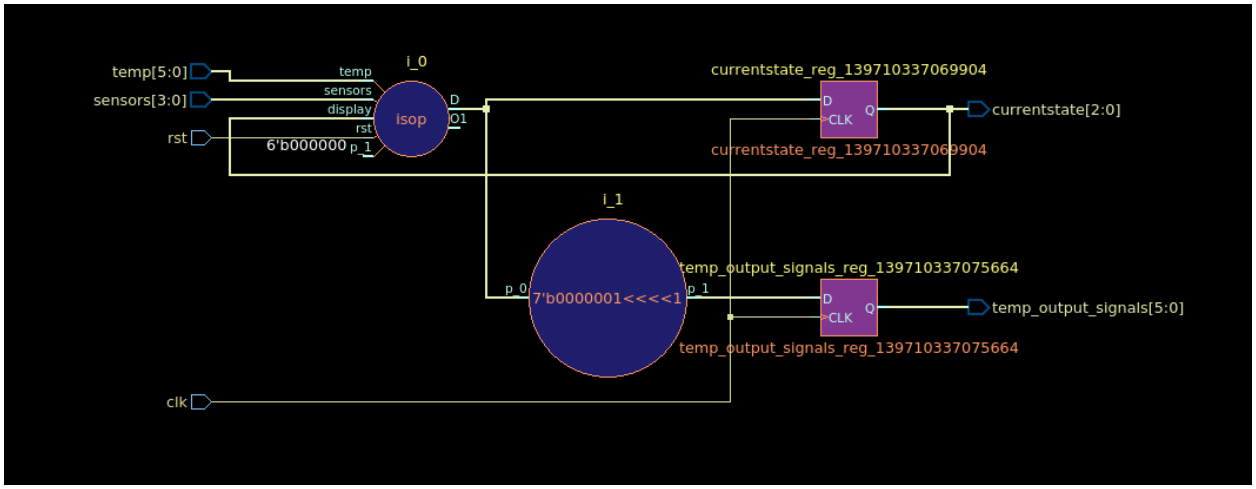


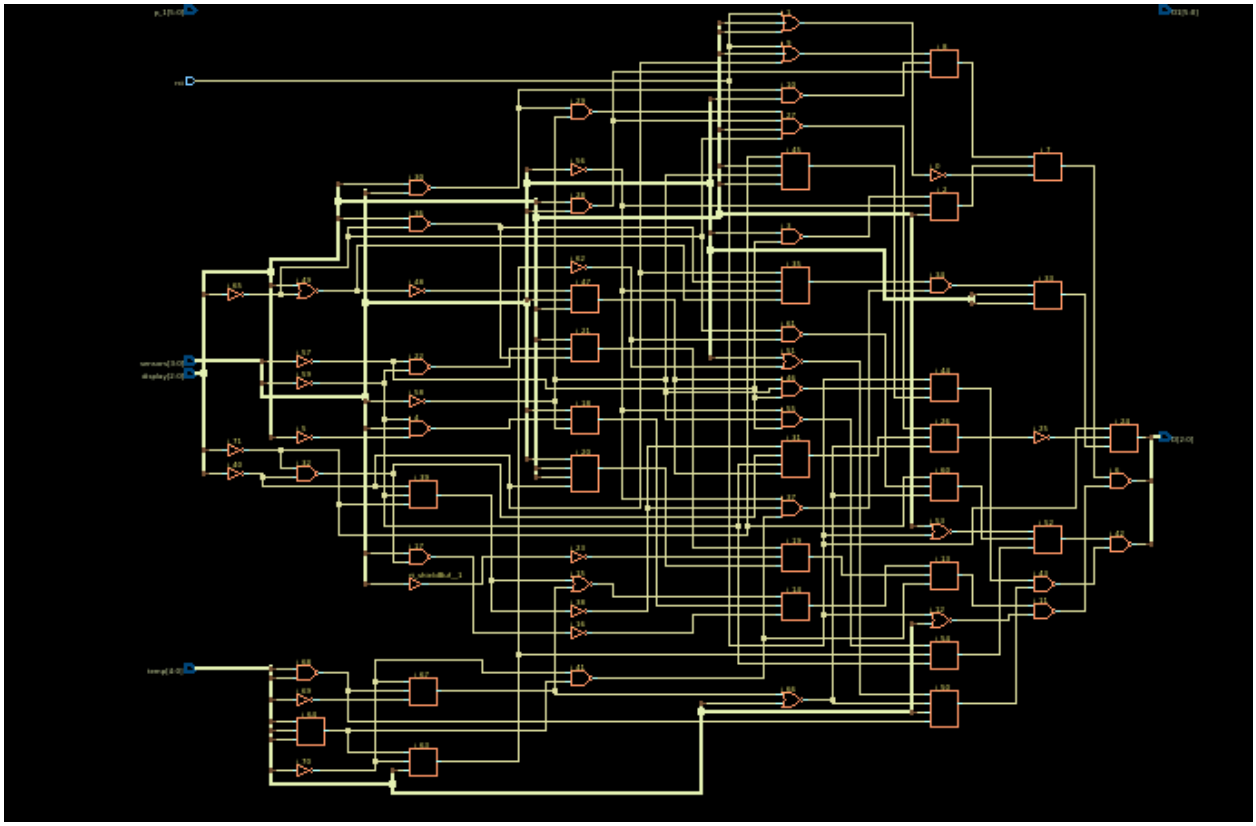


ii. Synthesis schematic


clk
rst
sensors[3:0]
temp[5:0]
i_0
clk
rst
sensors
temp
display
output_signals
display[2:0]
output_signals[5:0]
FSMHomeAutomation__genmod__0


always_139710337069824
clk
rst
sensors[3:0]
temp[4:0]
clk
rst
sensors
temp
always
temp_output_signals
currentstate
output_signals[5:0]
display[2:0]


temp[5:0]
sensors[3:0]
rst
i_0
temp
sensors
display
rst
6'b000000
isop
D
O1
p_1
currentstate_reg_139710337069904
D
CLK
Q
currentstate[2:0]
currentstate_reg_139710337069904
i_1
p_0
7'b0000001<<<<1
temp_output_signals_reg_139710337075664
p_1
D
CLK
Q
temp_output_signals[5:0]
temp_output_signals_reg_139710337075664
clk



iii. Reports (**design, path and power**.)

Design

Report Physical info:

		Area (squm)	Leakage (uW)
Design Name	FSMHomeAutomation		
Total Instances	95	117	2.566
Macros	0	0	0.000
Pads	0	0	0.000
Phys	0	0	0.000
Blackboxes	0	0	0.000
Cells	95	117	2.566
Buffers	1	1	0.021
Inverters	20	11	0.287
Clock-Gates	0	0	0.000
Combinational	65	63	1.402
Latches	0	0	0.000
FlipFlops	9	43	0.856
Single-Bit FF	9	43	0.856
Multi-Bit FF	0	0	0.000
Clock-Gated	0		
Bits	9	43	0.856
Load-Enabled	0		
Clock-Gated	0		
Tristate Pin Count	0		
Physical Info	Placed		
Chip Size (mm x mm)	0.074 x 0.074	5469	
Fixed Cell Area		0	
Phys Only	0	0	
Placeable Area		175	
Movable Cell Area		117	
Utilization (%)	66		
Chip Utilization (%)	66		
Total Wire Length (mm)	0.741		
Longest Wire (mm)	0.038		
Average Wire (mm)	0.037		

Path:

Report Path Groups:

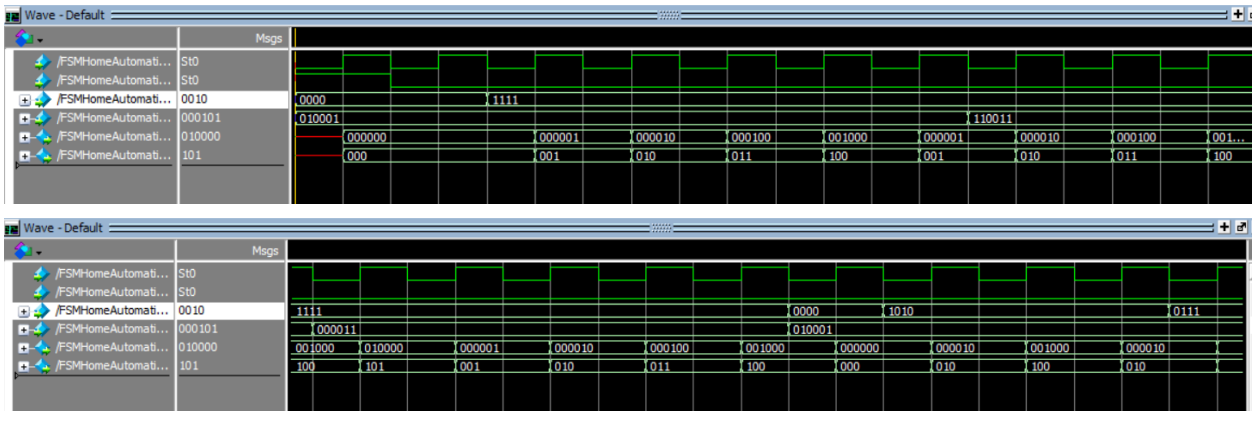
	Path Group	Weight	Critical Range(ps)	Worst Slack(ps)
1	default	1.000	0.0	527.7
2	I2R	1.000	0.0	2.0
3	I2O	1.000	0.0	<ill>
4	R2O	1.000	0.0	532.2

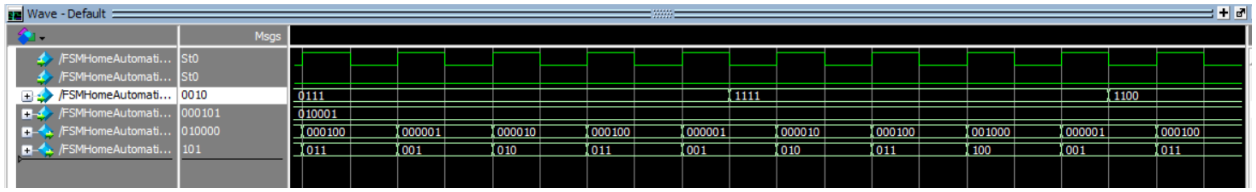
Power:

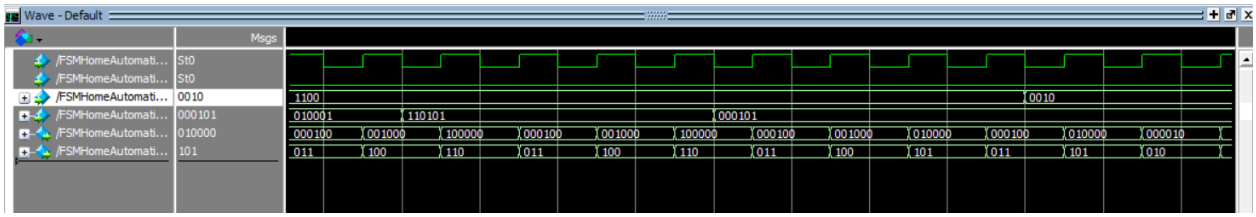
Report Power (instances with prefix '*' are included in total) :

	Instance	Internal Power(uw)	Switching Power(uw)	Leakage Power(uw)	Total Power(uw)
1	*currentstate_reg[2]	2.935725	19.337921	0.079112	22.352758
2	*currentstate_reg[1]	3.652205	16.202061	0.079112	19.933378
3	*currentstate_reg[0]	4.315013	11.734542	0.115104	16.164660
4	*i_0_0_0	0.378692	1.152881	0.014353	1.545925
5	*i_0_0_1	1.224394	6.211556	0.024415	7.460365
6	*i_0_0_2	0.857061	1.421797	0.022619	2.301477
7	*i_0_0_3	0.669239	1.043649	0.017393	1.730282
8	*i_0_0_4	0.636444	0.902992	0.018105	1.557541
9	*i_0_0_5	0.325187	1.049291	0.014353	1.388831
10	*rt_shieldBuf__1	1.590944	7.873654	0.021438	9.486036
.					
.					
.					
.					
81	*temp_output_signals_reg[2]	1.223820	0.784732	0.115104	2.123656
82	*temp_output_signals_reg[0]	2.569811	1.647801	0.115104	4.332716
83	*temp_output_signals_reg[1]	2.682796	2.819801	0.079112	5.581709
84					
85	*TOTAL	187.830688	260.153900	2.566280	450.550842

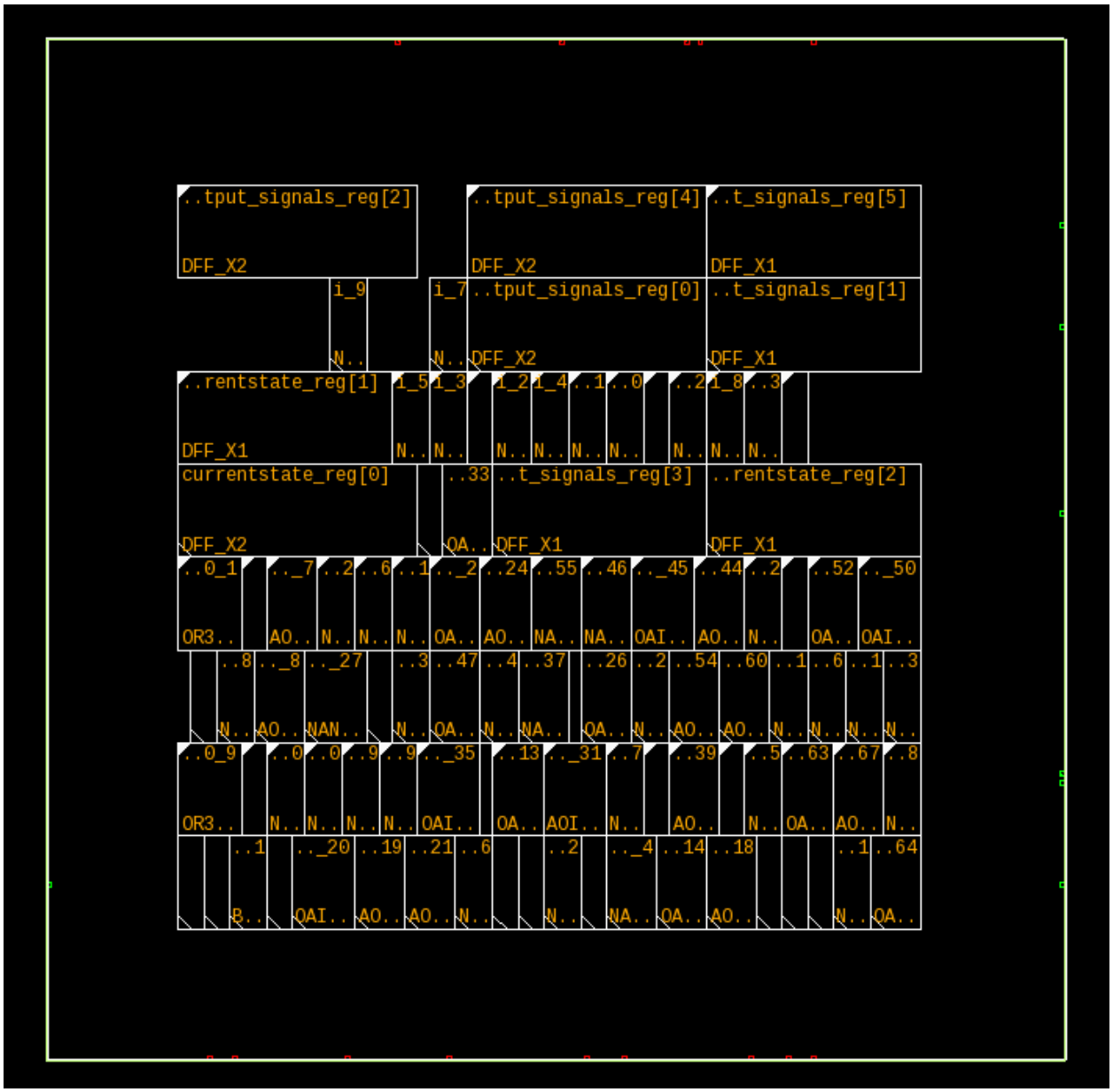
iv. Post-synthesis simulation

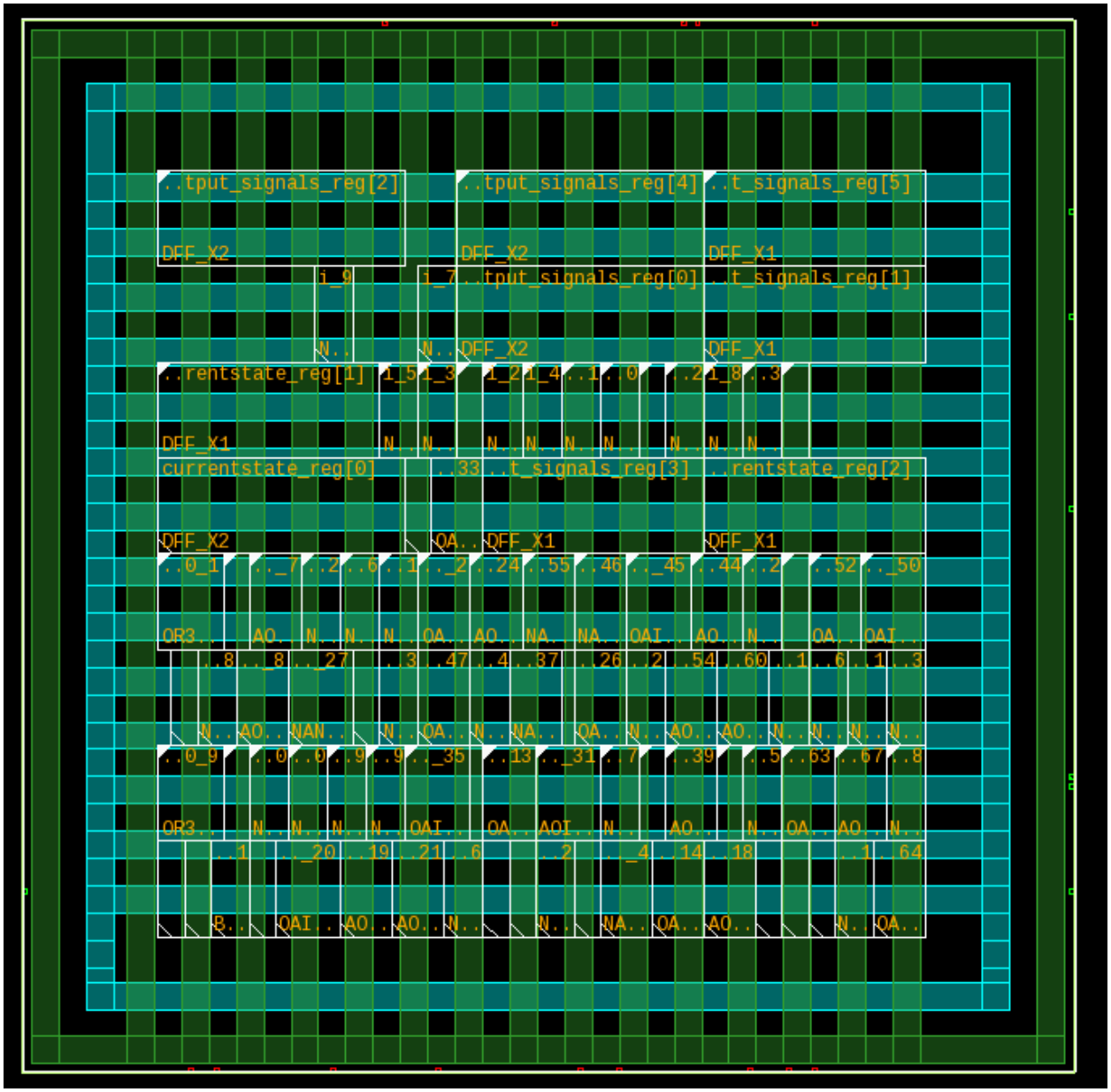


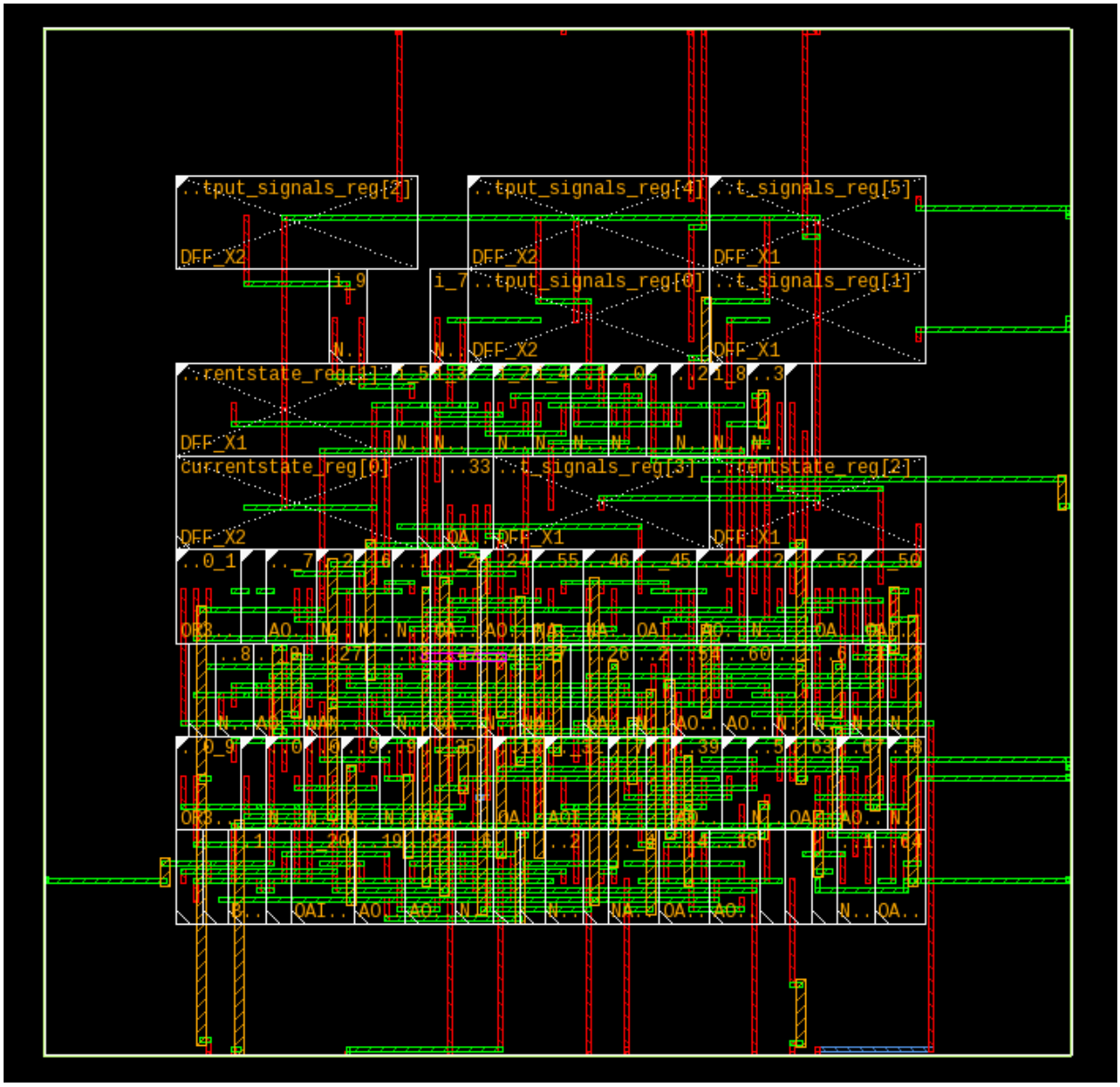




v. Floorplanning & Routing

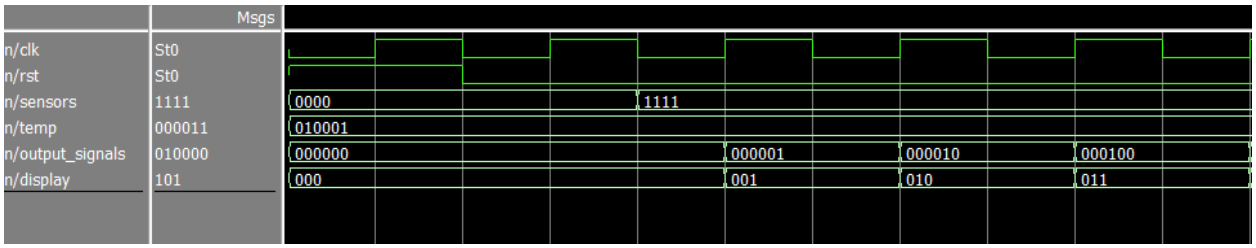


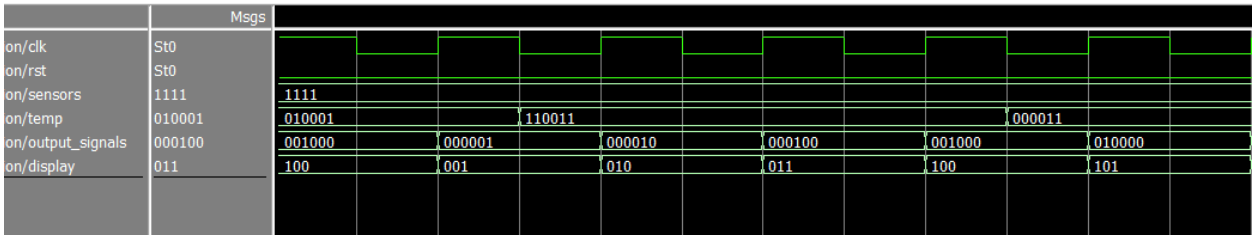

..tput_signals_reg[2]
..tput_signals_reg[4]
..t_signals_reg[5]
DFF_X2
DFF_X2
DFF_X1
i_9
i_7
..tput_signals_reg[0]
..t_signals_reg[1]
N..
N..
DFF_X2
DFF_X1
..rentstate_reg[1]
DFF_X1
currentstate_reg[0]
..t_signals_reg[3]
..rentstate_reg[2]
DFF_X2
DFF_X1
DFF_X1
OR3..
AO..
OA..
OAI..
N..
AO..
OA..
OAI..
N..
AO..
NAN..
OA..
OR3..
OAI..
OA..
AOI..
AO..
B..
QAI..
AO..
AO..
NA..
OA..
AO..

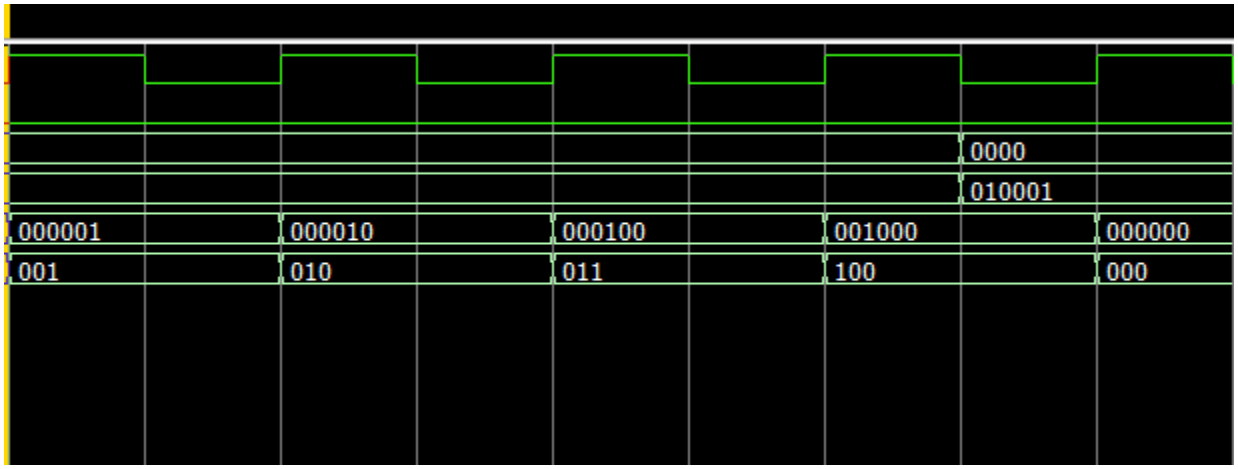


d. Design 4

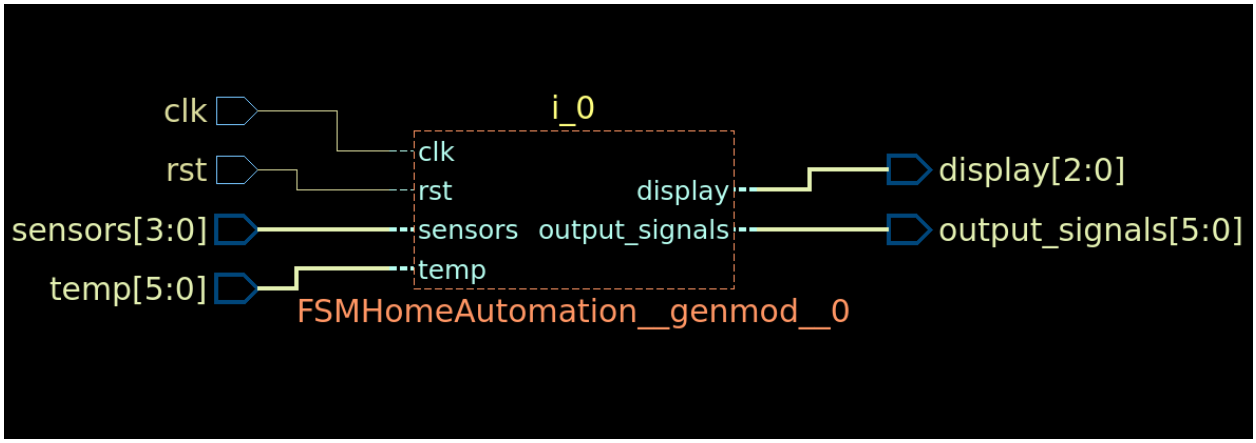
i. Pre-synthesis simulation

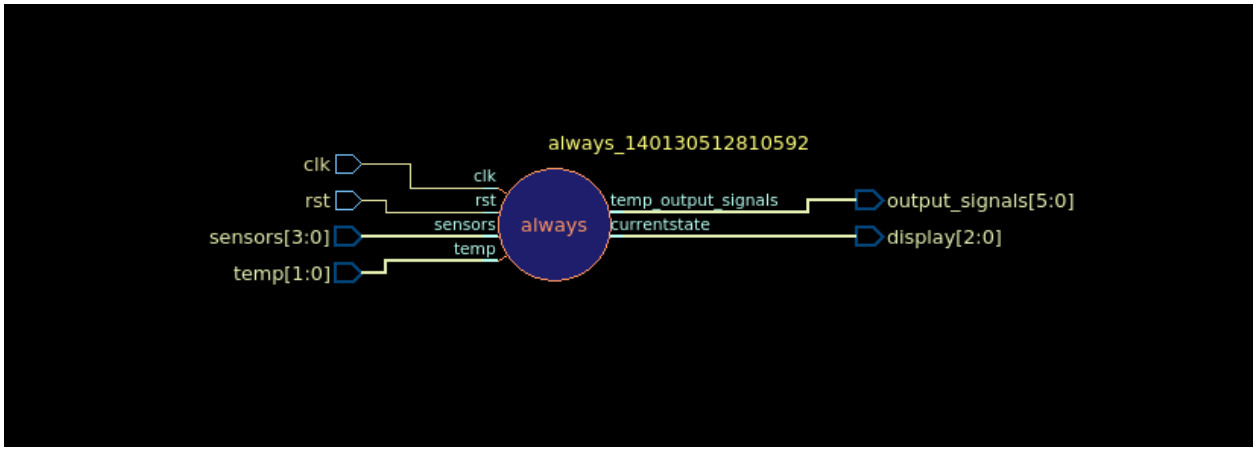


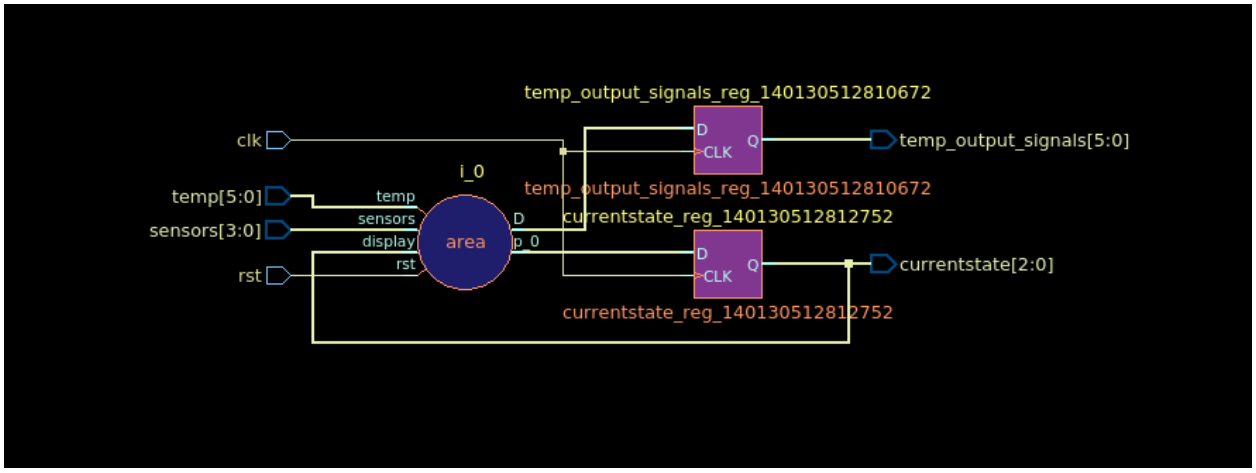


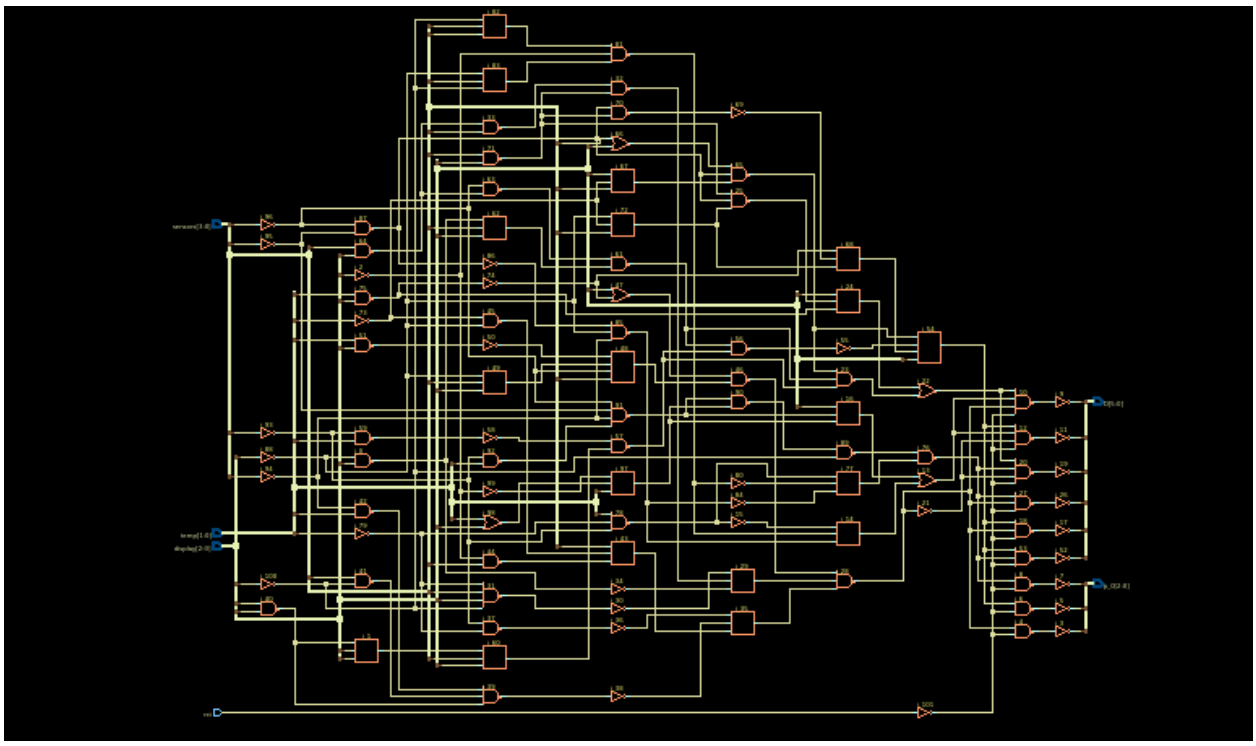


ii. Synthesis schematic









iii. Reports (**design, path and power**.)

Design:

Report Physical info:

		Area (squm)	Leakage (uW)
Design Name	FSMHomeAutomation		
Total Instances	111	124	2.560
Macros	0	0	0.000
Pads	0	0	0.000
Phys	0	0	0.000
Blackboxes	0	0	0.000
Cells	111	124	2.560
Buffers	0	0	0.000
Inverters	34	18	0.488
Clock-Gates	0	0	0.000
Combinational	68	65	1.360
Latches	0	0	0.000
FlipFlops	9	41	0.712
Single-Bit FF	9	41	0.712
Multi-Bit FF	0	0	0.000
Clock-Gated	0		
Bits	9	41	0.712
Load-Enabled	0		
Clock-Gated	0		
Tristate Pin Count	0		
Physical Info	Placed		
Chip Size (mm x mm)	0.074 x 0.074	5533	
Fixed Cell Area		0	
Phys Only	0	0	
Placeable Area		199	
Movable Cell Area		124	
Utilization (%)	62		
Chip Utilization (%)	62		
Total Wire Length (mm)	0.638		
Longest Wire (mm)	0.038		
Average Wire (mm)	0.038		

Path:

Report Path Groups:

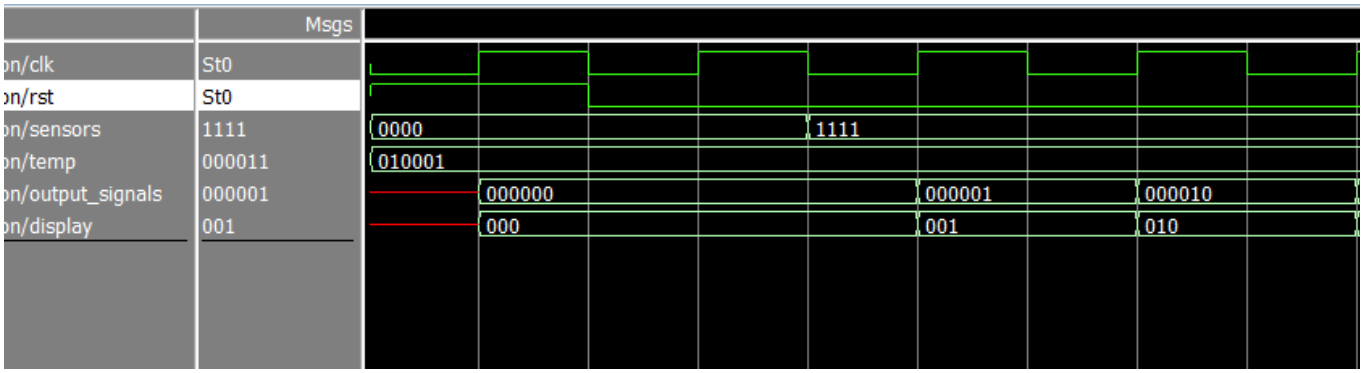
	Path Group	Weight	Critical Range(ps)	Worst Slack(ps)
1	default	1.000	0.0	575.1
2	I2R	1.000	0.0	28.3
3	I2O	1.000	0.0	<ill>
4	R2O	1.000	0.0	534.5

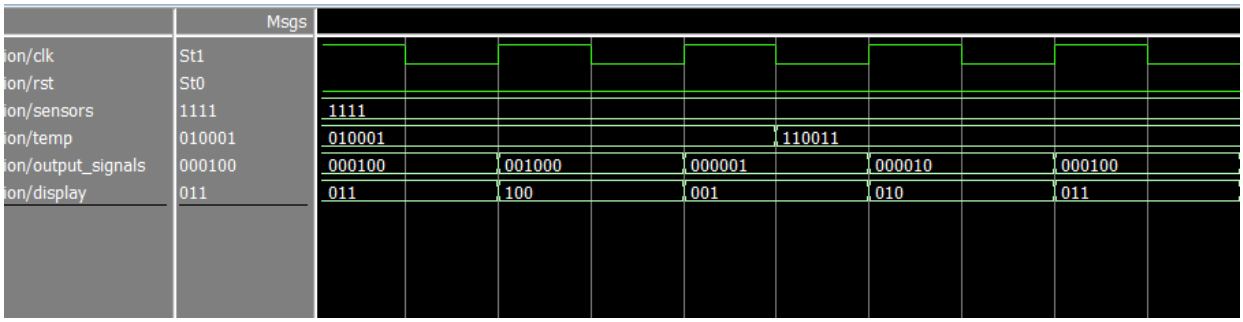
Power:

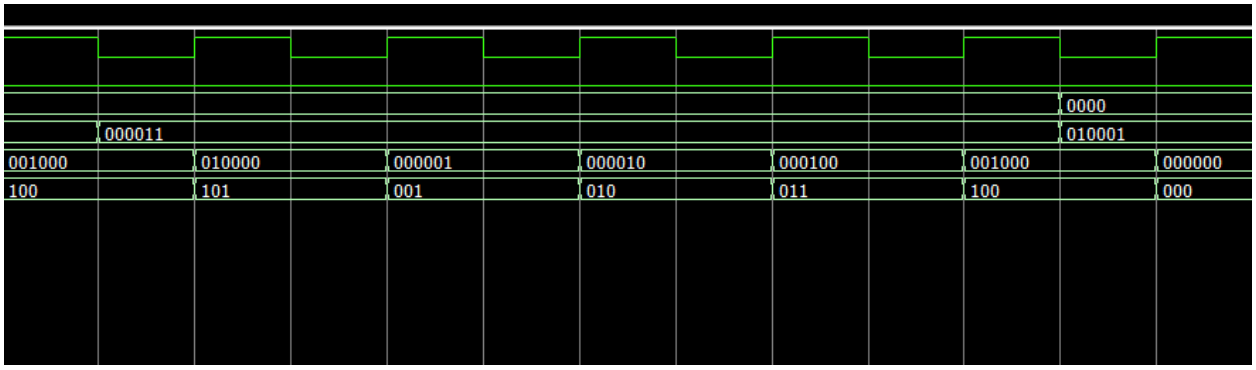
Report Power (instances with prefix '*' are included in total) :

	Instance	Internal Power(uw)	Switching Power(uw)	Leakage Power(uw)	Total Power(uw)
1	*temp_output_signals_reg[5]	1.453432	1.533949	0.079112	3.066494
2	*temp_output_signals_reg[4]	1.200631	1.264599	0.079112	2.544343
3	*temp_output_signals_reg[3]	0.821929	0.866240	0.079112	1.767281
4	*temp_output_signals_reg[2]	1.653739	1.740654	0.079112	3.473505
5	*temp_output_signals_reg[1]	1.477865	1.556470	0.079112	3.113447
6	*temp_output_signals_reg[0]	1.028753	1.083888	0.079112	2.191753
7	*currentstate_reg[2]	2.539055	14.867807	0.079112	17.485973
8	*currentstate_reg[1]	3.281270	18.098841	0.079112	21.459223
9	*currentstate_reg[0]	2.834105	11.082655	0.079112	13.995872
.					
.					
.					
.					
104	*i_0_0_94	9.177187	4.233553	0.014353	13.425093
105	*i_0_0_95	9.412773	2.740402	0.014353	12.167528
106	*i_0_0_96	9.003258	5.534140	0.014353	14.551751
107	*i_0_0_97	3.668983	2.612561	0.022619	6.304163
108	*i_0_0_98	3.607303	1.351678	0.021200	4.980182
109	*i_0_0_99	0.279927	0.823057	0.014353	1.117337
110	*i_0_0_100	0.364343	5.371625	0.014353	5.750321
111	*i_0_0_101	0.482598	12.944932	0.014353	13.441883
112					
113	*TOTAL	281.314941	305.811493	2.560085	589.686462

iv. Post-synthesis simulation

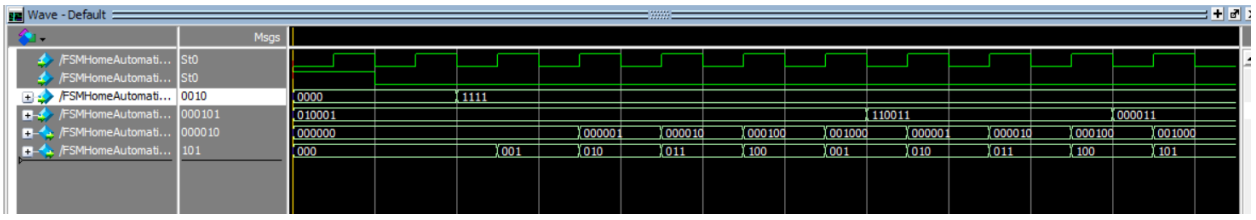


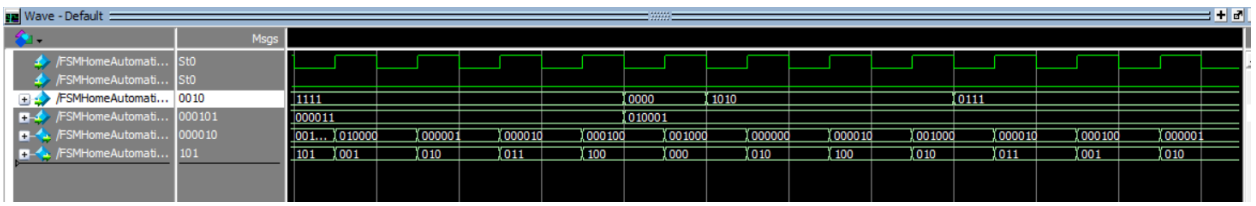


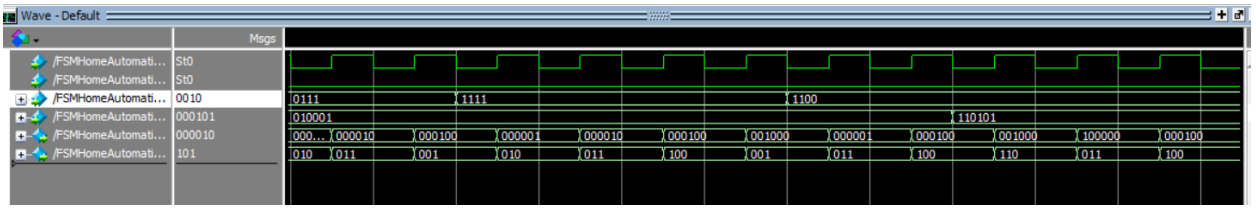


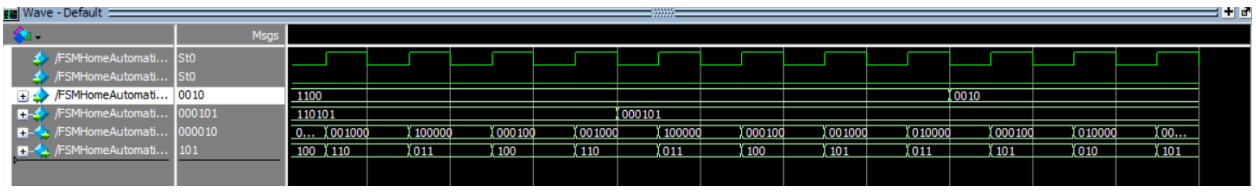
e. Design 5

i. Pre-synthesis simulation

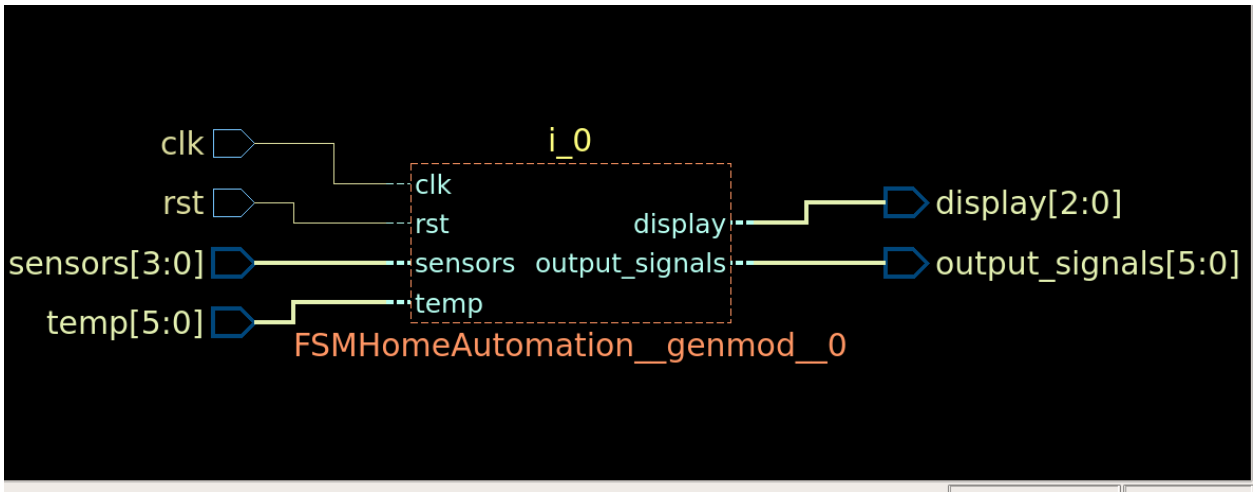


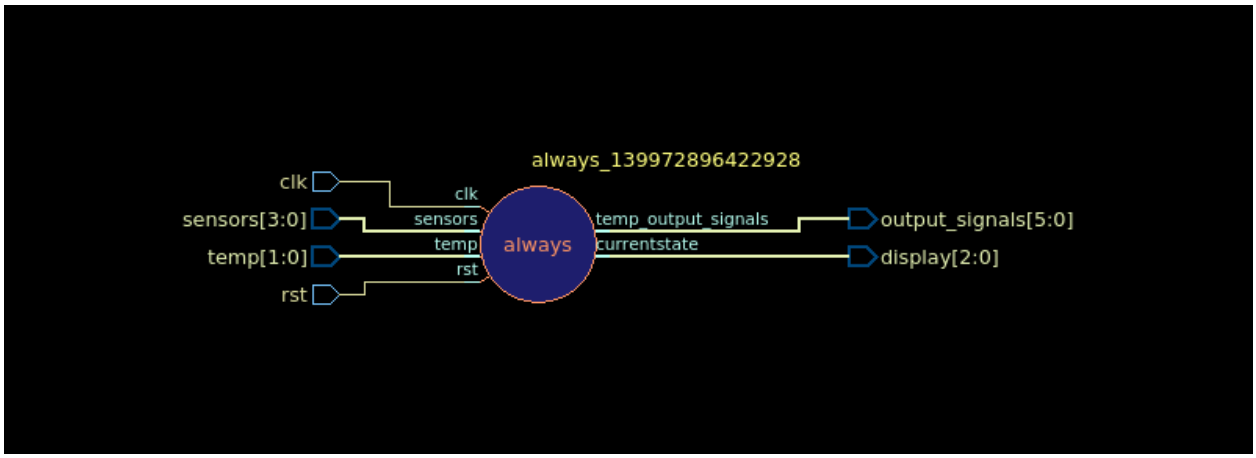


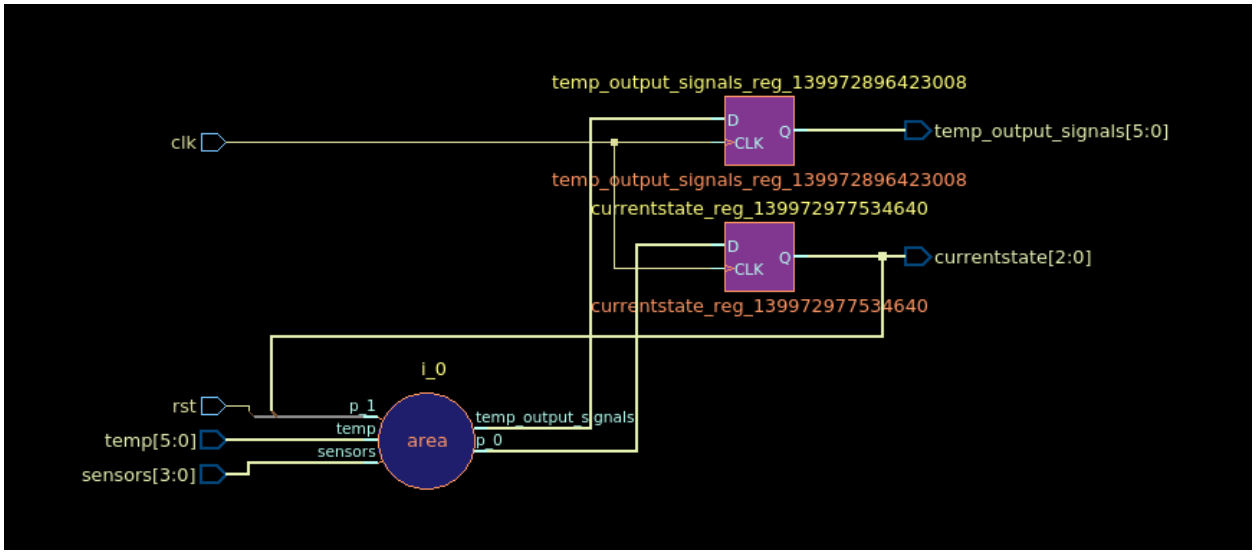


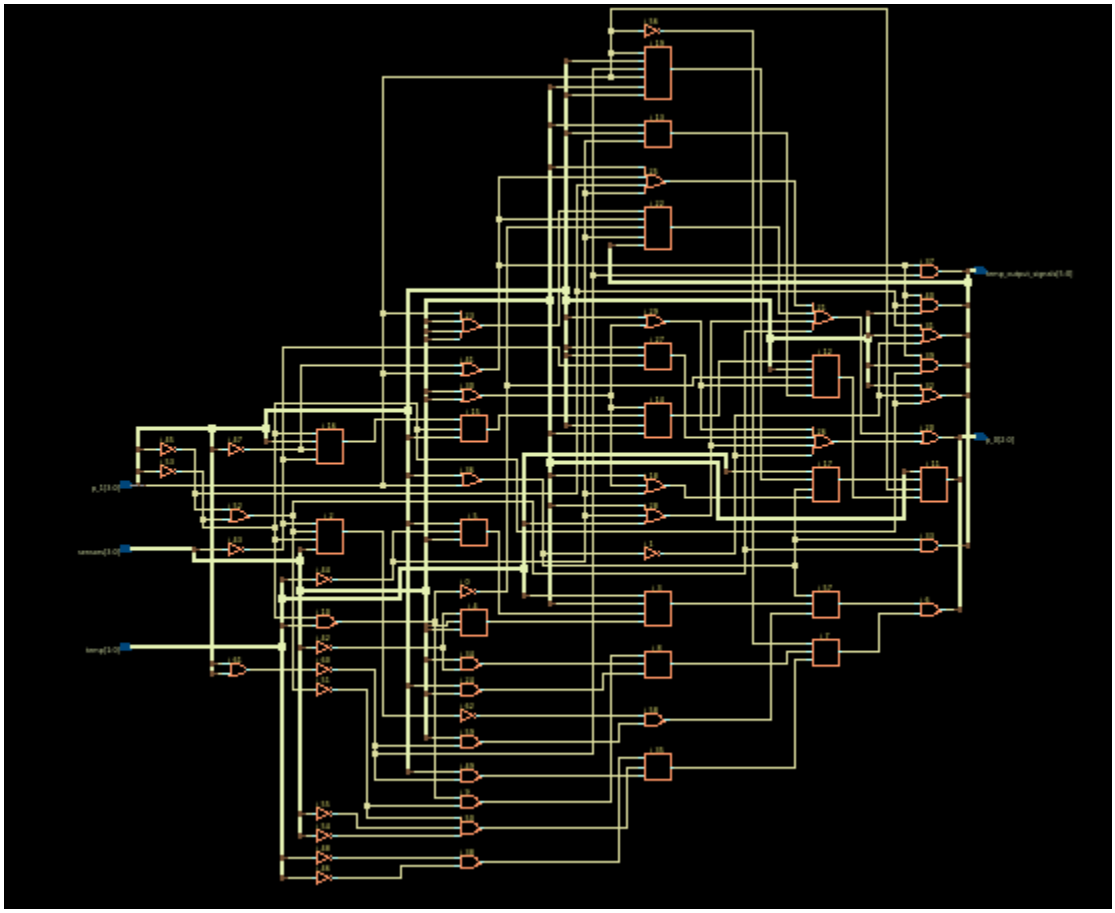


ii. Synthesis schematic


clk
rst
sensors[3:0]
temp[5:0]
i_0
clk
rst
sensors
temp
display
output_signals
display[2:0]
output_signals[5:0]
FSMHomeAutomation__genmod__0


always_139972896422928
clk
sensors[3:0]
temp[1:0]
rst
clk
sensors
temp
rst
always
temp_output_signals
currentstate
output_signals[5:0]
display[2:0]





iii. Reports (**design, path and power**.)

Design:

design.rpt - Notepad

File Edit Format View Help

Report Physical info:

		Area (squm)	Leakage (uW)
Design Name	FSMHomeAutomation		
Total Instances	72	101	2.175
Macros	0	0	0.000
Pads	0	0	0.000
Phys	0	0	0.000
Blackboxes	0	0	0.000
Cells	72	101	2.175
Buffers	0	0	0.000
Inverters	16	9	0.230
Clock-Gates	0	0	0.000
Combinational	47	51	1.233
Latches	0	0	0.000
FlipFlops	9	41	0.712
Single-Bit FF	9	41	0.712
Multi-Bit FF	0	0	0.000
Clock-Gated	0		
Bits	9	41	0.712
Load-Enabled	0		
Clock-Gated	0		
Tristate Pin Count	0		
Physical Info	Placed		
Chip Size (mm x mm)	0.073 x 0.073	5321	
Fixed Cell Area		0	
Phys Only	0	0	
Placeable Area		163	
Movable Cell Area		101	
Utilization (%)	61		
Chip Utilization (%)	61		
Total Wire Length (mm)	0.626		
Longest Wire (mm)	0.037		
Average Wire (mm)	0.037		

Path:

path.rpt - Notepad

File Edit Format View Help

```
Report Path Groups:
-----+-------+------+---------+---------
     | Path  |Weight|Critical |Worst
     | Group |      |Range(ps)|Slack(ps)
-----+-------+------+---------+---------
1    |default| 1.000|      0.0|    564.6
2    |I2R    | 1.000|      0.0|     40.0
3    |I2O    | 1.000|      0.0|<ill>
4    |R2O    | 1.000|      0.0|    538.2
-----+-------+------+---------+---------
```

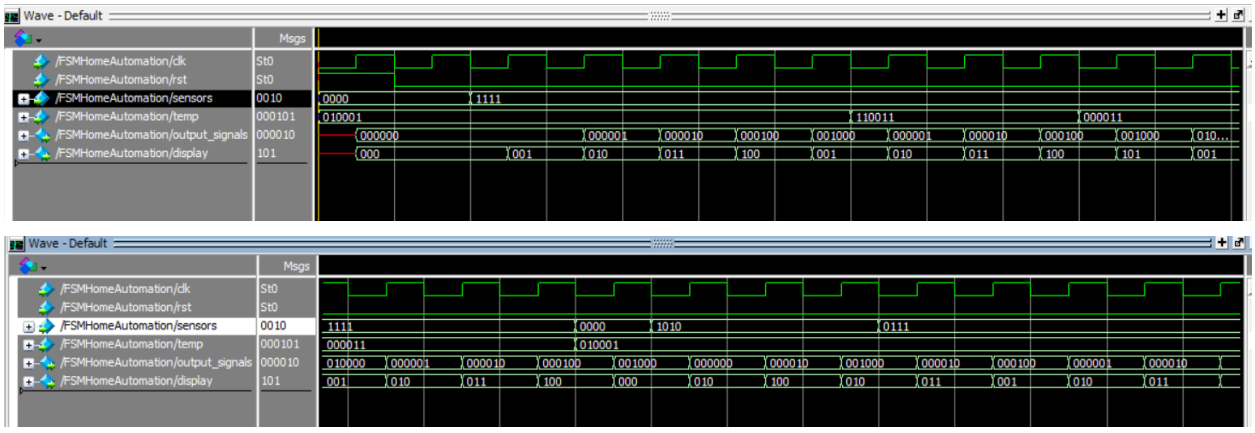
Power:

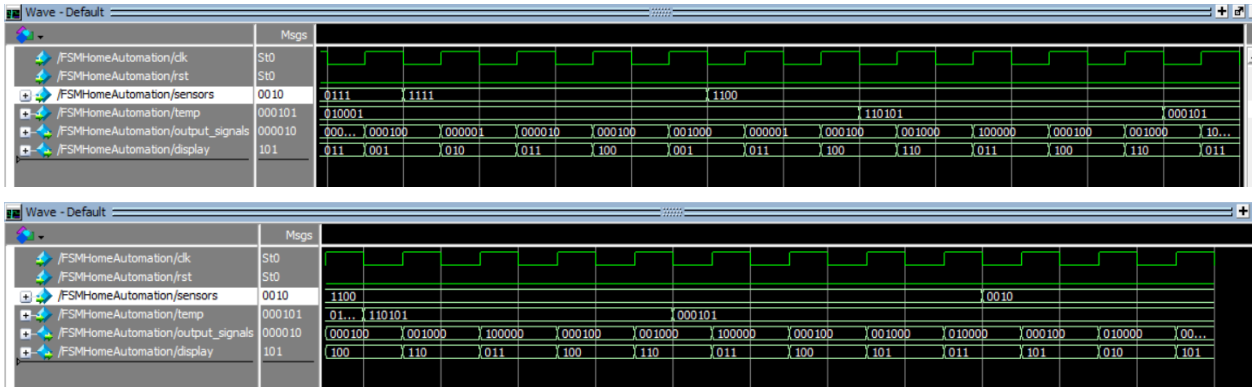
power.rpt - Notepad

File Edit Format View Help

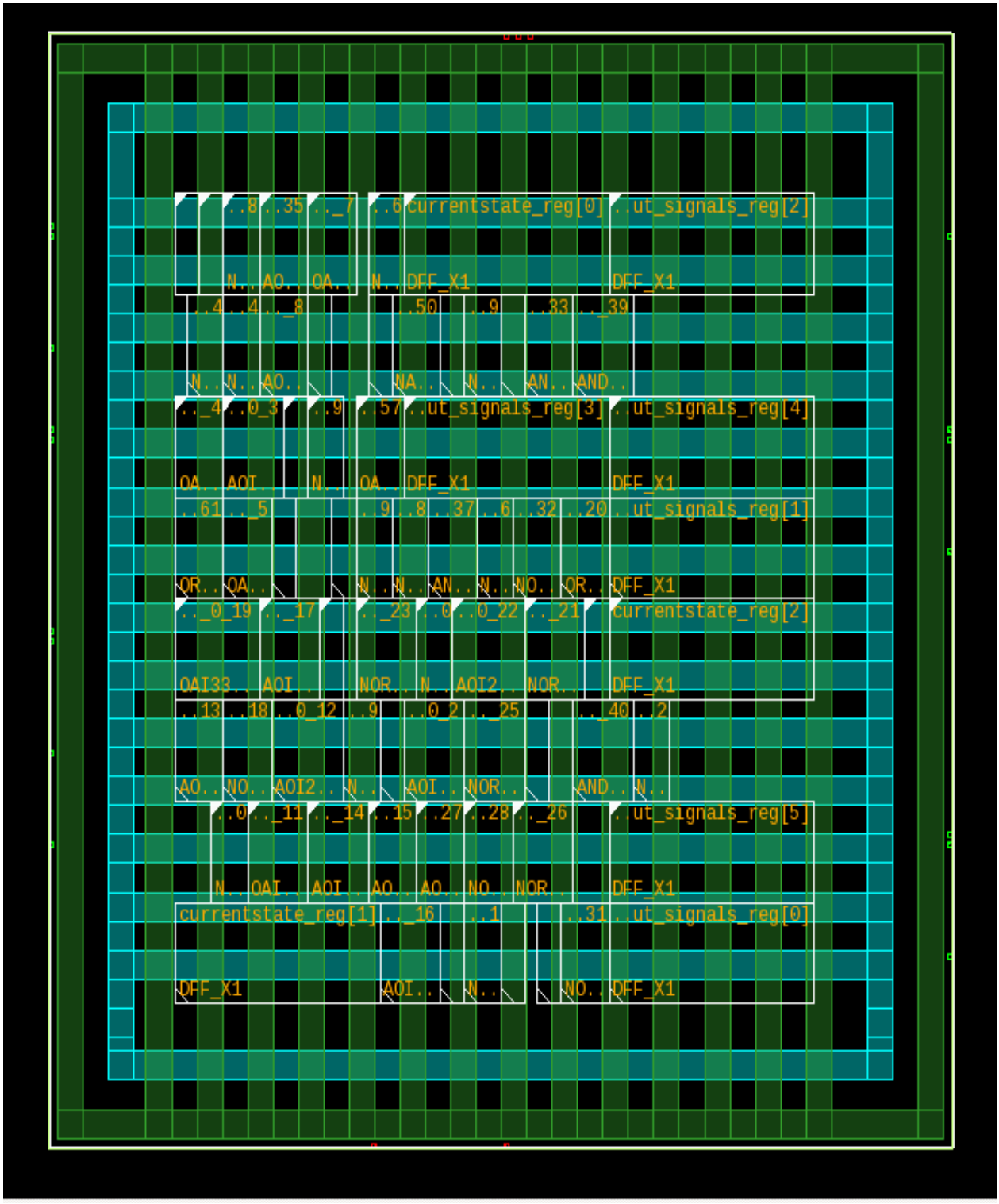
36	*i_0_0_36	0.626975	11.166432	0.021200	11.814606
37	*i_0_0_37	0.231364	0.273740	0.025066	0.530169
38	*i_0_0_39	0.231319	0.097258	0.026481	0.355058
39	*i_0_0_40	0.182462	0.076546	0.026481	0.285490
40	*i_0_0_41	0.206627	1.525657	0.021200	1.753483
41	*i_0_0_42	0.941058	2.714055	0.014353	3.669466
42	*i_0_0_43	9.303542	3.432711	0.014353	12.750606
43	*i_0_0_44	0.696646	8.252778	0.014353	8.963777
44	*i_0_0_45	0.355801	3.835073	0.014353	4.205227
45	*i_0_0_47	0.263637	1.327079	0.014353	1.605069
46	*i_0_0_0	3.305162	1.782153	0.014353	5.101668
47	*i_0_0_1	0.462138	4.044818	0.014353	4.521309
48	*i_0_0_6	1.088194	0.446162	0.017393	1.551750
49	*i_0_0_7	0.332493	0.547767	0.022619	0.902879
50	*i_0_0_8	0.487438	0.830163	0.027858	1.345459
51	*i_0_0_9	0.609346	1.326484	0.017393	1.953223
52	*i_0_0_10	3.291689	8.472428	0.017393	11.781511
53	*i_0_0_24	0.296416	0.448422	0.017393	0.762231
54	*i_0_0_34	0.669221	1.064466	0.017393	1.751080
55	*i_0_0_35	0.168313	0.301405	0.027858	0.497576
56	*i_0_0_38	0.514620	1.032332	0.017393	1.564345
57	*i_0_0_46	1.036302	1.363718	0.014353	2.414373
58	*i_0_0_48	1.039903	1.316520	0.014353	2.370776
59	*i_0_0_49	0.104344	0.234374	0.017393	0.356112
60	*i_0_0_50	0.620612	1.026815	0.018105	1.665531
61	*i_0_0_51	0.123509	0.754298	0.014353	0.892160
62	*i_0_0_52	0.183991	2.921178	0.021200	3.126368
63	*i_0_0_53	0.382244	6.816661	0.014353	7.213258
64	*i_0_0_54	1.026915	1.486756	0.014353	2.528024
65	*i_0_0_55	1.034922	1.381805	0.014353	2.431080
66	*i_0_0_56	0.495241	1.385444	0.014353	1.895038
67	*i_0_0_57	2.510361	0.842990	0.022619	3.375971
68	*i_0_0_58	2.544704	1.421934	0.017393	3.984032
69	*i_0_0_59	0.737665	1.081135	0.017393	1.836193
70	*i_0_0_60	0.475430	4.265195	0.014353	4.754978
71	*i_0_0_61	1.358432	7.819768	0.022695	9.200895
72	*i_0_0_62	3.063365	1.100851	0.014353	4.178569
73					
74	*TOTAL	95.217430	164.926651	2.174988	262.319092

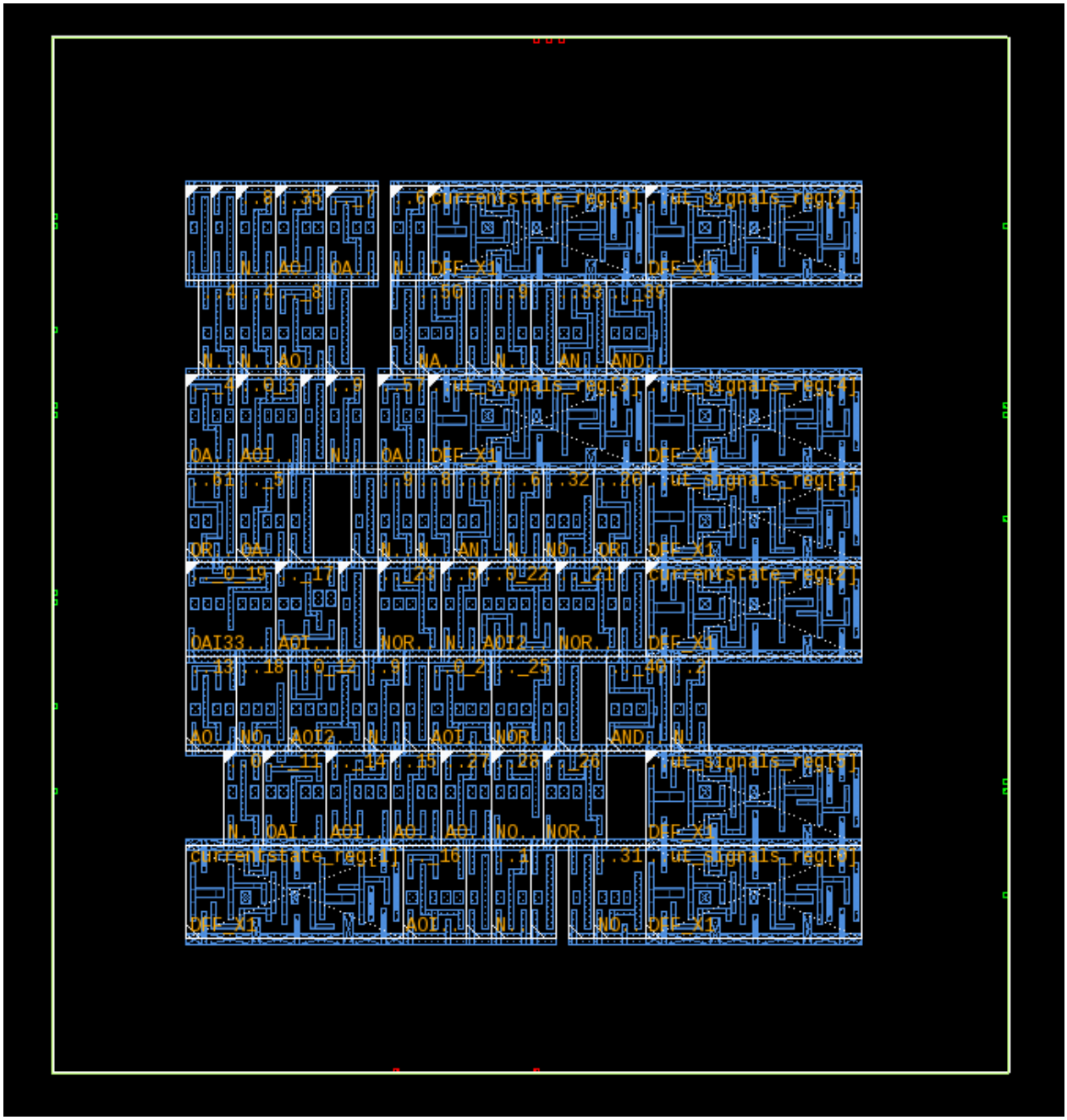
iv. Post-synthesis simulation

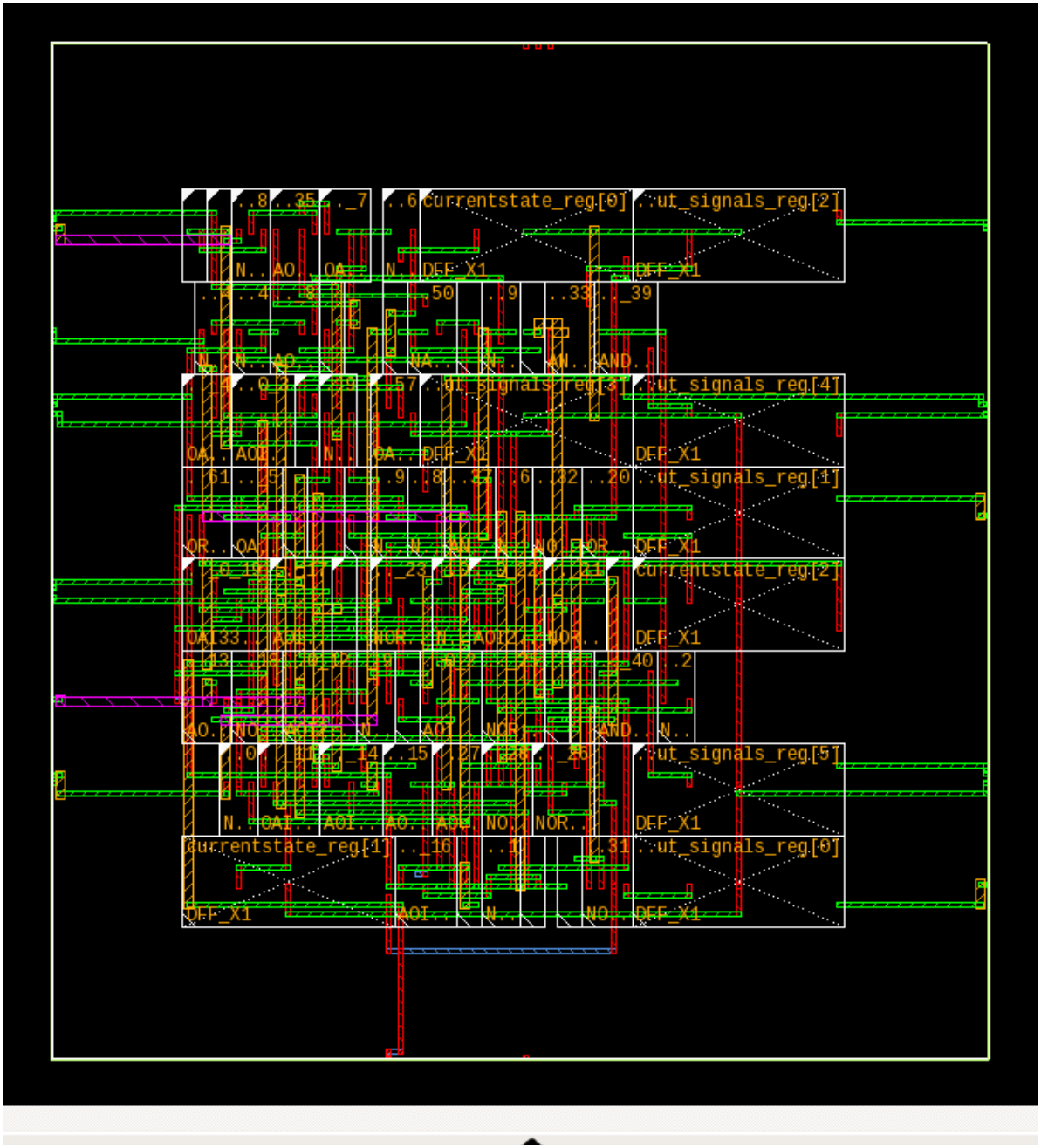




v. Floorplanning & Routing


..8..35..._7 ..6 currentstate_reg[0] ..ut_signals_reg[2]
N.. AO.. OA.. N.. DFF_X1 DFF_X1
..4..4..._8 .50 ..9 ..33 ..39
N.. N.. AO.. NA.. N.. AN.. AND..
..._4..0_3 ..9 ..57 ..ut_signals_reg[3] ..ut_signals_reg[4]
OA.. AOI.. N.. OA.. DFF_X1 DFF_X1
..61..._5 ..9 ..8 ..37 ..6 ..32 ..20 ..ut_signals_reg[1]
OR.. OA.. N.. N.. AN.. N.. NO.. OR.. DFF_X1
..._0_19 ..._17 ..._23 ..0 ..0_22 ..._21 currentstate_reg[2]
OAI33.. AOI.. NOR.. N.. AOI2.. NOR.. DFF_X1
..13..18..0_12 ..9 ..0_2 ..._25 ..._40 ..2
AO.. NO.. AOI2.. N.. AOI.. NOR.. AND.. N..
..0..._11 ..._14 ..15 ..27 ..28 ..._26 ..ut_signals_reg[5]
N.. OAI.. AOI.. AO.. AO.. NO.. NOR.. DFF_X1
currentstate_reg[1]..._16 ..1 ..31 ..ut_signals_reg[0]
DFF_X1 AOI.. N.. NO.. DFF_X1





3. Comparison and justification why did you choose this design

Design	Design 1	Design 2	Design 3	Design 4	Design 5
Area	1178	164	117	124	101
Worst slack	25.6	0.1	2.0	28.3	40.0
Clock	1500	1000	1000	1000	1000
Power	3698	714	450	589	262

Equation result	1771	524	448	471	391

Although all the designs that are stated above are derivatives from the initial two designs we can see the results of several optimizations done on those two in the table above until reaching the final form of those two designs. But due in order to achieve the best possible result under the constraints (equation) that is bestowed upon us we choose the final design to be number 5 simply because it achieved the best possible outcomes.

4. The **score** obtained for your chosen design using the following equation:
   0.5*Movable Cell Area in squm+0.3*(clock period in ps-worst case slack in ps)+0.2*total power in uw

   Score = 0.5 * 101 + 0.3 * (1000 - 40.0) + 0.2 * 262 = 391