Laboratory Exercise 4

Flip-Flops, Counters and Shift Registers

Part I

The objective of this task is to write a system Verilog code and test bench, for a memory element JK Flip-Flop in Vivado. Students will learn how to model sequential circuits, understand the behavior of a JK Flip-Flop, and verify its functionality through simulation.

Theory:
A JK Flip-Flop is a sequential circuit with two inputs, J (set) and K (reset), along with a clock (CLK) and an asynchronous reset (RST). The functionality is defined as follows:

- If J = 0 and K = 0, the output remains unchanged (no change state).
- If J = 0 and K = 1, the output is reset to 0.
- If J = 1 and K = 0, the output is set to 1.
- If J = 1 and K = 1, the output toggles.

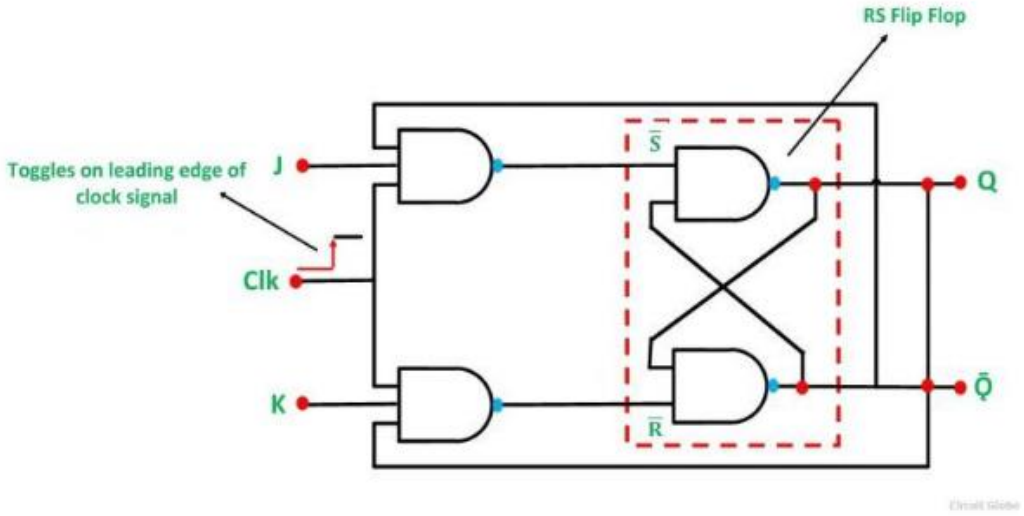

Figure 1: JK Flip Flop circuit.

Part II

The objective of this lab is to design, implement, and simulate a 4-bit synchronous up counter using Verilog in Xilinx Vivado. Students will understand the working principle of synchronous counters, write Verilog code, and verify the functionality through simulation.

Theory:
A **synchronous up counter** is a sequential circuit where all flip-flops are triggered simultaneously by a common clock signal. A 4-bit up counter counts from 0 (0000) to 15 (1111) and then resets back to 0. The next state depends on the current state, with each clock pulse incrementing the count.

The counter consists of four **D flip-flops** connected in such a way that their outputs increment in binary sequence upon each clock pulse. The design includes:

- A **clock input** to drive the counter.
- A **reset signal** to initialize the counter.
- Four **output bits (QA, QB, QC, QD)** representing the binary count.

Lab Tasks:

1. Write a Verilog module for a 4-bit synchronous up counter.
2. Simulate the design in Vivado using a test bench.
3. Verify the waveform results to ensure correct operation

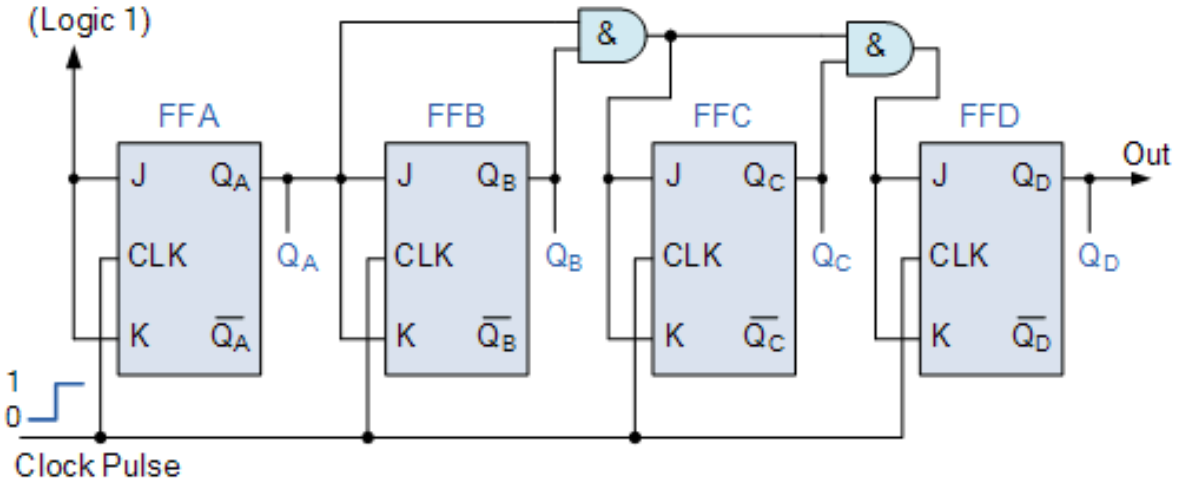

Figure 2: 4 Bit Synchronous Up Counter

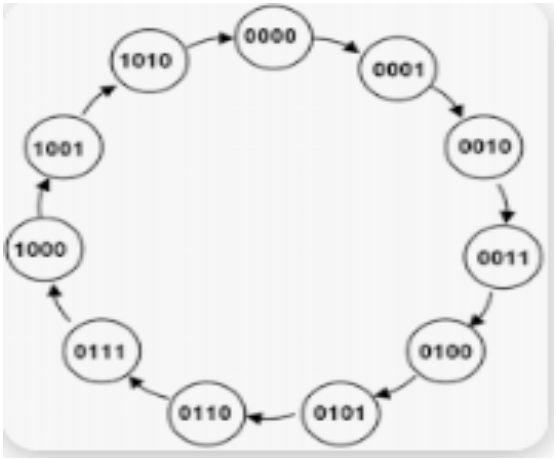

Figure 3: State Diagram of 4 Bit Synchronous Up counter

Part III

The objective of this lab task is to design, implement, and simulate a 4-bit asynchronous down counter using Verilog in Xilinx Vivado. Students will understand the working principle of asynchronous counters, write Verilog code, and verify the functionality through simulation.

Theory:
An **asynchronous down counter** is a sequential circuit where the flip-flops are triggered by different clock signals. A 4-bit down counter counts from 15 (1111) to 0 (0000) and then resets back to 15. Each flip-flop's clock input is driven by the previous stage's output, creating an asynchronous behavior.

The counter consists of four **JK flip-flops** connected in such a way that their outputs decrement in binary sequence upon each clock pulse. The design includes:

- A **clock input** to drive the counter.
- A **reset signal** to initialize the counter.
- Four **output bits (QA, QB, QC, QD)** representing the binary count.

Lab Tasks:

1. Write a Verilog module for a 4-bit asynchronous down counter.
2. Simulate the design in Vivado using a test bench.
3. Verify the waveform results to ensure correct operation.

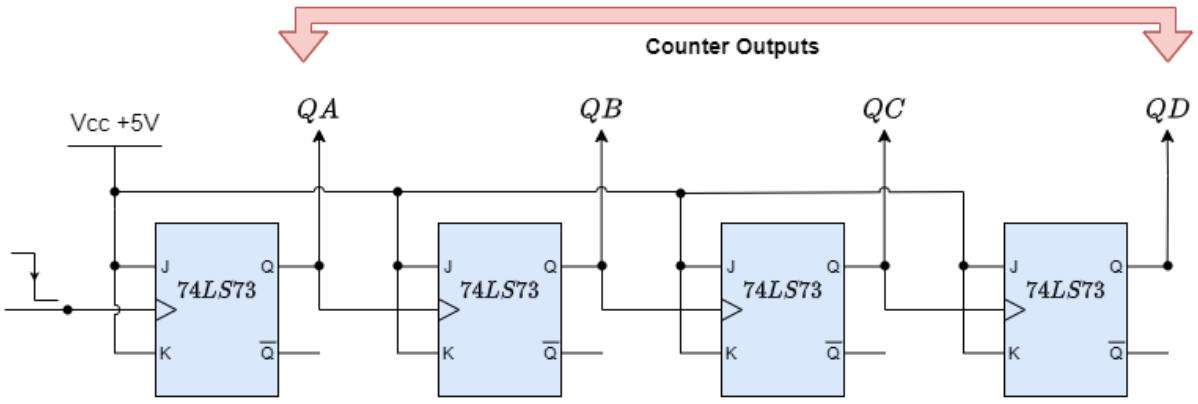

Figure 4: 4 Bit Asynchronous down counter

Part III

Objective:
The objective of this task is to design, implement, and simulate a 4-bit Serial-In Parallel-Out (SIPO) shift register using Verilog in Xilinx Vivado. Students will understand the working principle of shift registers, write Verilog code, and verify the functionality through simulation.

Theory:
A **Serial-In Parallel-Out (SIPO) shift register** is a sequential circuit that accepts serial data one bit at a time and outputs all bits in parallel after a specified number of clock pulses. It is commonly used in data conversion and communication systems. A 4-bit SIPO register consists of four D flip-flops connected in series, where each flip-flop shifts its stored bit to the next stage on the rising edge of the clock. The shift register consists of:

- A **clock input** to drive the shift register.
- A **serial data input** to receive data sequentially.
- A **reset signal** to initialize the register.
- Four **parallel output bits (QA, QB, QC, QD)** representing the stored data.

Lab Tasks:

1. Write a Verilog module for a 4-bit Serial-In Parallel-Out shift register.
2. Simulate the design in Vivado using a test bench.
3. Verify the waveform results to ensure correct operation.

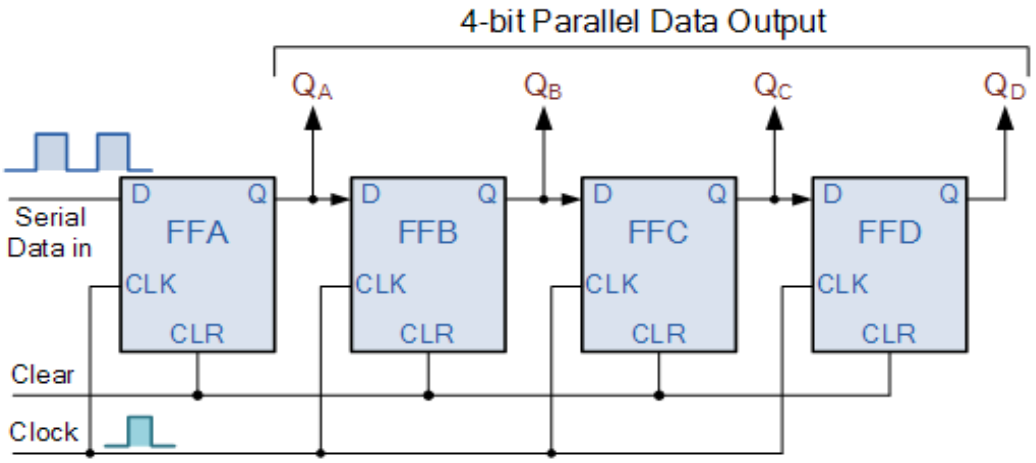

Figure 4: 4 Bit Asynchronous down counter

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Clock Pulse No	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	0	0	0	0