Group No:

Experiment-06

Study of I-V Characteristics of MOSFET, BJT and Implementation of Logic Functions Using LTspice Software

CSE251 - Electronic Devices and Circuits Lab

Objective

1. To implement a NAND gate and a Logic Function using MOSFETs and BJTs and verify the truth tables.
2. To observe and understand the I-V characteristics of MOSFET and BJT.

Background Theory

Introduction to MOSFET

Three-terminal devices are far more useful than two-terminal ones (such as Diodes) because they can be used in a multitude of applications, ranging from signal amplification to digital logic and memory. The basic principle involved is the use of the voltage between two terminals to control the current flowing in the third terminal. In this way a three-terminal device can be used to realize a controlled source.

The control signal can be used to cause the current in the third terminal to change from zero to a large value, thus allowing the device to act as a switch. Switch is the basis for the realization of the logic inverter, which is a basic element of digital circuits.

There are two major types of three-terminal semiconductor devices: (i) MOSFET (Metal-Oxide Semiconductor Field-Effect Transistor) and (ii) BJT (Bipolar Junction Transistor). Although both of them offer unique features and areas of application, MOSFET has become by far the most widely used electronic device, especially in the design of integrated circuits (ICs).

There are two kinds of MOSFET: (i) NMOS and (ii) PMOS. In this experiment, we will study about the I-V characteristics of NMOS and design an NAND gate and a Boolean Logic Function using the NMOS transistor. The figure above shows the IC and the circuit diagram of a MOSFET (NMOS).

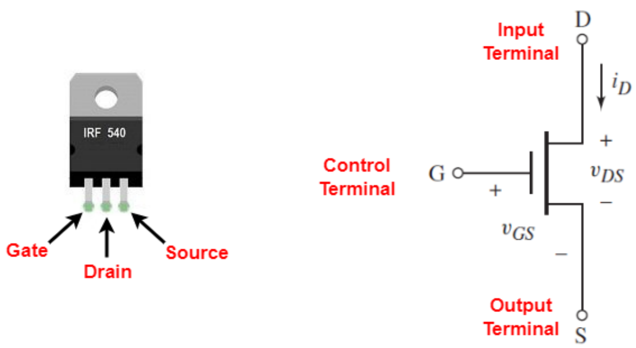


Figure 1: ***NMOS IC and Circuit Diagram***

MOSFET as a Switch

MOSFET is a three-terminal device with a control terminal, an input terminal, and an output terminal. The control terminal of the MOSFET is called its gate G, the input terminal its drain D, and the output terminal its source S. MOSFET can act as a switch depending upon the applied voltage in the input terminal. A simple circuit model known as 'Switch Model' or 'S-Model' is used to model this behavior.

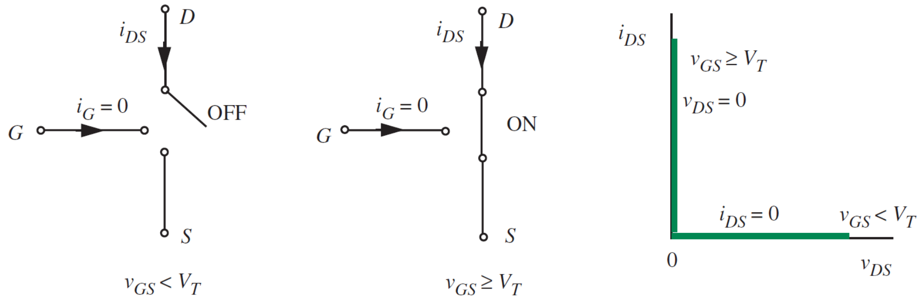


Figure 2: ***S-Model of MOSFET***

We can summarize the S-model of the MOSFET in algebraic form as:

$$\text{when} \longrightarrow v_{GS} < V_T, \quad \text{then} \longrightarrow i_{DS} = 0 \quad \texttt{and} \quad \text{when} \longrightarrow v_{GS} \geq V_T, \quad \text{then} \longrightarrow v_{DS} = 0$$

MOSFET Switch Implementation of Logic Gates and Logic Functions

Switches can be used to build logic gates. As we can use MOSFET as a switch, logic gates can be built using MOSFETs. The following subsections discuss two logic gates, NOT gate and NAND gate, which are implemented using MOSFETs. We can also implement various Logic Functions using MOSFETs. To demonstrate this thing, a logic function will be implemented in Task-01.

NOT Gate/Inverter Using MOSFET

Consider the circuit shown in following figure, which comprises a MOSFET and a load resistor powered by a supply voltage V_S. This circuit acts as a NOT Gate/Inverter.

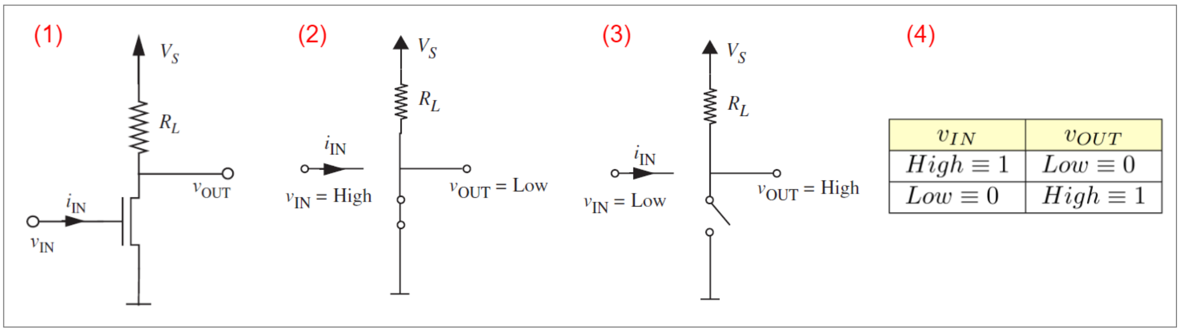


Figure 3: ***(1) MOSFET NOT Gate (2) When Input is '1' (3) When Input is '0' (4) Truth Table***

NAND Gate Using MOSFET

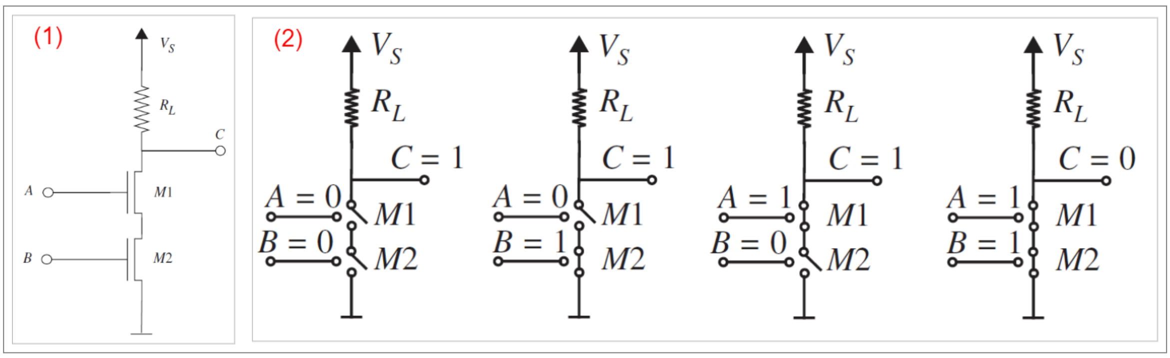


Figure 4: ***(1) MOSFET NAND Gate (2) Equivalent Circuits for Different Inputs***

Consider the circuit shown in the figure above, which comprises a two MOSFETs and a load resistor powered by a supply voltage V_S. This circuit acts as a NAND gate. NAND gate is a universal gate that can be used to implement any Logic Function.

Logic Function Using MOSFET

We can use combinations of MOSFETs to implement various logic funtions. The circuit shown in **Figure-5** implements $f = \overline{xy + z}$.

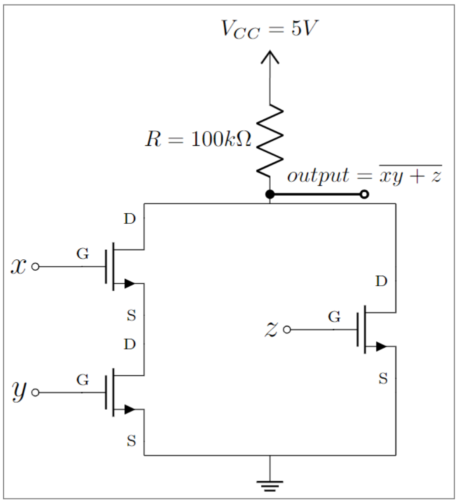


Figure 5: ***Logic Function using MOSFET***

I-V Characteristics of a MOSFET

The S-model of a MOSFET is a simplification of the actual I-V characteristics of a MOSFET which helps us understand the behavior of a MOSFET as a switch. But the actual I-V characteristics is very different from it.

Figure-6 represents the actual I-V characteristics of a MOSFET. There are 3 operating regions in the I-V characteristics graph: **Cut-off, Triode, Saturation**. The first two are useful if we want to use MOSFET as a switch. On the other hand, if we want to use MOSFET as an amplifier, we must operate it in the saturation region.

MOSFET's operating region depends on the applied voltages at Gate, Drain, Source terminals which can be seen in the I-V characteristics graph.

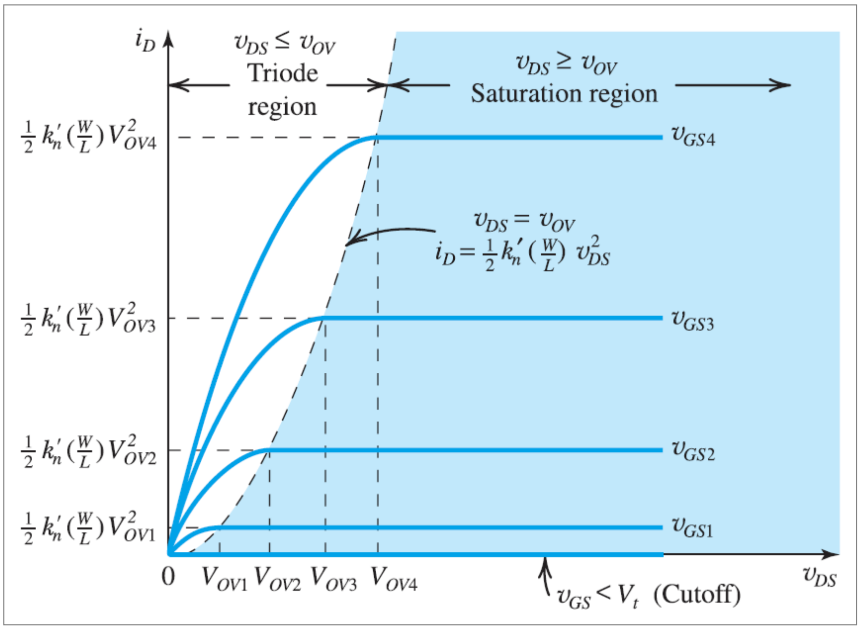


Figure 6: ***I-V Characteristics of a MOSFET***

In this graph

V_T = ***Threshold Voltage***

v_{OV} = ***Overdrive voltage***

L = ***Channel Length***

W = ***Channel Width***

k_n' = ***Process Transconductance Parameter***

$v_{GS} = v_G - v_S$

$v_{DS} = v_D - v_S$

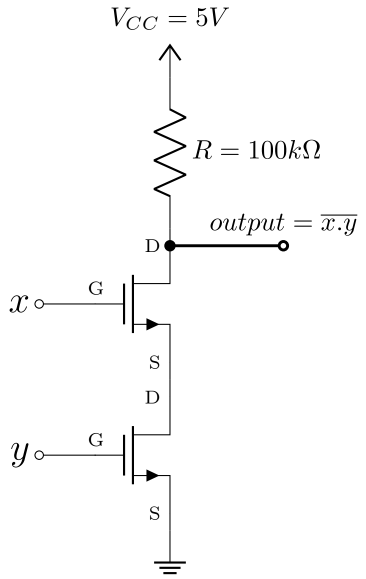
$v_{OV} = v_{GS} - V_T$

We can summarize the operating regions of as MOSFET as:

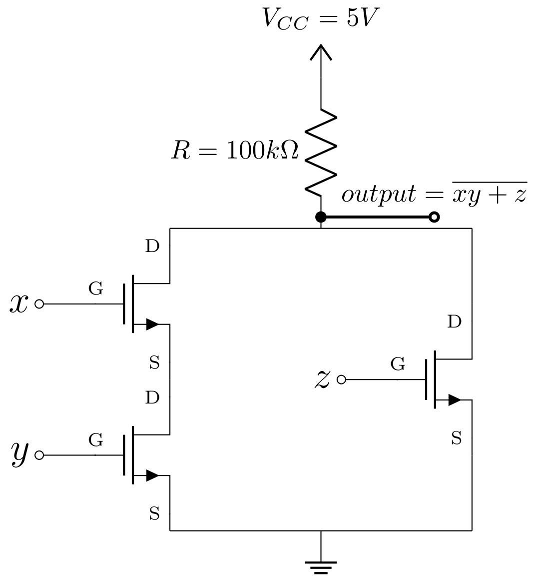
When	Operating Mode	Equation of Current
$v_{GS} < V_T$	Cutoff Mode	$i_D = 0$
$v_{GS} \ge V_T, v_{DS} \le v_{OV}$	Triode Mode	$i_D = k_n'\,(W/L)\left(v_{OV} - \frac{1}{2}v_{DS}\right)v_{DS}$
$v_{GS} \ge V_T, v_{DS} > v_{OV}$	Saturation Mode	$i_D = \frac{1}{2}k_n'\,(W/L)\,v_{OV}^2$

The value of V_T is controlled during device fabrication and typically lies in the range of 0.3 V to 1 V. From the graph, we see that, for the same value of v_{DS}, i_{DS} increases if we increase v_{GS}. Also, for a lower value of v_{GS}, the MOSFET operates in Saturation for a lower value of v_{DS} and for higher value of v_{GS}, the MOSFET goes into Saturation for a higher value of v_{DS}.

Task-01: Logic Gate and Logic Function Implementation



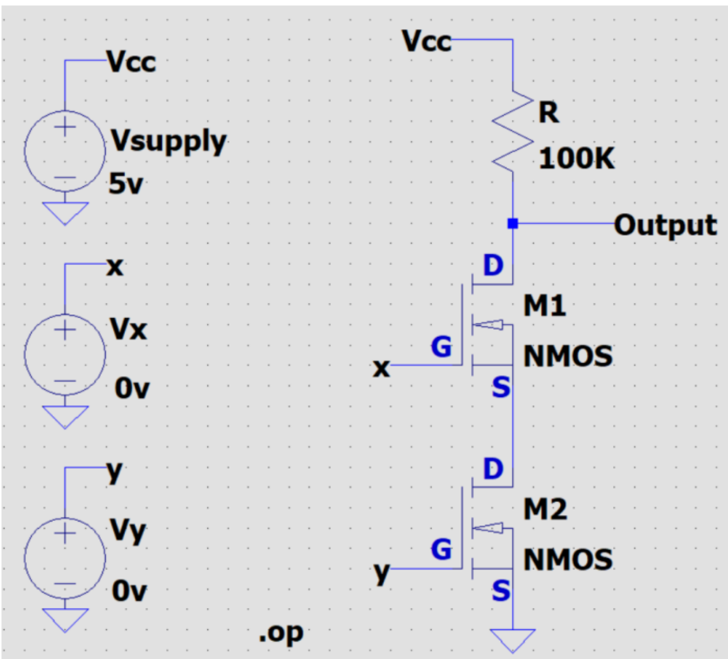
Circuit-1
NAND Gate using MOSFET

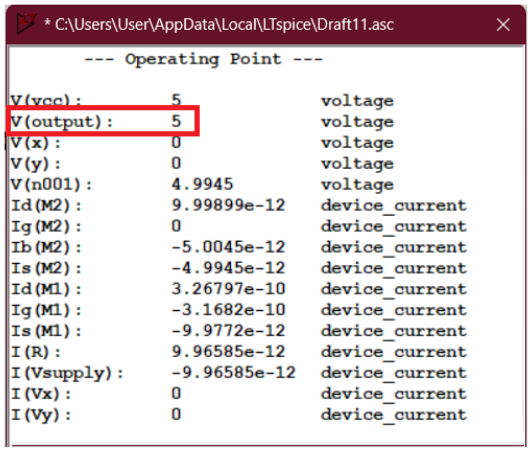


Circuit-2
Logic Function, $f = \overline{xy + z}$ using MOSFET

Procedure

1. Open a new schematic in LTspice and construct circuit-1 which represents NAND gate with the boolean inputs 'x = 0' and 'y = 0' as shown in the figure above. Use the component **'nmos'** for MOSFETs. Your schematic should look like the following one.

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--- Operating Point ---

V(vcc):	5	voltage
V(output):	5	voltage
V(x):	0	voltage
V(y):	0	voltage
V(n001):	4.9945	voltage
Id(M2):	9.99899e-12	device_current
Ig(M2):	0	device_current
Ib(M2):	-5.0045e-12	device_current
Is(M2):	-4.9945e-12	device_current
Id(M1):	3.26797e-10	device_current
Ig(M1):	-3.1682e-10	device_current
Is(M1):	-9.9772e-12	device_current
I(R):	9.96585e-12	device_current
I(Vsupply):	-9.96585e-12	device_current
I(Vx):	0	device_current
I(Vy):	0	device_current

2. Use **'DC op pnt'** simulation for this circuit. Run the simulation. You should observe the simulation results like the following ones given above. Here, V(output) = 5v is representing boolean 1 at the output.

3. Run the simulation for rest of the combinations of the boolean inputs 'x' and 'y' and fill in the relevant cells of 'Data Table 1'.

4. Now, Open a new schematic in LTspice and construct circuit-2 according as shown in the figure above.

5. Run the simulation for all the combinations of the boolean inputs 'x', 'y' and 'z' and fill in the relevant cells of 'Data Table 1'.

Data Table 1: Verification of the Truth Tables of Logic Gate and Logic Function

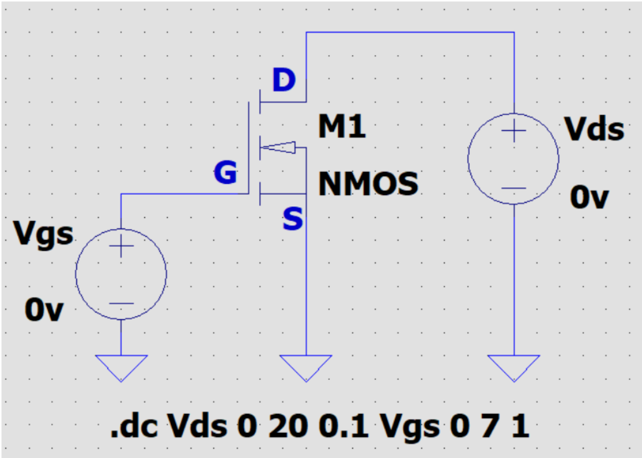
1. NAND Gate

Input Voltage, V_x (volt)	**Input Voltage, V_y (volt)**	**V(output) (volt)**	**Boolean Output (0 or 1)**
0V	0V		
0V	5V		
5V	0V		
5V	5V		

2. Logic Function, f = $\overline{xy + z}$

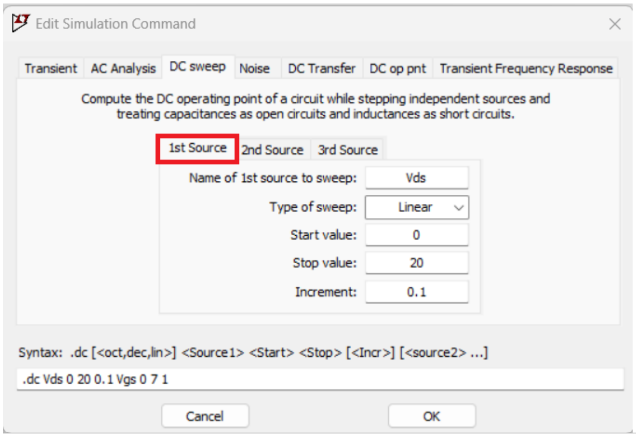
Input Voltage, V_x (volt)	**Input Voltage, V_y (volt)**	**Input Voltage, V_z (volt)**	**V(output) (volt)**	**Boolean Output (0 or 1)**
0V	0V	0V		
0V	0V	5V		
0V	5V	0V		
0V	5V	5V		
5V	0V	0V		
5V	0V	5V		
5V	5V	0V		
5V	5V	5V		

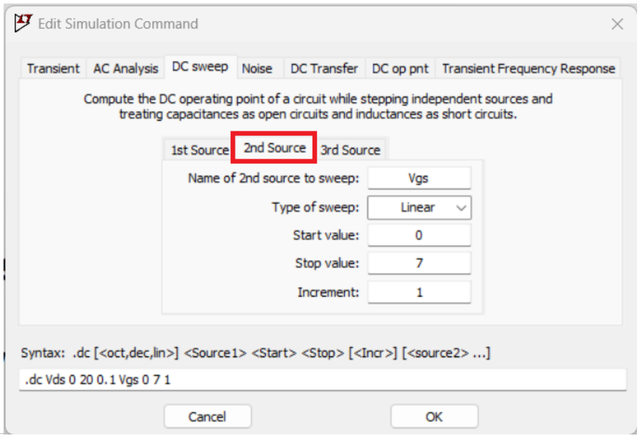
Task-02: I-V Characteristics of a MOSFET



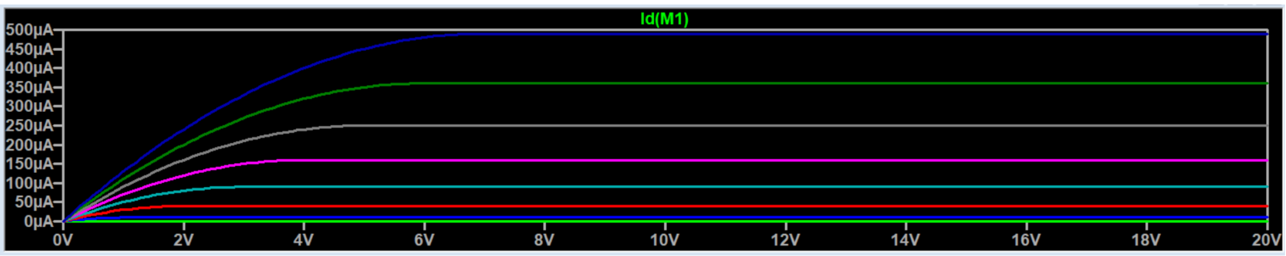
Procedure

1. Open a new schematic in LTspice and construct the circuit shown above.
2. Use "DC Sweep" simulation for this circuit. Use the following parameters.

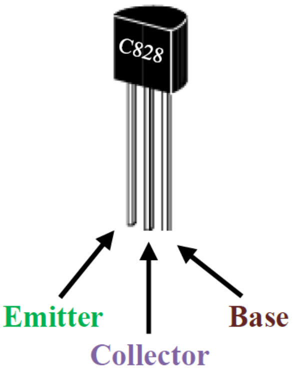


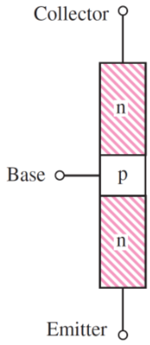


3. Run the simulation. Plot **Id(M1)**. You should get an I-V characteristics graph like the following one.



Introduction to BJT





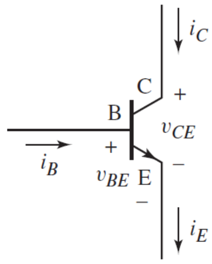


Figure 7: ***IC, Simple Geometry and Circuit Symbol of an npn BJT***

The bipolar junction transistor (BJT) is a type of transistor that is used for electrical amplification and in very-high frequency applications such as radio frequency (RF) circuits for wireless systems and high-speed switching emitter-coupled logic (ECL) gates. BJT is primarily a three terminal device consisting of the following terminals: Base (B), Emitter (E), Collector (C). There are two types of BJTs: (i) npn BJT and (ii) pnp BJT. Our discussion and experiment will be confined to npn BJT.

Figure 7 shows the IC, circuit symbol and simple geometry of an npn BJT. The arrowhead in the circuit symbol is always placed on the emitter terminal, and it indicates the direction of the emitter current. For an npn BJT, this direction is out of the emitter. The npn BJT contains a thin p-region between two n-regions. So the transistor consists of two pn junctions, the emitter–base junction (EBJ) and the collector–base junction (CBJ). Depending on the bias condition (forward or reverse) of each of these junctions, different modes of operation of the BJT are obtained. The operating modes are: Cut-off, Active and Saturation. The following table summarizes the modes of operation.

The active mode is the one used if the transistor is to operate as an amplifier. Switching applications (e.g. logic circuits) utilize both the cutoff mode and the saturation mode. There can be a fourth mode of a BJT called the reverse-active mode which occurs when the EBJ is reversed biased and the CBJ junction is forward biased (not shown in the table).

BJT Modes of Operation		
Mode	EBJ	CBJ
Cutoff	Reverse	Reverse
Active	Forward	Reverse
Saturation	Forward	Forward

Of the 3 modes of operation of BJT, the active mode is the most important one because BJT can be used as an amplifier only in this mode. BJT will be in active mode when EBJ is in Forward Bias and CBJ is in Reverse Bias. BJT operates in saturation mode when its collector current is not dependent on the base current and has reached a maximum. This happens when both the EBJ and the CBJ are in Forward Bias. In saturation mode, huge amount of current flows through BJT and it acts like a closed switch. Cut-off mode is the opposite of saturation mode. In cut-off mode, both junctions of BJT remain reverse biased. That is why no current flows through the device (actually, very negligible amount of current flows) and the BJT acts like an open switch.

Input and Output I-V Characteristics of BJT

The I-V characteristics of a BJT depends on the circuit configuration. There are three basic configurations for connecting the BJT: the common base (CB) configuration, the common emitter (CE) configuration, and the common collector (CC) configuration. Though each configuration has their own applications, the CE is the most widely used configuration and by far the most popular for amplifiers.

In CE configuration, the emitter is the common terminal. Hence, the input is between the base and the emitter while the output is between the collector and the emitter. So, the input I-V characteristics is the variation of the base current I_B with the base-emitter voltage V_{BE}, and the output I-V characteristics is the variation of the collector current I_C with the collector-emitter voltage V_{CE}.

The following figure shows the input I-V characteristics of an npn BJT for the CE circuit configuration which illustrates the variation in I_B with respect to V_{BE} when V_{CE} is kept constant. In the graph, I_B changes exponentially as V_{BE} changes. This is obvious since the BJT's base-emitter junction is similar to a pn junction diode. So it's current voltage relationship should also be like a pn junction diode.

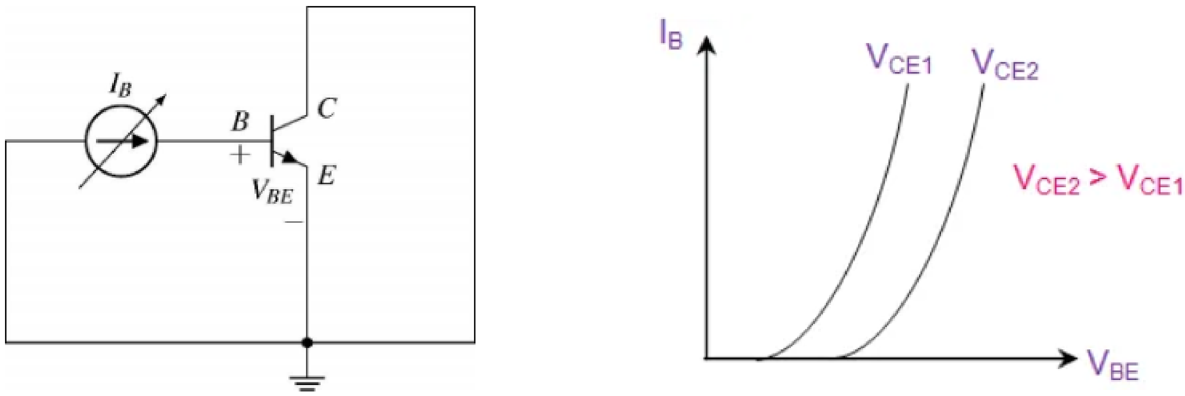


Figure 8: BJT input I-V characteristics Circuit and Graph in CE configuration

The output I-V characteristic of a BJT in CE configuration is also referred to as the collector characteristic. We are mainly interested in this one. The following circuit and graph shows the output I-V characteristics of a BJT in CE configuration. The I-V characteristics shows the variation in I_C with the changes in V_{CE} when I_B is held constant. In the graph we can see a rapid increase in collector current at the beginning. Then the collector current becomes almost constant. This graph can be divided into 3 regions:

1. Active Region (where output current becomes almost constant)
2. Saturation Region (where I_C increases rapidly)
3. Cut-off Region (where the current is zero/almost zero)

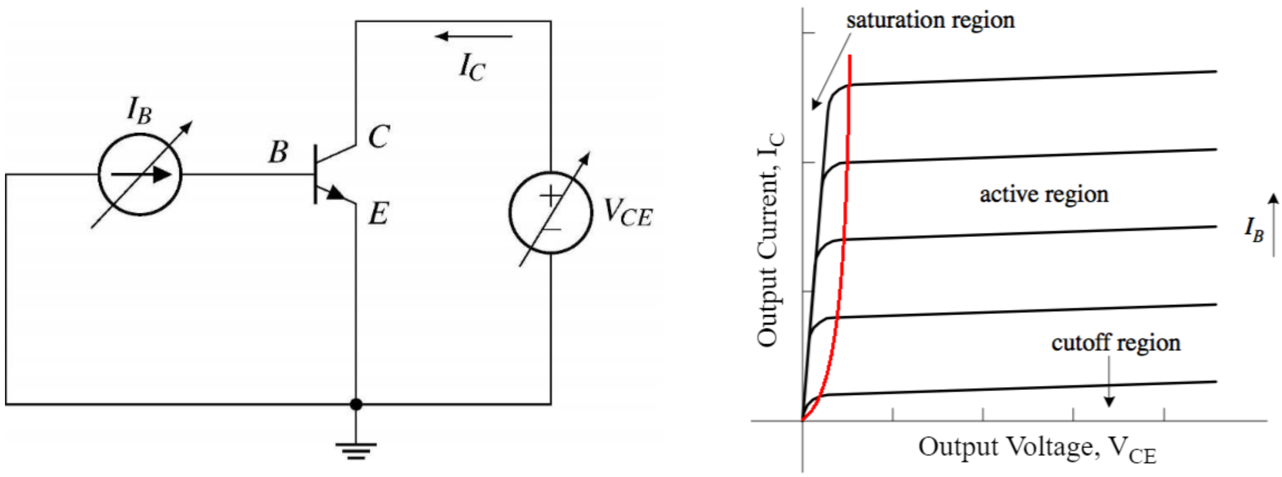
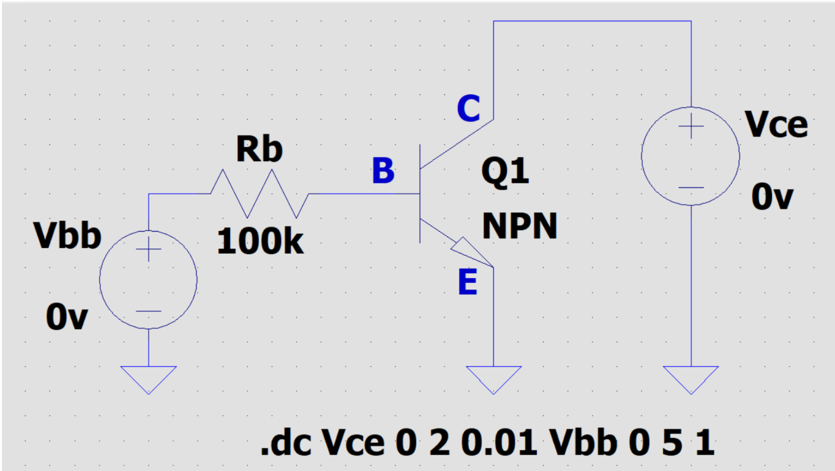


Figure 9: BJT output I-V characteristics Circuit and Graph in CE configuration

From the output I-V characteristics we see that, in the active region, if we keep V_{CE} constant, I_C increases with the increase of I_B. This relationship between I_C and I_B in active mode is actually linear in nature which can be represented by the following equation: $I_C = \beta I_B$, where β is a constant. Typically, $\beta = 50$ to 200.

Task-03: I-V Characteristics of a BJT (Class Work)



1. Carefully observe and understand the image given above and construct the circuit to obtain the I-V characteristics graph of BJT according to it.
2. Run the simulation, plot the I-V graph (i.e. I_C vs V_{CE}) and take a screenshot of the graph.

Task-04: Report

1. Cover page [include course code, course title, name, student ID, group, semester, date of performance, date of submission]
2. Attach all the screenshots of the graphs and describe them properly.
3. Answer the questions of the Test Your Understanding section.
4. Did you face any challenges in simulation? If yes, explain briefly.
5. Add a brief Discussion regarding the experiment.

Test Your Understanding

Answer the following questions:

1. We can use the MOSFET as a switch. Which operating regions do we need for this purpose and why?
   Answer:

2. Draw a circuit using MOSFETs that implements the following logic function, $\boldsymbol{f = (x+y)z}$
   Answer:

3. We used MOSFET as a switch and implemented various logic funtions. Can we do the same using BJTs? Explain briefly.
   Answer: