2120170]
Tahmid

04.16.23
(DZK)

Memory

RAM

memory unit : collection of registers + associated circuits

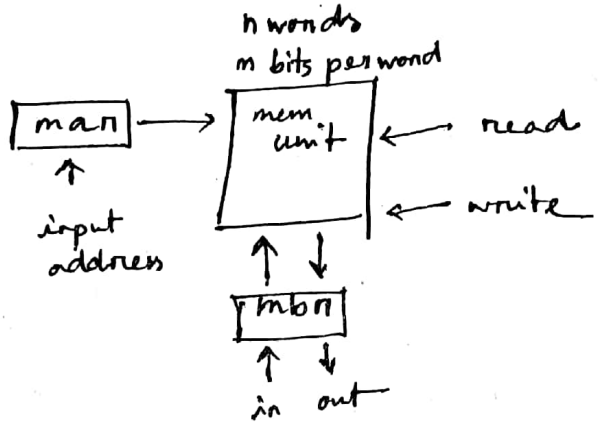
binary cell : storage

word : group of bits (16 bit)

- 1 Byte (8 bit)

MAR : memory address register

MBR : memory buffer register



read → (10 adds in mem) ← mar → mbr → user

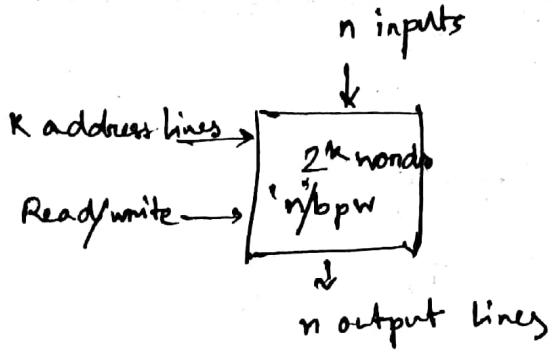
write → mbr → (mem adds free) ← mar

mbr → read এর time write এর time input stay

mar → access of memory address.

1024 x 16

- no of words x bits



- K number address lines = 2^K words.

e.g.

1024 x 8

$\Rightarrow 2^{10} \times 8$

K = 10 = address register contains 10 F.F.

bits = 8 = buffer register contains 8 F.F.

Base 2

K = 2^{10} = 1024

M = 2^{20} = 1048 576

G = 2^{30} = 1,073,741 824

Base 10

10^3 = 1000

10^6 = 1000 000

10^9 = 1000 000 000

Formulas

capacity = no of words × bit/word

no of words = $2^{(address\ line = k)}$

e.g. $2^{16} \times 16$ mem

capacity = 1048576 bits

= 1048576/8 bytes

= 131072 bytes

= 131072/1024 KB

= 128 KB

e.g. how many address liner for 64 MB Ram 32 bit

∴ no of words = $\frac{64\ MB}{32}$

= 16777216 bits

= 2^{24} bits

∴ address lines = 24

cap = 64 MB

bits = 32 bit/word

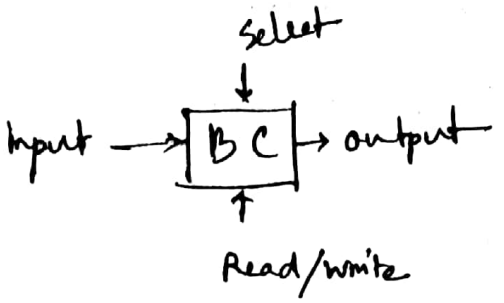
64 MB

⇒ 64 × 1024 KB × 1024 Byte × 8 B

⇒ 16777216 bits

[∵ use log to calculate]

Binary Cell :



Logic construction w/ Decoder & OR gates (4X3 RAM)

- address line = dec. inputs
- dec outputs = 2^n inputs
  = no of words
- binary cells = bits/word
  for each word
- binary cells will be connected to Data inputs.
- Data inputs = bits/word
  lines