Set B

BRAC University Department of Computer Science and Engineering	
Semester: **Fall 2024** Course Code: **CSE460** Course Title: **VLSI Design** **Submission Link:** https://forms.gle/NGgtADy285WajePv8	**Lab Assessment 5** **S03** Full Marks: **10** Deadline: **3:20 PM**

****Submission Instructions:**

- Create a word/doc file in which you should have at least the following for **ALL** of the questions.
    1. Verilog Code
    2. Screenshot of the timing diagram as per question requirement.
    3. State diagram
- You have to submit the PDF of the word document in the link mentioned above.
  You have to submit all your code files after zipping the folder containing all files in the link mentioned above.
- You must mention your Student ID and section in the filename.
- The PDF should be named as follows: `LA2_<section>_<ID>.pdf`
    - Example: `LA2_01_2011022.pdf`

Problem 1:

Objective:

Design a vending machine with only one product worth Tk. 60.

Input: cash_in (clock and reset will be used as input by default)
Output: purchase, cash_return

Possible notes you can provide as input: Tk. 30, Tk. 50 and Tk. 100 (Consider an input of Tk. 0 as a wait period)

Deliverables:

1. **Verilog Code**:
    - Write a Verilog module to implement the above system.
2. **Simulation**:
    - Simulate the module and provide a timing diagram (waveform) that includes different input scenarios. Provide all the codes after zipping the folder that contains them.