



UNIVERSITY OF ASIA PACIFIC

DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING(CSE)

Course Title: Computer Architecture

Course Code: CSE 303

Submitted By,

Name: H.M. Tahsin Sheikh

ID:22201243

Sec: E

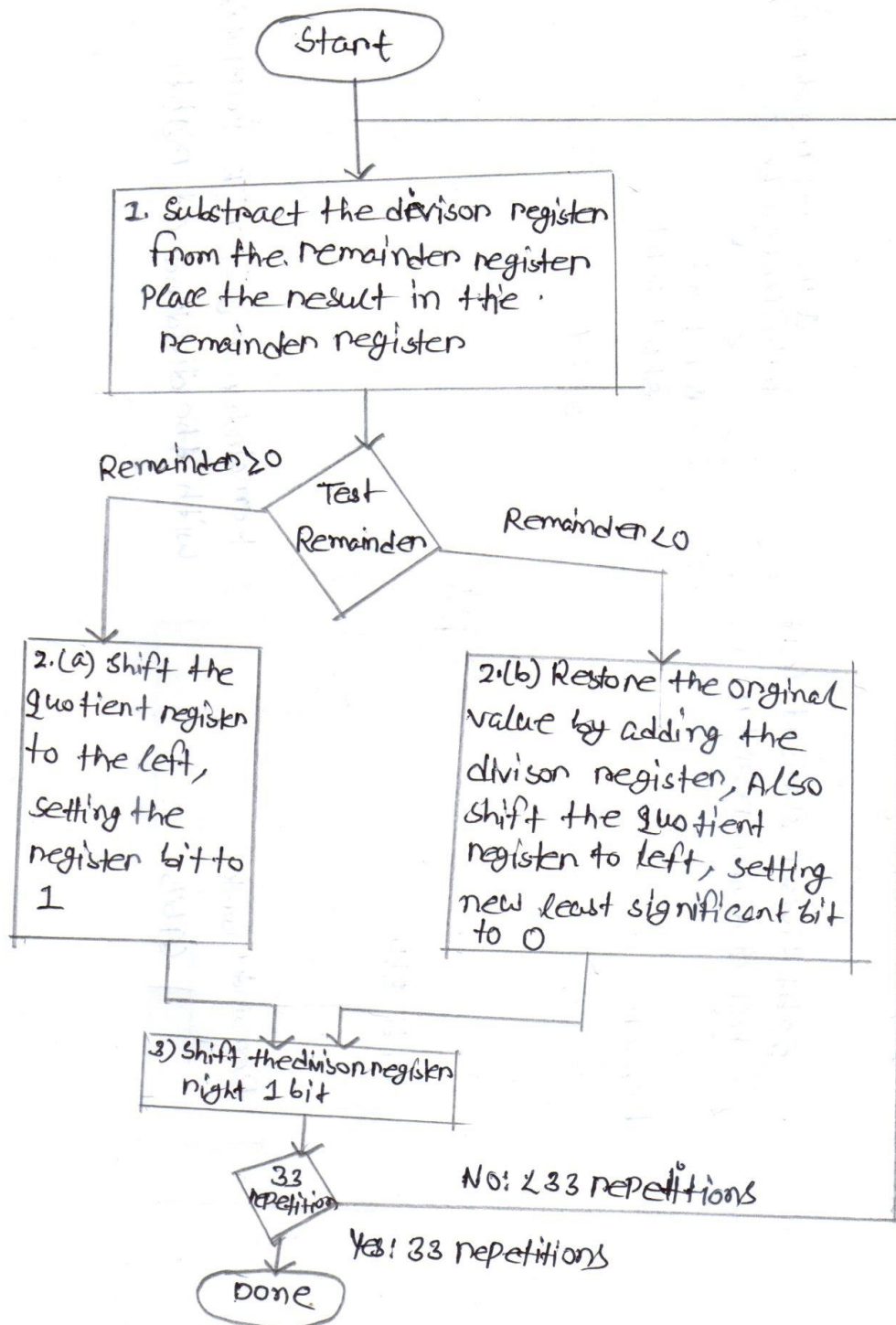
Submitted To,

Shammi Akhter,

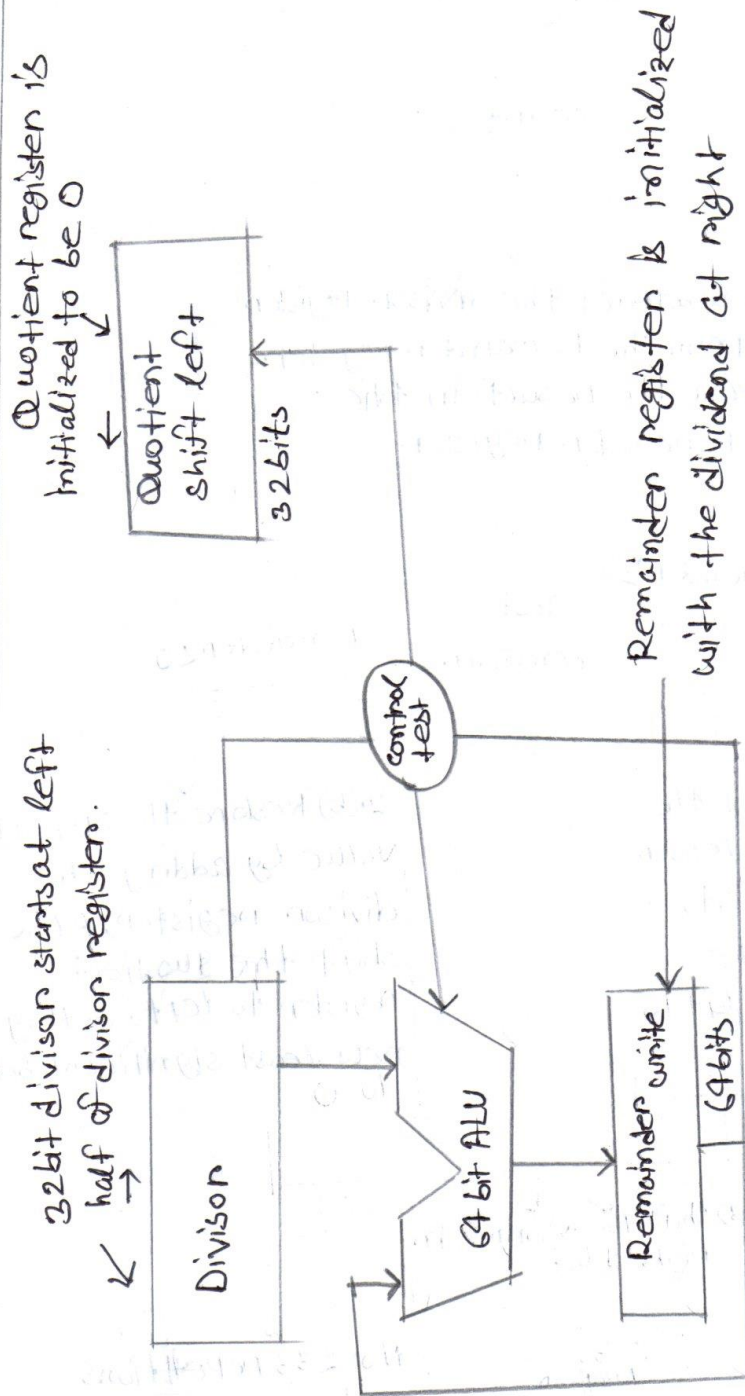
Assistant Professor

**Department of CSE
University of Asia pacific**

Version 1 Algorithm:



Version 1 Hardware:



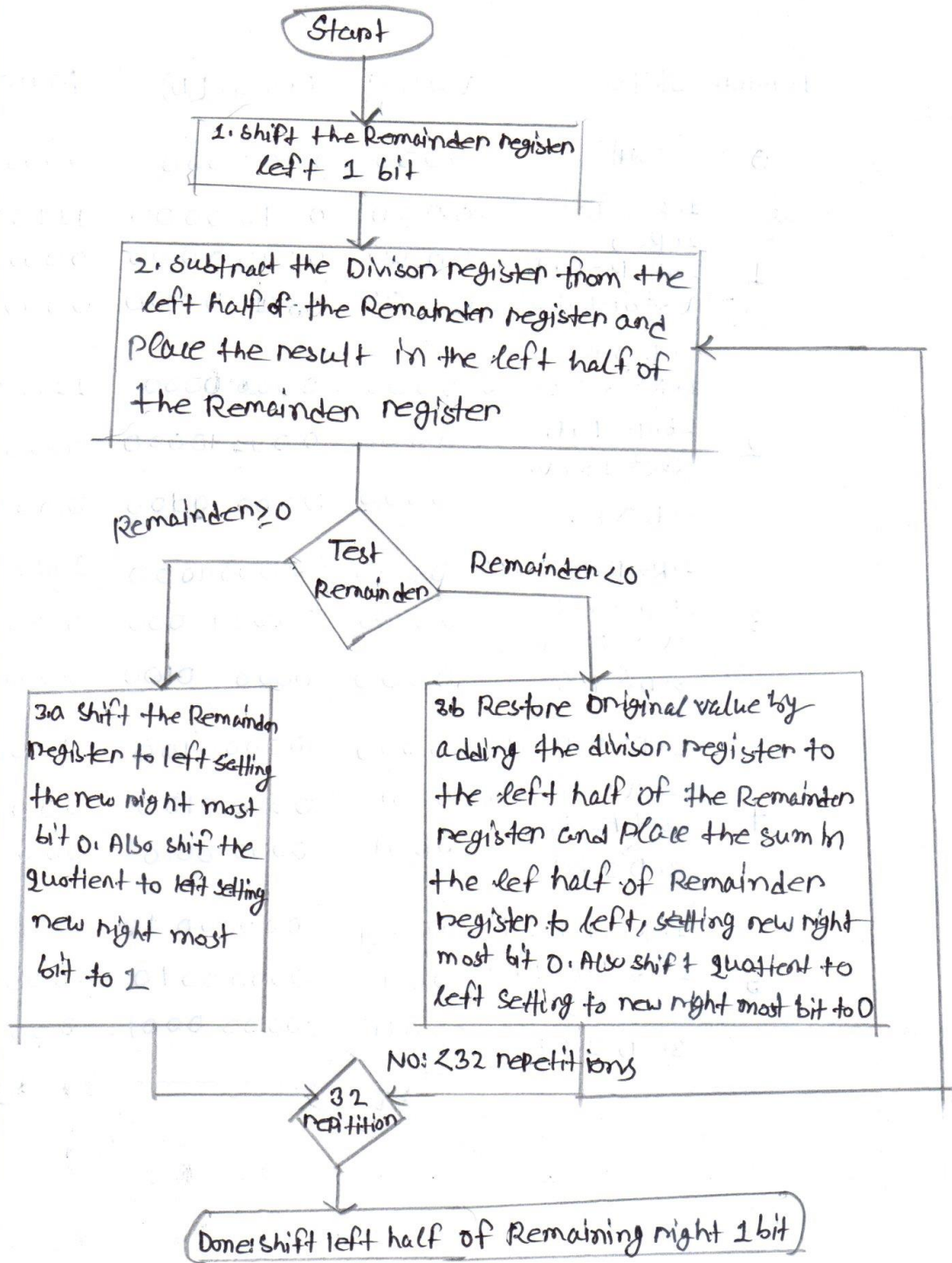
Version 1 Example:

$$\begin{array}{l} \nearrow 011 \\ 7 \div 2 \rightarrow 0010 \end{array}$$

Iteration	Steps	Quotient (Q)	Divisor (D)	Remainder (R)
0	init	0000	0010 0000	0000 0111
1	1. $R = R - D$ 2. $R < 0$ 2. (b) $R = R + D$ Q \leftarrow 1 bit left shift, $Q_0 = 0$ 3. $D \rightarrow RS$	0000 00 00 0000	0010 0000 0010 0000 0001 0000	1110 0111 0000 0111 0000 0111
2	1. $R = R - D$ 2. $R < 0$ 2b. $R = R + D$ Q \leftarrow 1s, $Q_0 = 0$ 3. $D \rightarrow RS$	0000 0000 0000	0001 0000 0001 0000 0000 1000	1111 1111 0000 0111 0000 0111
3	1. $R = R - D$ 2. $R < 0$ 2b. $R = R + D$ Q \leftarrow 1s, $Q_0 = 0$ 3. $D \rightarrow RS$	0000 0000 0000	0000 1000 0000 1000 0000 0100	1111 1111 0000 0111 0000 0111
4	1. $R = R - D$ 2. $R > 0$ 2a. Q \leftarrow 1 bit and set 15b to 1 3. $D \rightarrow 1$ bit	0000 0001 0001	0000 0100 0000 0100 0000 0010	0000 0011 0000 0011 0000 0011
5	1. $R = R - D$ 2. $R > 0$ 2a. \leftarrow 1 bit and set 15b to 1 3. $D \rightarrow 1$ bit	0001 0011 0011	0000 0010 0000 0010 0000 0001	0000 0001 0000 0001 0000 0001

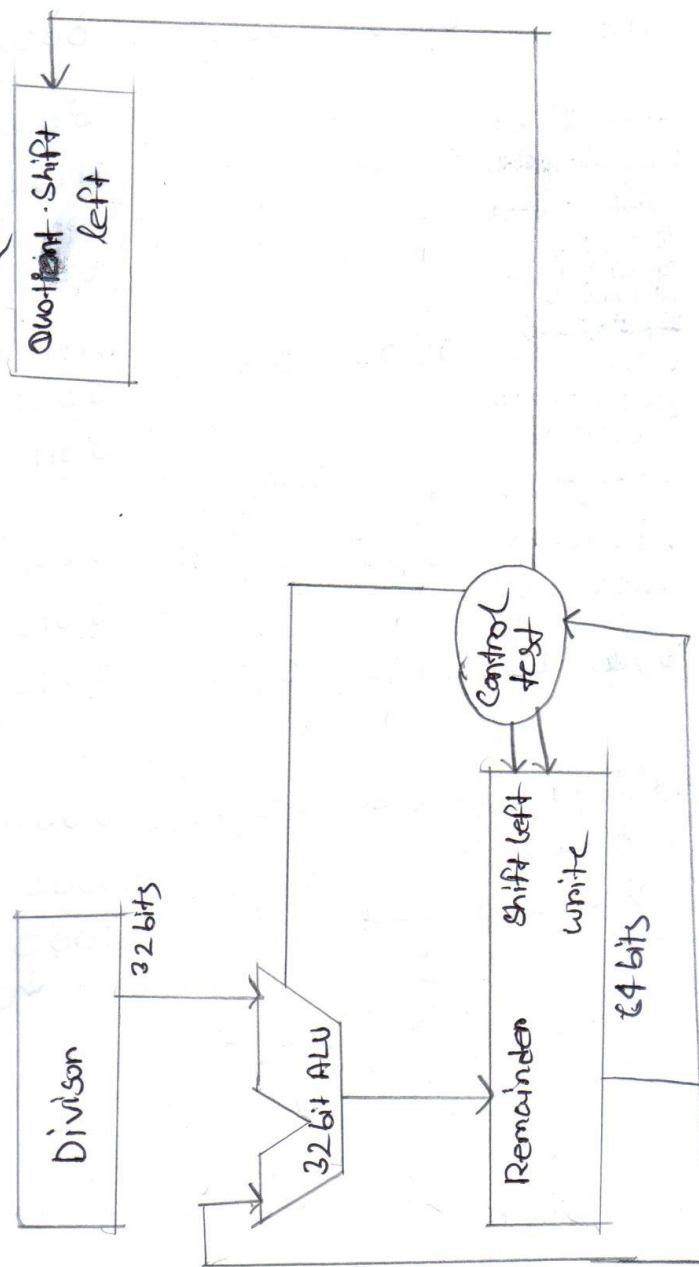
 $\rightarrow 3$
 $\rightarrow 1$

Version 2 Algorithm:



Version 2 Hardware:

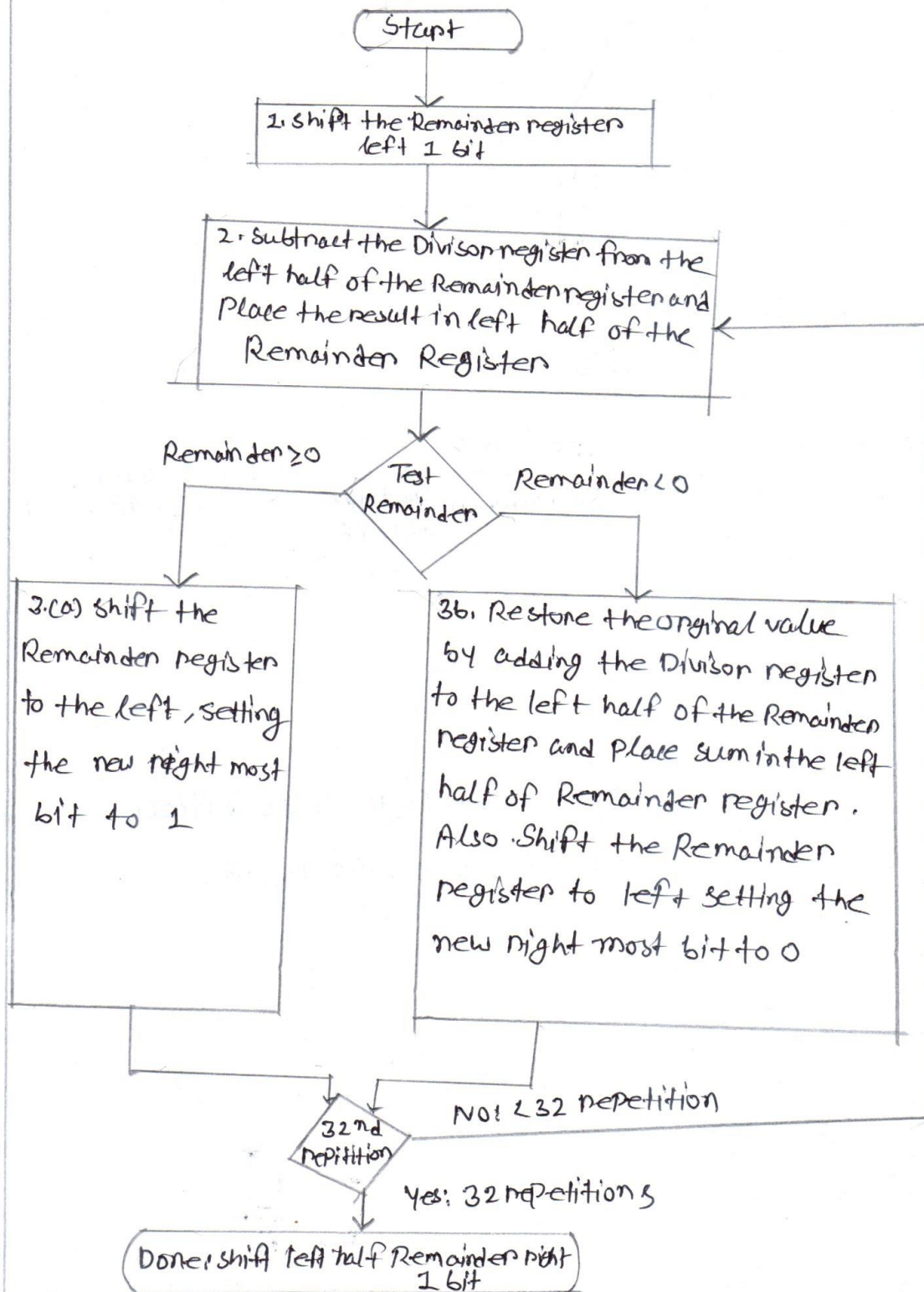
Remainder register is initialized with the dividend at right



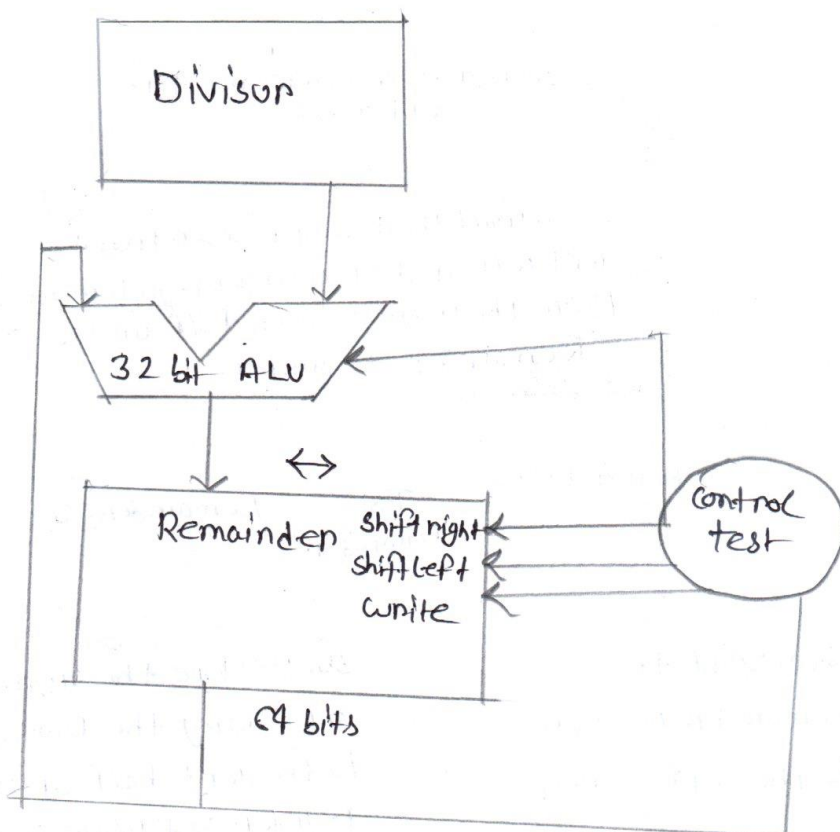
Version 2 Example:

Iteration	Steps	Quotient Q	Divisor D	Remainder R
0	init	0000	0010	0000 0110
1	1. shift \hat{R} 1 bit 2. $R(L) = R(L) - D$ 3. $R(L) = R(L) + D$ \hat{R} set LSB 0 1 bit set 1 sb right most 0	0000	0010	0000 1100 1110 1100 0000 1100 0001 1000
2	1. $R(L) = R(L) - D$ 3. $R(L)$ 3. $R(L) = R(L) + D$ $R \leftarrow LS, R_0 \leftarrow 0$ $Q \leftarrow LS, Q_0 \leftarrow 0$	0000	0010	1111 1000 0001 1000 0011 0000
3	2. $R(L) = R(L) - D$ 3. \hat{R} set LSB 0 $\hat{Q}, Q_0 = 1$	0000 0001	0010 0010	0001 0000 0010 0000 0010 0000
4	2. $R(L) = R(L) - D$ 3. $\hat{R}, R_0 = 0$ $\hat{Q}, Q_0 = 1$	0001 0011 ↓ 3	0010	0000 0000 0000 0000 0000 0000 ↓ 0

Version 3 Algorithm



Version 3 Hardware:



Remainder register is initialized with the dividend at right

22201243

Version 3 Example:

$$\begin{array}{c} \nearrow 011 \\ (7 \div 2) \nearrow 0010 \end{array}$$

Iteration	Steps	Divisor, D	Remainder, R
0	init	0010	0000 0111
1	1. shift \overleftarrow{R} 1 bit 2. $R(L) = R(L) - D$ 3. $R \geq 0$, 3b. $R(L) = R(L) + D$ 4. \overleftarrow{R} 1 bit, $R_0 = 0$	0010	0000 1110 1110 1110 0000 1110 0001 1100
2	2. $R(L) = R(L) - D$ 3. $R \geq 0$ 3b. $R(L) = R(L) + D$ 4. \overleftarrow{R} 1 bit, $R_0 = 0$	0010	1111 1100 0001 1100 0011 1000
3	2. $R(L) = R(L) - D$ 3a. \overleftarrow{R} 1 bit, $R_0 = 1$	0010	0001 1000 0011 0001
4	2. $R(L) = R(L) - D$ 3a. \overleftarrow{R} 1 bit, $R_0 = 1$	0010	0001 0001 0010 0011
	Done! $R(L) \xrightarrow{1} R_1$	0010	0001 0011