

Datapath

- Datapath consists of the functional units of the processor.
- Two types of data element:
 1. Elements that hold data - Program counter, register file, instruction memory etc.
 2. Elements that operate on data - ALU, address etc.
- There are two paths for every instruction.
 - (i) Fetch cycle → Same for all instruction (I, R, J).
 - (ii) Execution cycle → Depends on the type of the instruction.

5. Components:

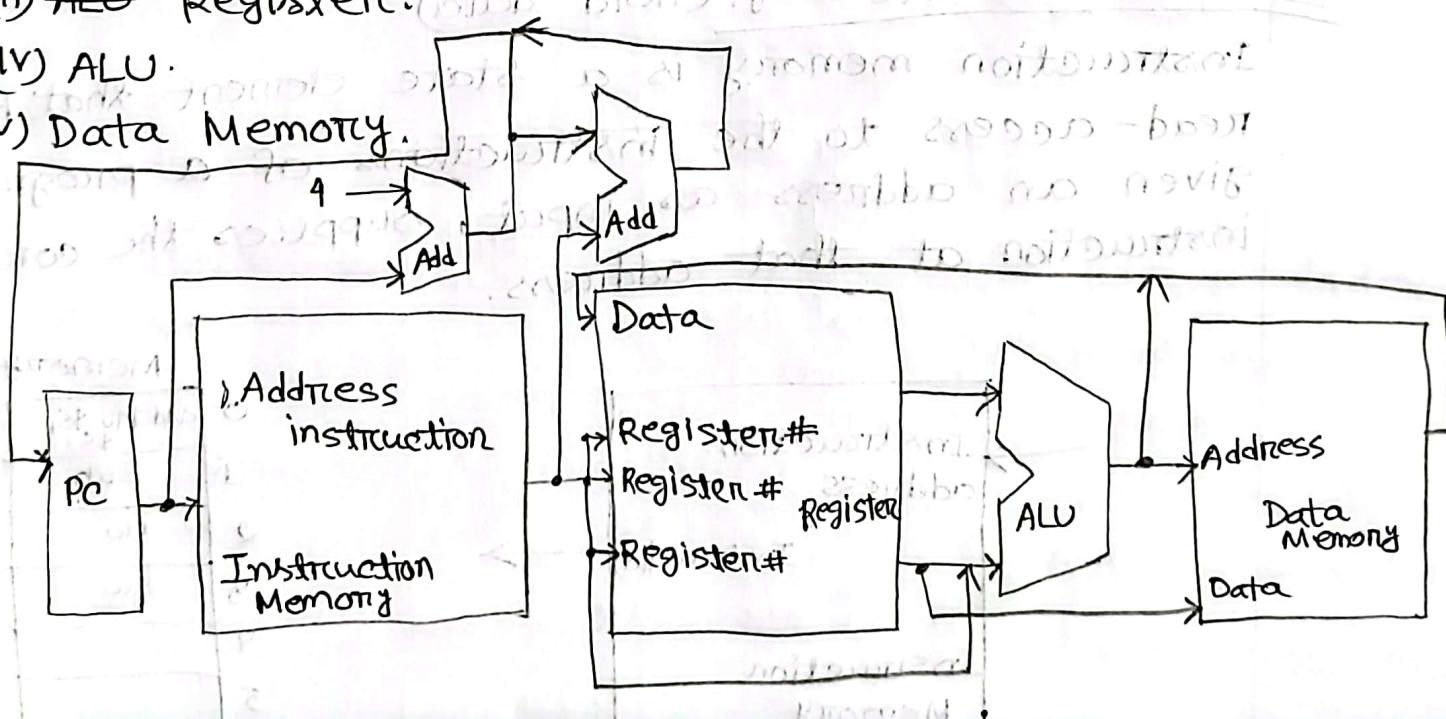
(i) PC (Program Counter)

(ii) Instruction Memory

(iii) ALU Register.

(iv) ALU.

(v) Data Memory.



Explain:

1. Program counter এর কাছে ইন্সেকশন যে instruction execute করবো তার address save রাখা।
So, তা instruction execute করবো তার address থাকবে program counter এর কাছে।

2. Instruction memory এর কাছে ইলেক্ট্রনিক বাইট কে address এ চিহ্ন যে instruction থাকবে তেটি load করবে।

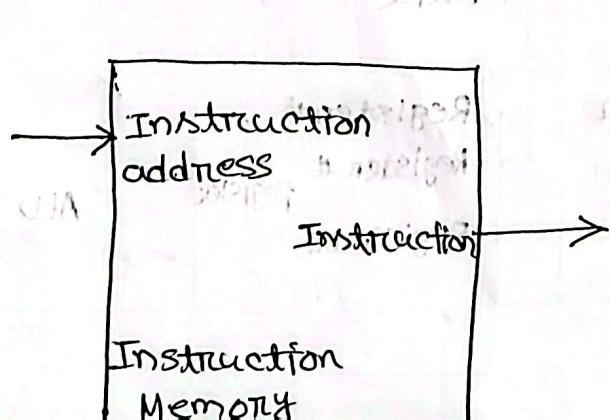
3.4. ALU তা যে arithmetic operation করবো তেটি ALU এর মধ্যে ইলেক্ট্রনিক বাইট কে ২টি variable মাবে এবং ১টি flag মাবে যেখানে যন্তা ইলেক্ট্রনিক operation করা হবে (addition/ sub/mul)।

এটি variable মাবে এবং operation calculate করবে।

5. Data memory কে ১টি address দিবে তেটি read/write করবে।

1. Instruction Memory: (Hold data)

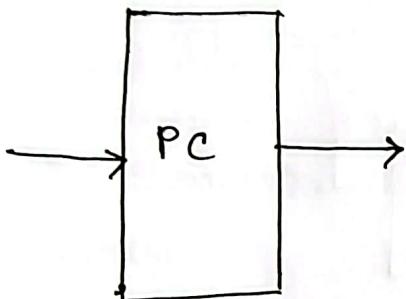
Instruction memory is a state element that provides read-access to the instructions of a program and given an address as input, supplies the corresponding instruction at that address.



Memory	
0	add \$t0,\$s1, \$s2
1	sub
2	lw
3	sw
4	
5	

2. Program Counter (PC): (Hold data)

The PC is a state element that holds the address of the current instruction.



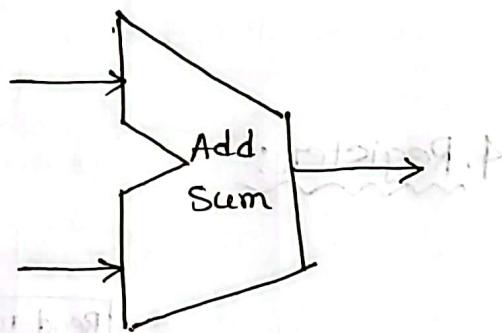
* The arrows on either side indicate that the PC state element is both readable and writeable.

3. ALU: (Add)

3. Adder (ALU):

The adder is responsible for incrementing the PC to hold the address of the next instruction.

It takes two input values, adds them together and outputs the result.

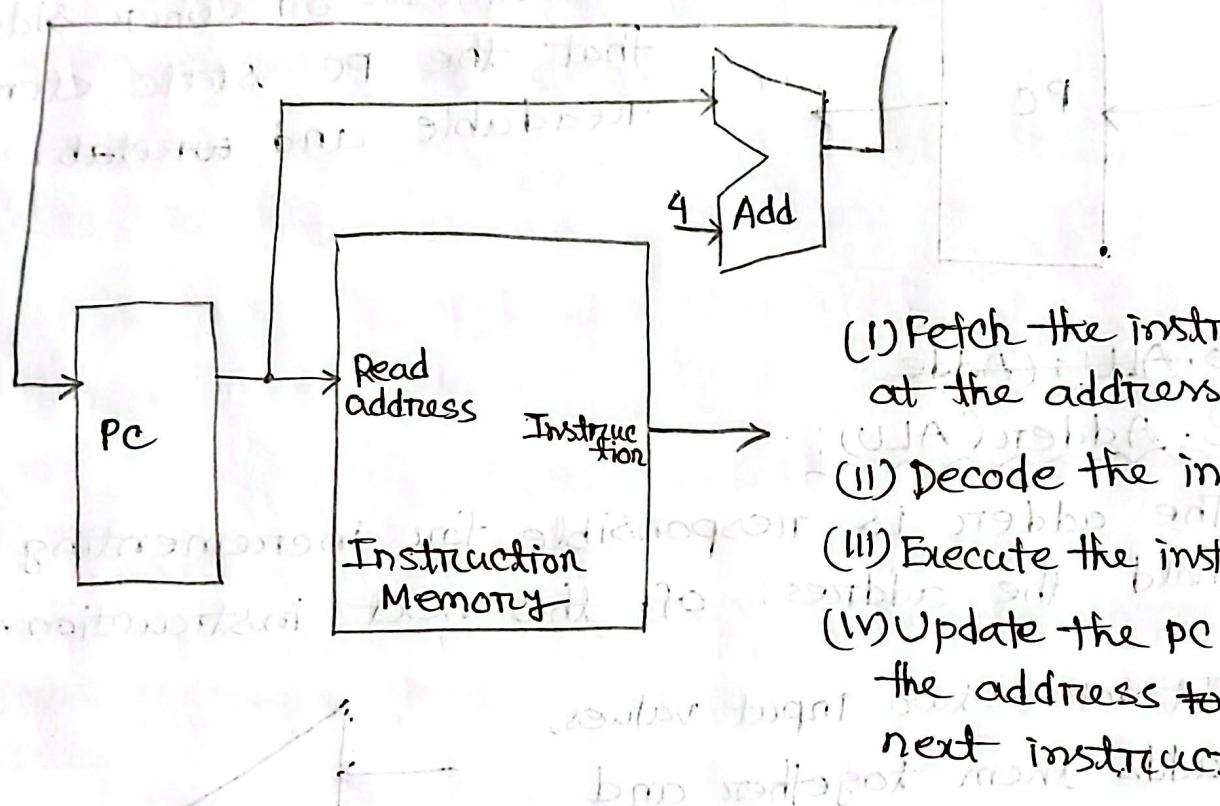


Now we have instruction memory, PC and adder datapath elements. Now, we can talk about the general steps taken to execute a program.

- Instruction fetching: Use the address in the PC to fetch the current instruction from instruction memory
- Instruction decoding: Determine the fields within the instruction.

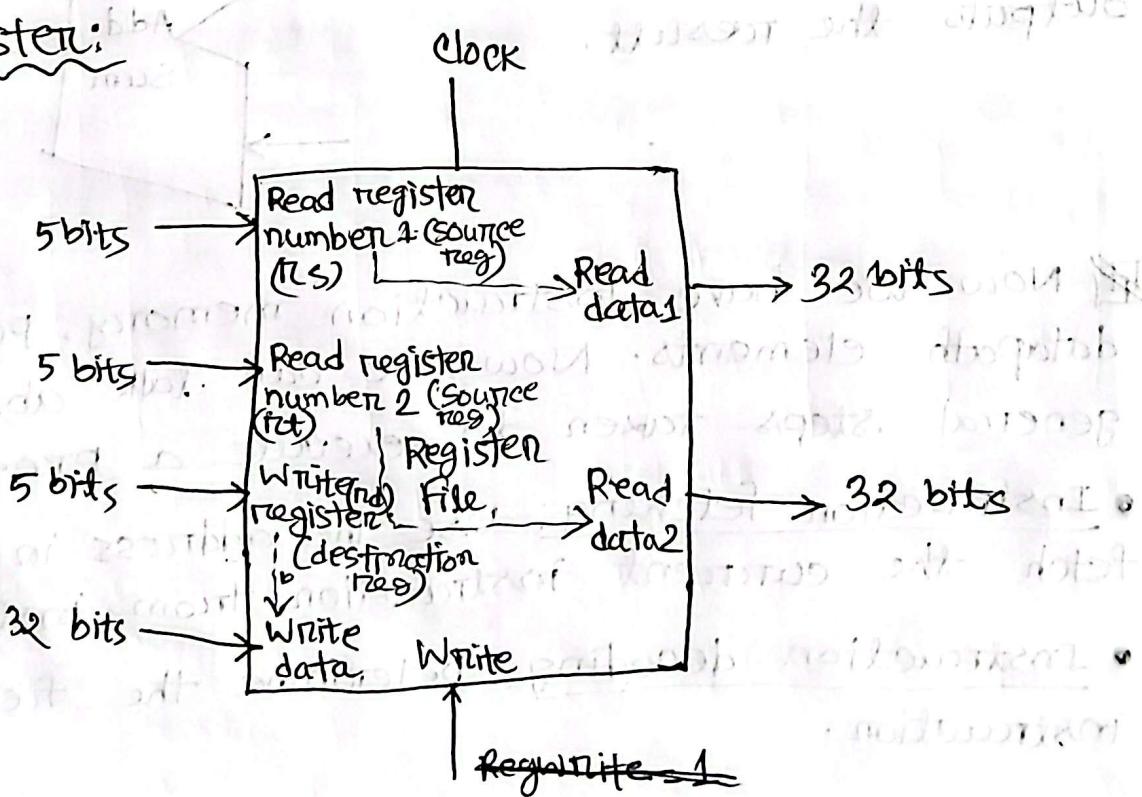
- Instruction execution: Perform the operation indicated by the instruction.

Update the PC to hold the address of the next instruction.



- (I) Fetch the instruction at the address in PC.
- (II) Decode the instruction.
- (III) Execute the instruction.
- (IV) Update the PC to hold the address to of the next instruction.

4. Registers



R-type Instruction:

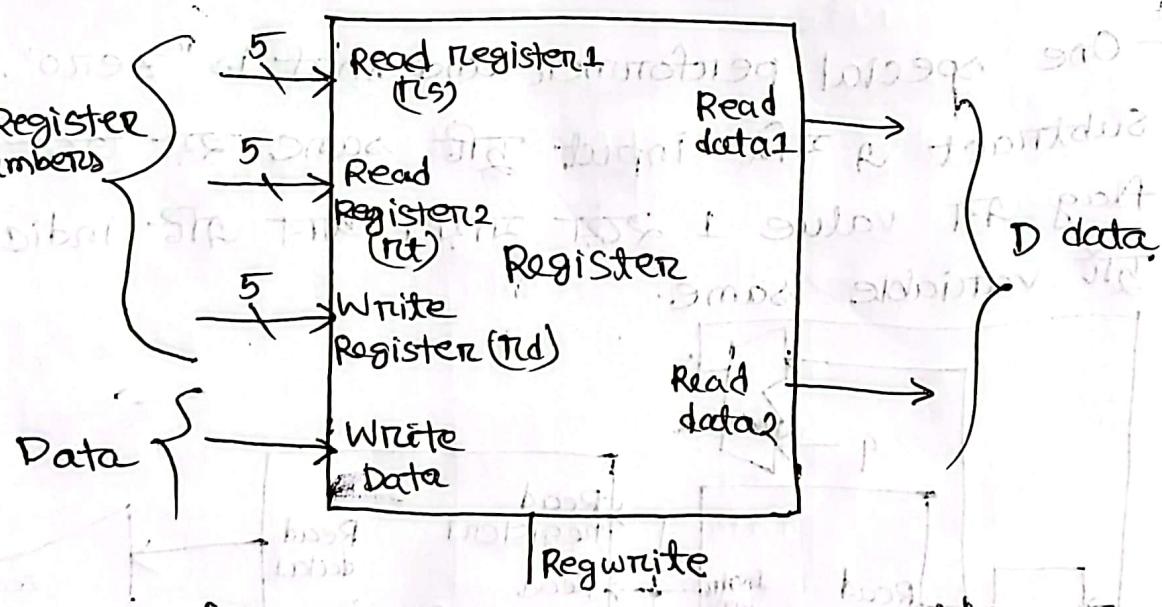
Name	Fields
Field size	6 bits 5 bits 5 bits 5 bits 5 bits 6 bits
R format	Op R _S R _t R _d Shamt funct

Two elements used to implement R-type instructions.

Register.

ALU.

Registers:



A register is a collection of readable/writeable registers.

- Read Register 1: First source register. 5 bits wide.
- Read Register 2: Second source register. 5 bits wide.
- Write Register: Destination register. 5 bits wide
- Write data: Data to be written to a register. 32 bits wide.

At the bottom, we have the RegWrite input. A writing operation only occurs when this bit is set.

The two outputs:

- Read data1: Contents of source register 1.
- Read data2: Contents of source register 2.

~~ALU~~
ALU:

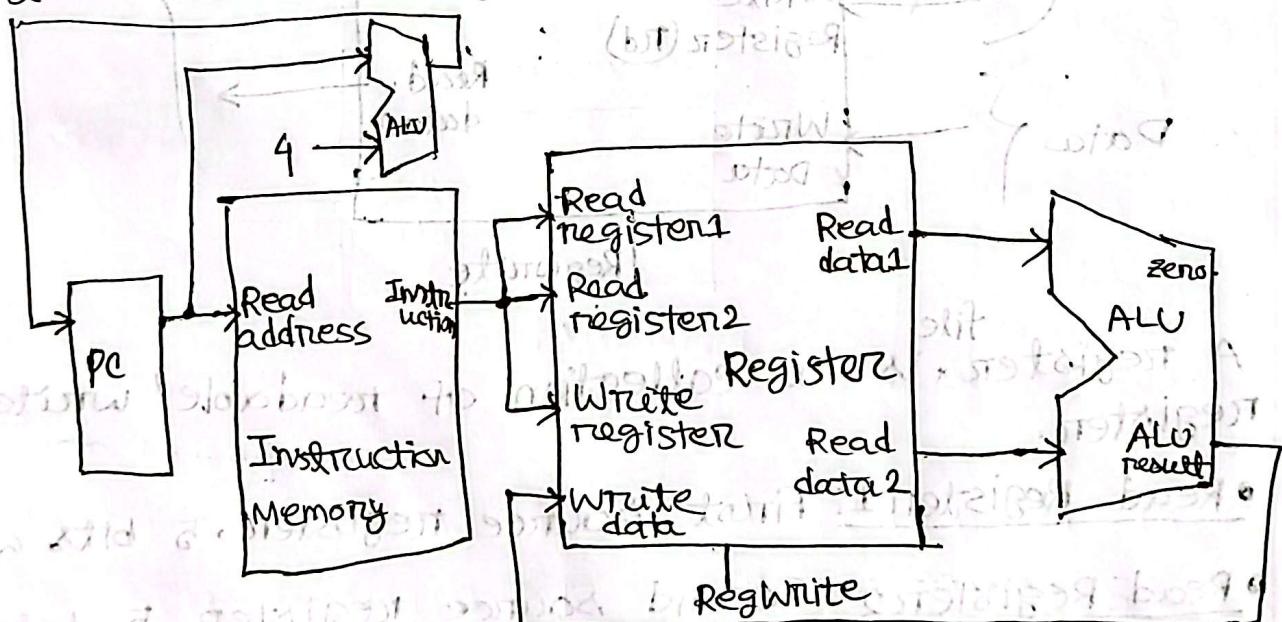
ALU performs the operation indicated by the instruction.

Two inputs and one output.

One special performer and that is "zero".

Subtract if first input is same as second then zero

flag पर value 1 होये याहे, आर एटी indicate करेते वरीच variable same.



1. Grab instruction address from PC
2. Fetch instruction from instruction memory.
3. Decode instruction
4. Pass rs, rt & rd into read register & write register assignments.

5. Retrieve data from read register 1 and read register 2 (rs & rt).
6. Pass contents of rs & rt into the ALU as operands of the operation to be performed.
7. Retrieve result of operation performed by ALU and pass back as the write data argument of the register file (with the RegWrite bit set)
8. Add 4 bytes to the PC value to obtain the word-aligned address of the next instruction.

I-Format Instructions:

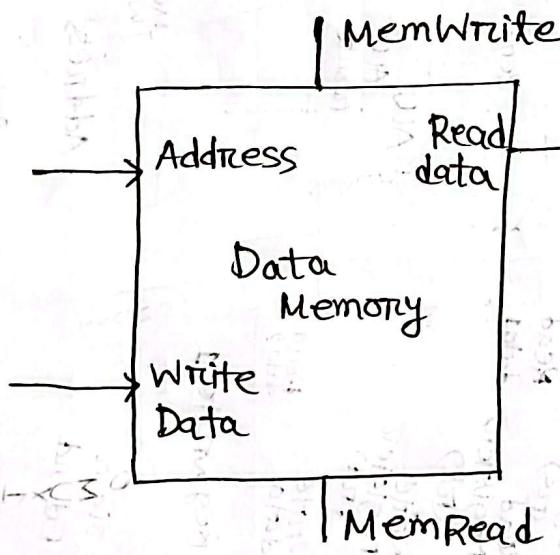
Two component:

1. Data memory unit
2. Sign extension bit

Name	Fields				
Field Size	6 bits	65 bits	5 bits	5 bits	6 bits
I Format	OP	RS	RT	Imm	

Data memory unit

-এটি address কে input হওয়ার হ্যাতে data memory এর data memory unit এ সেই address কে memory তে plot করবে। Address এর value থাকে মাটিকে output করে দেয়। & data.read ও write এর জন্য MemRead এবং MemWrite.



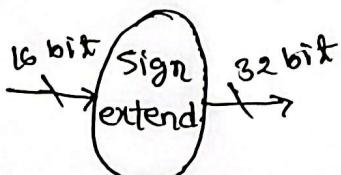
-Two inputs. Address and write data.

-One output.

-Reads & writes are signaled by MemRead and MemWrite respectively.

Sign Extend:

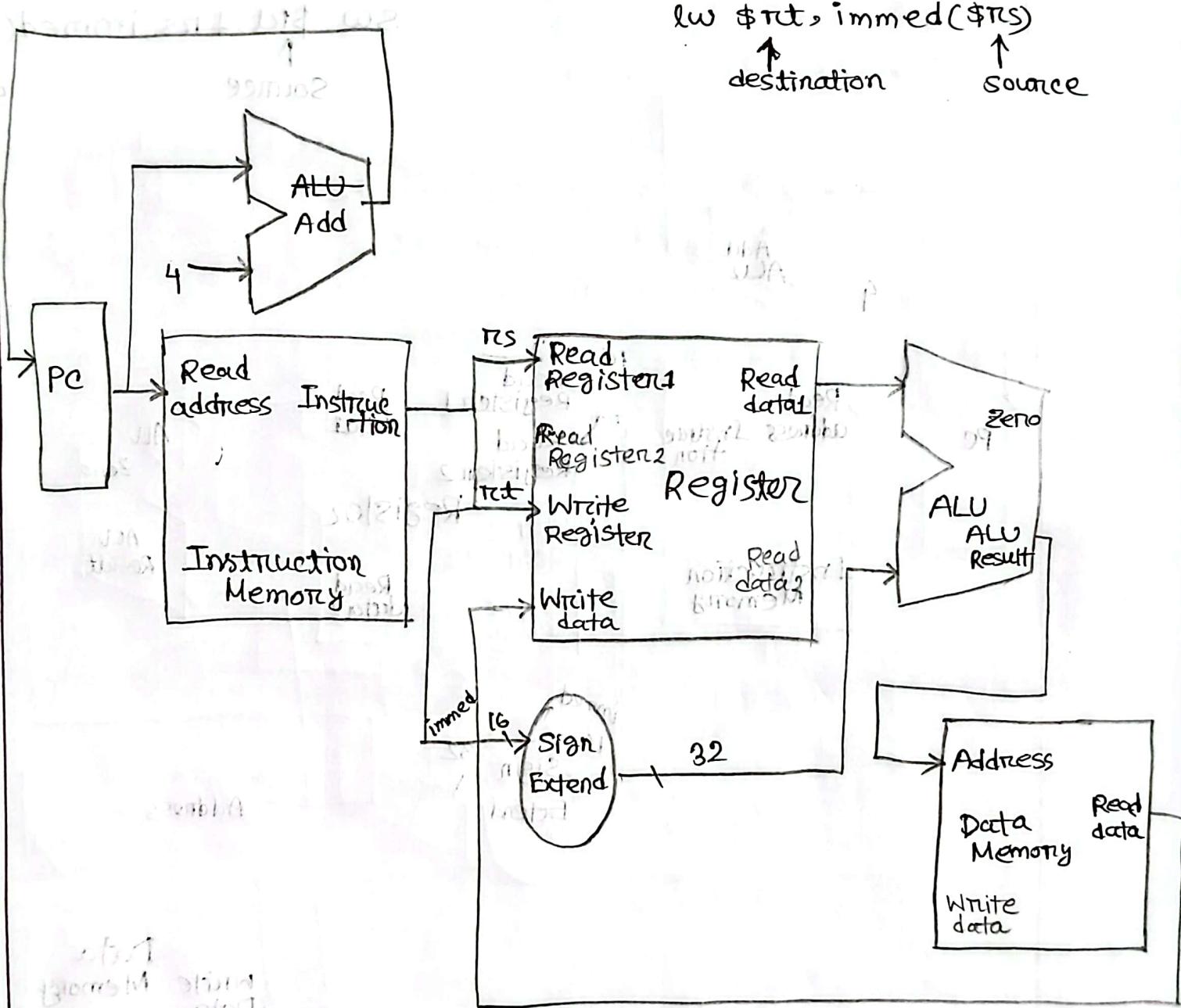
16 bit কে 32 bit এ convert করবে দিবে, যদি 16-bit এর number positive হ্যাতে MSB = 0 হ্যাতে 16-bit এর MSB এ 16-bit 0 দিয়ে 32 bit করব দিব। Same আবে negative এর ক্ষেত্রে 1 দিব।



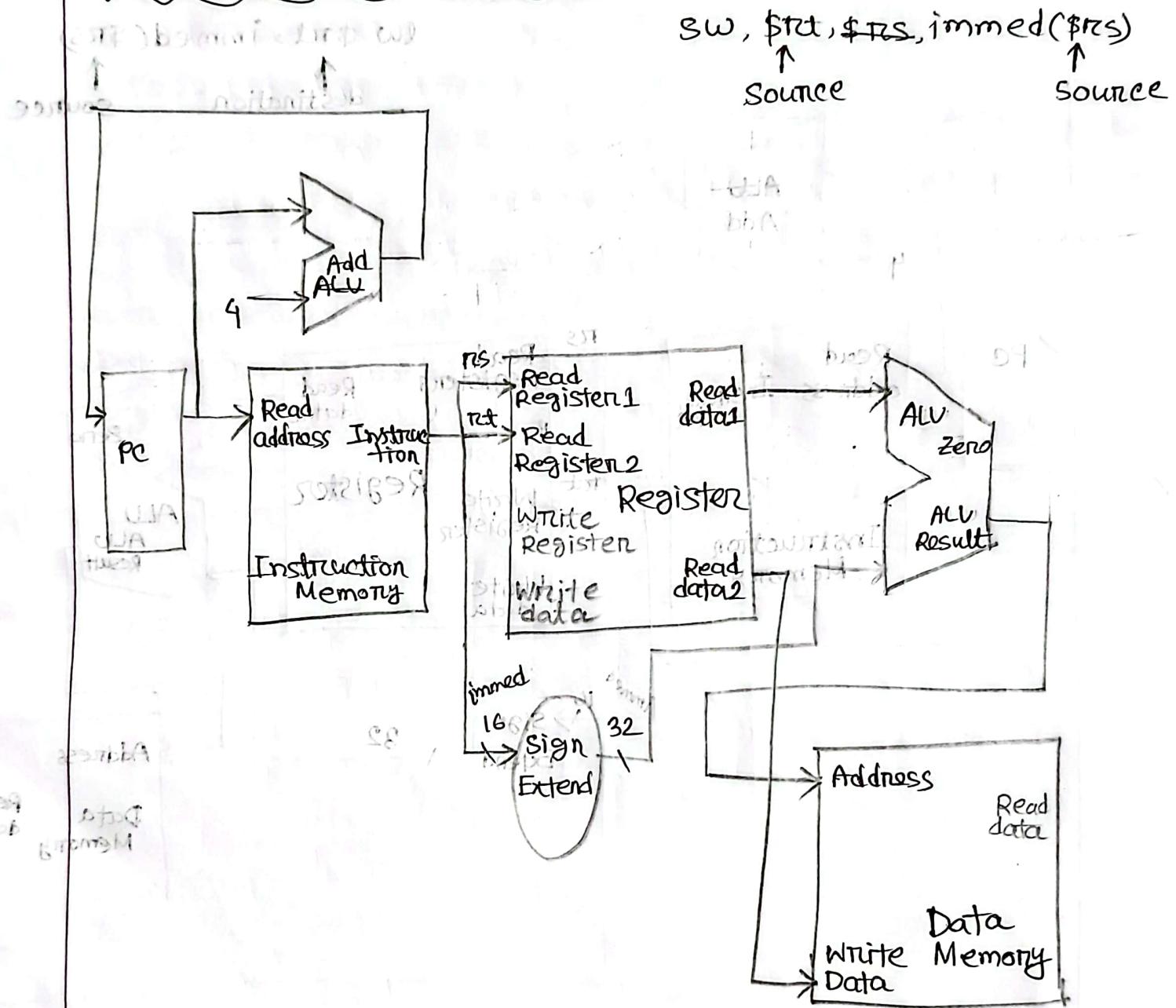
The sign extension element takes as input a 16-bit wide value to be extended to 32-bits.

Datapath for Load Word

lw \$rt, immed(\$rs)
 destination source



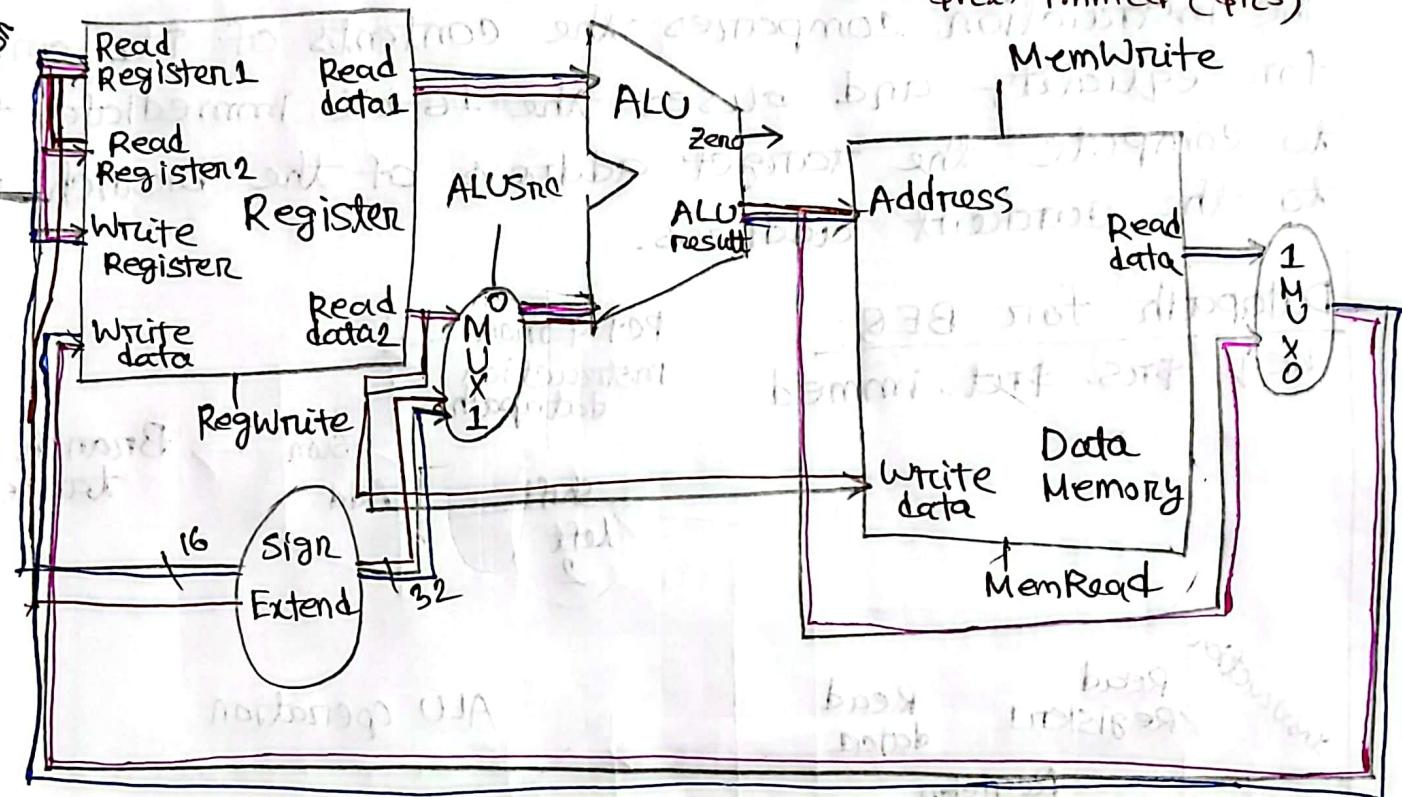
Datapath for Store Word



Datapath for R-format and I-format Memory Access:

add \$rd, \$rs, \$rt
 lw, \$rt, immed (\$rs)
 sw, \$rt, immed (\$rs)

MemWrite



Datapath

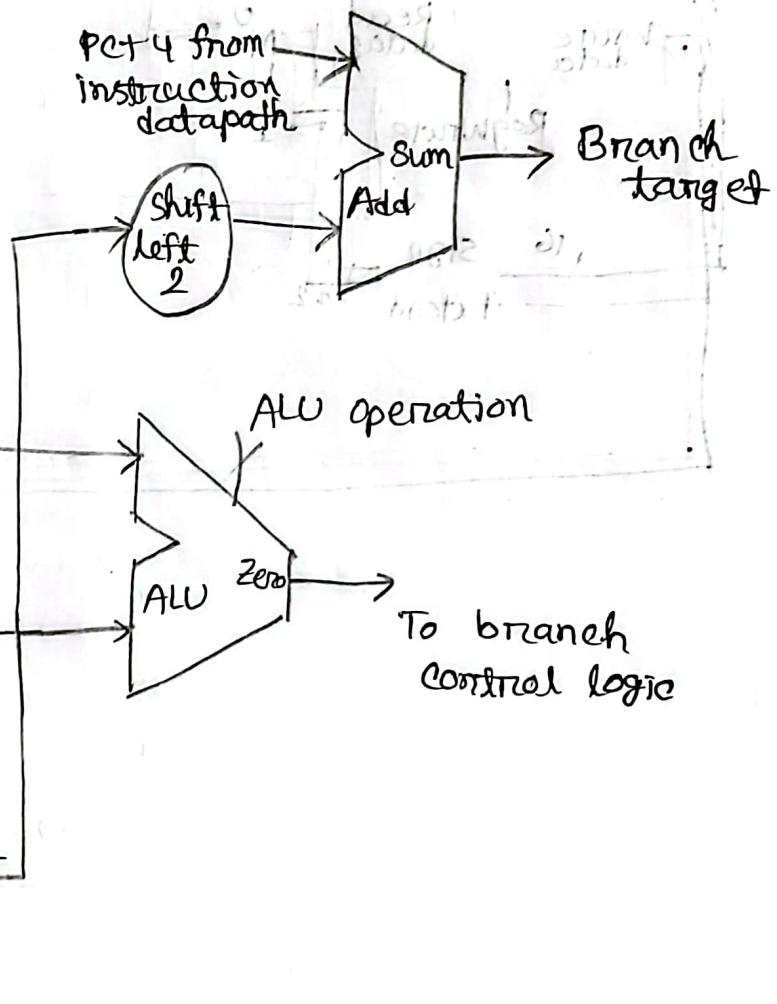
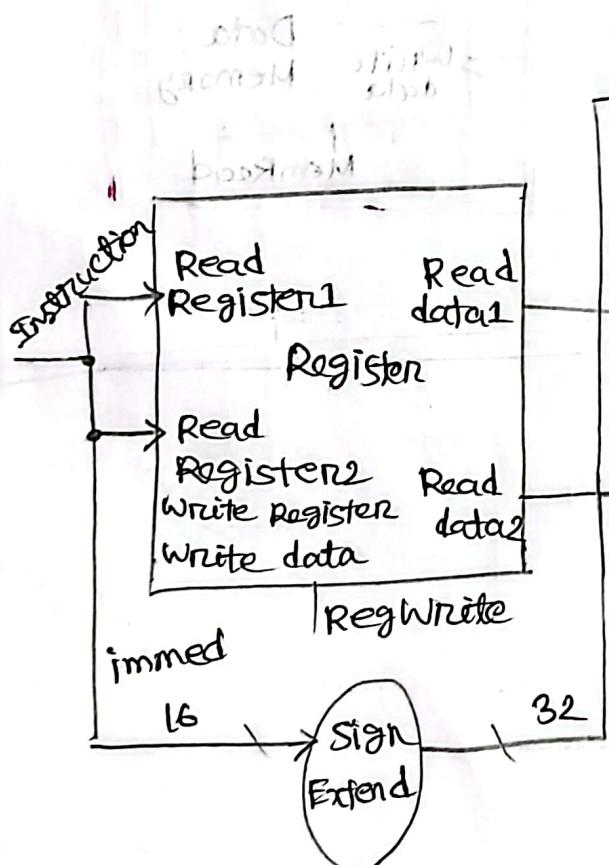
Branching Instructions:

beq \$t1, \$t2, target

The instruction compares the contents of $\$t_1$ and $\$t_2$ for equality and uses the 16-bit immediate field to compute the target address of the branch relative to the current address.

Datapath for BEQ:

beq \$rs, \$rt, immed



Datapath of R-format and I-format

