CPU request the following Block addresses (x+15), (x+25) and (x+12).
There are 16 one-word blocks in cache. Design and Show the memory mapping for the following cache configurations.

I. Direct mapped.

II. 4-way ,8-way and 16- way set associative mapped. (use LRU replacement policy) *
Where X= last two digits of your ID.

For the following configuration Determine the number of bits required for physical address, tag, index and block offset.

i) Consider 32 words cache and 512 words main memory. Block size 4 words. Determine the number of memory blocks and cache lines.
ii) Consider 16 words cache and 64 words main memory. Block size 4 words.
iii) Consider 16 words cache and 128 words main memory. Block size 4 words.
iv) Consider 32 words cache and 1024 words main memory. Block size 4 words.
v) Consider 8 words cache and 32words main memory. Block size 2 words
Also draw the required block for direct mapping cache.

~~Ans~~ Ans# No-01

X = 03

∴ Requested block addresses are 18, 28, 15

Given cache block = 16

(i°) Direct Mapping

Associative	Hit/Miss	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
18	Miss			MEM[18]													
28	Miss													MEM[28]			
15	Miss																MEM[15]

- For 18;

  18 mod 16 → 2 no block

  = 2

- for 28;

  28 mod 16 → 12 no block

  = 12

- For 15

  15 mod 16 → 15 no block

  = 15

(ii)

[ii] 4-way set associative mapping

Block set = $\frac{\text{no of cache block}}{\text{no of way}}$

$= \frac{16}{4}$

$= 4$

		0				1				2				3			
Associative	Hit/Miss	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
18	Miss									MEM[18]							
28	Miss	MEM[28]															
25														MEM[25]			

Here for 18:

18 mod 4 = 2 → 2 no block

∴ Now block of set will be 4

For 28:

28 mod 4 = 0 → 0 no block

For 15:

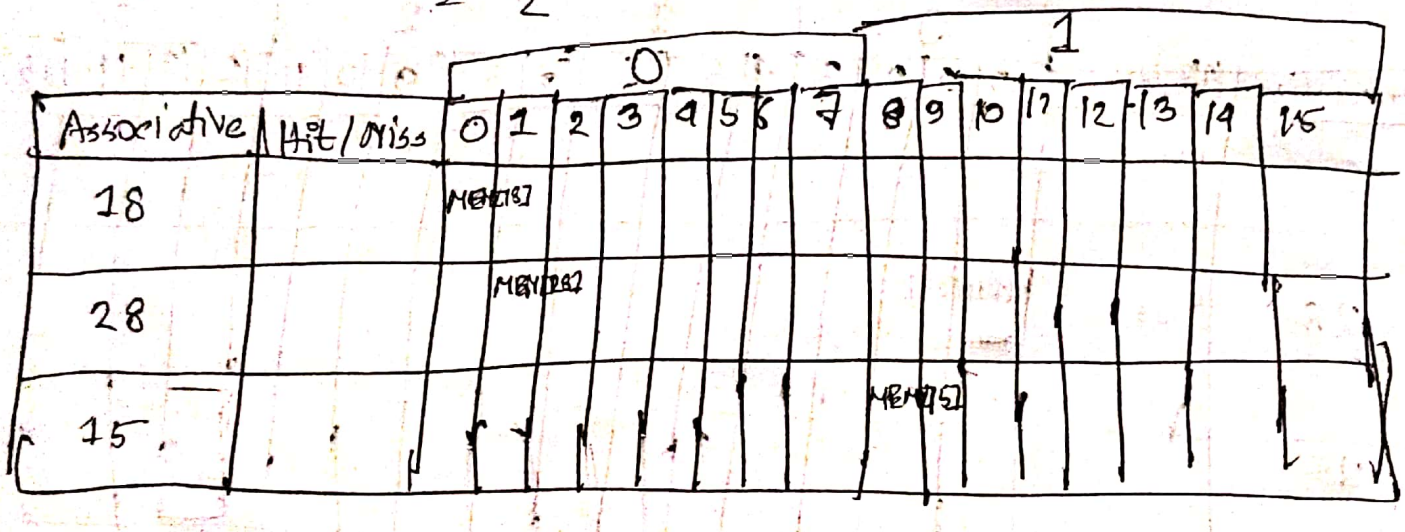
15 mod 4 = 3 → 3 no block

8-way set associative method:

$$\text{Set block} = \frac{\text{No of cache block}}{\text{No of way}}$$

$$= \frac{16}{8}$$

$$= 2$$



For 18:

18 mod 2
= 0 → 0 No block

For 28:

28 mod 2
= 0 → 0 No block

For 15:

15 mod 2
= 1 → 1 No block

16-way set associative mapping:

$$\text{Block of set} = \frac{\text{No of cache block}}{\text{No of way}}$$

$$= \frac{16}{16}$$

$$= 1 \longrightarrow \text{Fully Associative}$$

Associative	Hit/Miss	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
18	Miss	MBN[8]															
28	Miss		MBN[28]														
15	Miss				MBN[15]												

As this is fully associative set mapping, so here we can store value ~~in any sequence~~ in any free spaced ~~box~~ block in any sequence.

Ans. No-02

(i) Cache size - 32 words

Main Memory size = 512 words

Block size = 4 words

So, here cache line will be :→

$$\text{No of cache size} = \frac{32}{4}$$

$$= 8$$

$$= 2^3$$

∴ cache line = 3 bits

Then block offset will be :

$$4$$

$$= 2^2$$

$$= 2 \text{ bits}$$

Next physical address will be :

$$512$$

$$= 2^9$$

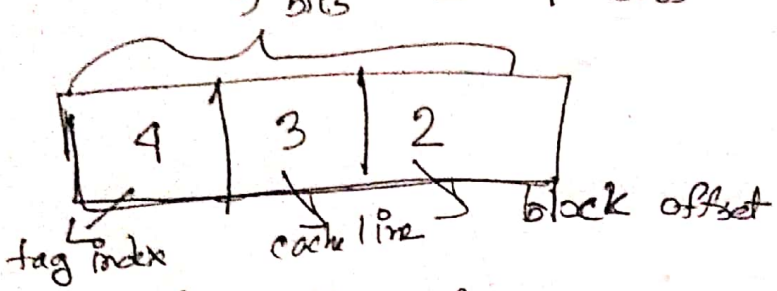
$$= 9 \text{ bits}$$

[∵ Main memory size = 512 words]

∴ Tag size will be: 9 − (3+2) → physical address, cache line, block offset

= 9 − 5

= 4 bits



(ii) Cache size = 16 words

Main Memory size = 64 words

Block size = 4 words

∴ physical address size = 64

= 2^6

= 6 bits

cache line size = $\frac{16}{4}$

= 4

= 2^2

= 2 bits

~~tag index size~~

block offset = 4

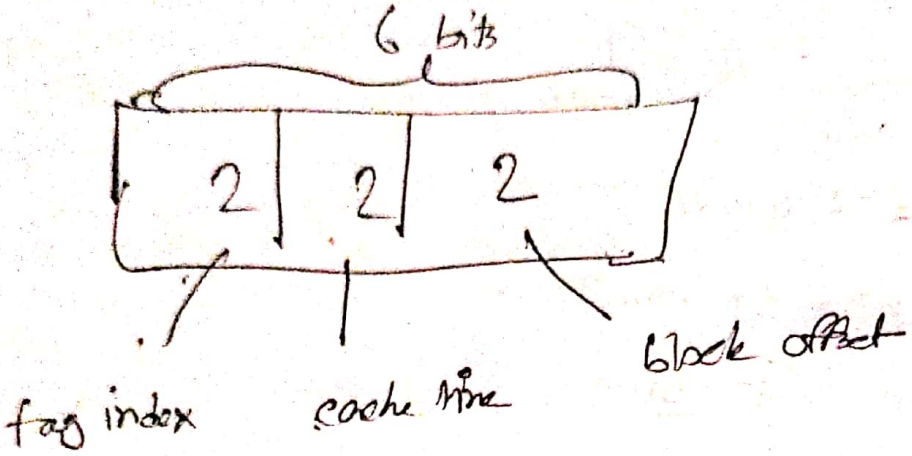
= 2^2

= 2 bits

∴ Tag index size = 6 − (2+2)

= 6 − 4

= 2



(iii) Cache size − 16 words

M. Memory size − 128 words

block size − 4 words

∴ physical address size = 128

= 27

= 7 bits

block offset = 4

= 2^2

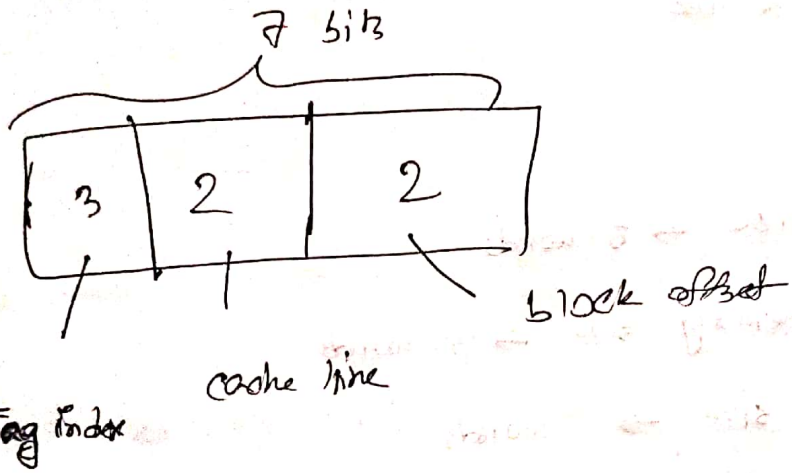
= 2 bits

cache line = $\frac{16}{4}$ = 4 = 2^2 = 2 bits

f. Tag index size = 7 - (2+2)

= 7 - 4

= 3 bits



(iv) Cache size → 32 words

M. Memory size → 1024 words

block size → 4 words.

Physical address size = 1024

= 2^{10}

= 10 bits

block offset = 4

= 2^2

= 2 bits

cache line size

= 32/4

= 8

= 2^3

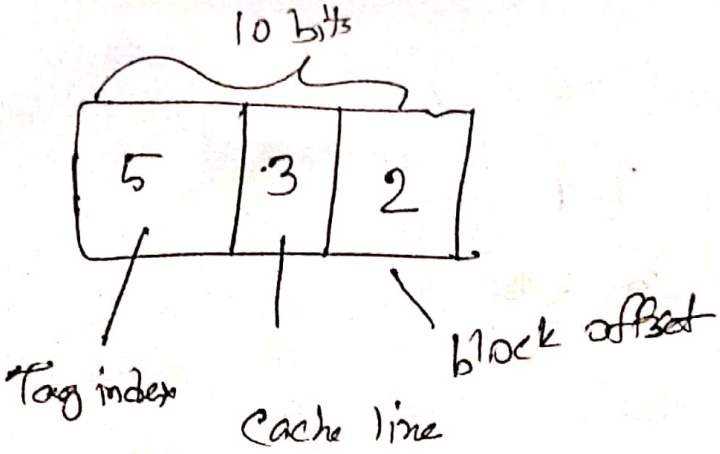
= 3 bits

∴ Tag index size

= 10 - (3+2)

= 10 - 5

= 5 bits



(V) Cache size → 8 words

Main memory size → 32 words

block size → 2 words

∴ Physical address size = 32

= 25

= 5 bits

block size = 2^1

= 1 bit

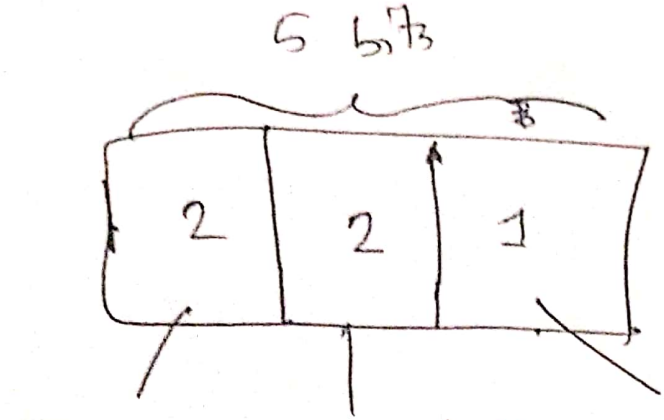
cache line size → 8/2

= 4

= 2^2

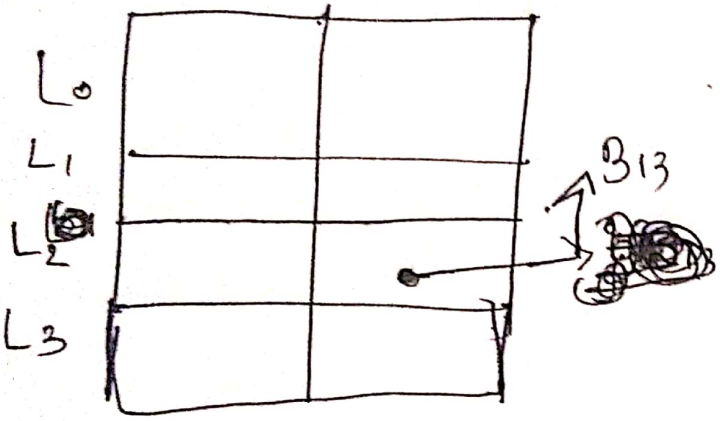
= 2 bits

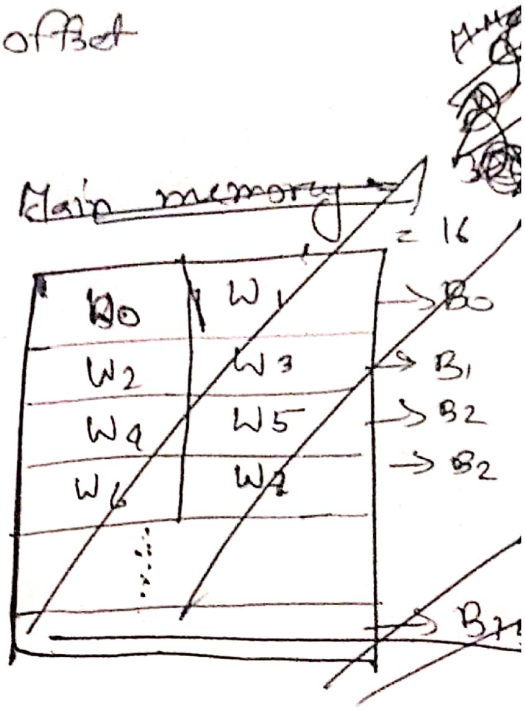
= 2 bits



Cache line size = 8/2 = 4

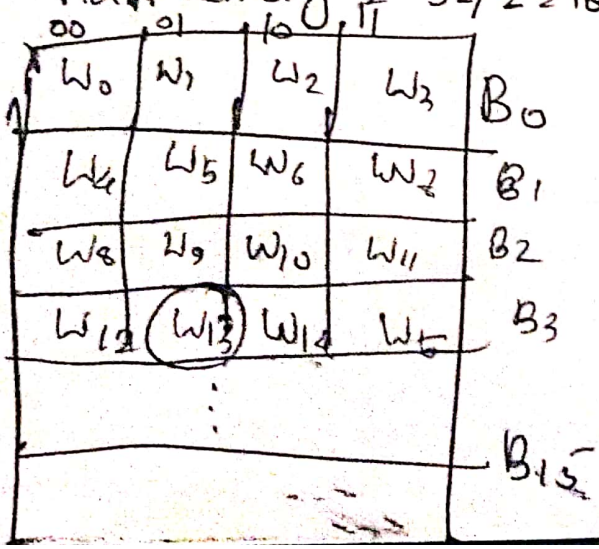
cache size
block size





Let assume requested address is 13

Main memory = 32/2 = 16



13 → Binary