Department of Computer Science & Engineering
University of Asia Pacific (UAP)

Final Examination **Spring 2022** **2nd Year 2nd Semester**

Course Code: CSE 209 **Course Title: Digital Logic & System Design** **Credits: 4**

Full Marks: 150 **Duration: 3 Hours**

Instructions:

1. There are **Six (6)** Questions. Answer all of them. All questions are of equal value. Part marks are shown in the margins.
2. Non-programmable calculators are allowed.

1. a) Discuss the universality of NOR gate. 06

b) Implement the following Boolean function with only NOR gate

$$Y = \overline{A}\,B + A\,\overline{B}\,C$$ 07

c) Implement the following function using K-map.

$$F(A, B, C, D) = \sum(0, 1, 2, 5, 6, 7, 8, 10, 12, 13, 14, 15)$$ 12

2. a) Design MOD 12 Johnson counter using JK flip-flop and describe its operation. 10

b) Design a BCD adder using IC # 7483 (4-bit parallel adder) and NOR gates only. Briefly describe its operation. 15

3. Design a synchronous counter that will count in this fashion: 25

$$000 \rightarrow 001 \rightarrow 011 \rightarrow 110 \rightarrow 111$$

4. a) Write down the instruction set and the corresponding op-code of SAP-1 Computer. 05

b) How many operations are possible in SAP-1 Computer? Explain your answer. 05

c) Create a SAP-1 assembly language program and then generate the machine code for the following expression 35 - 24 + 32 – 53 - 7. These numbers are in decimal form. 15

5. a) Draw the block diagram of 4 bit ALU chip (IC # 74382). Describe 8(Eight) operations of the 4 bit ALU chip that perform by select inputs. 10

b) Write down the truth tables of half adder and full adder. Design half adder and full adder using K-map or otherwise. 07

c) Briefly describe the operation of IC # 7483(4-bit parallel adder). Design a 4-bit parallel Adder/Subtractor using IC # 7483 and basic gates if necessary. Briefly describe its operation. 08

OR

a) Draw the circuit diagram of MOD-13 synchronous up counter using JK flip-flops and briefly describe its operation. 10

b) Design MOD 80 counter using IC # 74293. 07

c) Design MOD 5 Ring counter using JK flip flop and describe its operation. 08

6. a) Draw the internal circuit of IC # 74138(Decoder). Briefly describe its operation. 10

b) Show that IC # 74138(Decoder) can be used as the 1of 8 Demultiplexer. 05

c) Design 4 lines to 16 lines decoder using IC# 74138. You can use other logic gates if necessary. 10

OR

a) Draw the internal circuit of IC # 74151(Multiplexer). Briefly describe its operation. 10

b) Show how IC # 74151 can be used to generate the logic function Z = AB + BC + CA. 05

c) Implement the function F (A, B, C, D) = $\sum(0, 2, 4, 6, 8, 10, 13, 15)$ using only an IC # 74151(Multiplexer) and NOR gate. 10

Department of Computer Science & Engineering
University of Asia Pacific (UAP)

Final Examination **Fall 2021** **2nd Year 2nd Semester**

Course Code: CSE 209 **Course Title: Digital Logic & System Design** **Credits: 4**

Full Marks: 150 **Duration: 3 Hours**

Instructions:

1. There are Six (6) Questions. Answer all of them. All questions are of equal value. Part marks are shown in the margins.
2. Non-programmable calculators are allowed.

1. a) Discuss the universality of NAND gate. 06

b) Implement the following Boolean function with only NAND gate

$y = A\overline{B} + \overline{A}\,B\,\overline{C}$ 07

c) Implement the following function using K-map.

$F(A, B, C, D) = \sum(0, 1, 2, 3, 6, 7, 8, 10, 11, 13, 14, 15)$ 12

2. a) Draw the internal circuit diagram of clocked JK flip-flop and briefly describe its operation. 10

b) Design D flip-flop from J-K flip-flop. 03

c) Design a logic circuits that controls the passage of a signal A according to the following requirements:

(i) Output X will equal A when inputs B and C are the same.

(ii) Output X will remain HIGH when B and C are different. 07

d) Write down the sum-of-products expression for a circuit with four inputs (A, B, C & D) and an output (Y) that is to be HIGH only when input A is HIGH at the same time at least two other inputs are LOW. 05

3. Design a synchronous counter that will count in this fashion: 25

$000 \rightarrow 010 \rightarrow 100 \rightarrow 110 \rightarrow 111$

4. a) Write down the instruction set and the corresponding op-code of SAP-1 Computer. 05

b) How many operations are possible in SAP-1 Computer? Explain your answer. 05

c) Create a SAP-1 assembly language program and then generate the machine code for the expression of 37 - 23 + 32 – 58 +8. These numbers are in decimal form. 15

5. a) Draw the block diagram of 4 bit ALU chip (IC # 74382). Describe 8(Eight) operations of the 4 bit ALU chip that perform by select inputs. 10

b) Write down the truth tables of half adder and full adder. Design half adder and full adder using K-map or otherwise. 07

c) Briefly describe the operation of IC # 7483(4-bit parallel adder). Design a 4-bit parallel Adder/Subtractor using IC # 7483 and basic gates if necessary. Briefly describe its operation. 08

OR

a) Draw the circuit diagram of MOD-10 synchronous up counter using JK flip-flops and briefly describe its operation. 10

b) Design MOD 60 counter using IC # 74293. 07

c) Design MOD 6 Ring counter using JK flip flop and describe its operation. 08

6. a) Draw the internal circuit of IC # 74138(Decoder). Briefly describe its operation. 10

b) Show that IC # 74138(Decoder) can be used as the 1of 8 Demultiplexer. 05

c) Design 5 lines to 32 lines decoder using IC# 74138. You can use other logic gates or IC if necessary. 10

OR

a) Draw the internal circuit of IC # 74151(Multiplexer). Briefly describe its operation. 10

b) Show how IC # 74151 can be used to generate the logic function Z = AB + BC + CA. 05

c) Implement the function F (A, B, C, D) = $\Sigma(1, 2, 4, 7, 11, 12, 13, 15)$ using an IC # 74151(Multiplexer) and basic gates if necessary. 10

Department of Computer Science & Engineering

University of Asia Pacific (UAP)

Program: B.Sc. in Computer Science and Engineering

Final Examination	**Spring 2021**	**2nd Year 2nd Semester**
Course Code: CSE 209	**Course Title: Digital Logic & System Design**	**Credits: 4**
Full Marks: 120* (Written)		**Duration: 2 Hours**

* Total Marks of Final Examination: 150 (Written: 120 + Viva: 30)

Instructions:

1. There are **Four (4)** Questions. Answer all of them. All questions are of equal value. Part marks are shown in the margins.
2. Non-programmable calculators are allowed.

1. **a)** What are the difference between arithmetic and logical operation? What types of operation are possible in SAP-1 Computer? 04

b) Write down the instruction set and the corresponding op-code of SAP-1 Computer. 05

c) How many operations are possible in SAP-1 computer? Explain your answer. 05

d) Create a SAP-1 assembly language program and then generate the machine code for the expression of 27 - 22 + 37 – 54 + 9. These numbers are in decimal form. 16

2. **a)** Design a synchronous counter using J-K FFs that has the following sequence: 000, 010, 100, 101, 111 and repeat. The undesired (unused) states 001, 011, and 110 must always go to 000 on the next clock pulse. 20

b) A photo detector circuit is being used to generate a pulse each time a customer walks into a certain establishment. The pulses are fed to a seven-bit counter. The counter is used to count these pulses as a means for determining how many customers have entered the store. After closing the store, the proprietor checks the counter and finds that it shows a count of $0011100_2=28_{10}$. He knows that this is incorrect because there were many more than twenty eight people in his store. Assuming that the counter circuit is working properly. 05

(i) What could be the reason for the discrepancy?

(ii) How can you overcome from the discrepancy?

c) Consider a counter circuit that contains ten JK flip-flops wired in the arrangement of 05

$Q_9Q_8Q_7Q_6Q_5Q_4Q_3Q_2Q_1Q_0$.

(i) Determine the counter's MOD number.

(ii) Determine the output frequency in KHz when the input clock frequency is 16 MHz.

(iii) What is the range of counting states for this counter?

(iv) Assume a starting state (count) of 0000100111. What will be the counter's state after 2050 pulses?

3. **a)** Implement the function F(A, B, C, D) = ∑(0, 2, 3, 6, 8, 9, 11, 13) using only one IC# 74151(Multiplexer) and one NOR gate. 12

b) Show how IC# 74151 can be used to generate the logic function Z = AB + BC + CA. 08

c) For each item, indicate whether it is referring to a Decoder, a MUX, or a DEMUX. 06

(i) Has more inputs than outputs.

(ii) Uses SELECT inputs.

(iii) Can be used in parallel-to-serial conversion.

(iv) Only one of its outputs can be active at one time.

(v) Can be used to route an input signal to one of several possible outputs.

(vi) Can be used to generate arbitrary logic functions.

d) For IC# 74138 (Decoder), what input conditions will produce the following outputs: 04
(i) LOW at O_7
(ii) LOW at O_5
(iii) LOW at O_0
(iv) All outputs are HIGH.

4. **a)** Design a logic circuit that follows the following requirements: 10

(i) Output X will be logical equivalent to (C EX-OR D) when A and B are different.

(ii) X will remain HIGH when A and B are the same.

b) Design MOD 12 Johnson counter using JK flip-flop and describe its operation. 10

c) Draw the block diagram of 4 bit ALU chip (IC# 74382) and label the all inputs & outputs. Describe 8(Eight) operations of the 4 bit ALU chip that perform by select input. 10

OR

a) Implement the following function using K-map. 10

F (A, B, C, D) = ∑(0, 1, 2, 3, 7, 8, 9, 10, 13, 14, 15)

b) Draw the internal circuit of IC# 74293(Counter). Design MOD 700 counter using IC# 74293. 10

c) Describe the basic operation of IC# 7483(4-bit parallel adder). Using this draw a 4-bit parallel adder/subtractor. You can use other logic gates if necessary. Briefly describe the operation of your diagram. 10

Department of Computer Science & Engineering

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Program: B.Sc. in Computer Science and Engineering

Final Examination	**Fall 2020**	**2nd Year 2nd Semester**
Course Code: CSE 209	**Course Title: Digital Logic & System Design**	**Credits: 4**
Full Marks: 120* (Written)		**Duration: 2 Hours**

* Total Marks of Final Examination: 150 (Written: 120 + Viva: 30)

Instructions:

1. There are **Four (4)** Questions. Answer all of them. All questions are of equal value. Part marks are shown in the margins.
2. Non-programmable calculators are allowed.

1. a) Implement the following function using K-map.

$$F(A, B, C, D) = \sum(0, 1, 2, 5, 7, 9, 10, 12, 13, 14, 15)$$ 10

b) Design a logic circuit that follows the following requirements:
(i) Output X will be logical equivalent to (A AND D) when B and C are different. 10
(ii) X will remain HIGH when B and C are the same.

c) Draw the block diagram of 4 bit ALU chip (IC# 74382) and label the all inputs & outputs. Describe 8(Eight) operations of the 4 bit ALU chip that perform by select input. 10

OR

a) Draw the block diagram of IC# 74293(Counter). Using this implement MOD 700 counter. 10

b) Design MOD 12 Johnson counter using JK flip-flop and describe its operation. 10

c) Design a BCD adder using IC # 7483 (4-bit parallel adder) and NAND gates only. Briefly describe its operation. 10

2. a) What are the difference between arithmetic and logical operation? What types of operation are possible in SAP-1 Computer? 4

b) Write down the instruction set and the corresponding op-code of SAP-1 Computer. 5

c) How many operations are possible in SAP-1 computer? Explain your answer. 5

d) Create a SAP-1 assembly language program and then generate the machine code for the expression of 52 + 28 - 38 + 72 - 12. These numbers are in decimal form. 16

3. **a)** Design a synchronous counter using J-K FFs that has the following sequence: 000, 010, 100, 110, 111 and repeat. The undesired (unused) states 001, 011 and 101 must always go to 000 on the next clock pulse. 20

b) i) What are the values of J and K so that the J-K flip-flop can operate as a toggle FF (changes states on each clock pulse)? Then apply a 10-kHz clock signal to its CLK input and determine the frequency of the waveform at Q (output of J-K flip-flop). 05

ii) Connect Q from this FF to the CLK input of a second J-K FF that also has same value of J and K of the first FF. Determine the frequency of the signal at this FF's output.

c) Consider a counter circuit that contains five FFs wired in the arrangement Q_4, Q_3, Q_2, Q_1, Q_0. 05

i) Determine the counter's MOD number.

ii) Determine the output frequency in Hz when the input clock frequency is 10-kHz.

iii) What is the range of counting states for this counter?

iv) Assume a starting state (count) of 01011. What will be the counter's state after 243 pulses?

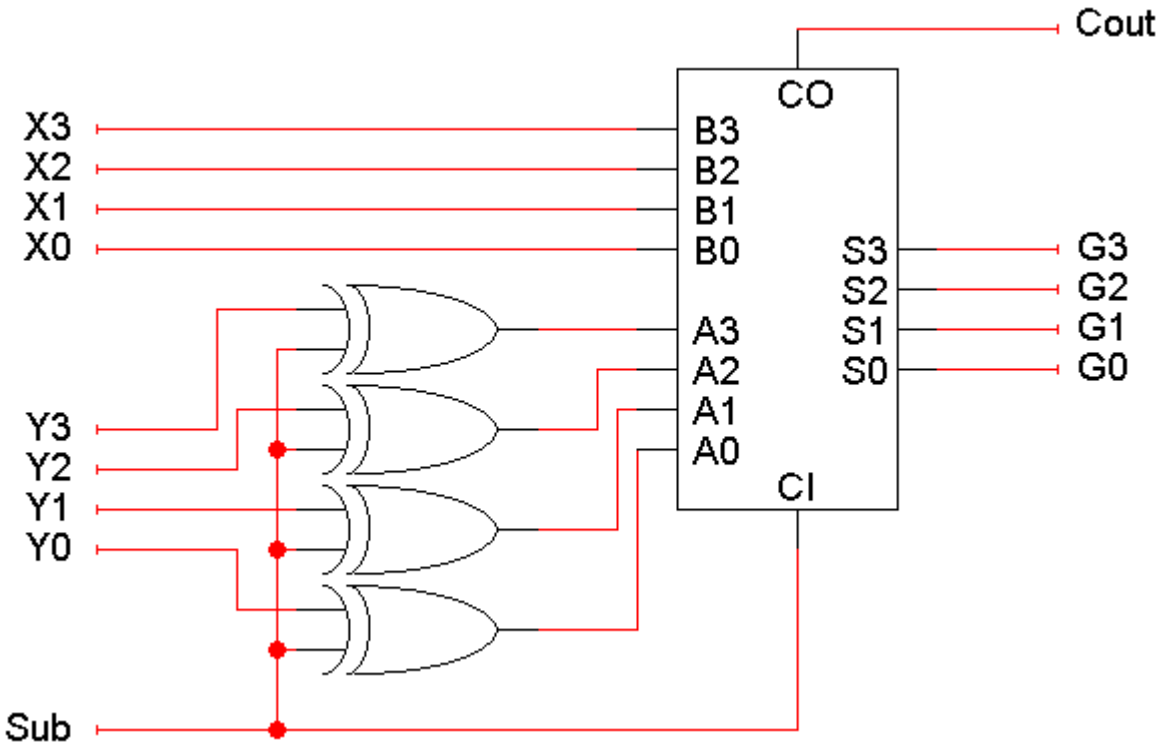
4. **a)** Implement the function F(A, B, C, D) = ∑(0, 1, 2, 5, 7, 8, 10, 12, 14, 15) using only one IC# 74151(Multiplexer). You can use other universal logic gate, if necessary. 12

b) Show how IC# 74151 can be used to generate the logic function y = AC` + A`B + B`C. 08

c) In the figure below, the signal Sub and some XOR gates alter the 4-bit parallel adder (IC # 7483) inputs. 10

i) Describe the operation of the circuit when Sub = 1.

ii) Describe the operation of the circuit when Sub = 0.



Department of Computer Science & Engineering

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Program: B.Sc. in Computer Science and Engineering

Final Examination	**Spring 2020**	**2nd Year 2nd Semester**
Course Code: CSE 209	**Course Title: Digital Logic & System Design**	**Credits: 4**
Full Marks: 120* (Written)		**Duration: 2 Hours**

* Total Marks of Final Examination: 150 (Written: 120 + Viva: 30)

Instructions:

1. There are **Four (4)** Questions. Answer all of them. All questions are of equal value. Part marks are shown in the margins.
2. Non-programmable calculators are allowed.

1. **a)** What are the difference between arithmetic and logical operation? What types of operation are possible in SAP-1 Computer? 04

b) Write down the instruction set and the corresponding op-code of SAP-1 Computer. 05

c) How many operations are possible in SAP-1 computer? Explain your answer. 05

d) Create a SAP-1 assembly language program and then generate the machine code for the expression of 18 - 20 + 35 – 52 + 8. These numbers are in decimal form. 16

2. **a)** Design a synchronous counter using J-K FFs that has the following sequence: 000, 010, 101, 110, and repeat. The undesired (unused) states 001, 011, 100, and 111 must always go to 000 on the next clock pulse. 20

b) A photo detector circuit is being used to generate a pulse each time a customer walks into a certain establishment. The pulses are fed to a seven-bit counter. The counter is used to count these pulses as a means for determining how many customers have entered the store. After closing the store, the proprietor checks the counter and finds that it shows a count of $0001100_2=12_{10}$. He knows that this is incorrect because there were many more than twelve people in his store. Assuming that the counter circuit is working properly. 05

(i) What could be the reason for the discrepancy?

(ii) How can you overcome from the discrepancy?

c) Consider a counter circuit that contains eight JK flip-flops wired in the arrangement of 05

$Q_7Q_6Q_5Q_4Q_3Q_2Q_1Q_0$.

(i) Determine the counter's MOD number.

(ii) Determine the output frequency in KHz when the input clock frequency is 8 MHz.

(iii) What is the range of counting states for this counter?

(iv) Assume a starting state (count) of 00100111. What will be the counter's state after 1325 pulses?

3. **a)** Implement the function F(A, B, C, D) = $\sum(0, 1, 2, 6, 7, 11, 12, 14, 15)$ using only one IC# 74151(Multiplexer). You can use other logic gates, if necessary. 12

b) Show how IC# 74151 can be used to generate the logic function Z = AB + BC + CA. 08

c) For each item, indicate whether it is referring to a decoder, a MUX, or a DEMUX. 06

(i) Has more inputs than outputs.

(ii) Uses SELECT inputs.

(iii) Can be used in parallel-to-serial conversion.

(iv) Only one of its outputs can be active at one time.

(v) Can be used to route an input signal to one of several possible outputs.

(vi) Can be used to generate arbitrary logic functions.

d) For IC# 74138 (Decoder), what input conditions will produce the following outputs: 04
(i) LOW at O_6
(ii) LOW at O_4
(iii) LOW at O2
(iv) All outputs are HIGH.

4. **a)** Implement the following function using K-map. 10

$$F(A, B, C, D) = \sum(0, 1, 2, 3, 7, 8, 10, 11, 13, 14, 15)$$

b) Design a logic circuit that follows the following requirements: 10

(i) Output X will be logical equivalent to (C AND D) when A and B are the same.

(ii) X will remain HIGH when A and B are different.

c) Draw the block diagram of 4 bit ALU chip (IC# 74382) and label the all inputs & outputs. Describe 8(Eight) operations of the 4 bit ALU chip that perform by select input. 10

OR

a) Draw the block diagram of IC# 74293(Counter). Using this implement MOD 500 counter. 10

b) Design MOD 12 Johnson counter using JK flip-flop and describe its operation. 10

c) Describe the basic operation of IC# 7483(4-bit parallel adder). Using this draw a 4-bit parallel adder/subtractor. You can use other logic gates if necessary. Briefly describe the operation of your diagram. 10

Department of Computer Science & Engineering
University of Asia Pacific (UAP)

Final Examination Fall 2019 2nd Year 2nd Semester

Course Code: CSE 209 **Course Title: Digital Logic & System Design** **Credits: 4**

Full Marks: 150 **Duration: 3 Hours**

Instructions:

1. There are **Six (6)** Questions. Answer all of them. All questions are of equal value. Part marks are shown in the margins.
2. Non-programmable calculators are allowed.

1. a) Discuss the universality of NOR gate. 06

   b) Implement the following Boolean function with only NOR gate

   $y = A\overline{B} + \overline{A}B\overline{C}$ 07

   c) Implement the following function using K-map.

   $F(A, B, C, D) = \sum(0, 1, 2, 3, 6, 7, 8, 10, 11, 13, 14, 15)$ 12

2. a) Draw the internal circuit diagram of clocked JK flip-flop and briefly describe its operation. 10

   b) Design D flip-flop from J-K flip-flop. 03

   c) Design a logic circuits that controls the passage of a signal A according to the following requirements:

   (i) Output X will equal A when inputs B and C are the same.

   (ii) Output X will remain HIGH when B and C are different. 07

   d) Write down the sum-of-products expression for a circuit with four inputs (A, B, C & D) and an output (Y) that is to be HIGH only when input A is HIGH at the same time at least two other inputs are LOW. 05

3. Design a synchronous counter that will count in this fashion: 25

   $000 \rightarrow 010 \rightarrow 011 \rightarrow 110 \rightarrow 111$

4. a) Write down the op-code of each Mnemonics of SAP-1 computer. 05

   b) Draw the architecture of SAP-1 computer. Explain the working procedure of Program Counter (PC). 10

   c) Write down both assembly and machine code according to the arithmetic operation basis on SAP-1 computer for the expression of 2+9+8-3-7. 10

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5. a) Draw the block diagram of 4 bit ALU chip (IC # 74382). Describe 8(Eight) operations of the 4 bit ALU chip that perform by select inputs. 10

b) Write down the truth tables of half adder and full adder. Design half adder and full adder using K-map or otherwise. 07

c) Briefly describe the operation of IC # 7483(4-bit parallel adder). Design a 4-bit parallel Adder/Subtractor using IC # 7483 and basic gates if necessary. Briefly describe its operation. 08

OR

a) Draw the circuit diagram of MOD-10 synchronous up counter using JK flip-flops and briefly describe its operation. 10

b) Design MOD 60 counter using IC # 74293. 07

c) Design MOD 10 Johnson counter sing JK flip flop and describe its operation. 08

6. a) Draw the internal circuit of IC # 74138(Decoder). Briefly describe its operation. 10

b) Show that IC # 74138 can be used as a 1 line to 8 lines Demultiplexer. 05

c) Design 5 lines to 32 lines decoder using IC# 74138. You can use other logic gates or IC if necessary. 10

OR

a) Draw the internal circuit of IC # 74151(Multiplexer). Briefly describe its operation. 10

b) Show how IC # 74151 can be used to generate the logic function $Z = AB + BC + CA$. 05

c) Implement the function $F(A, B, C, D) = \sum(0, 1, 2, 4, 7, 11, 12, 13, 15)$ using an IC # 74151(Multiplexer) and basic gates if necessary. 10