

DLSD : Digital Logic and system design (i)

CSE 209 : credit - 04

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why dlsd?

ALU → Arithmetic and logic units.

Book:

1. Digital Systems by Ronald J. Tocci ** Reference Book.



Chapter - 3, 4, 5, 6, 7, 9

No question from chapter 1 & 2, but read yourself.

Chapter : 3 (Logic gates and boolean algebra)

Logic Gates:

(i) AND gate:

(ii) OR gate:

(iii) NOT gate:

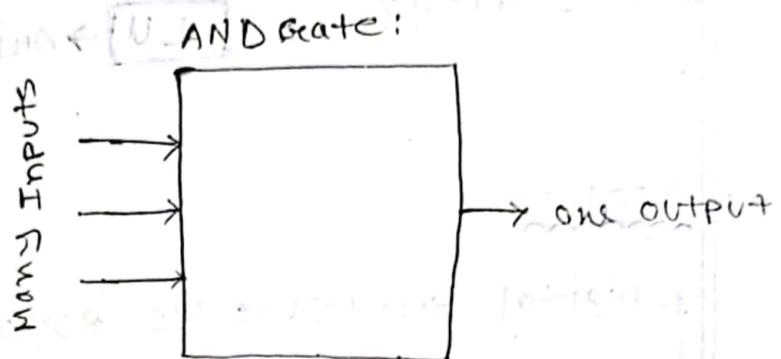
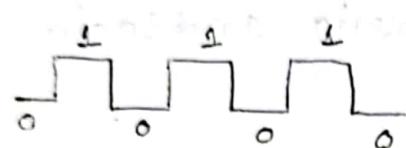
} basic logic gate because

} we can draw all other circuits using these gates.

(i) AND gate: (conjunction):

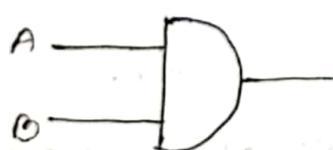
T \rightarrow 1 or (High) \rightarrow 5V

F \rightarrow 0 or (low) \rightarrow 0V



- ④ AND gate is a device where there are many inputs and one output. and outputs will be high, only when all the inputs are high, otherwise output will be low.

Symbol:

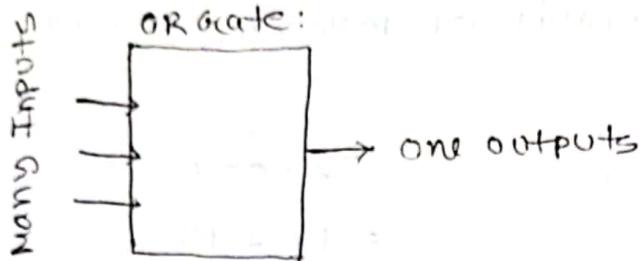


$$Y = A \cdot B$$

Truth Table:

A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

(ii) OR gate : (Disjunction):



- * OR gate is a device where output will be low only when all the inputs are low. otherwise output will be high.

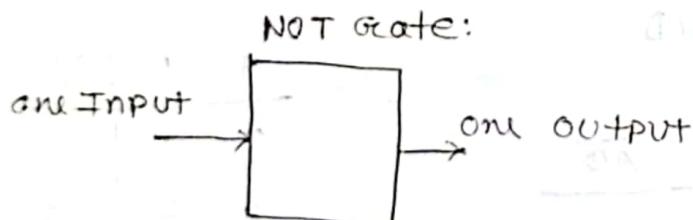
Symbol:



Truth Table:

A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

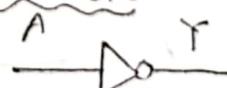
(iii) NOT gate : (Negation):



Truth Table:

A	Y
0	1
1	0

Symbol:



$$Y = \bar{A}$$

- * Output is opposite of input.

- * one input, one output.

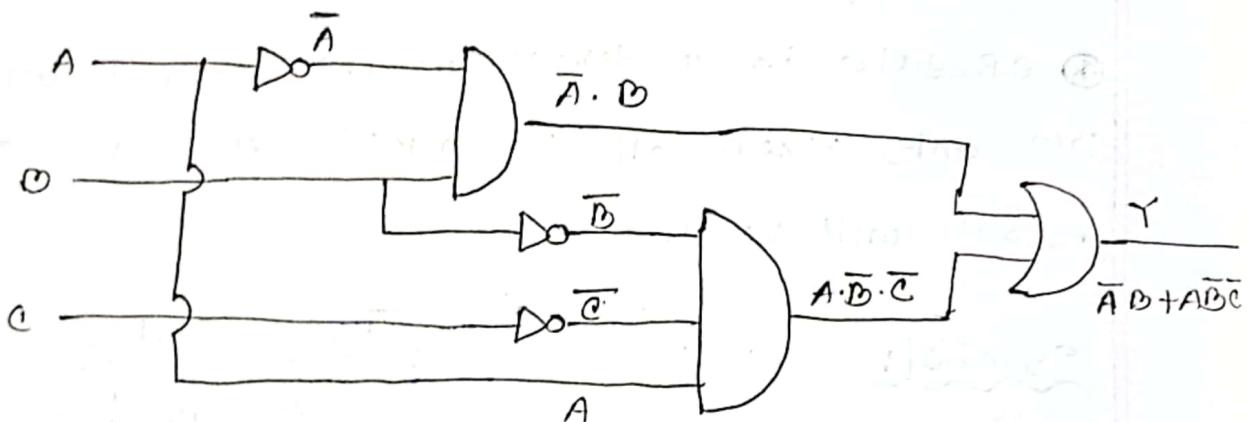
Q) Basic Logic Gate:

* Draw the logic circuit of following logic expression:

$$Y = \bar{A}B + A\bar{B}\bar{C}$$

TK 20x7.

= TK 440

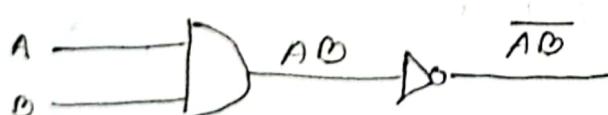


** Boolean Algebra.

Q) Compound Logic Gates:

NAND Gate:

$$\text{NOT} + \text{AND} \Rightarrow \text{NAND}$$

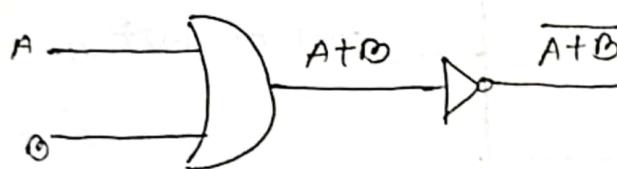


Truth Table:

A	B	Y
0	0	1 $\rightarrow \bar{A}\bar{B}$
0	1	1 $\rightarrow A\bar{B}$
1	0	1 $\rightarrow \bar{A}B$
1	1	0

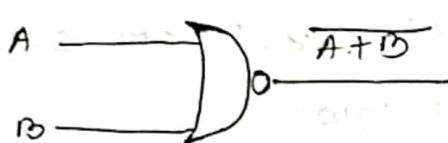
5. NOR Gate:

$$\text{NOT} + \text{OR} = \text{NOR}$$



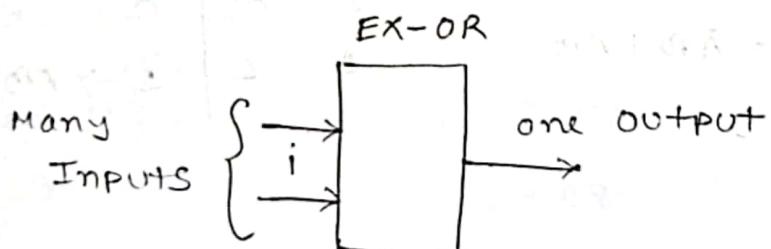
Truth Table:

A	B	Y
0	0	1 $\rightarrow \bar{A}\bar{B}$
0	1	0
1	0	0
1	1	0



Design a circuit using basic gates.

6. Exclusive OR / EX-OR / X-OR:



Truth Table:

A	B	Y
0	0	0
0	1	1 $\rightarrow \bar{A}\bar{B}$
1	0	1 $\rightarrow \bar{A}\bar{B}$
1	1	0

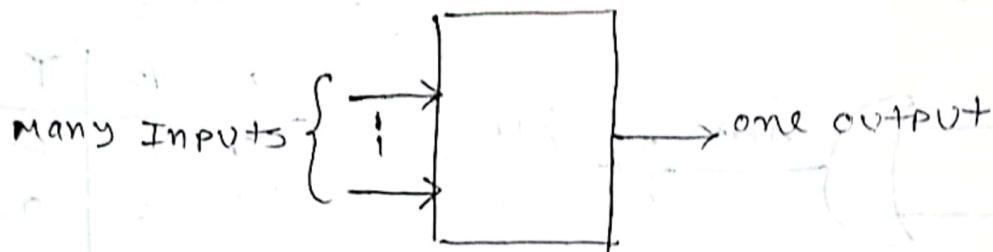
\Rightarrow Output will be high when inputs are different.

\Rightarrow Output will be low when inputs are same.

Symbol: $Y = A \oplus B$

$$= \bar{A}B + A\bar{B}$$

7 Exclusive NOR / EX-NOR / X-NOR :



⇒ output will be high when inputs are same,
otherwise outputs will be low.

Symbol:

$$\begin{array}{c} A \longrightarrow \\ B \longrightarrow \end{array} \circ \quad Y = \overline{A \oplus B}$$

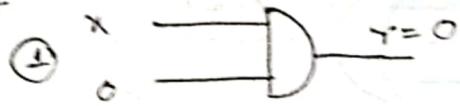
$$= \overline{AB} + AB$$

Truth Table

A	B	Y
0	0	$1 \rightarrow \overline{AB}$
0	1	0
1	0	0
1	1	$1 \rightarrow AB$

Boolean Algebra:

1. $x \cdot 0 = 0$ → Don't care input

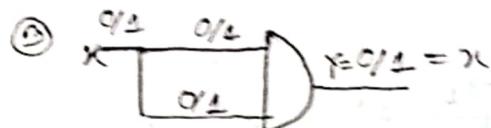


AND { 2. $x \cdot 1 = x$



3. $x \cdot x = x$

4. $x \cdot \bar{x} = 0$

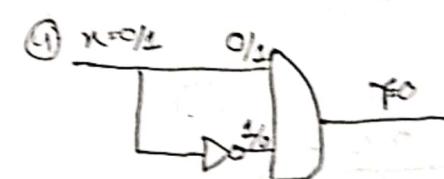


5. $x + 0 = x$

OR { 6. $x + 1 = 1$

7. $x + x = x$

8. $x + \bar{x} = 1$



Commutative

Law { 9. $x+y = y+x$

10. $x \cdot y = y \cdot x$

11. $x + (y+z) = (x+y)+z = x+y+z$

12. $x(yz) = (xy)z = xyz$

13. (a) $x(y+z) = xy+xz$

(b) $(w+x)(y+z) = wy+wz+xy+xz$

14. $x + \bar{x}y = x \rightarrow x + xy = x(1+y) = x \cdot 1 = x$

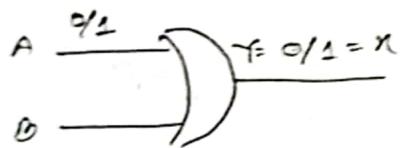
15. (a) $x + \bar{x}y = x+y \rightarrow x + \bar{x}y = x + xy + \bar{x} \cdot y = xy(x+\bar{x})$

16. $\overline{x+y} = \overline{x} \cdot \overline{y}$ } De Morgan's Theorem $= x+y \cdot 1$

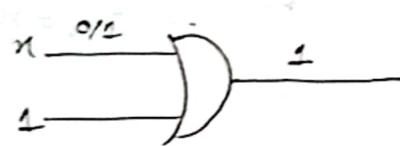
17. $\overline{x \cdot y} = \overline{x} + \overline{y}$ } De Morgan's Theorem $= x+y$

(H.W)

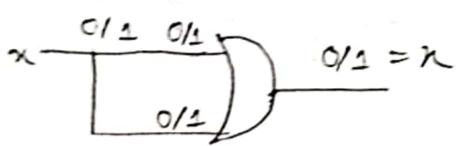
⑤



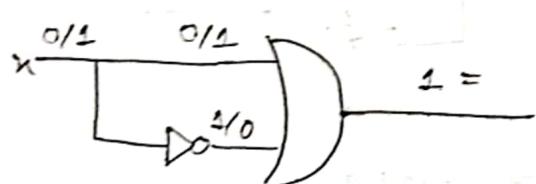
⑥



⑦



⑧



$$\cancel{A} + A\bar{B} = \bar{A} + \bar{B} \text{ [Absorption law]}$$

$$④ x + \bar{x} \cdot y = x + xy + \bar{x}xy$$

$$15 \cdot (b) \Rightarrow x + \bar{x}y = \bar{x} + y = x + y(x + \bar{x})$$

$$= x + y \cdot 1$$

$$= x + y$$

common
अनन्त नियम

$$\left\{ \begin{array}{l} x + \bar{x} = 1 \\ x + xy = \bar{x} + y \end{array} \right.$$

Simplification of logic Expression using Boolean Algebra:

Algebra:

(i) $y = A\bar{B}D + A\bar{B}\bar{D} \rightarrow 5 \text{ gates}$

$$= A\bar{B}(D + \bar{D}) \quad [\text{Distributive Law}]$$

$$= A\bar{B} \cdot 1$$

$$= A\bar{B} \rightarrow 2 \text{ gates}$$

(ii) $y = (\bar{A}+B)(A+B)$

$$= \bar{A}A + \bar{A}B + AB + BB$$

$$= 0 + \bar{A}B + AB + B$$

$$= B(\bar{A} + A + 1)$$

$$= B(\bar{A} + 1)$$

$$= B \cdot 1$$

$$= B$$

(iii) $y = AC\bar{D} + \bar{A}BC\bar{D}$

$$= CD(A + \bar{A}B)$$

$$= CD(A + B) \Rightarrow 3 \text{ gate}$$

$$= AC\bar{D} + BC\bar{D} \Rightarrow$$

(iv) $y = A\bar{B}\bar{C} + A\bar{B}C + ABC = 10$
gates

$$= A\bar{B}\bar{C} + AC(\bar{B} + B)$$

$$= A\bar{B}\bar{C} + AC \cdot 1$$

$$= A(C + \bar{B}\bar{C})$$

$$x + \bar{x}y = xy$$

$$x + \bar{x} \neq R$$

$$\leftarrow = A(C + \bar{B})R$$

$$\Rightarrow x + PR$$

$$\text{Q} \ L = A\bar{B}C + A\bar{B}\bar{C} + \bar{A}BC + ABC$$

$$= A\bar{B}C + A\bar{B}\bar{C} + A\bar{B}\bar{C} + \bar{A}BC$$

Step 2

$$= AC(\bar{B} + B) + A\bar{B}\bar{C} + \bar{A}BC$$

$$= AC \cdot 1 + A\bar{B}\bar{C} + \bar{A}BC$$

$$= C(A + \bar{A}B) + A\bar{B}\bar{C}$$

$$= C(A + B) + A\bar{B}\bar{C}$$

$$= CA + CB + A\bar{B}\bar{C}$$

$$= CA + B(C + A\bar{B})$$

$$= CA + B(C + A)$$

$$= AB + BC + CA$$

Step 3

$$= AB + BC + CA$$

De Morgan's : (Proof)

$$\text{16. } \overline{x+y} = \overline{x} \cdot \overline{y}$$

\Rightarrow we know that,

$$x + \overline{x} = 1$$

$$\text{so, } \overline{x+y} = \overline{x} \cdot \overline{y}$$

$$\Rightarrow (x+y) + \overline{x} \cdot \overline{y} = 1 \quad [\because (x+y) + \overline{(x+y)} = 1]$$

$$\text{L.H.S} = (x+y) + \overline{x} \cdot \overline{y}$$

$$\Rightarrow ((x+y)+\overline{x}) \cdot ((x+y)+\overline{y})$$

$$\Rightarrow (x+y+\overline{x}) \cdot (x+y+\overline{y})$$

$$\Rightarrow (1+y)(1+z)$$

$$\Rightarrow 1 \cdot 1$$

$$\Rightarrow 1 \quad \underline{\text{R.H.S}}$$

TRUTH TABLE:

INPUTS		OUTPUTS				
x	y	$x+y$	$\overline{x+y}$	\overline{x}	\overline{y}	$\overline{x} \cdot \overline{y}$
0	0	0	1	1	1	1
0	1	1	0	0	1	0
1	0	1	0	1	0	0
1	1	1	0	0	0	0

$$\overline{x+y} = \overline{x} \cdot \overline{y}$$

$$\text{L.H.S} = \overline{x} \cdot \overline{y} = \overline{x} + \overline{y} \dots \text{(i)}$$

$$\underline{\text{L.H.S}} = \overline{x} \cdot \overline{y}$$

$$\Rightarrow \overline{x} = (x + \overline{x}) \quad [\text{complement Law}]$$

$$\overline{y} = (y + \overline{y})$$

$$\Rightarrow (x + \overline{x})(y + \overline{y}) \quad [\text{substitutes values back to L.H.S}]$$

$$\Rightarrow x \cdot y + x \cdot \overline{y} + \overline{x} \cdot y + \overline{x} \cdot \overline{y} \quad [\text{distributive law}]$$

$$\Rightarrow (x \cdot y + 0 + 0 + \overline{x} \cdot \overline{y}) \quad [\text{idempotent law}]$$

$$\Rightarrow x \cdot y + \overline{x} \cdot \overline{y} \quad [\text{simplify}]$$

$$\Rightarrow x \cdot y = \overline{x} + \overline{y} \quad [\text{complement law}]$$

$$\Rightarrow (\overline{x} + \overline{y}) + \overline{x} \cdot \overline{y} \quad [\text{substitute Again}]$$

$$\Rightarrow \overline{x} + \overline{y} + \overline{x} \cdot \overline{y} \quad [\text{distributive law}]$$

$$\Rightarrow \overline{x} + \overline{y} \quad [\text{idempotent law}]$$

$$= \underline{\text{R.H.S}}$$

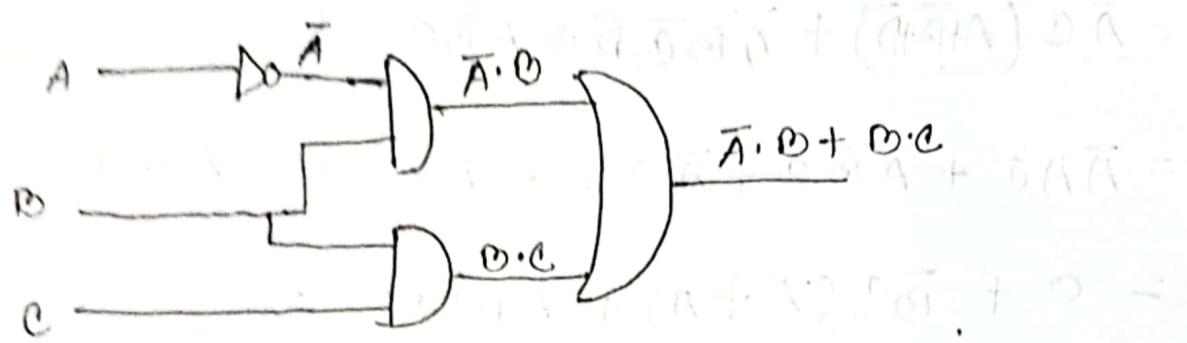
Truth Table:

Inputs		Outputs				
x	y	xy	\overline{xy}	\overline{x}	\overline{y}	$\overline{x} + \overline{y}$
0	0	0	1	1	1	1
0	1	0	1	0	1	1
1	0	0	1	1	0	1
1	1	1	0	0	0	0

$$\begin{aligned}
 \textcircled{2} \quad Y &= \overline{AC}(\overline{A}\oplus\overline{D}) + \overline{A}\oplus\overline{C}\overline{D} + A\overline{B}C \\
 &= \overline{AC}(A\oplus\overline{B}\overline{D}) + \overline{A}\oplus\overline{C}\overline{D} + A\overline{B}C \\
 &= \overline{AAC} + \overline{A}\overline{B}\overline{C} + \overline{A}\overline{C}\overline{D} + \overline{A}\overline{B}\overline{C}\overline{D} + A\overline{B}C \\
 &= 0 + \overline{B}C(\overline{A}+A) + \overline{A}\overline{D}(C+\overline{C}B) \\
 &= \overline{B}C + \overline{A}\overline{D}(C+B) \\
 &= \overline{B}C + \overline{A}C\overline{D} + \overline{A}\overline{B}\overline{D}
 \end{aligned}$$

Q Design the logic circuit from a given truth table:

A B C			Y	sum of ↓ OR	Product form: ↓ AND
0 0 0			0		
0 0 1			0		
0 1 0			1 → $\overline{A}\oplus\overline{C}$	$\overline{A}\oplus\overline{C} + A\overline{B}C + ABC$	
0 1 1			1 → $\overline{A}\oplus C$		$= \overline{A}B(\overline{C}+C) + ABC$
1 0 0			0		$= \overline{A}B + ABC$
1 0 1			0		$= B(\overline{A}+AC)$
1 1 0			0	+	$= B(\overline{A}+C)$
1 1 1			1 → ABC		$= \overline{A}D + BC$



design the logic circuit from a given truth table:

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1 $\rightarrow \bar{A}BC$
1	0	0	0
1	0	1	1 $\rightarrow \bar{A}\bar{B}C$
1	1	0	1 $\rightarrow A\bar{B}\bar{C}$
1	1	1	1 $\rightarrow A\bar{B}C$

$$Y = \bar{A}B\bar{C} + A\bar{B}C + AB\bar{C} + ABC$$

$$= \cancel{\bar{A}B\bar{C}} + A\bar{B}C + AB(\bar{C} + C)$$

$$= \bar{A}B\bar{C} + A\bar{B}C + AB$$

$$= \bar{A}B\bar{C} + A(\bar{B}C + B)$$

$$= \cancel{\bar{A}B\bar{C}} + A(B + \bar{B}C)$$

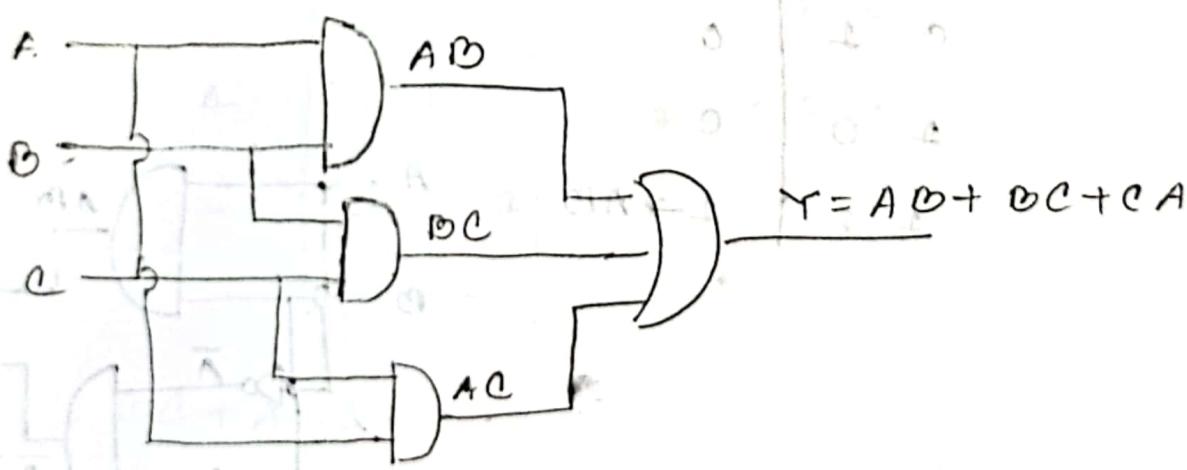
$$= \bar{A}B\bar{C} + A(B + C)$$

$$= \bar{A}B\bar{C} + AB + CA$$

$$= B(\bar{A}\bar{C} + A) + CA$$

$$= B(A + C) + CA$$

$$= \cancel{AB} + BC + CA$$

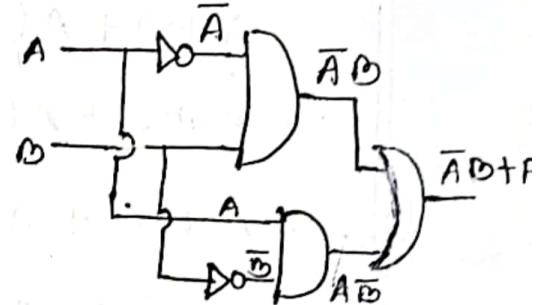


Q) Why EX-OR is compound?

A	B	Y
0	0	0
0	1	1 $\rightarrow \overline{AB}$
1	0	1 $\rightarrow A\overline{B}$
1	1	0

$$Y = A \oplus B$$

$$= AB + A\overline{B}$$

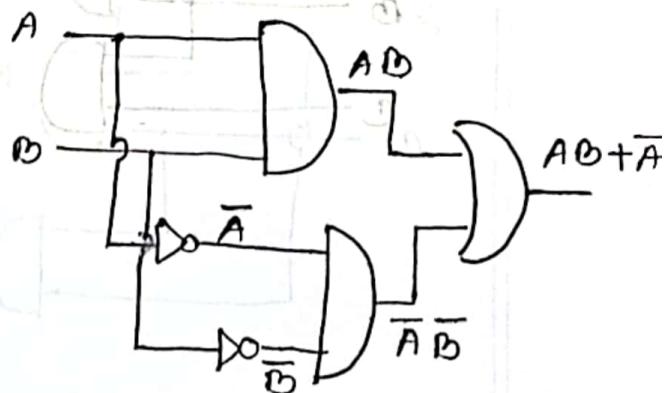


Q) EX-NOR:

A	B	Y
0	0	1 $\rightarrow \overline{AB}$
0	1	0
1	0	0
1	1	1 $\rightarrow A\overline{B}$

$$Y = \overline{A \oplus B}$$

$$= AB + \overline{A}\overline{B}$$



Design the logic circuit from a given statement:

Ex: 01, suppose A, B, C are inputs and Y is the output. Output will be high when majority of inputs are high. Design the circuit.

Y	A	B	C	Y (Ans)
	0	0	0	0
	0	0	1	0
	0	1	0	0
	0	1	1	1 $\rightarrow \bar{A}BC$
	1	0	0	0
	1	0	1	1 $\rightarrow A\bar{B}C$
	1	1	0	1 $\rightarrow A\bar{B}\bar{C}$
	1	1	1	1 $\rightarrow A\bar{B}C$

Step: 1 \rightarrow Truth Table

Step: 2 \rightarrow Simplification

Step: 3 \rightarrow Circuit

$$Y = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$$

$$= AB + BC + CA$$

$$\textcircled{R} \quad Y = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$$

$$= \bar{A}BC + A\bar{B}C + AB(\bar{C} + C)$$

$$= \bar{A}BC + A\bar{B}C + AB$$

$$= \bar{A}BC + A(\bar{B}C + B)$$

$$\Rightarrow \bar{A}BC + A(B+C)$$

state At start + 92.5

Final state $\Rightarrow \bar{A}BC +$

Initial state - 92.5

	B	C	A
0	0	0	0
0	1	0	0
0	0	1	0
0	1	1	0
1	0	0	0
1	1	0	0
1	0	1	0
1	1	1	0
1	0	0	1
1	1	0	1
1	0	1	1
1	1	1	1

DATA $\leftarrow 0$

DATA $\leftarrow 1$

DATA $\leftarrow 2$

DATA $\leftarrow 3$

DATA $\leftarrow 4$

$$0BC + 1BC + 2BC + 3BC$$

$$AB + BC + CA$$

If suppose, A, B, C are inputs and Y is the output. Output will be high when majority of inputs are low.

A	B	C	Y
0	0	0	$1 \rightarrow \bar{A}\bar{B}\bar{C}$
0	0	1	$1 \rightarrow \bar{A}\bar{B}C$
0	1	0	$1 \rightarrow \bar{A}B\bar{C}$
0	1	1	0
1	0	0	$1 \rightarrow A\bar{B}\bar{C}$
1	0	1	0
1	1	0	0
1	1	1	0

$$Y = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C}$$

$$= \bar{A}\bar{B}(\bar{C}+C) + \bar{A}B\bar{C} + A\bar{B}\bar{C}$$

$$= \bar{A}\bar{B} + \bar{C}(\bar{A}B + A\bar{B})$$

$$= \bar{A}\bar{B} + \bar{C}(A \oplus B)$$

$$= \bar{A}\bar{B} + (\bar{C}A \oplus \bar{C}B)$$

$$\Rightarrow \bar{A}\bar{B} + \bar{A}B\bar{C} + A\bar{B}\bar{C}$$

$$\Rightarrow \bar{B}(\bar{A} + A\bar{C}) + \bar{A}B\bar{C}$$

$$\Rightarrow \bar{B}(\bar{A} + \bar{C}) + \bar{A}B\bar{C}$$

$$\text{Ansatz } Y = \bar{A}\bar{B} + \bar{B}\bar{C} + \bar{A}\bar{B}\bar{C}$$

$$\begin{aligned} \text{Test: } & Y = \bar{A}\bar{B} + \bar{C}(\bar{B} + \bar{A}\bar{B}) \\ & = \bar{A}\bar{B} + \bar{C}(\bar{B} + \bar{A}) \\ & = \bar{A}\bar{B} + \bar{B}\bar{C} + \bar{C}\bar{A}. \end{aligned}$$

$$\text{OR, } Y = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C}$$

$$= \bar{A}\bar{B} + \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C}$$

$$= \bar{A}(\bar{B} + B\bar{C}) + A\bar{B}\bar{C}$$

$$= \bar{A}(\bar{B} + \bar{C}) + A\bar{B}\bar{C}$$

$$= \bar{A}\bar{B} + \bar{A}\bar{C} + A\bar{B}\bar{C}$$

$$= \bar{A}\bar{B} + \bar{C}(\bar{A} + A\bar{B})$$

$$\Rightarrow \bar{A}\bar{B} + \bar{C}(\bar{A} + \bar{B})$$

$$= \bar{A}\bar{B} + \bar{A}\bar{C} + \bar{B}\bar{C}$$

$$\text{Durchsetzen in } Y = \bar{A}\bar{B} + \bar{A}\bar{C} + \bar{B}\bar{C}$$

$$\text{Durchsetzen in } Y = \bar{A}\bar{B} + (\bar{B}\bar{C} + \bar{A})\bar{C}$$

$$\text{Durchsetzen in } Y = \bar{A}\bar{B} + (\bar{B} + \bar{A})\bar{C}$$

iii) Design a logic circuit that follows the following requirements:

- (i) output x will equal to A when B and C are same.
- (ii) output x will (remain) HIGH when B and C are different.

A	B	C	x
0	0	1	$\bar{A} \bar{B} C + A \bar{B} \bar{C}$
0	1	0	$\bar{A} B \bar{C} + A \bar{B} \bar{C}$
0	1	1	0
1	0	0	$\bar{A} B \bar{C}$
1	0	1	$\bar{A} B C$
1	1	0	$\bar{A} B \bar{C}$
1	1	1	$\bar{A} B C$

$$T = \bar{A} \bar{B} C + \bar{A} B \bar{C} + A \bar{B} \bar{C} + A \bar{B} C + A B \bar{C} + A B C$$

$$Y' = \overline{A}\overline{B}C + \overline{A}\overline{B}\overline{C} + A\overline{B}\overline{C} + \overline{A}\overline{B}C + \overline{A}B\overline{C} + ABC$$

$$= \overline{A}B(\overline{C} + C) + A\overline{B}(\overline{C} + C) + \overline{A}\overline{B}C + \overline{A}\overline{B}\overline{C}$$

$$= \overline{A}B + A\overline{B} + \overline{A}\overline{B}C + \overline{A}\overline{B}\overline{C}$$

$$Q_6 = A(B + \overline{B}\overline{C}) + \overline{A}(B + \overline{B}C)$$

$$= A(B + (\overline{B} + \overline{C})) + \overline{A}(B + C)$$

$$= AB + A\overline{B} + \overline{A}\overline{C} + \overline{A}B + \overline{A}C$$

$$= A(B + \overline{B}) + \overline{A}(B + C) + \overline{A}\overline{C} \rightarrow A(B + \overline{B}) +$$

$$= A + \overline{A}(B + C) + A\overline{C}$$

$$= A(1 + \overline{C}) + \overline{A}(B + C)$$

$$= A + \overline{A}(B + C)$$

$$\text{DATA} \rightarrow 1$$

$$\overline{\text{DATA}} \rightarrow 0$$

$$\text{DATA} \rightarrow 1$$

$$\text{DATA} + \overline{\text{DATA}} + \text{DATA} \cdot \overline{\text{DATA}} = \text{DATA} \cdot 1 = \text{DATA}$$

$$\text{OR, } \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + A\bar{B}C + A\bar{B}C + ABC$$

$$= \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + A\bar{B}C + AB$$

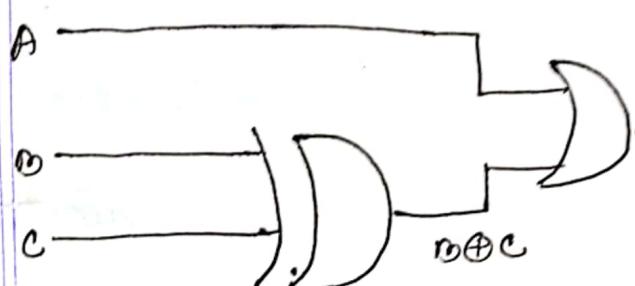
$$= \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B} + AB \quad [\text{LHS} = 4]$$

$$= \bar{A}\bar{B}C + \bar{A}B\bar{C} + A$$

$$\text{therefore } A(\bar{B}C + B\bar{C}) + A$$

$$= A + \bar{A}(B \oplus C)$$

$$= A + (B \oplus C)$$



$$x = A + (B \oplus C)$$

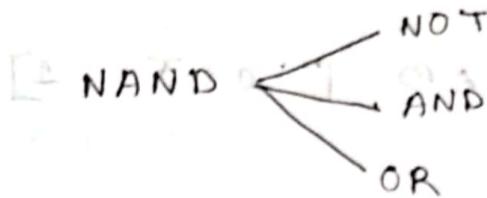
equation of circuit (ii)



equation of circuit (iv)

Universality of NAND gate:

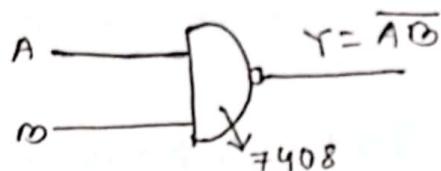
→ design gates only using NAND gate.



④ Discuss universality of NAND gate.

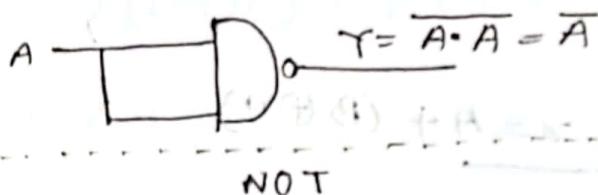
→ We can design any gate using NAND gate, this is called universality of NAND gate.

(i) NAND to NOT:

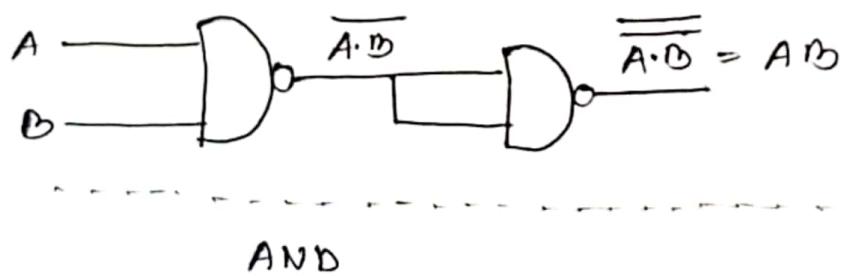
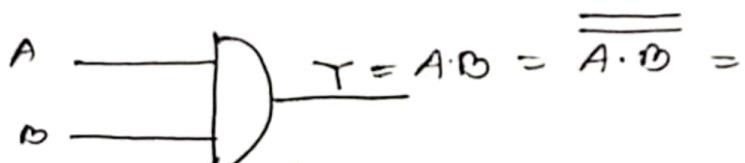


$$Y = \bar{A} = \overline{A \cdot A}$$

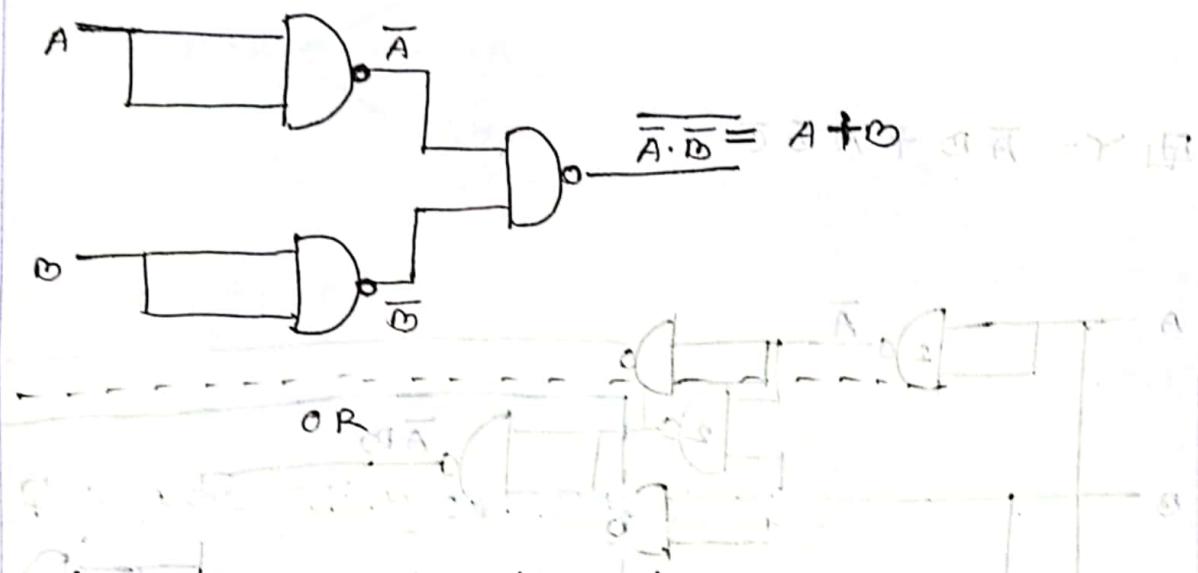
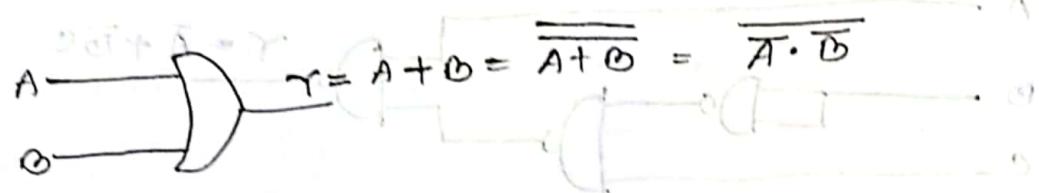
$$(0 \oplus 0) + 1$$



(ii) NAND to AND:

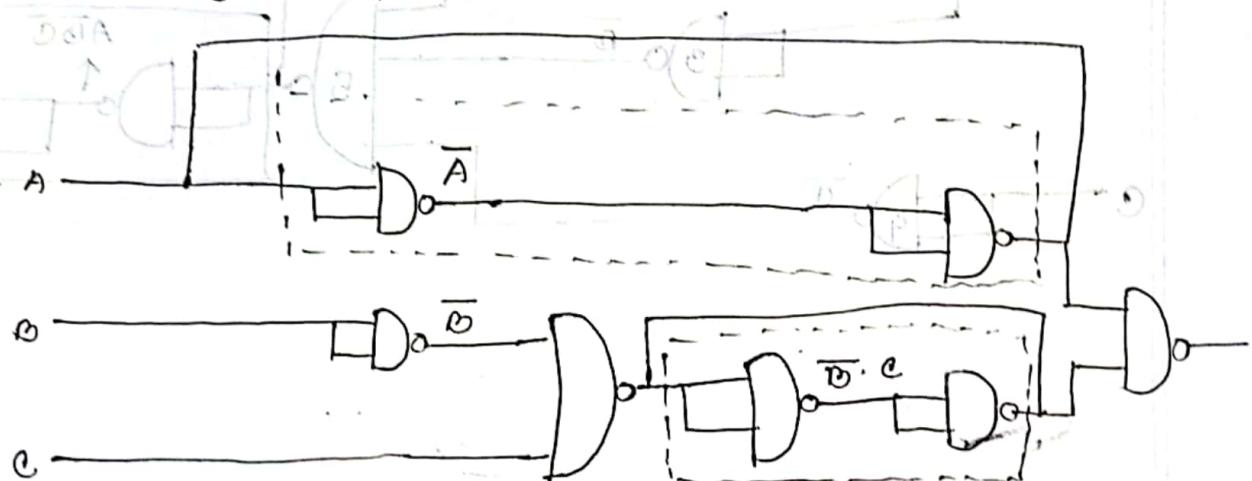


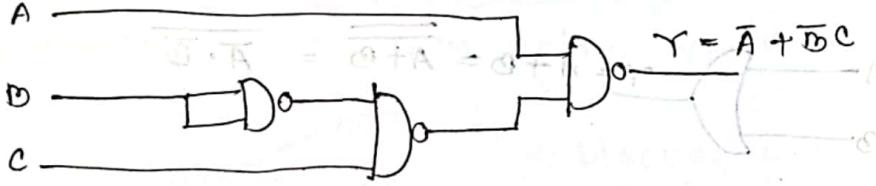
(iii) NAND to OR:



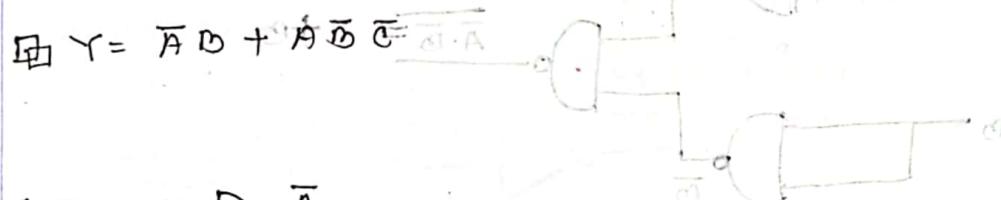
2. * Design a circuit using NAND gate only.

$$y = \overline{A} + \overline{B}C$$



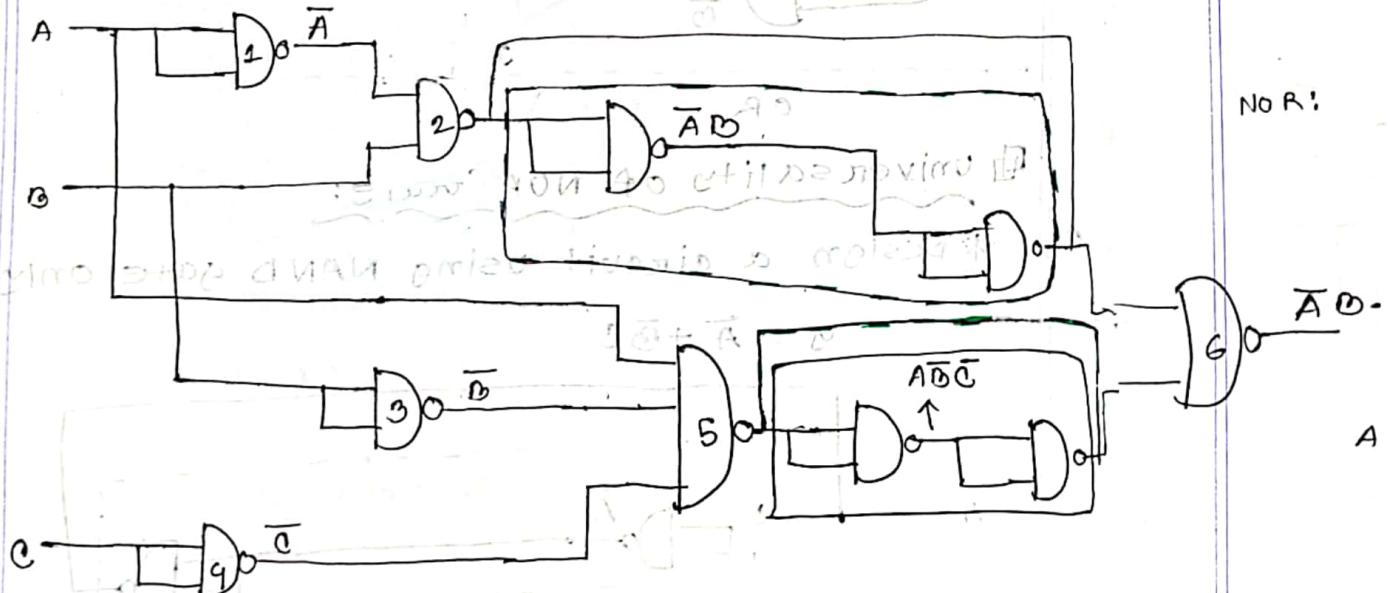


Universal
→ Des.



1. NO 6

NO R!

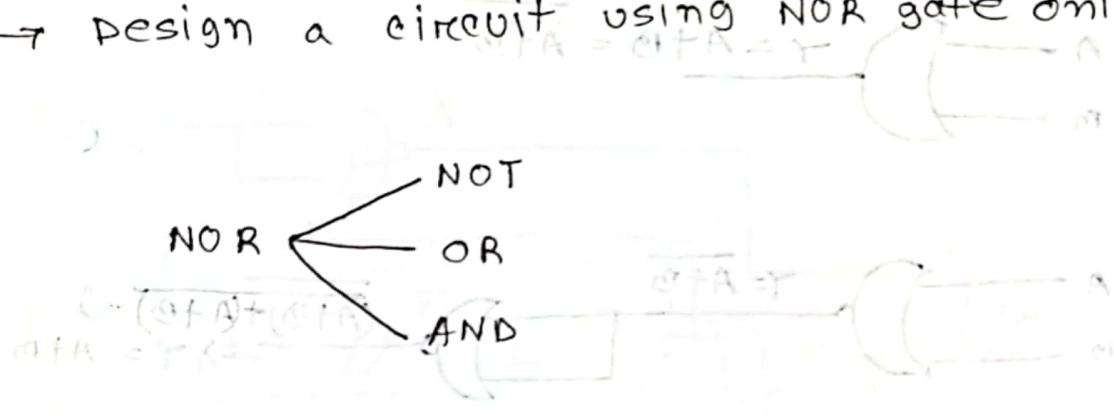


A

ANSWER

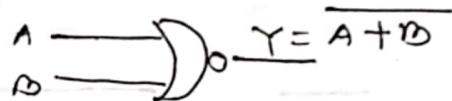
Universality of NOR gate: : 92 at 8.33 (ii)

→ Design a circuit using NOR gate only.

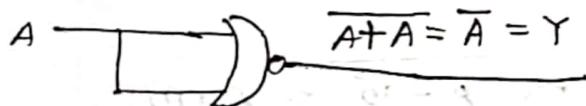
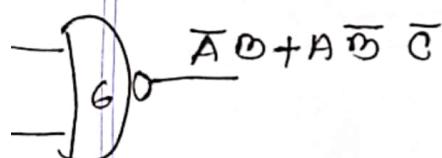
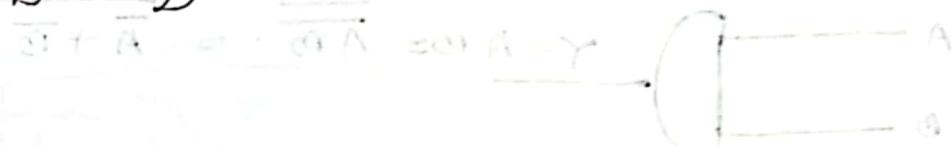
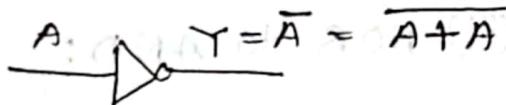


1. NOR to NOT:

NOR:



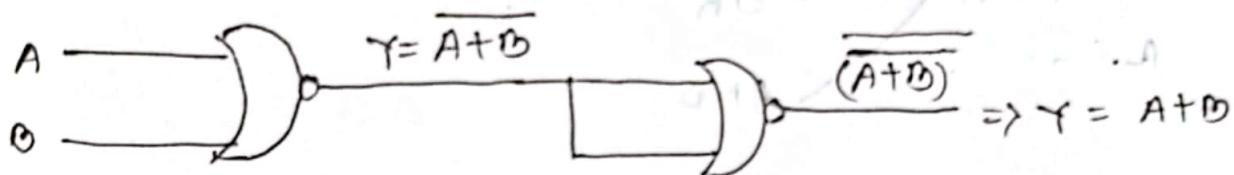
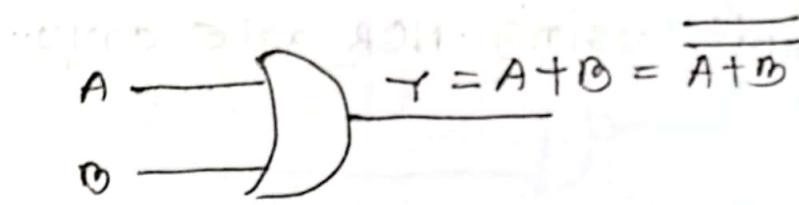
NOT:



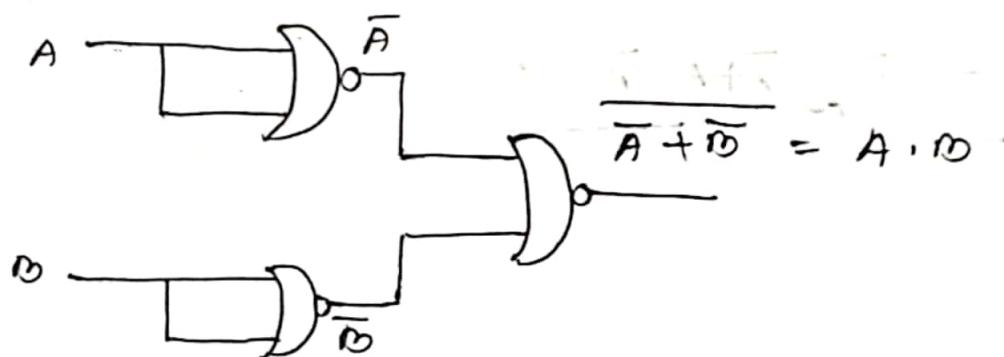
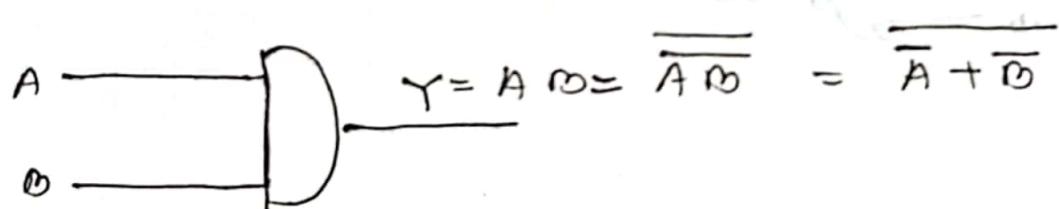
This result proves that it is possible to implement any logic function using only NOR gates.

After learning about universal gates, we can now move on to other topics.

(ii) NOR to OR:

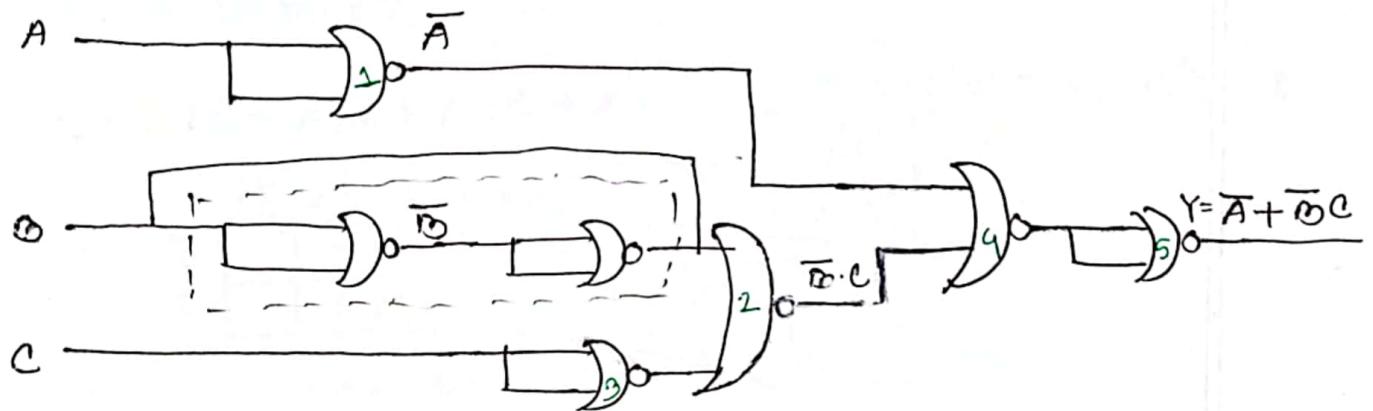


(iii) NOR to AND:

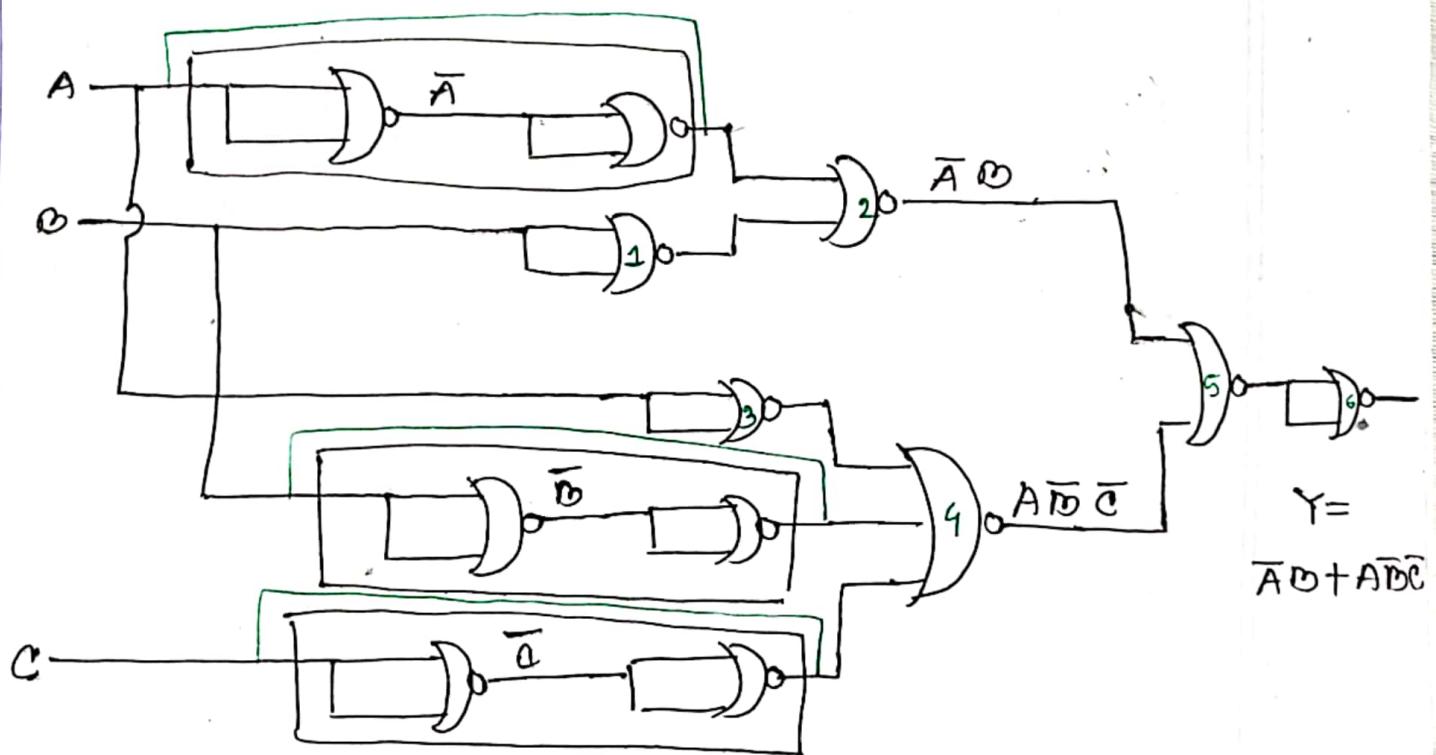


Thus we can design all gates using NOR gate only, so NOR gate is universal gate.

由 draw $y = \overline{A} + \overline{B}C$ using NOR gate only.



由 $y = \overline{AB} + A\overline{BC}$ using NOR gate:



Karnaugh Map (K-Map):

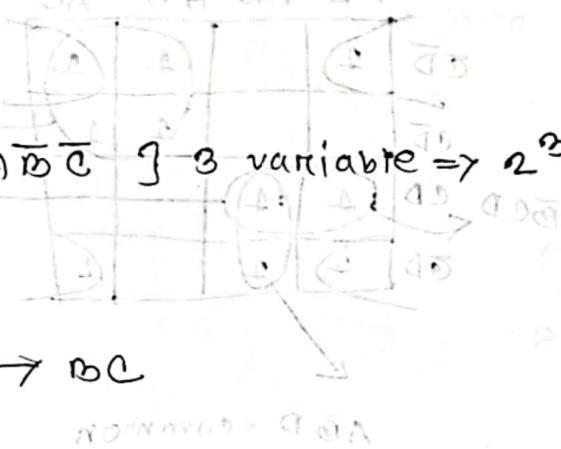
→ simplify logic expression.

what is K-map?

$$\Rightarrow y = \bar{A}BC + A\bar{B}C + AB\bar{C} + A\bar{B}\bar{C} \quad \left\{ 3 \text{ variable} \Rightarrow 2^3 = 8 \right.$$

	$\bar{A}\bar{B}$	$A\bar{B}$	$\bar{A}B$	AB
\bar{C}	1			
C	1	1	1	1

2x4 K-Map



$$y = \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{C}D + \bar{A}\bar{B}\bar{C}\bar{D} + A\bar{B}C\bar{D} + \bar{A}B\bar{C}D \Rightarrow 2^9 = 16$$

	$\bar{A}\bar{B}$	$A\bar{B}$	$\bar{A}B$	AB
$\bar{C}\bar{D}$	1	0	0	1
$\bar{C}D$	0	0	0	0
$C\bar{D}$	1	0	0	0
CD	0	1	1	0



Method of simplifying K-MAP: Pairing, Quad, Octet

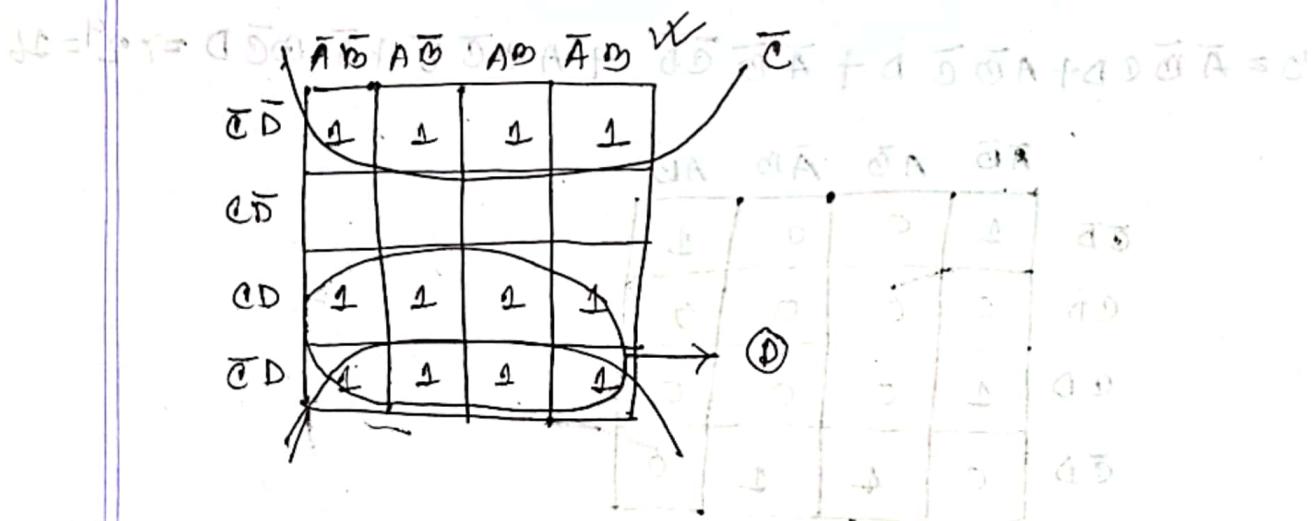
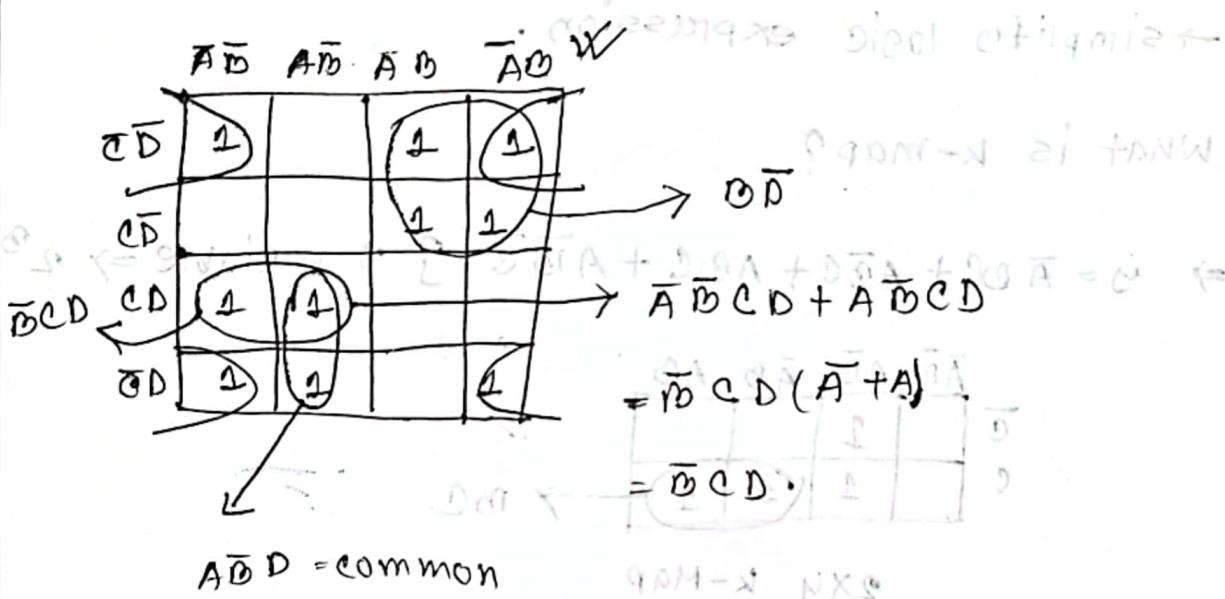
Pairing: \rightarrow pair 2 adjacent '1's (less 1 variable)

Quad: \rightarrow 4 adjacent '1's (less 2 variables)

Octet: \rightarrow 8 adjacent '1's (less 3 variables)

■

: (904 - 8) 904 Normal



■ Octet is better than Quad which is better than pair which is better than nothing.

$\Rightarrow \text{Octet} > \text{Quad} > \text{pair} > \text{Nothing}$

Octet is better than Quad which is better than pair which is better than nothing.

Octet is better than Quad which is better than pair which is better than nothing.

Algorithmi:

2. Draw the K-map according to number of inputs and insert '1's in appropriate position.

2. find 'is' (if any) that has no adjacent 'is'.
This 'is' is called isolated 'is'. If so, 200 P
itself.

1	.	1	1
		1	
2		2	1

3. Find 1's that has only one adjacent '1', if so, pair them.
 4. find octec, if any.
 5. find Quad, if any.
 6. Find pairs if any.
 7. write the result of each loop as a sum form.

Example:

$$y = A\bar{B}C + A\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C}$$

	$\bar{A}\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$
\bar{C}	1	1	1	1
C	1	1	1	1

loop 1: $\bar{A}\bar{B}C + A\bar{B}\bar{C}$
loop 2: $\bar{A}\bar{B}C + A\bar{B}\bar{C}$

$$y = AB + AC + BC = AB + BC + CA$$

$$y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}CD + A\bar{B}\bar{C}\bar{D}$$

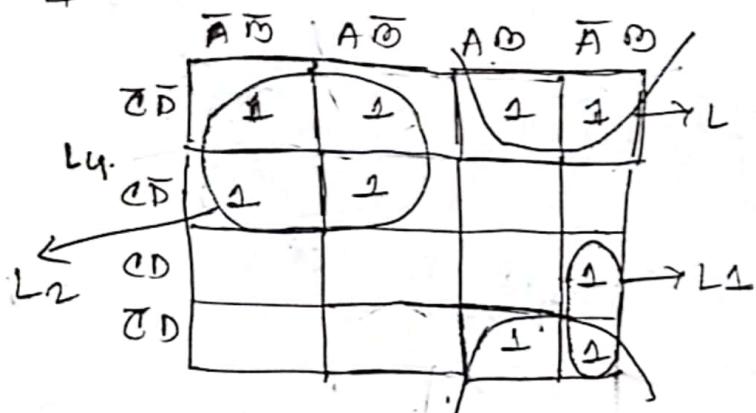
$$ABCD + A\bar{B}\bar{C}D + \bar{A}BC\bar{D}$$

	$\bar{A}\bar{D}$	$A\bar{D}$	AB	$\bar{A}B$
$\bar{C}\bar{D}$	1	1	1	1
CD	1	1	1	1
$\bar{C}D$	1	1	1	1

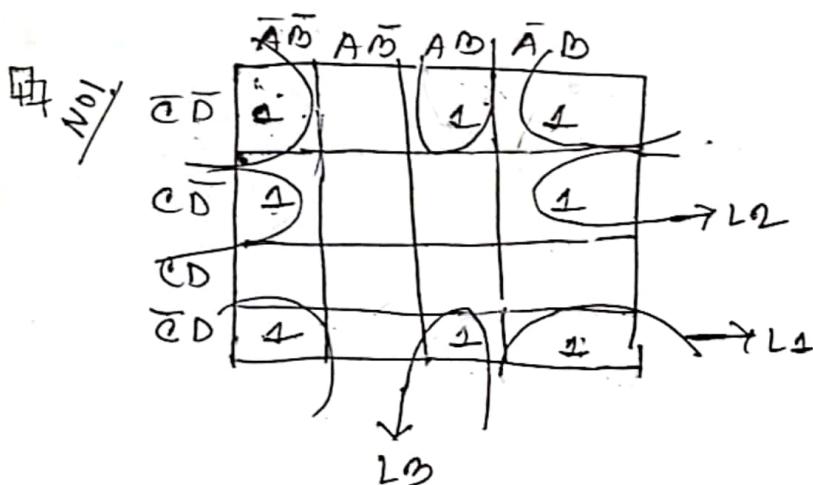
LS: $\bar{A}\bar{D}$
L1: $\bar{A}\bar{D}$
L2: AB
L3: $\bar{A}B$
L4: CD

$$y = A\bar{B}\bar{C}\bar{D} + A\bar{B}CD + \bar{A}C\bar{D} + \bar{B}\bar{C}D + \bar{A}\bar{B} \text{ (NO X-OR)}$$

Q4



$$y = \bar{A}BD + \bar{B}\bar{D} + BC$$

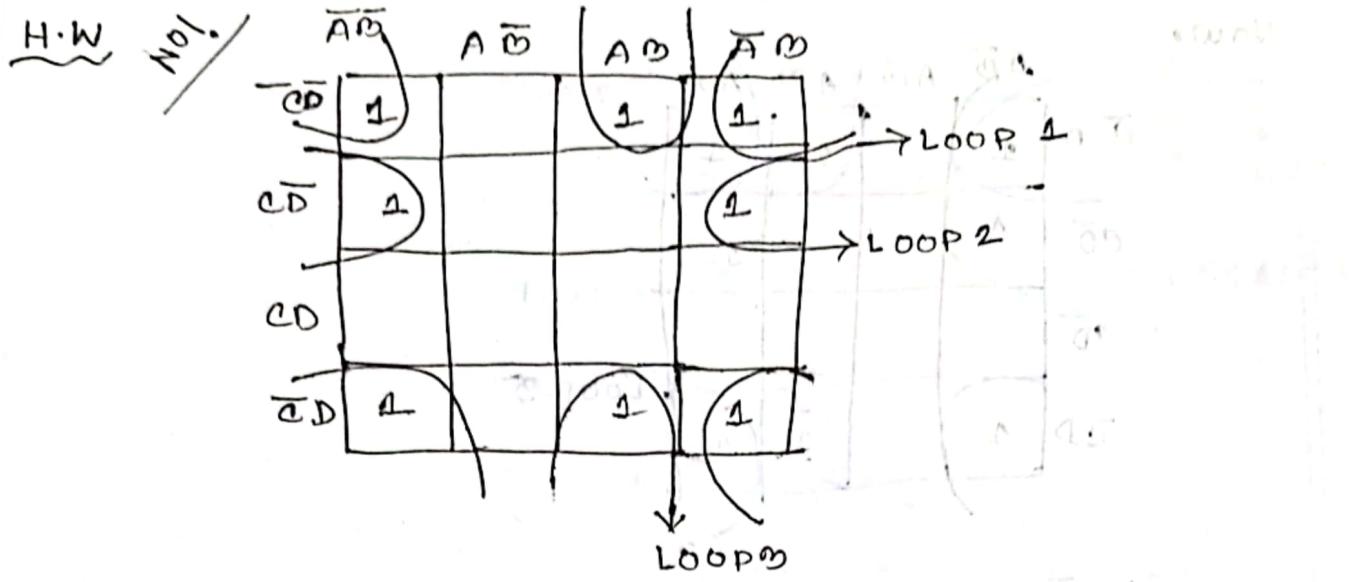


$$y = \bar{A}\bar{C} + \bar{A}C\bar{D} + AB\bar{C}$$

$$\bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}B\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{C}D \leq \bar{A}\bar{C}$$

$$L_2 = \underline{\bar{A}\bar{B}\bar{C}\bar{D}} + \underline{\bar{A}B\bar{C}\bar{D}} = \bar{A}\bar{C}\bar{D}$$

$$L_3 = A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}D = A\bar{B}\bar{C}$$



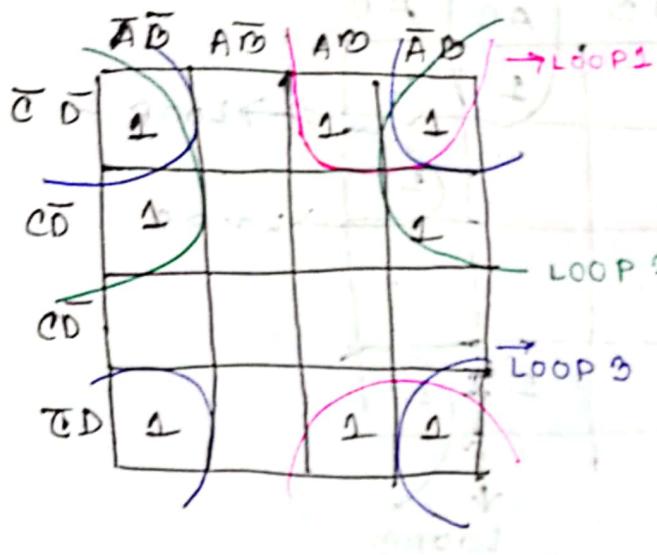
$$\begin{aligned} \text{Loop 1} &= \overline{A}\overline{B}\overline{C}\overline{D} + \overline{A}B\overline{C}\overline{D} + A\overline{B}\overline{C}D + AB\overline{C}D \\ &= \overline{A}\overline{C} \end{aligned}$$

$$\text{Loop 2} = \overline{A}\overline{B}C\overline{D} + \overline{A}B\overline{C}\overline{D} = \overline{A}C\overline{D}$$

$$\text{Loop 3} = A\overline{B}C\overline{D} + A\overline{B}CD = A\overline{B}\overline{C}$$

$$\therefore y = \overline{A}\overline{C} + \overline{A}C\overline{D} + A\overline{B}\overline{C}$$

Now,



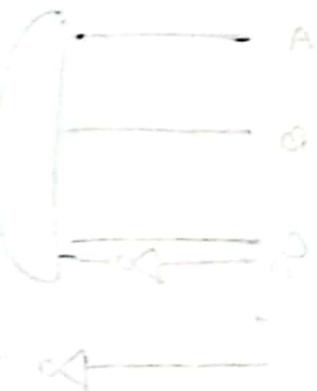
$$Y = \overline{A} \overline{D} + B \overline{C} + \overline{A} \overline{C}$$

[u-7] (1-3)

Example: 04 A four-bit binary number is represented as DCBA, where D, C, B and A represent the individual bits and A is equal to the LSD. Design a logic circuit that will produce a high output whenever the binary number is greater than 0010 and less than 1010.

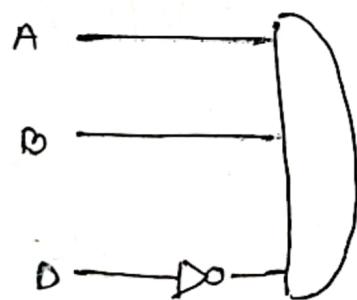
D	C	B	A	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0 0 1 1				$= 0 \times 10^2 + 0 \times 10^1 + 0 \times 10^0$
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0 1 0 1				$= 0 \times 10^3 + 1 \times 10^2 + 0 \times 10^1 + 1 \times 10^0 = 1$
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

072
 ↓
 ↓
 MSB LSB



$\bar{A}\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$
$\bar{C}\bar{D}$			
1	1	1	1
$C\bar{D}$			
1	1	0	1
$\bar{C}D$			
1	1	0	0
$C D$			
0	0	0	0

$y = A\bar{B}\bar{D} + \bar{B}\bar{C}D + C\bar{D}$, draw the circuit.



Example 5 A 4-bit binary number is represented as $D C B A$, where D, C, B and A represent the individual bits with A equal to the LSB. Design a logic circuit that will produce a High output whenever (the binary number is greater than 0011 and less than 1011) or (all inputs are Low) ~~or all~~ inputs are High.

LSB				
D	C	B	A	Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
-	-	-	-	-
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
-	-	-	-	-
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
-	-	-	-	-
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

$\bar{A}\bar{B} \quad A\bar{B} \quad AB \quad \bar{A}B$

$\bar{C}\bar{D}$	$\bar{C}D$	$C\bar{D}$	CD
1	0	0	0
1	1	1	1
0	0	1	0
1	1	0	1

$$Y = A\bar{B}C + \bar{B}\bar{C}D + \bar{A}\bar{C}D + C\bar{D} + A\bar{B}\bar{D}$$

Draw circuit

$$Y \rightarrow \bar{A}\bar{B}C$$

A 0 0 0 0

B 0 0 1 1

C 0 1 0 1

D 0 1 1 0

Y 0 1 0 1

0 1 1 0

0 1 0 1

1 0 1 0

1 0 0 1

0 1 1 0

0 1 0 1

1 0 1 0

1 0 0 1

Example : 6: Design a logic circuit which has four inputs A, B, C, D and an output Y that is to be HIGH only when A is HIGH at the same time that at least two other inputs are HIGH. Design the circuit.

Ans:

P	Q	R	S	A	Y
0	0	0	0	0	0
X	0	0	0	1	0
0	0	1	0	0	0
X	0	0	1	1	0
0	1	0	0	0	0
X	0	1	0	1	0
0	1	1	0	0	0
X	0	1	1	1	1
1	0	0	0	0	0
1	0	0	1	0	0
1	0	1	0	0	0
X	0	1	1	1	1
1	1	0	0	0	0
1	1	1	0	0	0
X	1	1	1	1	1

$\bar{A}\bar{B}$	$\bar{A}\bar{B}$	$\bar{A}B\bar{C}$	$\bar{A}B\bar{C}$
0	0	0	0
0	0	1	0
0	1	1	0
0	0	1	0

$$y = AB'C + A'CD + ABC'D$$

Draw the circuit.

Q1 what are the limitations of K-map?

→ which expression are uniform, we can only input them in K-map. If the equation is 3 bit or 4 bit.

$$y = A\bar{B}C + \bar{A}\bar{B}C + A\bar{B}C + A\bar{B}C \rightarrow C(A + \bar{A}) \Rightarrow AC + \bar{AC}$$

	$\bar{A}\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$	
\bar{C}	0	0	1	0	
C	1	1	1	1	

$y = C + A\bar{B}$

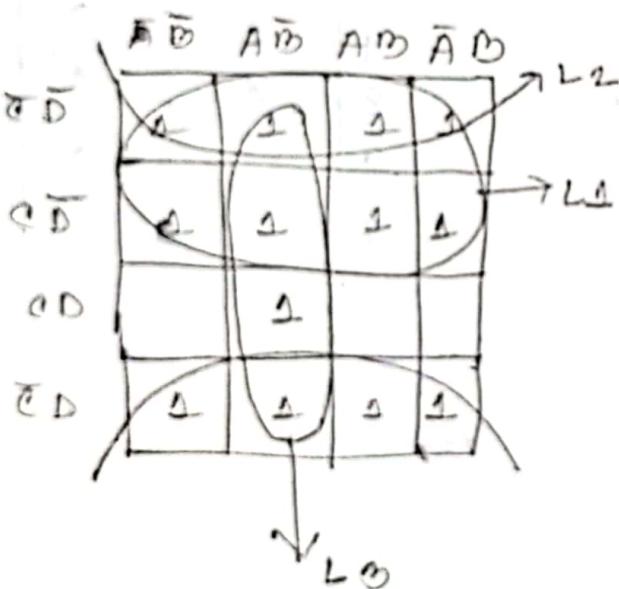
Example 9: Simplify the following expression

using K-map $Y = ACD + A'D'CD + ABC'D + A'DC + AB + C'D$

	$\bar{A}\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$
$\bar{C}D$		1	1	
CD		1	1	
$\bar{C}D$		1	1	

$$y = A + CD \cdot$$

Example: $y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{C}D + A\bar{B}C + D$



$$y = \bar{D} + \bar{C} + A\bar{B}$$

→ Till today (CT)

Indexing:

CT 1 → } 08.08.23
Emap 384
upto k-map

A	$\bar{A}\bar{B}$	$A\bar{B}$	$A\bar{B}$	$\bar{A}B$
\bar{C}				01
C				10

$$F(A, B, C) = \sum(0, 1, 3, 6, 7)$$

	$\bar{A}\bar{B}$	$A\bar{B}$	$A\bar{B}$	$\bar{A}B$
\bar{C}	1	1	1	1
C		1	1	1

$$Y = \bar{B}\bar{C} + A\bar{B} + BC$$

$$= A\bar{B} + \overline{B \oplus C}$$

A	B	C	Y
0	0	0	1
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

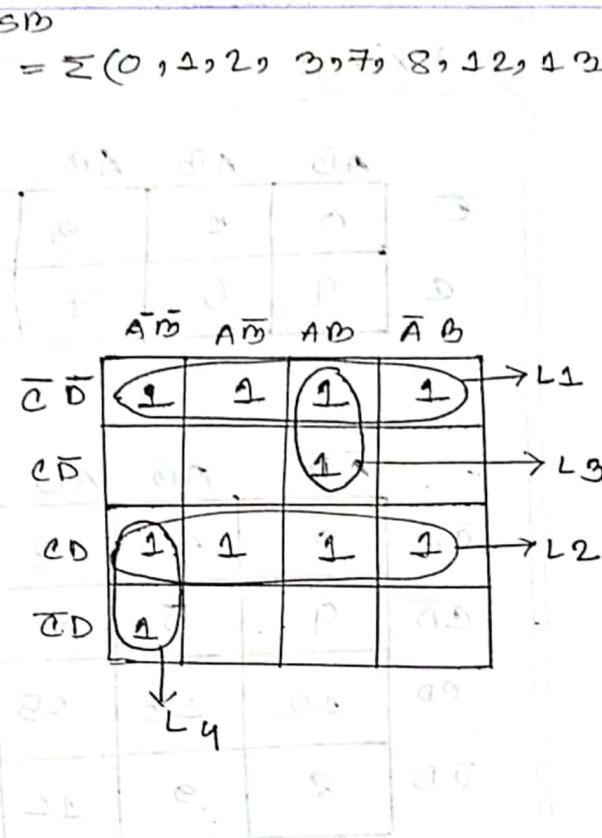
$$\bar{B}\bar{A} + \bar{B} + \bar{B} -$$

Example: Minimize the given function

Implement $F(A, B, C, D) = \sum(0, 1, 2, 3, 7, 8, 12, 13, 14, 15)$

using K-map

MSB Decimal	D	C	B	A	Σ
0	0	0	0	0	1
1	0	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	0
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	0
10	1	0	1	0	0
11	1	0	1	1	0
12	1	1	0	0	1
13	1	1	0	1	1
14	1	1	1	0	1
15	1	1	1	1	1



$$F(A, B, C, D) = \overline{C}\overline{D} + CD + AB\overline{D} +$$

$$(AD + CD + AB) + \overline{A}\overline{B}D$$

$$\overline{C} + \overline{D} + A\overline{B}D + \overline{A}\overline{B}D$$



$$AB + BD + \overline{A}\overline{B} = (AB + BD) + \overline{A}\overline{B}$$

④ Design a logic circuit for the given function.

Indexing:

	$\bar{A}\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$
C	0	1	3	2
D	9	5	7	6

2x4 K-Map

	$\bar{A}\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$
$\bar{C}\bar{D}$	0	1	3	2
$\bar{C}D$	9	5	7	6
CD	12	13	15	14
$C\bar{D}$	8	9	11	10

→ 1 NO

→ 2 NO

→ 4 NO

→ 3 NO

Example: $F(A, B, C, D) = \sum (0, 1, 2, 3, 6, 7, 9, 11, 14, 15)$, implement without truth table.

	$\bar{A}\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$
$\bar{C}\bar{D}$	1	1	1	1
$\bar{C}D$.	.	1	1
CD	.	.	1	1
$C\bar{D}$.	1	1	.

L_1

L_2

L_3

$$F(A, B, C, D) = \bar{C}\bar{D} + BC + AC$$

☆☆☆

$$\text{Ex: } 08 \quad f(A, B, C, D) = \sum (0, 2, 3, 4, 8, 9, 12, 13, 14, 15)$$

EDA + aDAt + ちばA + ひりA + ひき

$\bar{A} \bar{B}$	$A \bar{B}$	AB	$\bar{A} B$
1		(1)	(1)
1			
(1)	(1)	(1)	(1)
1	1		

$$F(A, B, C, D) = \overline{C}\overline{D} + \overline{A}\overline{B} + \overline{AB}D + B\overline{CD} + \overline{A} + \dots$$

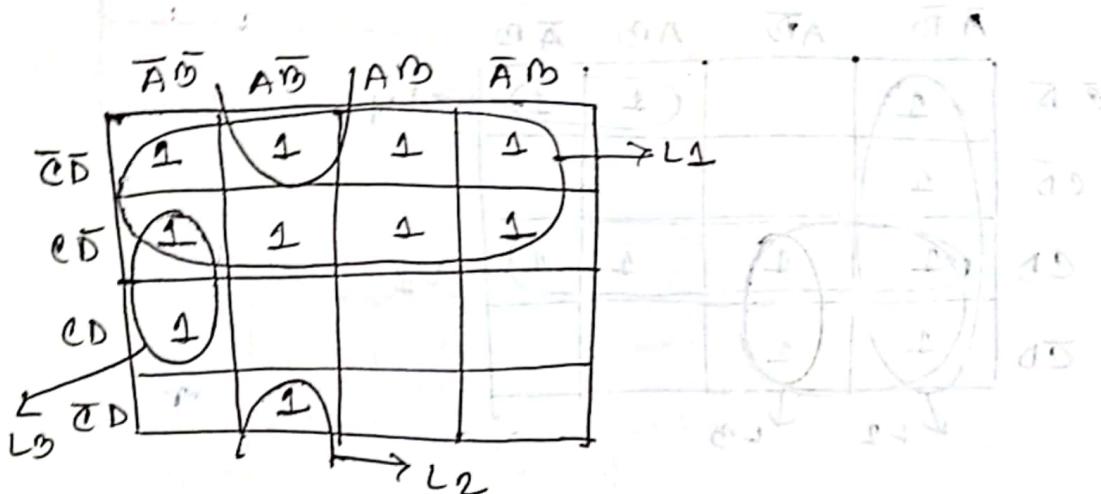
$$\underline{\text{Ex:}} \quad F(A, B, C) = \Sigma(0, 4, 4, 6, 7)$$

$$\therefore F(A, B, C) = \overline{BC} + \overline{B} \overline{C} + \overline{A} \overline{B}$$

$$= \overline{B+C} - \overline{A} \overline{B}$$

$$Q2 \quad y = \overline{C+D} + \overline{A} \overline{CD} + A \overline{B} \overline{C} + \overline{A} \overline{B} C D + A C \overline{D}$$

$$= \overline{CD} + \overline{ACD} + A\overline{DC} + \overline{ABC}CD + AC\overline{D}$$



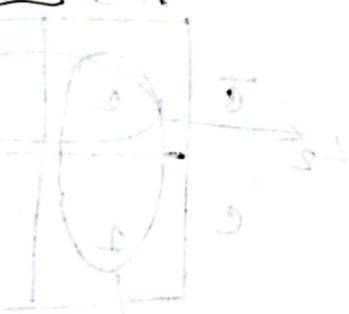
$$y = \overline{D} + \overline{ABC} + A \overline{BC} + \overline{B} \overline{A} + AB = (A+B+C) \overline{D}$$

Chapter 6

Digital Arithmetic:

$$\begin{array}{r}
 0 \\
 + 0 \\
 \hline
 00
 \end{array}
 \quad
 \begin{array}{r}
 0 \\
 + 1 \\
 \hline
 01
 \end{array}
 \quad
 \begin{array}{r}
 1 \\
 + 0 \\
 \hline
 01
 \end{array}
 \quad
 \begin{array}{r}
 1 \\
 + 1 \\
 \hline
 10
 \end{array}$$

↓ carry ↓ sum ↓ carry ↓ sum
 carry sum carry sum

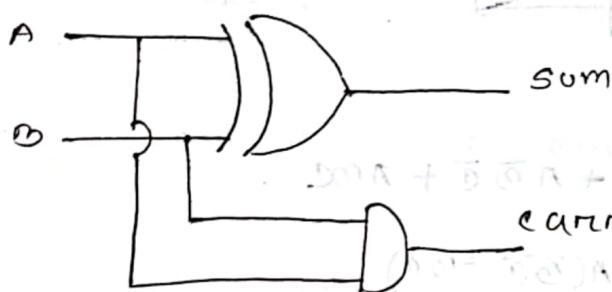


A	B	sum	carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$$\therefore \text{sum} = \bar{A}B + A\bar{B}$$

$$= A \oplus B$$

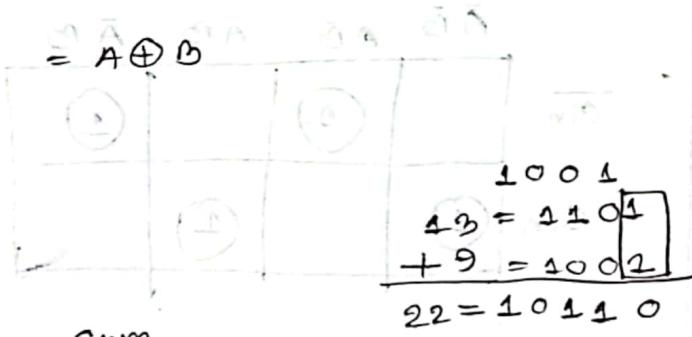
$$\text{carry} = A \cdot B$$



Half Adder: 2 Input

Full Adder: 3 Input

A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1
<u> </u>			<u>0</u>	



$$\begin{array}{r}
 1001 \\
 43 = 1101 \\
 + 9 = 1001 \\
 \hline
 22 = 10110
 \end{array}$$

	$\bar{A}\bar{B}$	$A\bar{B}$	$A\bar{B}$	$\bar{A}B$
\bar{C}_{in}		(1)		(1)
C_{in}	(1)		(1)	

→ K-Map Failed.

Boolean,

$$\text{sum} = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}\bar{C} + A\bar{B}C$$

$$= \bar{A}(\bar{B}\bar{C} + B\bar{C}) + A(\bar{B}\bar{C} + \bar{B}C)$$

$$= \bar{A}(B \oplus C) + A(\bar{B} \oplus C)$$

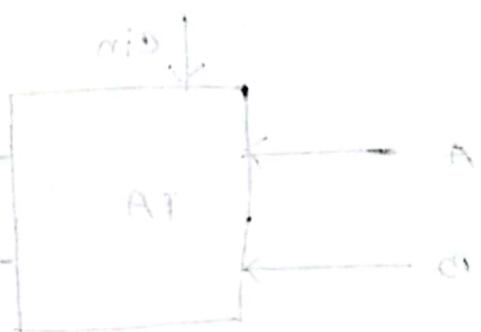
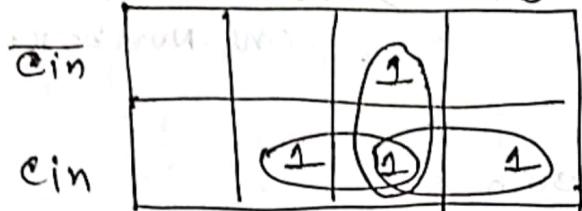
Let, $B \oplus C = x$

$$= \bar{A}x + A\bar{x}$$

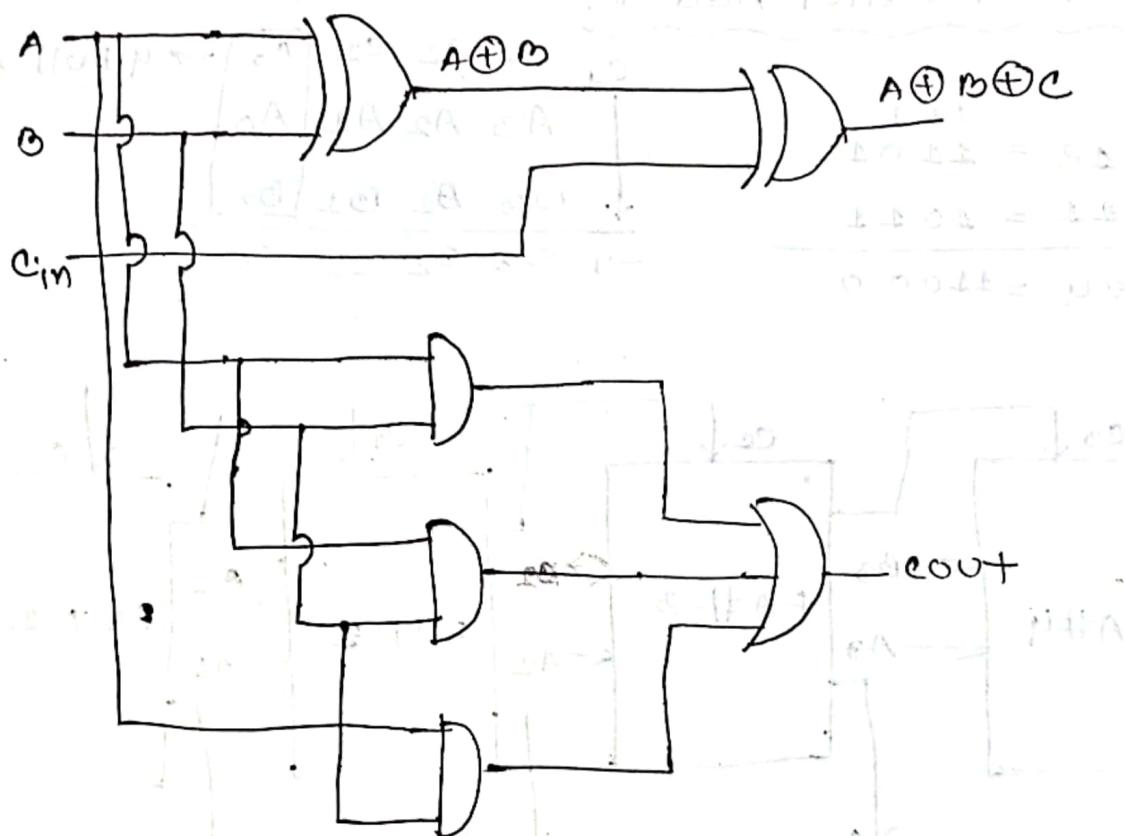
$$= A \oplus x$$

$$= A \oplus B \oplus C \quad (\text{Ans.})$$

\square $A\bar{B} + A\bar{B} + A\bar{B} + \bar{A}B$ (107) incomplete solution

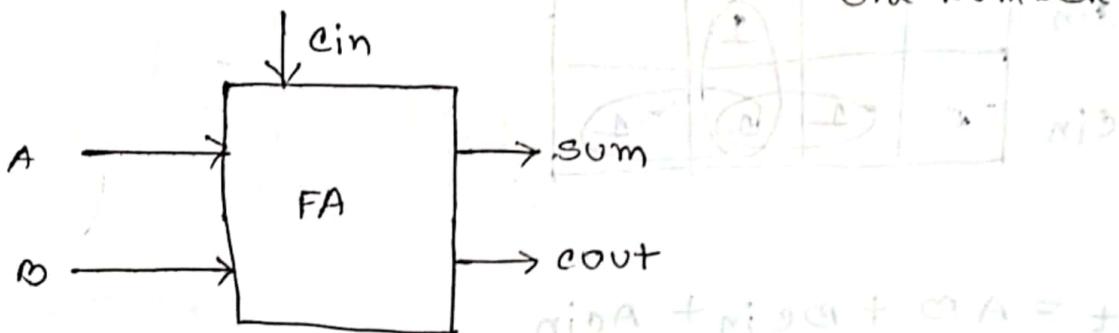


$$c_{\text{out}} = A \oplus B \text{cin} + A \text{cin}$$



= 6 gates in total.

Block Diagram: (Full Adder) \rightarrow can only sum one Number.

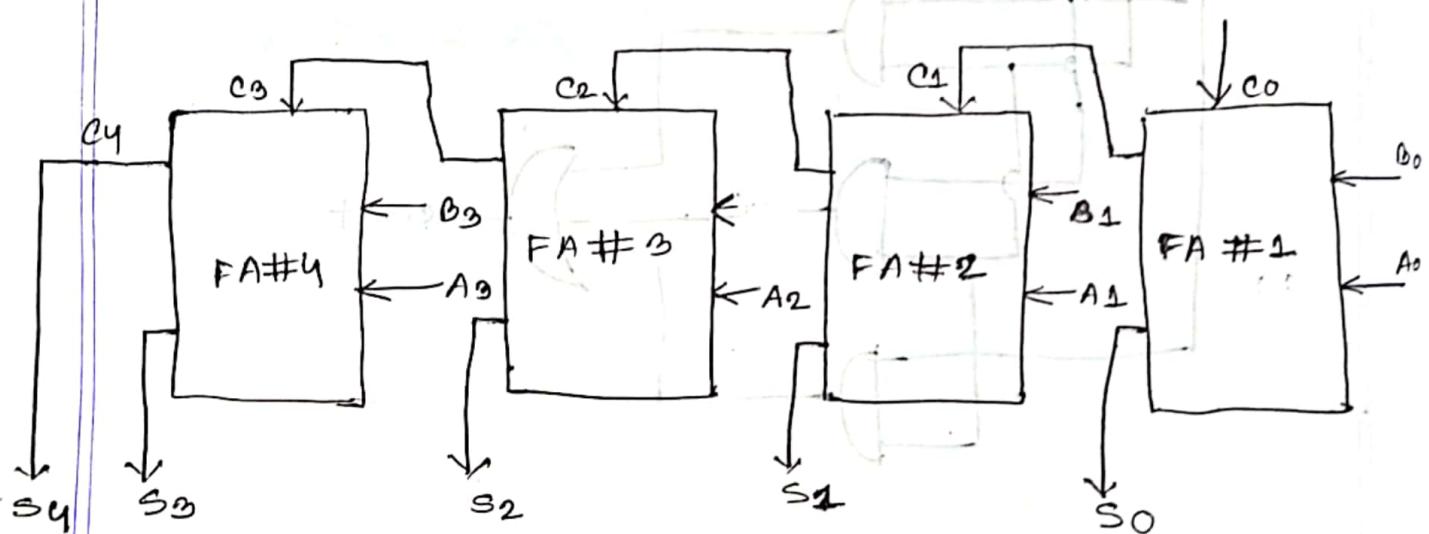
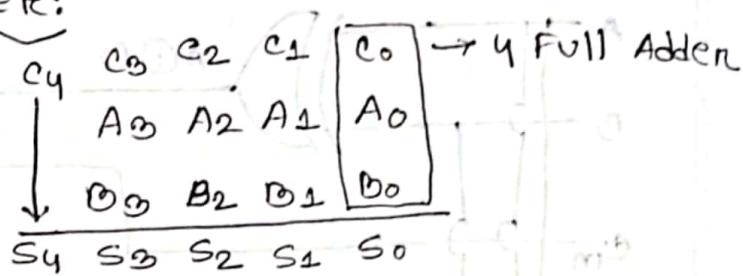


$$m_0A + m_1B + cA = f_{000}$$

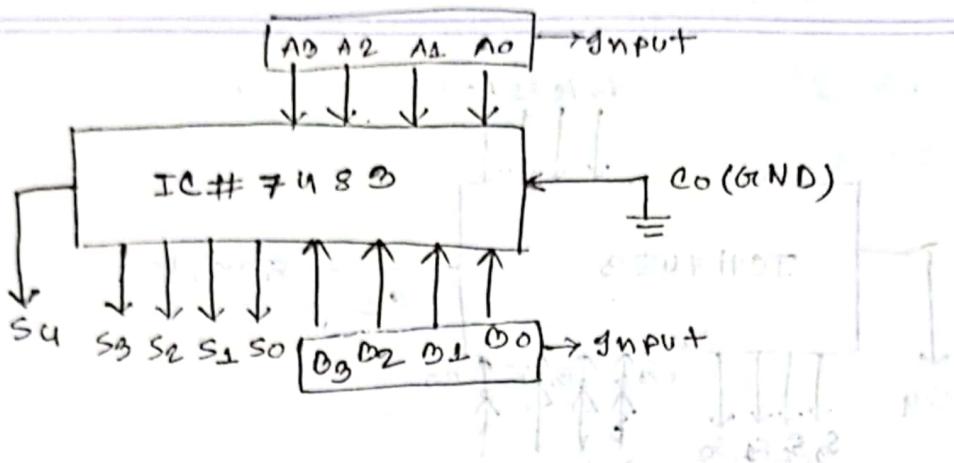
4 Bit Parallel Adder:

Addition:

$$\begin{array}{r}
 \begin{array}{r} 1101 \\ + 1011 \\ \hline 24 = 11000 \end{array}
 \end{array}$$



= 24 Total Logic Gates TC# 7483/4283



Here C_0 is not made ground by default because we can connect another adder to make 8bit/12bit adder by this open line.

4 bit parallel subtraction:

$$A - B \\ = A + (-B)$$

$$0 \rightarrow 2^{\text{'}s} = -B \\ 1^{\text{'}s} \text{ complement; } \rightarrow \text{NOT}$$

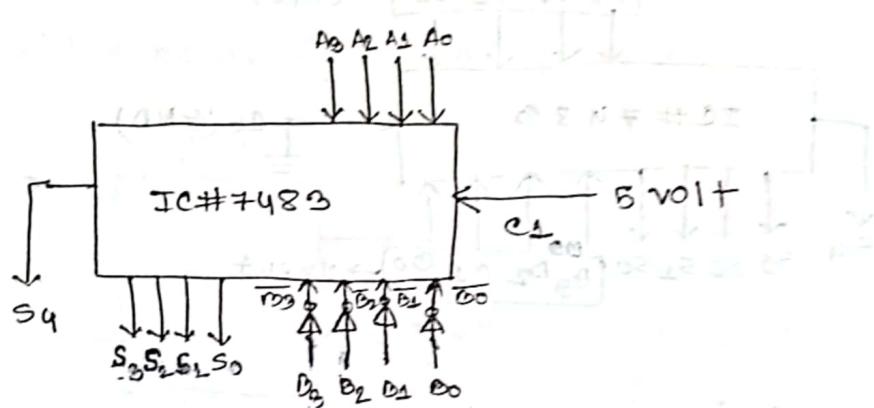
$$\overline{B_3} \quad \overline{B_2} \quad \overline{B_1} \quad \overline{B_0}$$

$$\text{output} = \overline{B_3} \overline{B_2} \overline{B_1} \overline{B_0} + 1$$

$2^{\text{'}}\text{s complement:}$

SUBTRACTOR	
81	- 35

46	
16	
16	
16	
16	



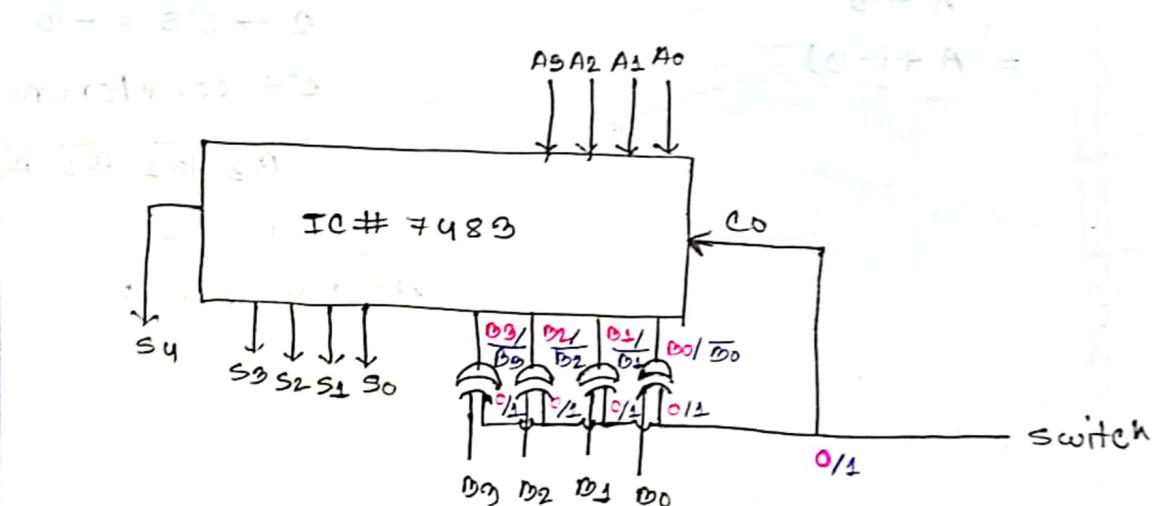
design

4 Bit Parallel Adder/Subtractor using IC #7483:

You can use other logic gates if necessary.

→ switch (S): If $S=0$ then $A+B$.

If $S=1$ then $A-B$.



XOR Truth Table:

A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

$$\begin{array}{c} \oplus \\ \Rightarrow \end{array} \rightarrow \text{XOR}$$

If $S=0$ then, 1st inputs are $A_3 A_2 A_1 A_0$
 2nd inputs are $B_3 B_2 B_1 B_0$
 and $C_0 = 0$.
 ∴ This is addition.

If $S=1$ then, 1st inputs are $A_3 A_2 A_1 A_0$.
 2nd inputs are $\bar{B}_3 \bar{B}_2 \bar{B}_1 \bar{B}_0$.
 and $C_0 = 1$.
 ∴ This is subtraction.

BCD Adder:

• What is BCD? \Rightarrow Binary Coded Decimal

\rightarrow Coding system

\rightarrow

0	$\rightarrow 0000$	}
1	$\rightarrow 0001$	
2	$\rightarrow 0010$	
3	$\rightarrow 0011$	
4	$\rightarrow 0100$	
5	$\rightarrow 0101$	
6	$\rightarrow 0110$	
7	$\rightarrow 0111$	
8	$\rightarrow 1000$	
9	$\rightarrow 1001$	

BCD code of 0 to 9.

$$\begin{array}{r}
 32 \rightarrow \boxed{0011} \quad \boxed{0010} \\
 96 \rightarrow \boxed{0100} \quad \boxed{0110} \\
 \hline
 78 \rightarrow \underline{0111} \quad \underline{1000}
 \end{array}$$

initiated at point 1.

$$85 \Rightarrow 1000 \quad 0101 \quad @ \text{greater than}$$

9 = Error

$$76 \Rightarrow 0111 \quad 0110 \quad @ \text{correct this Error}$$

$$161 \Rightarrow 1111 \quad 1011$$

$$0110 \quad 0110$$

$$\boxed{0001} \quad \boxed{0110} \quad \boxed{0001}$$

} why to add +6

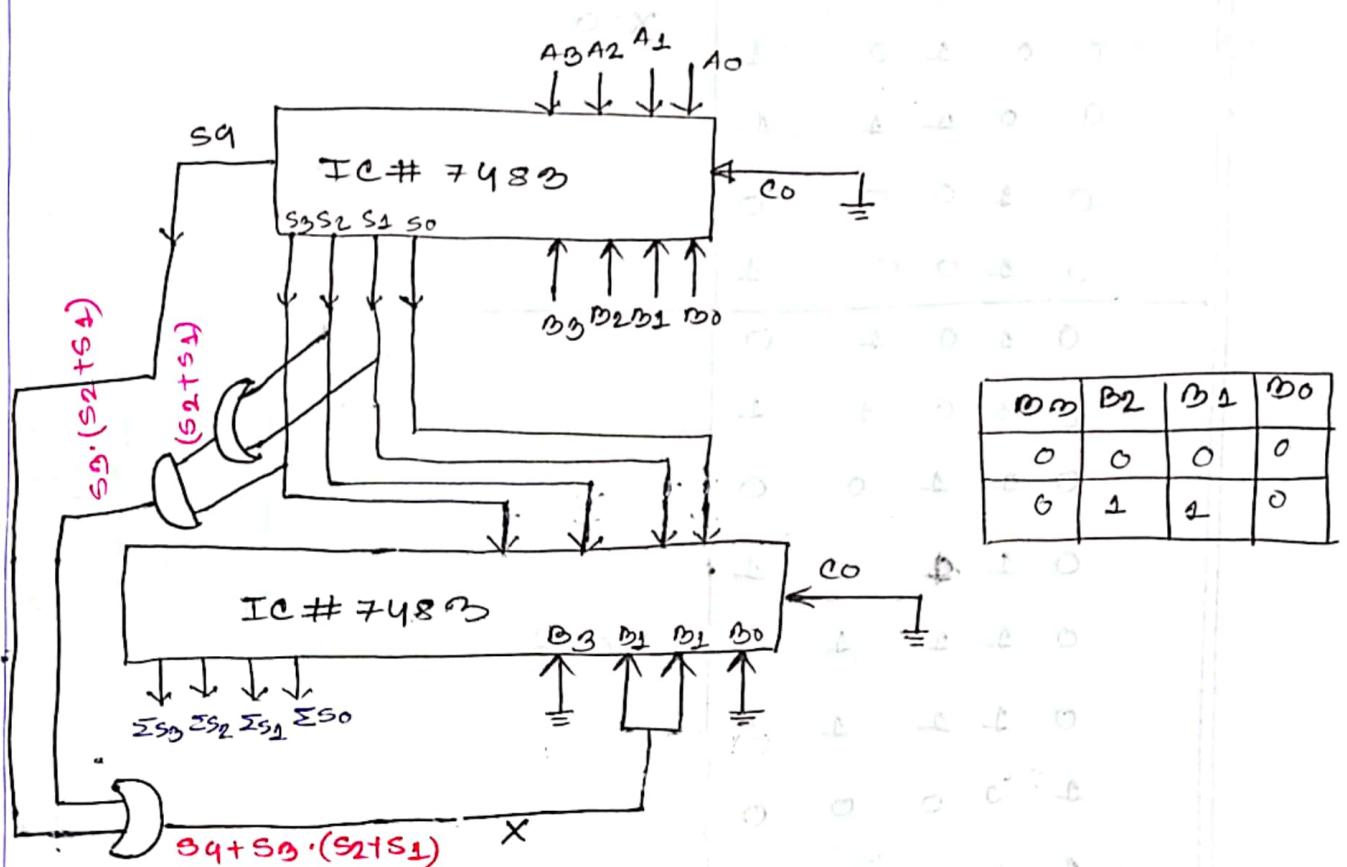
when BCD addition
is greater than 9?

$$\begin{array}{l}
 9 \rightarrow 1001 \\
 \downarrow \text{overflow error from 1000} \\
 \rightarrow 10 \rightarrow 0001 - 0000 = 100 (+6)
 \end{array}$$



BCD Adder Using Logic Gates:

- ④ If sum > 9 , then add 6.
 - ⑤ If sum ≤ 9 , then add 0.



- ⊗ If sum ≤ 9 then $x=0$.
 - ⊗ If sum > 9 then $x=1$

- ④ DCD addition can be maximum $(9+9) = 48$.

s_4	s_3	s_2	s_1	s_0	X	Display
0	0	0	0	0	0	0000
0	0	0	0	1	1	1111
0	0	0	1	0	2	1010
0	0	0	1	1	3	1101
0	0	1	0	0	4	0000
0	0	1	0	1	5	1111
0	0	1	1	0	6	1010
0	0	1	1	1	7	1101
0	1	0	0	0	8	0000
0	1	0	0	1	9	1111
0	1	0	1	0	10	1010
0	1	1	0	1	11	1101
0	1	1	1	0	12	0000
0	1	1	1	1	13	1111
1	0	0	0	0	14	0000
1	0	0	1	0	15	1111
1	0	0	1	1	16	1010
1	0	0	1	0	17	1101

$x=0$

input 0000

$x=1$

input 1111

0000

Q) Flip-Flop and Related Devices:

What is Flip-Flop?

Ans:

Flip-Flop is a device

where there is one input

or Many inputs.

Assignment #1:

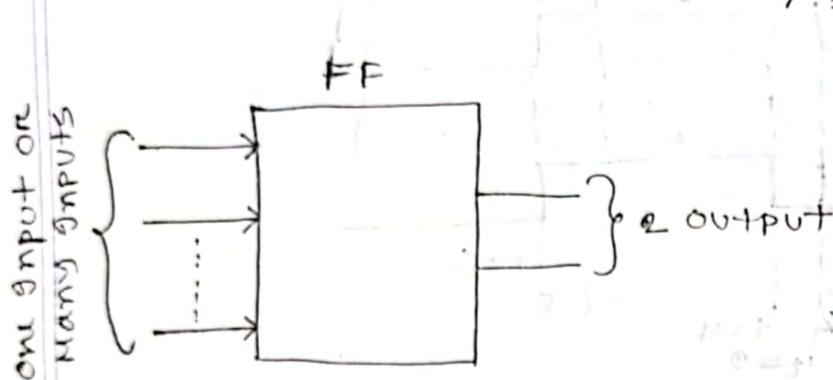
write a short note on
Flip-Flop.

→ 20 Marks.

→ Not more than 4 page.

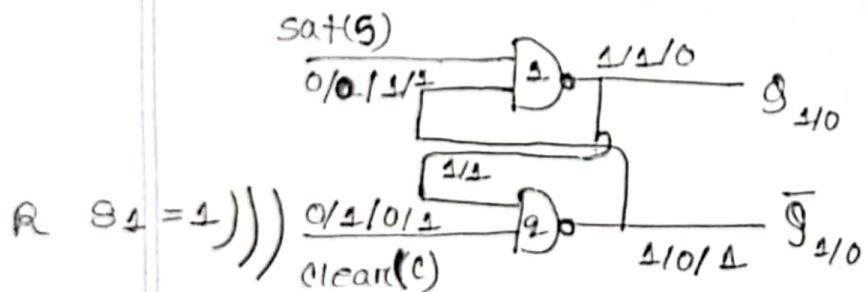
→ No cover notes.

→ 16th August.



one input is opposite of other output.

NAND latch:



Truth Table:

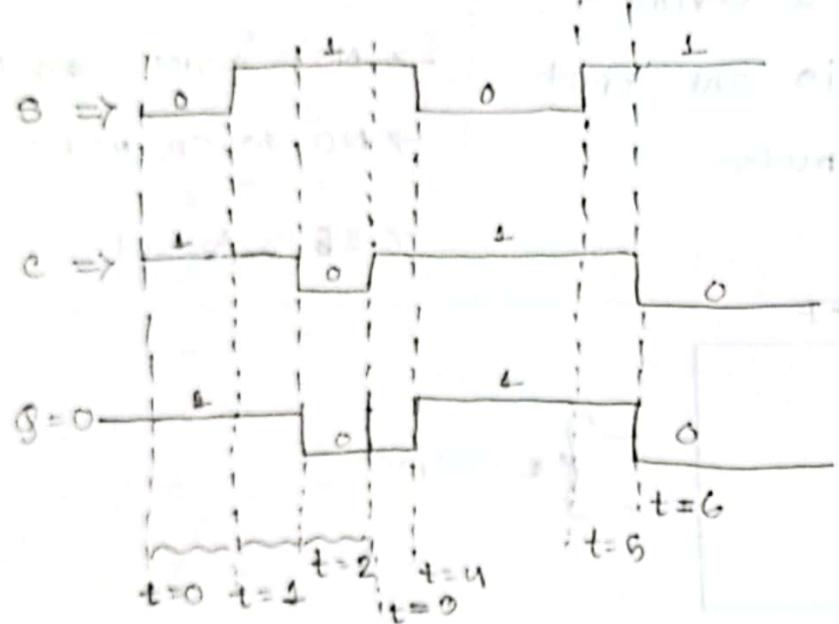
S	C	Q
0	0	Invalid
0	1	1
1	0	0
1	1	No change

at initially, $Q=0$, then finally $Q=1$

$S = 1$, $C = 0$, $Q = 0$, $S = 0$, $C = 1$, $Q = 1$

so it's a positive edge triggered

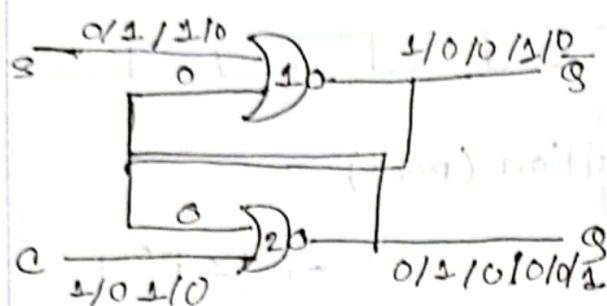
b) Wave-form Diagram of NAND latch:



Draw the waveform of Q .

NOR Latch:

Internal circuit:



NOR gate:

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

If initially $Q=0$ turn

finally $Q=0$.

If initially $Q=1$ turn

finally $Q=1$.

Truth Table:

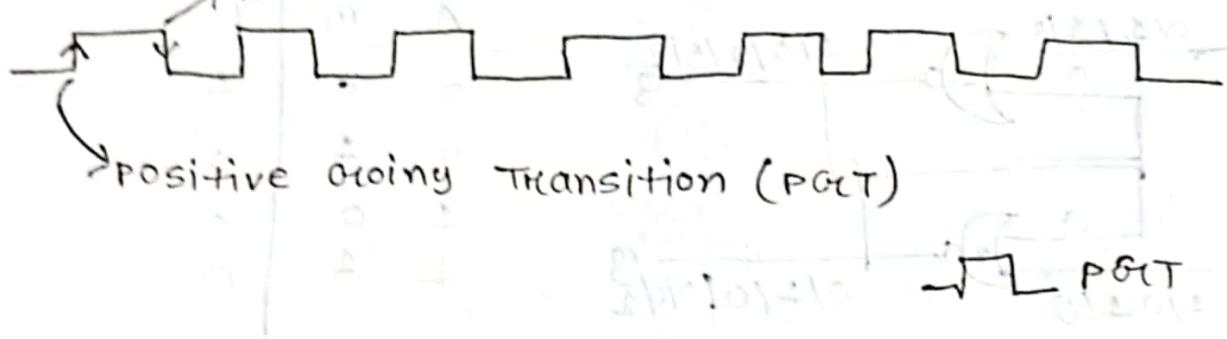
S	C	Q
0	0	NO change
0	1	0
1	0	1
1	1	invalid

Waveform diagram of NOR Gate:



Clocked S-C FLIP FLOP:

clock: negative going transition (NGT)



PGT

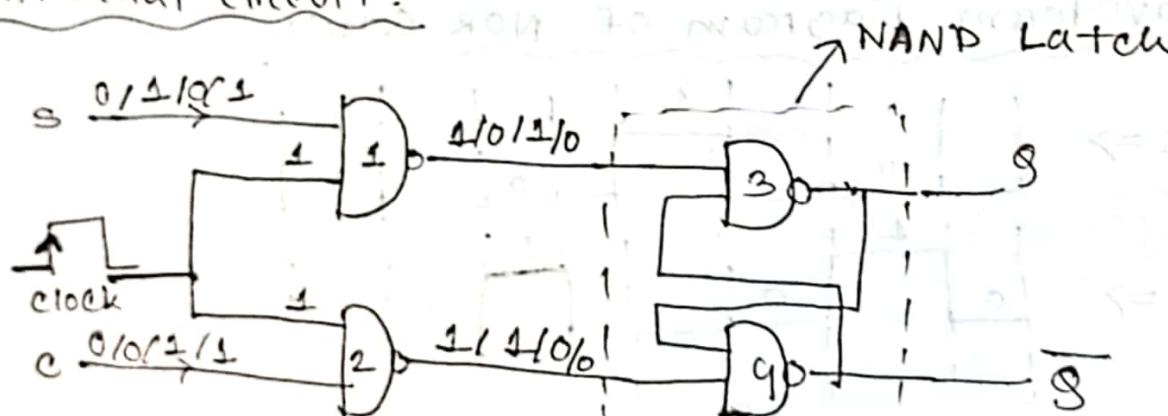
Δ

NGT

$$\text{Freqency } f = \frac{1}{T}$$

1Hz No of oscillation
per second

Internal circuit:

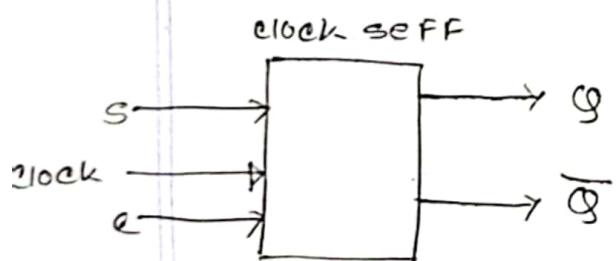


<u>s</u>	<u>c</u>	<u>clock</u>	<u>Q</u>
0	0	↑	NO change
0	1	↑	0
1	0	↑	1
1	1	↑	invalid

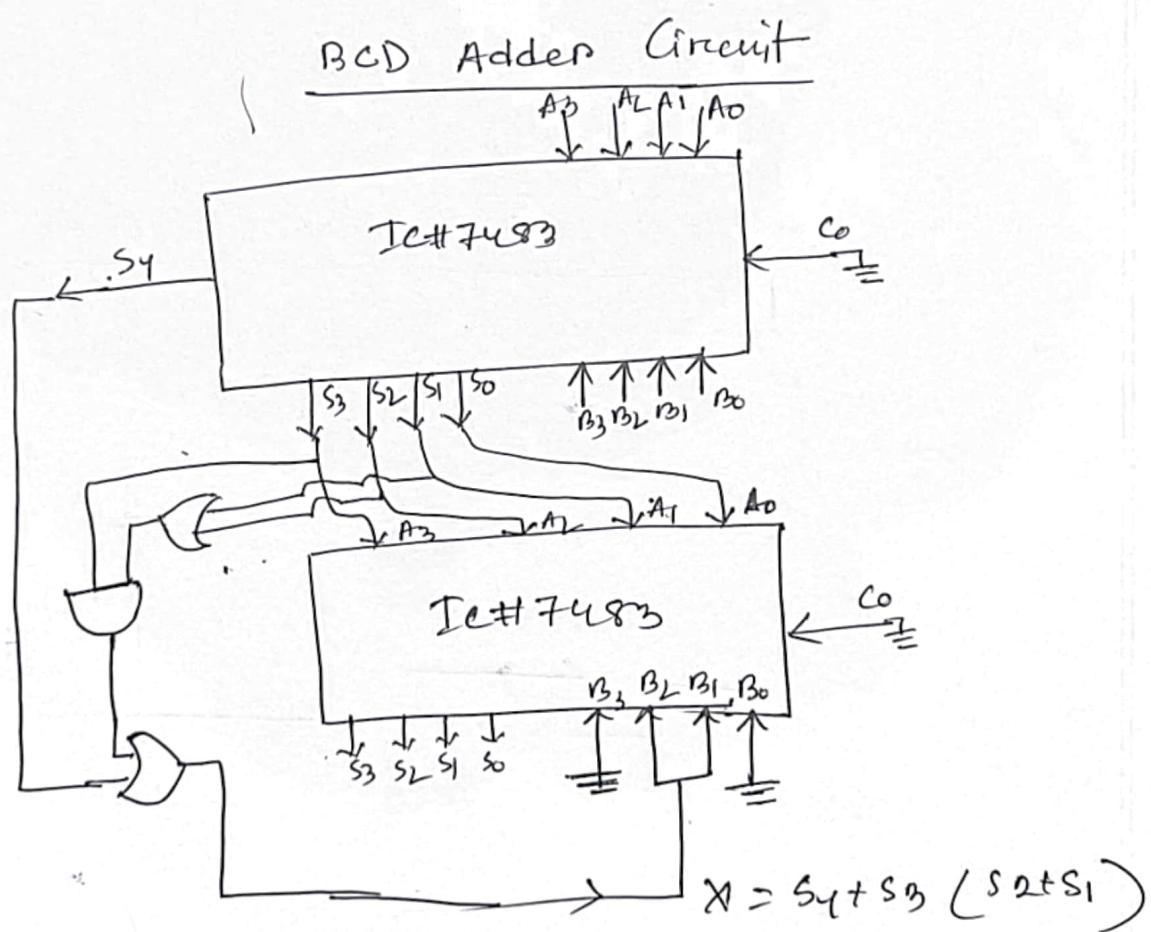
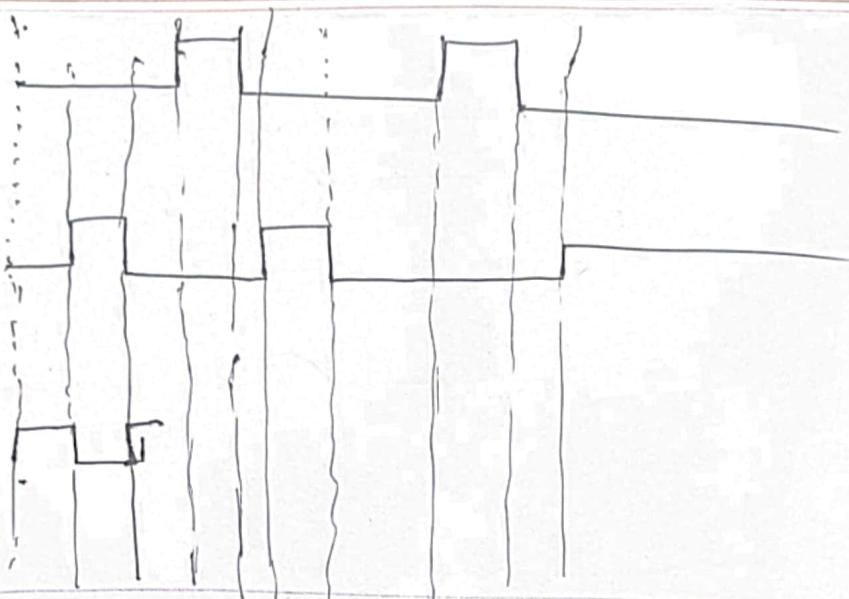
NAND Table:

<u>SA</u>	<u>C⊕M</u>	<u>Y</u>
0	0	invalid
0	1	1
1	0	0
1	1	NO change

Block diagram:



Waveform diagram of clock SCFF



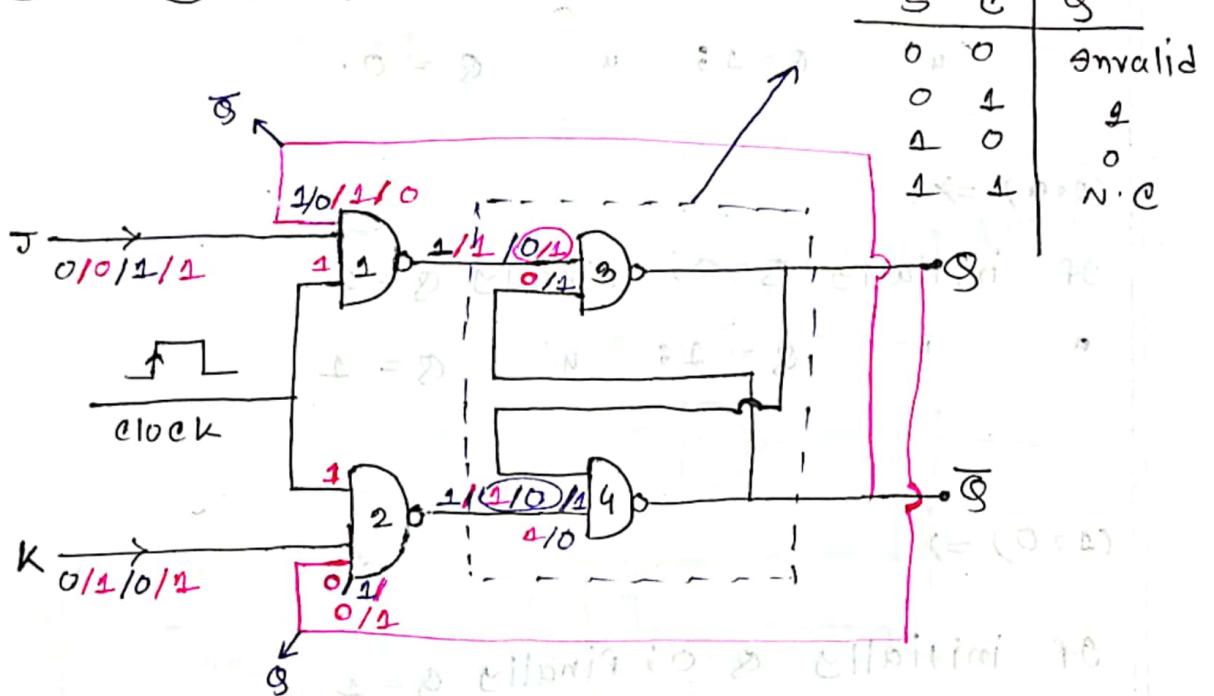
if $\text{sum} > 9$, then $X = 1$

if $\text{sum} \leq 9$ then $X = 0$

VV I

*** clock JK flip flop: (complete flip flop)

internal circuit:



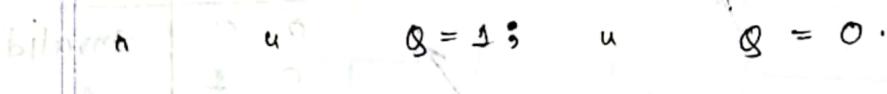
Operation and Truth Table:

J	K	clock	Q
0	0	↑	NO change
0	1	↑	Set (1)
1	0	↑	Reset (0)
1	1	↑	Toggle (opposite)

$(0,1) \Rightarrow$

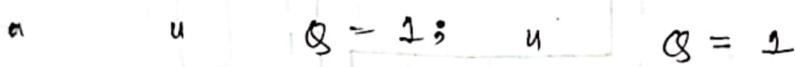
(quill quill of signals) quill quill at length

if initially $Q=0$; finally $Q=0$ ~~no change~~



$(1,0) \Rightarrow$

if initially $Q=0$; finally $Q=1$



$(1,1) \Rightarrow$

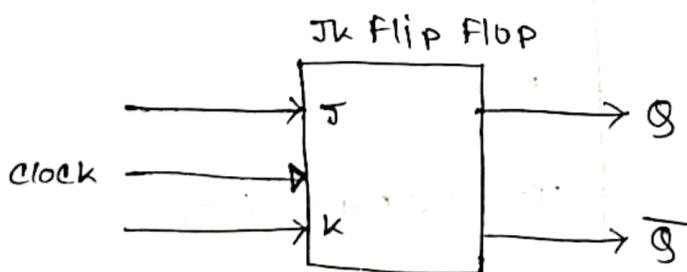
if initially $Q=0$; finally $Q=1$

~~so don't have waiting~~

$u \quad u \quad Q=1; \quad u \quad Q=0$

why complete Flip Flop?

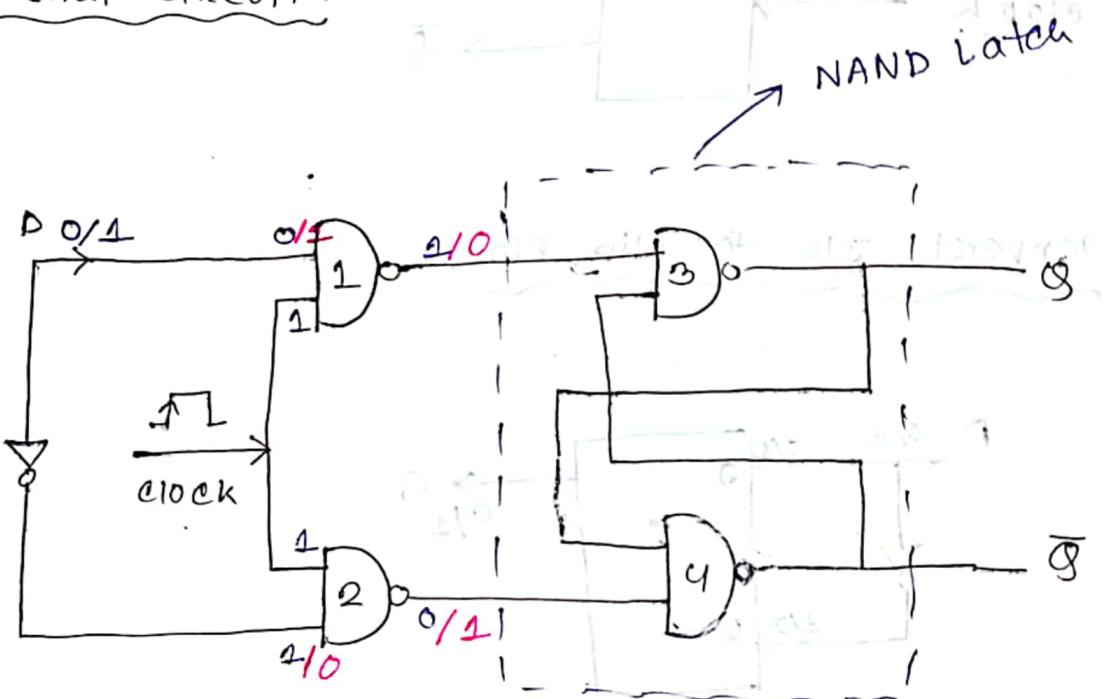
Block Diagram:



Find out where did JK came from? H.W.

Clock D flip flop:

Internal circuit:



Operation and Truth Table:

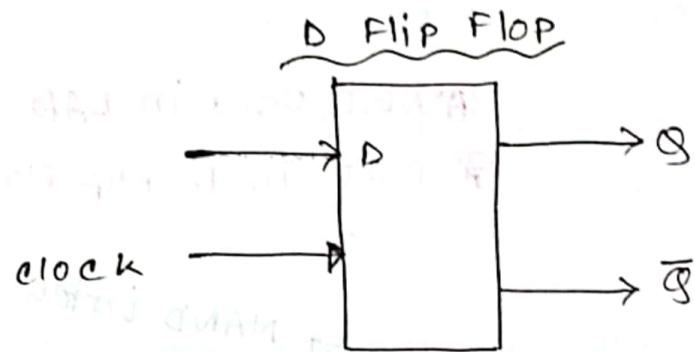
D	clock	Q
0	↑	0
1	↑	1



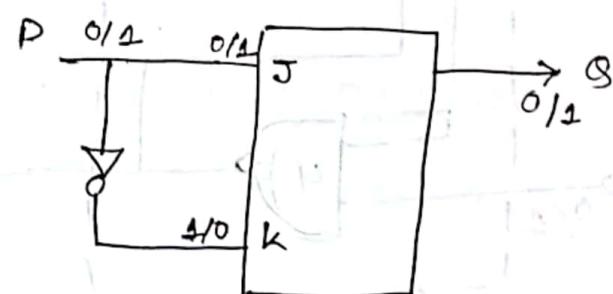
MOD 60 counter used in clock.

MOD 10 = BCD counter (0 to 9)

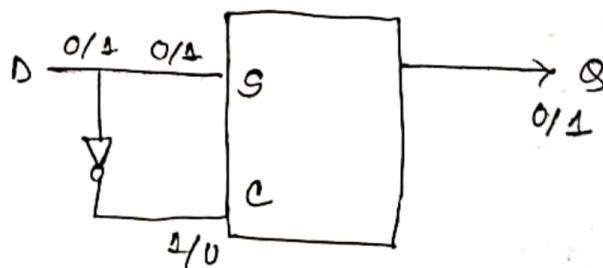
Block Diagram: ~~and its truth table for initial~~



convert JK to Flip Flop:



convert clock SC to D flip flop:



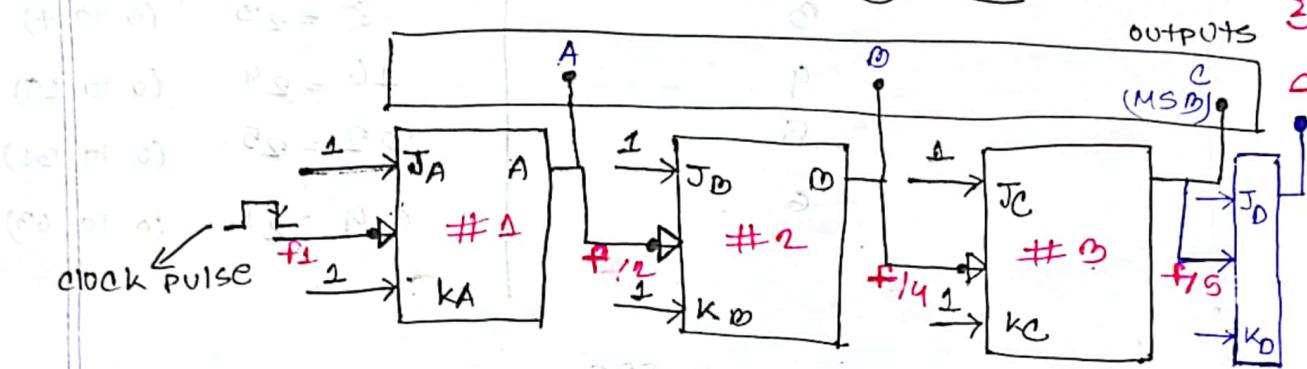
S-C:

S	C	clk	Q
0	0	↑	N.C.
0	1	↑	0
1	0	↑	1
1	1	↑	Invalid

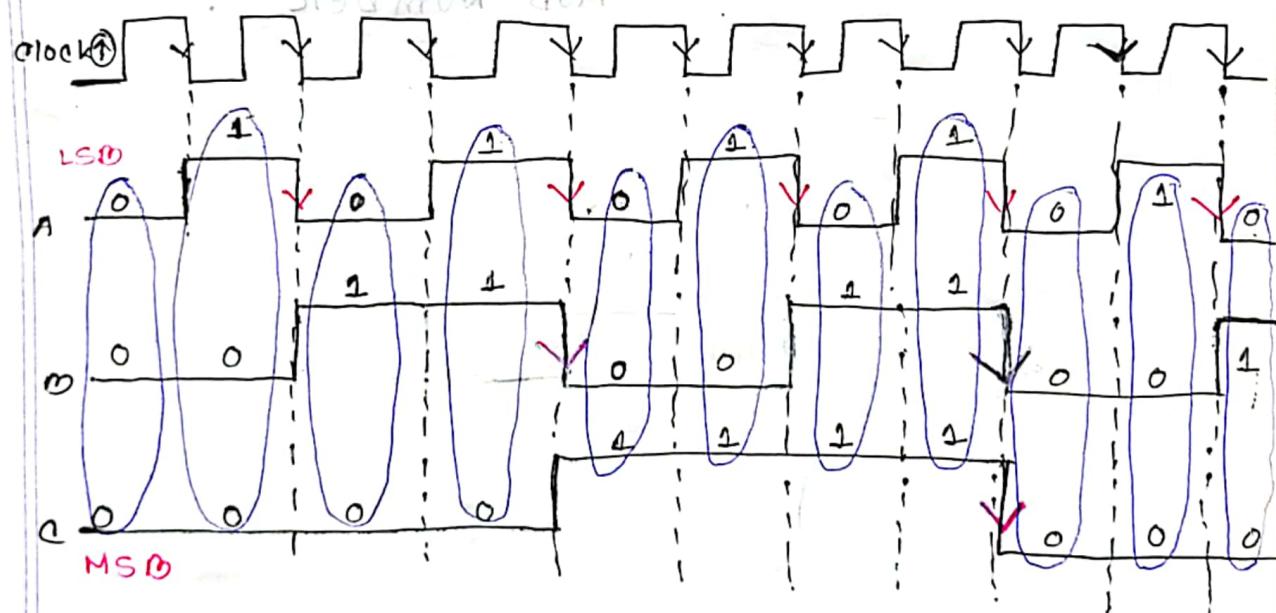
Thursday : counter. ~~star~~ to do : ~~maximum value~~

counter:

counting and Frequency Division: (NGT use)



Initially, $A=B=C=0$ [FOR MOD 8 counter]



0 to 7 \Rightarrow Mod 8 up counter.

MOD Number: No of different steps of the counter is called MOD Number.

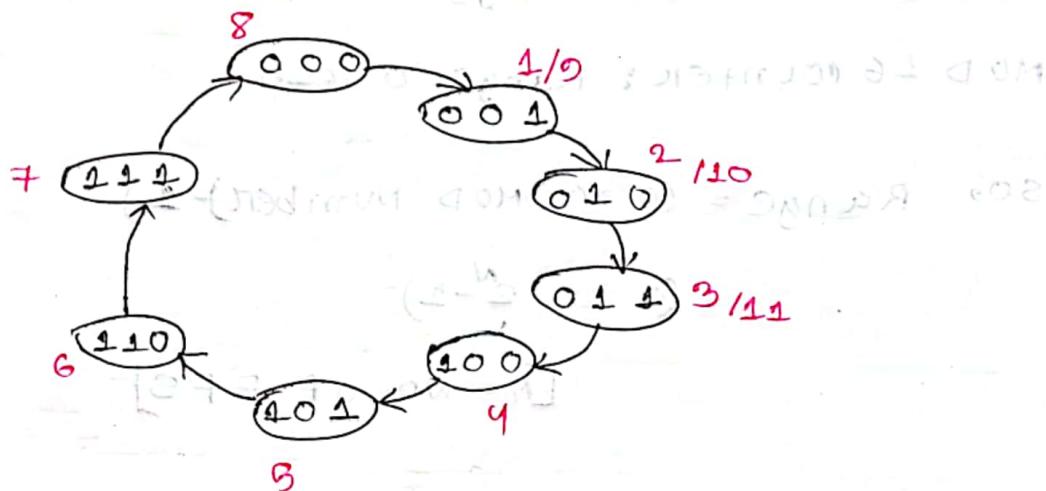
<u>NO. of FLIP FLOP</u>	<u>MOD Number</u>
3	$8 = 2^3$ (0 to 7)
4	$16 = 2^4$ (0 to 15)
5	$32 = 2^5$ (0 to 31)
6	$64 = 2^6$ (0 to 63)

(i) Mod Number = $2^{\text{No. of ffs}}$

(ii) Output Frequency = $\frac{\text{Input Frequency}}{\text{Mod Number}}$

Output = $Q_1 \oplus Q_2 \oplus Q_3$

state transition diagram:



If initial state is 000.

④ Find the state after 11 pulse.

⑤ Find the state after 129 pulse?

$$\Rightarrow \frac{129}{8} = 16 \text{ remainder } 1$$

$$\frac{48}{4} = 12 \text{ remainder } 0$$

$$12 \rightarrow 001$$

(decimal)

⑥ If initial state is 101, what is the state after 139 pulse?

Ans:

$$\Rightarrow 139 + 5 = 144$$

$$\frac{144}{8} = 18 \text{ remainder } 0$$

$$\frac{56}{4} = 14 \text{ remainder } 0$$

$$\frac{24}{4} = 6 \text{ remainder } 0$$

$$6 \rightarrow 011$$

Range:

MOD 8 counter : Range 0 to 7

MOD 16 counter : Range 0 to 15

so, Range = (0 to MOD Number - 1)

$$= (0 \text{ to } 2^N - 1)$$

[N = No of FFs]

- # There are 6 flip flops connected like this:
their outputs are:

Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
-------	-------	-------	-------	-------	-------

- Determine the mod number of the counter.
- Determine the output frequency in kHz if in. frequency is 12 MHz.
- What is the range of the counter.
- If initial state is 101101, find the state after 120 pulses.

(a) $2^6 = 64$ [MOD Number]

(b) $O.F = \frac{I.F}{M.N} = \frac{42 \times 10^3 \text{ kHz}}{64} \text{ kHz}$ [$1 \text{ MHz} = 1000 \text{ kHz}$]
= 187.5 kHz

(c) Range = 0 to 63

(d) $95 + 129 = 224$

$$\begin{array}{r} 64 | 224 | 2 \\ \underline{-128} \\ 96 \end{array} \rightarrow \boxed{\begin{array}{r} 92 | 148 | 4 | 2 | 1 \\ \underline{-104} \\ 10 \end{array}}$$

2nd CT : 24.08.2025 → chapter 58 6.

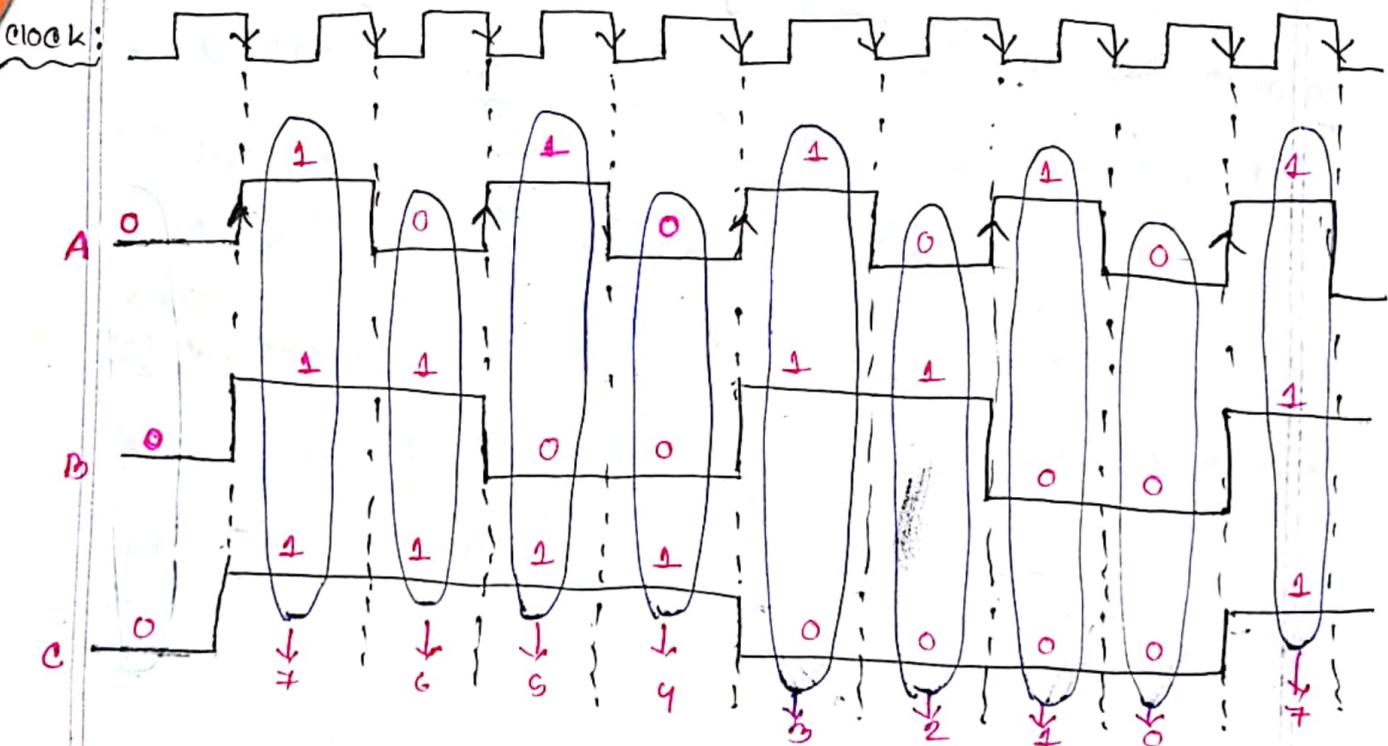
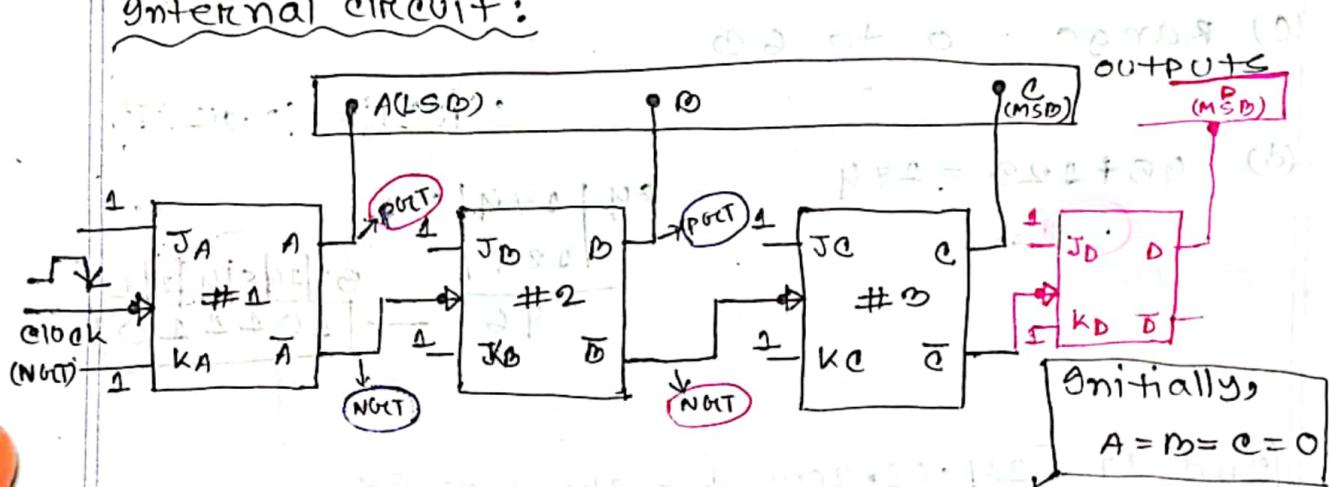
MOD 8 Down Counter: (+ to 0)

Down counter = Highest to Lowest.

Range of MOD 8 down counter : (+ to 0)

(111 to 000)

Internal circuit:

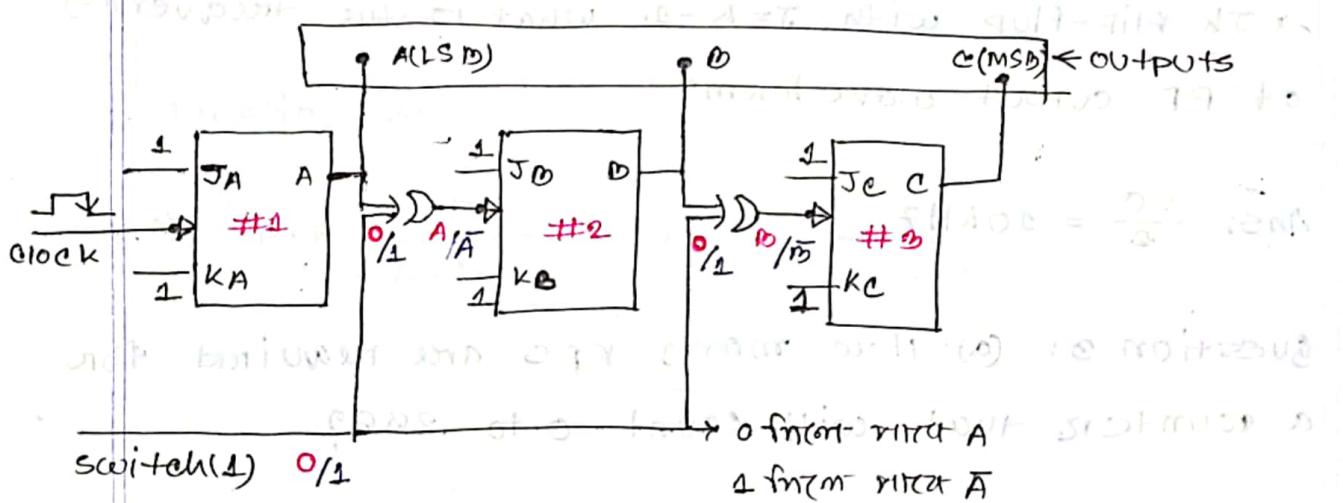


④ BCD to 7 segment display
#IC

⑤ A NGT output zu einer PGT output, same input

design MOD 8 UP/DOWN counter using JK flip flop, you can use other logic gates if necessary.

→ switch(a); if $s=0$ then UP counter.
if $s=1$ then DOWN counter.



Application:

If $s=0$ then 2nd clock pulse = A

• command 3rd. clock pulse = B

If $s=1$ then 2nd clock pulse = \bar{A}
and 3rd clock pulse = \bar{B}

8 bit binary number + 4 bit BCD =

10101010

7 segment display:

$f \begin{array}{|c|} \hline a \\ \hline g \\ \hline b \\ \hline \end{array} \rightarrow \text{G} \rightarrow 7 \text{ segment display for clock}$

and NO DMUL methods around 2004 applied
conversion of 8 bit binary into 320 and 200

question 2: A 20 kHz clock signal is applied to
a JK flip-flop with $J=K=1$. What is the frequency
of FF output waveform?

Ans: $\frac{20}{2} = 10 \text{ kHz}$



Question 3: (a) How many FFs are required for a counter that will count 0 to 256?

Ans: $2^N = 2^8 = 256 \therefore 8 \text{ Flip Flops}$

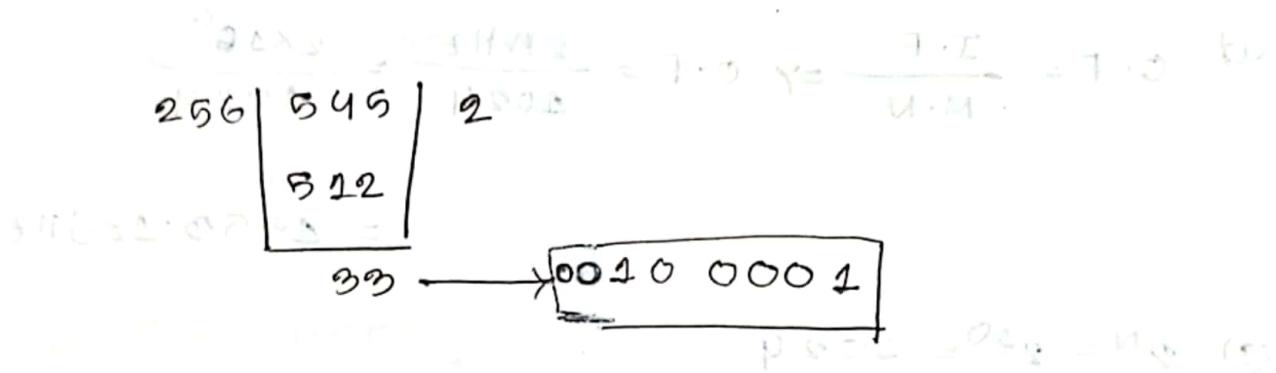
Question 4:

(a) Ans: Mod Number = $2^N = 2^8 = 256$

$$O.F = \frac{I.F}{M.N} = \frac{312 \text{ kHz}}{256} = 1.2 \text{ kHz}$$

(b) Ans: $1100 \downarrow = 25$

$$\therefore 2+520 = 545 \text{ Octal pass band width (b)}$$



Question 9:

(a) $O.F = \frac{I.F}{M.N} \Rightarrow 256 \text{ kHz} = \frac{256 \text{ kHz}}{M.N}$

~~Only 256 kHz is present~~

$$\Rightarrow M.N = 128$$

(b) Range $\Rightarrow 0 \text{ to } 127$

Question 6:

$$Q.S = 400 \text{ dB } (10)$$

(a) $2^N = 2^{10} = 1024 \rightarrow 10 \text{ FFS} = 0.25 + 8 \text{ dB}$

(b) $O.F = \frac{I.F}{M.N} \Rightarrow O.F = \frac{2 \mu \text{Hz}}{1024} = \frac{2 \times 10^6}{2^{10} \cdot 1024}$

~~2048~~ → 800

$$= 1963.125 \text{ Hz}$$

(c) $2^N = 2^{10} = 1024$

(d)

$$\begin{array}{r} 2024 \\ \overline{)2060} \end{array} \quad \begin{array}{r} 2 \\ \overline{)2048} \end{array} \quad \begin{array}{r} 2 \\ \overline{)12} \end{array} \quad \begin{array}{r} 1000 \\ 1100 \end{array}$$

← $\frac{1.1}{1.1} = 1.0 \quad (1)$

Question 8:

(a) Ans:

$$+8.4 \text{ dB } O.S = 50 \mu \text{W} \quad (2)$$

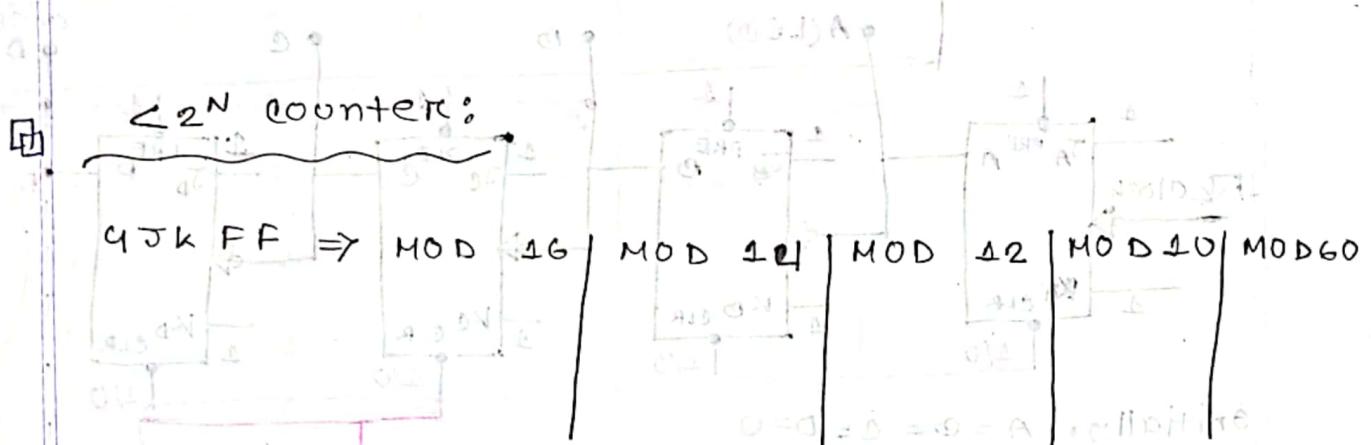
題 Counter: 由 8 位的二進制數字到 64 位的模數器

MOD 8 → 8 位二進制數字到 8 位 MOD 8 → 911

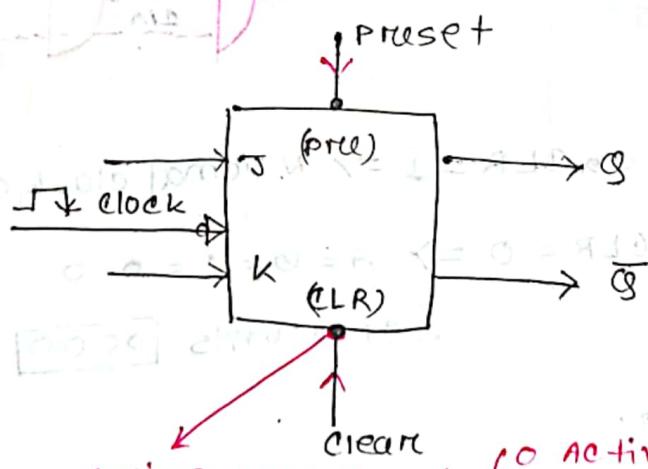
MOD 16 } 2^N counter

MOD 32

MOD 64



題 Asynchronous Inputs JK flip flop:



Active low input (0 active 1 Inactive)

PRE	C LR	Q	Notes
0	0	Not used	
0	1	1	
1	0	0	
1	1	Normal clock operation	Normal clock

題 FOR NORMAL JK: set PRESET

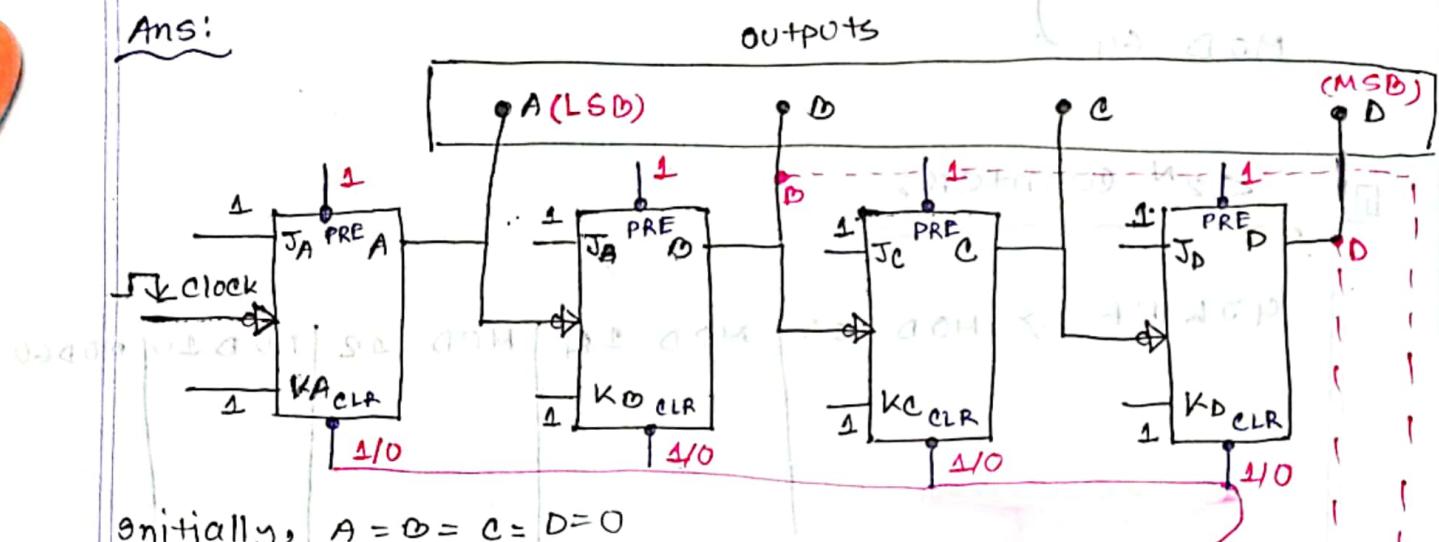
and clear by default 1 input.

題 NO ASYNCHRONOUS found in market.

works like Normal JK

Q Design MOD 40 UP counter using JK flip flop. You can use other logic gates if necessary.

Ans:



Initially, $A = B = C = D = 0$

operations:

For $(0 \rightarrow 0)$: $\text{PRE} = 1, \text{CLR} = 1 \Rightarrow$ Normal clock operation

For $1 \rightarrow 0$: $\text{PRE} = 1, \text{CLR} = 0 \Rightarrow A = 1 = C = D = 0$

$\therefore 0 + 0 \text{ counts } [0000]$

\therefore After 0 it comes 0.

This is MOD 40 UP counter.

Normal clock operation \rightarrow pre(A), CLR(A)

(0-10%) 140:

D	C	B	A	
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	(0000 1A)
0	1	0	0	PRE = 1 ✓
0	1	0	1	CLR = 1
0	1	1	0	(0001 01)
0	1	1	1	A = 0
1	0	0	0	4 = 0
1	0	0	1	
✓ 0	✓ 1	0		PRE = 1 ✓
				CLR = 0
USE NAND Gate to get 0 for D BY D = 1 1.				

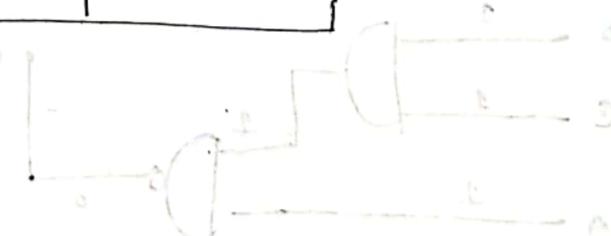
Above

10
↓

2

use NAND
Gate
to get 0 for
 $D \oplus D = 1$

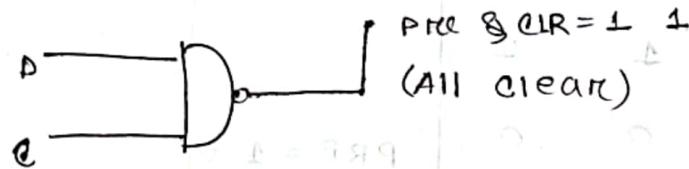
$$\text{PRE} = 1$$



MOD 12:

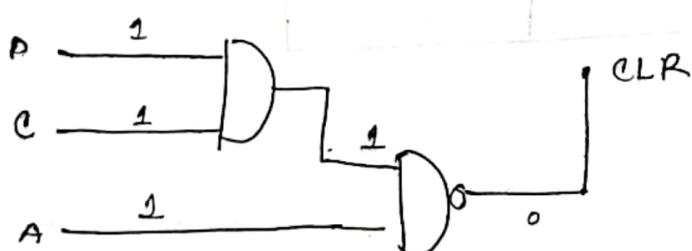
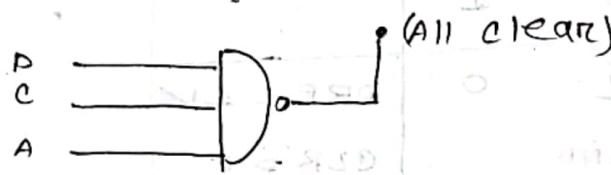
0 to 11

$$\begin{array}{r} D \ C \ B \ A \\ \hline 1 \ 1 \ 0 \ 0 \end{array} \rightarrow$$

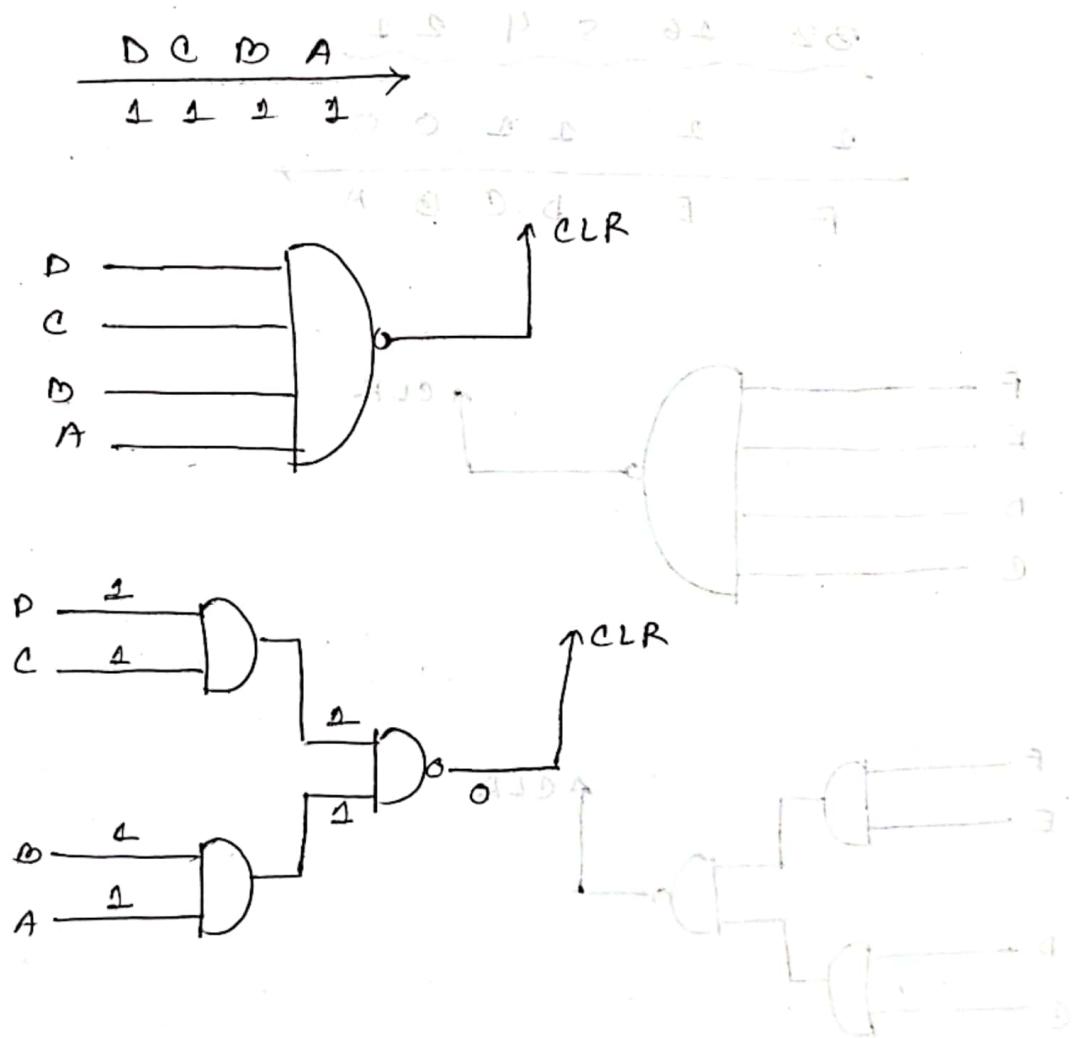


MOD 13% (0 to 12)

$$\begin{array}{r} D \ C \ B \ A \\ \hline 1 \ 1 \ 0 \ 1 \end{array} \rightarrow$$

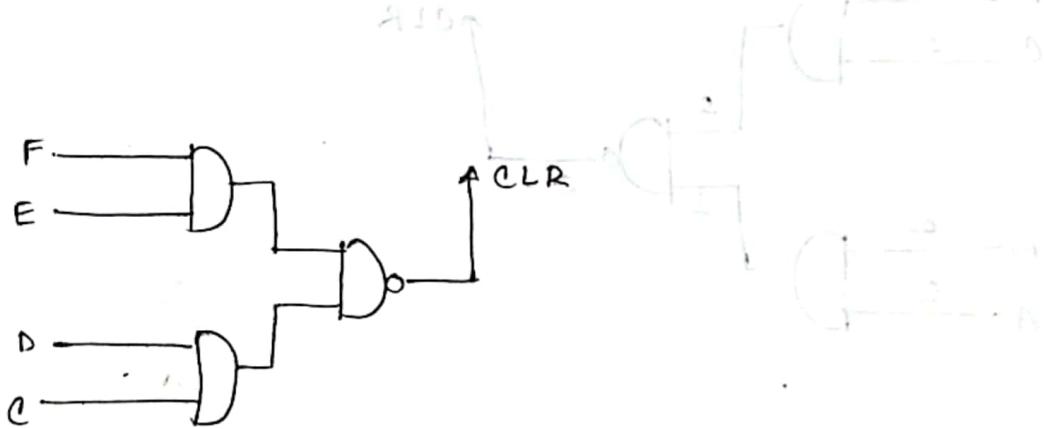
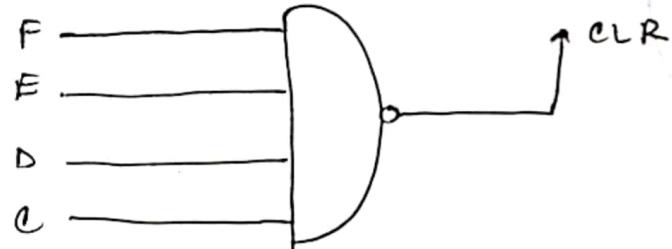
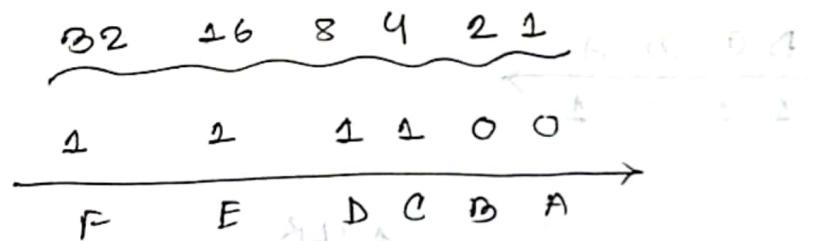


MOD 15: (0 to 29)



IC# 74293

MOD 60 UP Counter:

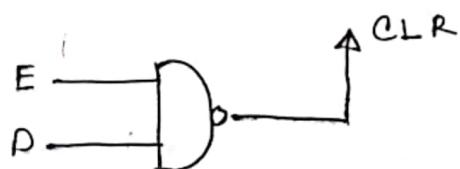


Hour Hand: 0 to 23 (to make clock)

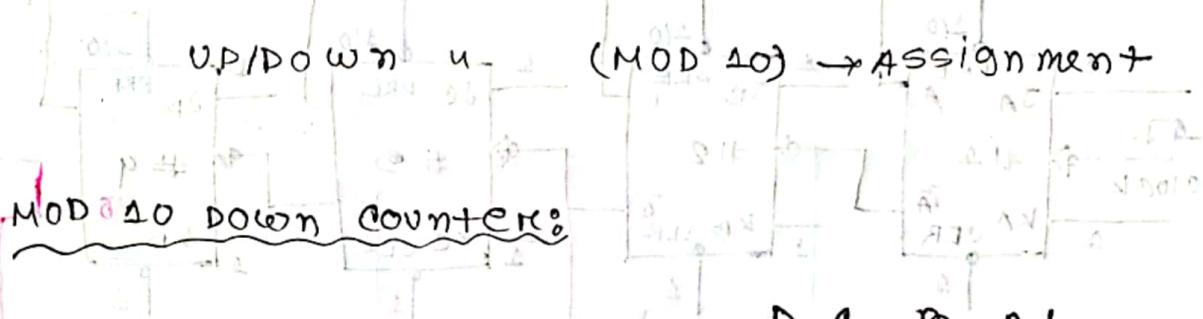
MOD 24

Binary Counter State:

E	D	C	B	A
16	8	4	2	1
1	1	0	0	0

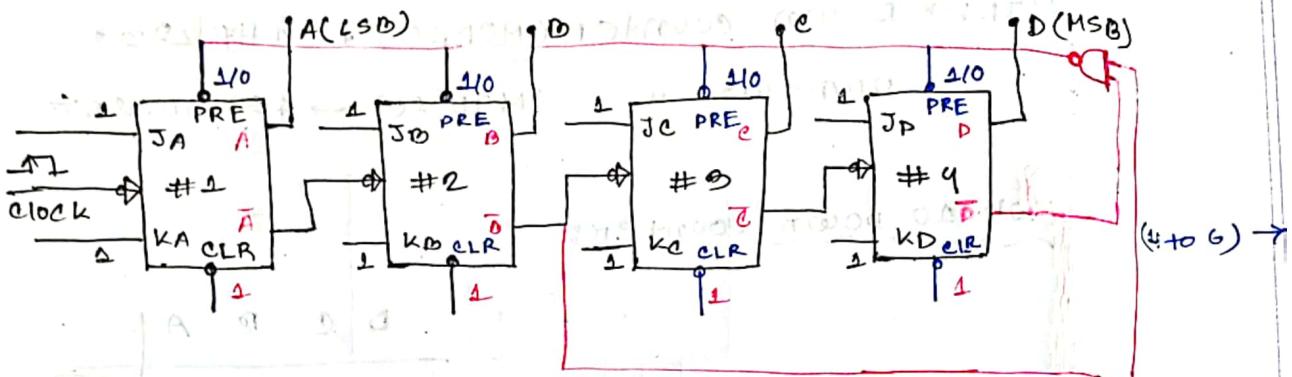


MID: → Down counter(MOD 40); IC #4293,



PRE	CLR	G
0	0	not used
0	1	1
1	0	0

D	C	R	A	
1	1	1	1	(LS) \rightarrow W
1	1	1	0	
1	1	0	1	POST 393
2	1	0	0	
1	0	1	1	PRE = 1
1	0	1	0	CLR = 1 ✓
1	0	0	1	
1	0	0	0	
0	1	1	1	
0	1	1	0	(S) \rightarrow W
0	1	0	1	
0	1	0	0	
0	1	0	1	PRE = 0
				CLR = 1 ✓



operation:

For (4 to 0) : PRE = 1, CLR = 1 (Normal clock operation)

For (5) : PRE = 0, CLR = 1 $\Rightarrow A = B = C = D = 1$, i.e.

Counts $1111_2 = 15_{10}$

Therefore, the counter counts from 15 to 0.

This is MOD 16 down counter.

For MOD 12 : Down $\rightarrow 1100 \rightarrow \overline{DC} \overline{A}$ (15 to 4)

MOD 13 : 1101 $\rightarrow \overline{DC} \overline{A}$

Down

Assignment:

Laboratory Book

Design MOD 40 UP/DOWN COUNTER using JK

FLIP FLOP. You can use other logic gates (if necessary)

$\Rightarrow G \rightarrow 1$

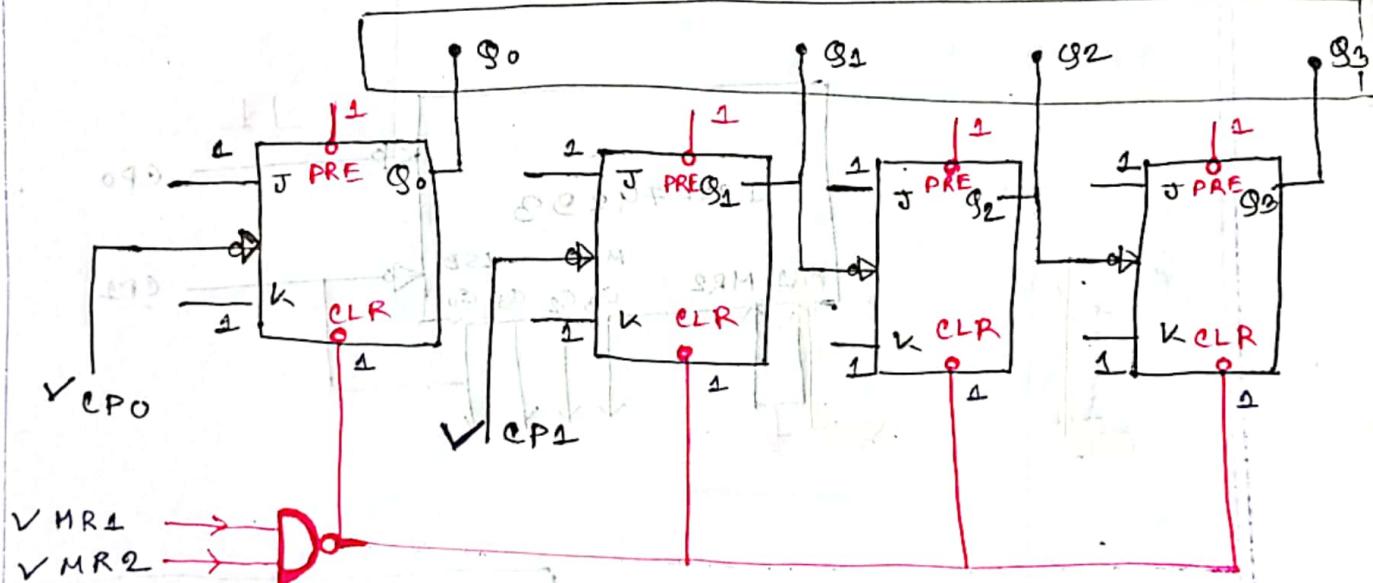
Scopelab

\rightarrow Date: 42.09.23

IC # 74293 (counter IC):

internal circuit:

outputs:



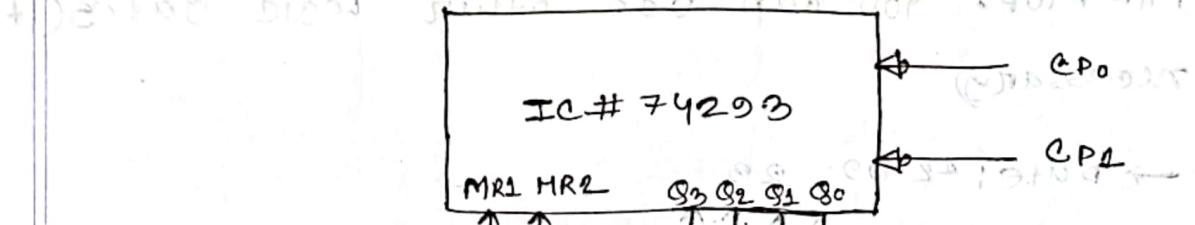
$V_{CP0} \rightarrow$ clock pulse 0

$MR1 \Rightarrow$ Master Reset 1

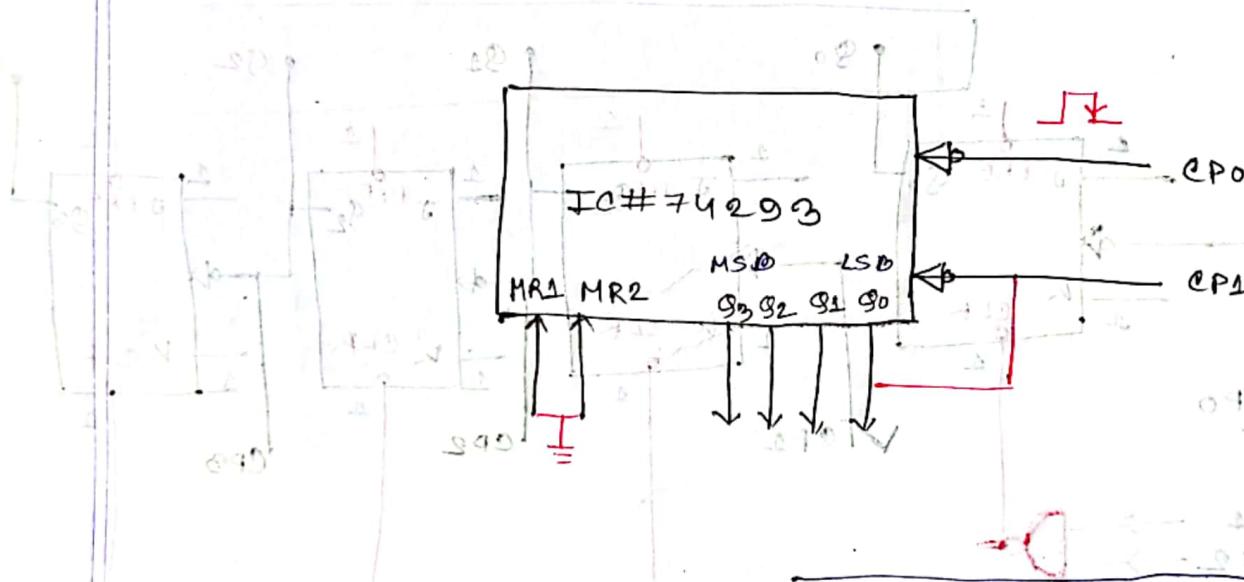
$V_{CP1} \rightarrow$ clock pulse 1

$MR2 \Rightarrow$ Master Reset 2

Block diagram:

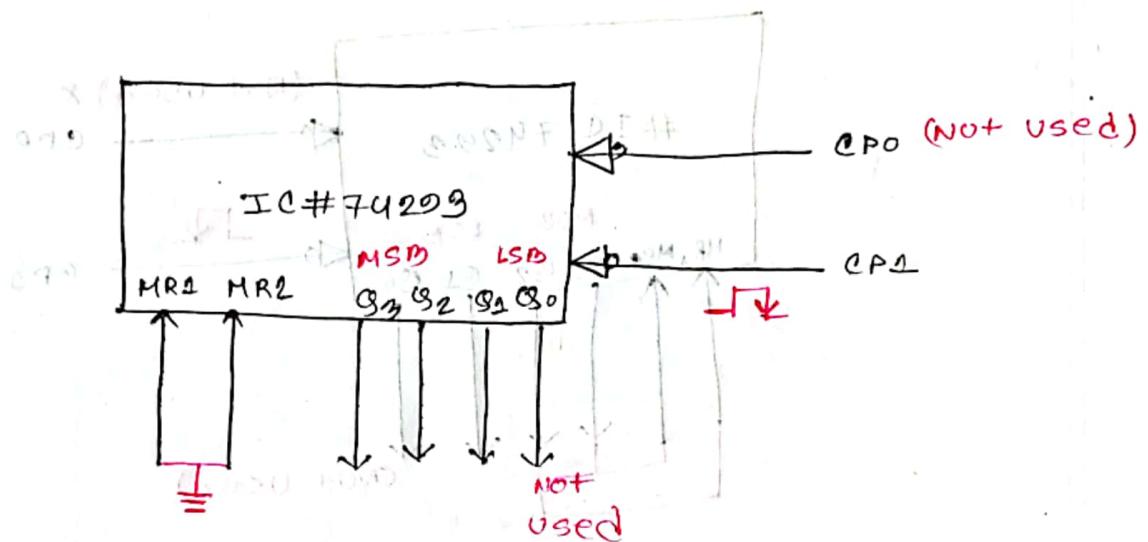


② Design MOD 16 counter using IC #74293;

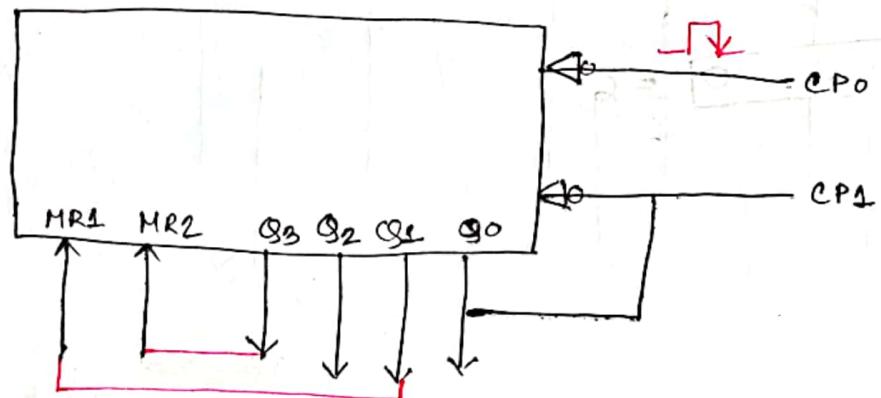


NAND gate: $\leq 2^N$ counter

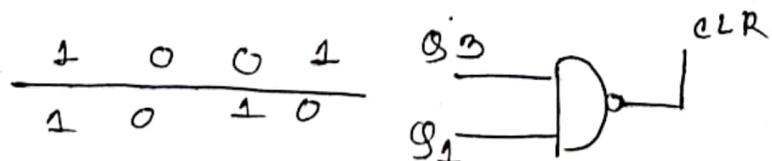
Design MOD 8 counter using IC #74293.



Design MOD 10 counter using IC #74293.

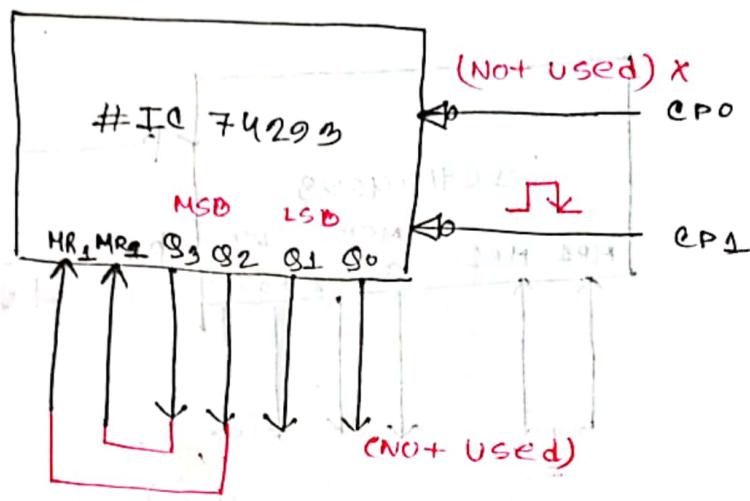


$$\begin{array}{cccc} Q_3 & Q_2 & Q_1 & Q_0 \\ \hline 0 & 0 & 0 & 0 \end{array}$$

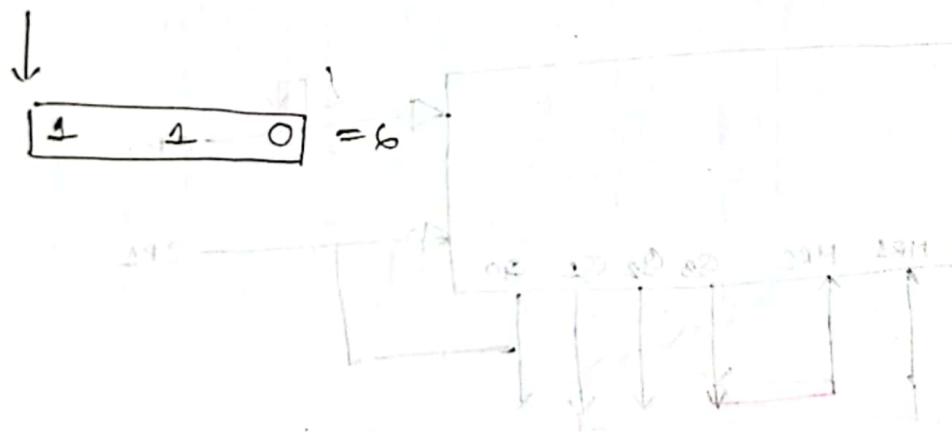


MOD 6:

multiple parallel instructions in data definition



Q_3	Q_2	Q_1	$Q_0 \times$
0	0	0	



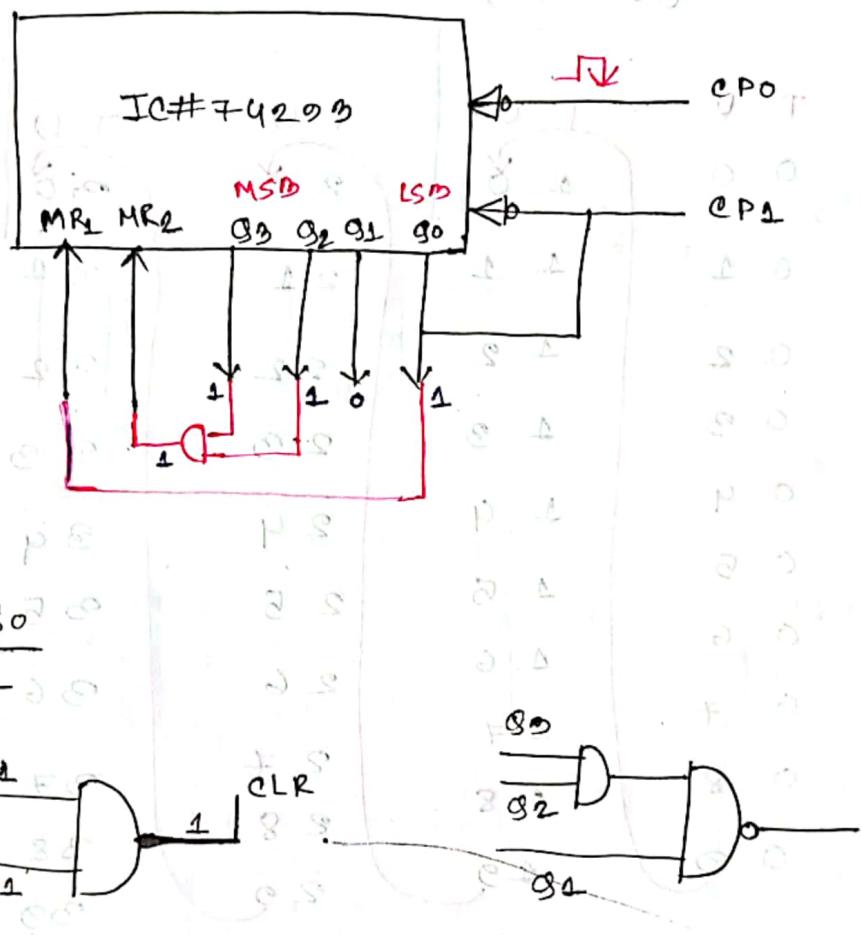
Q_3	Q_2	Q_1	Q_0
0	0	0	1



$13 = 1101$

MOD 13:

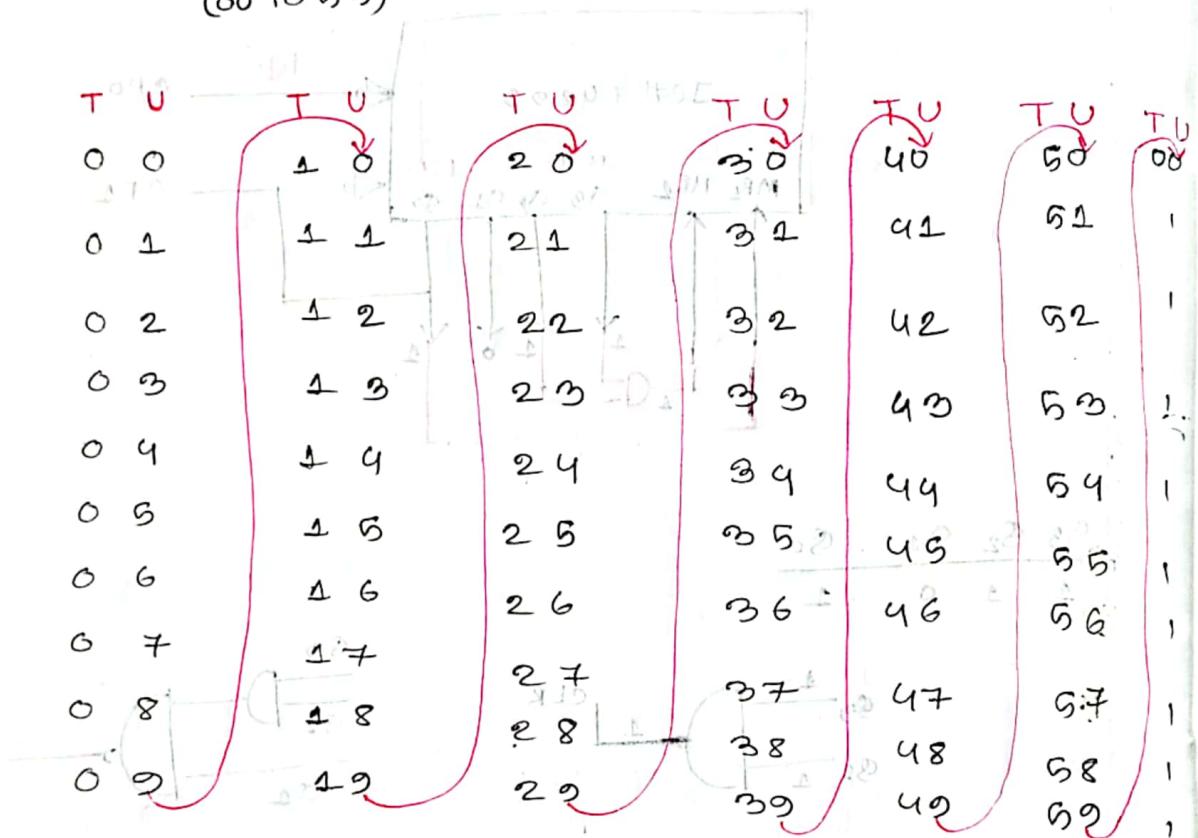
COMPONENTS OF A MODULATOR AND THEIR WORKING
(CONT'D)



MOD 60 → Next class

MOD 60:

Design MOD 60 counter using IC #74299.
(00 to 59)



U → Units/One

⊕ Unit Digits \Rightarrow 0 to 9 \Rightarrow

T → Tens

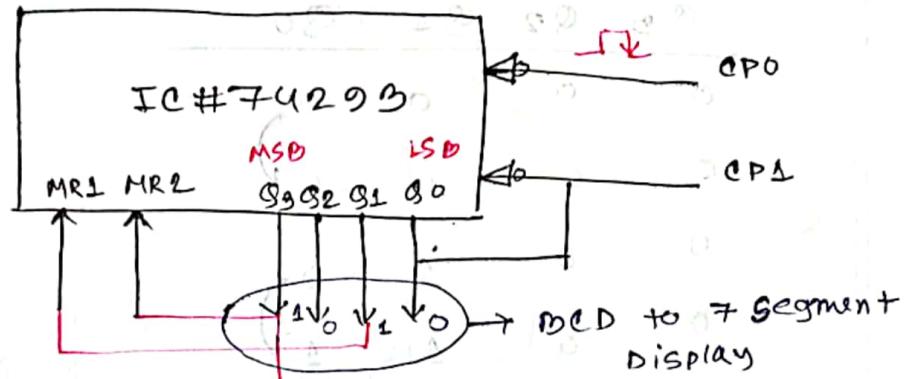
\Rightarrow MOD 10 counter

⊕ Tens Digits \Rightarrow 0 to 5 \Rightarrow

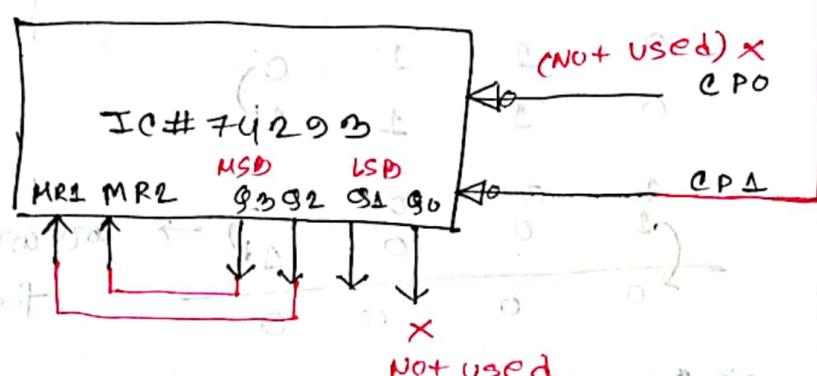
\Rightarrow MOD 6 counter

$$60 = 11 \quad 1100$$

unit digits (MOD 10 counter)



TENS digits (MOD 6 counter)



④ unit digit \rightarrow 0 to 9 MOD 10 counter

④ Tens digits \rightarrow 0 to 5 MOD 6 counter

unit digits:

(निम्नांक उनके लिए ही)

$$\begin{array}{r} \text{Q}_3 \quad \text{Q}_2 \quad \text{Q}_1 \quad \text{Q}_0 \\ \hline 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 \\ \hline 0 & 0 & 0 & 0 \\ \end{array}$$

NGCT = $\frac{1}{0}$

वर्तमान उनके लिए ही

$$\begin{array}{r} \text{Q}_3 \quad \text{Q}_2 \quad \text{Q}_1 \quad \text{Q}_0 \\ \hline 0 & 1 & 1 & 0 \\ 0 & 1 & 1 & 0 \\ 0 & 1 & 1 & 0 \\ 0 & 1 & 1 & 0 \\ \hline 0 & 0 & 0 & 0 \\ \end{array}$$

वर्तमान उनके लिए ही

$$\begin{array}{r} \text{Q}_3 \quad \text{Q}_2 \quad \text{Q}_1 \quad \text{Q}_0 \\ \hline 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ \hline 0 & 0 & 0 & 0 \\ \end{array}$$

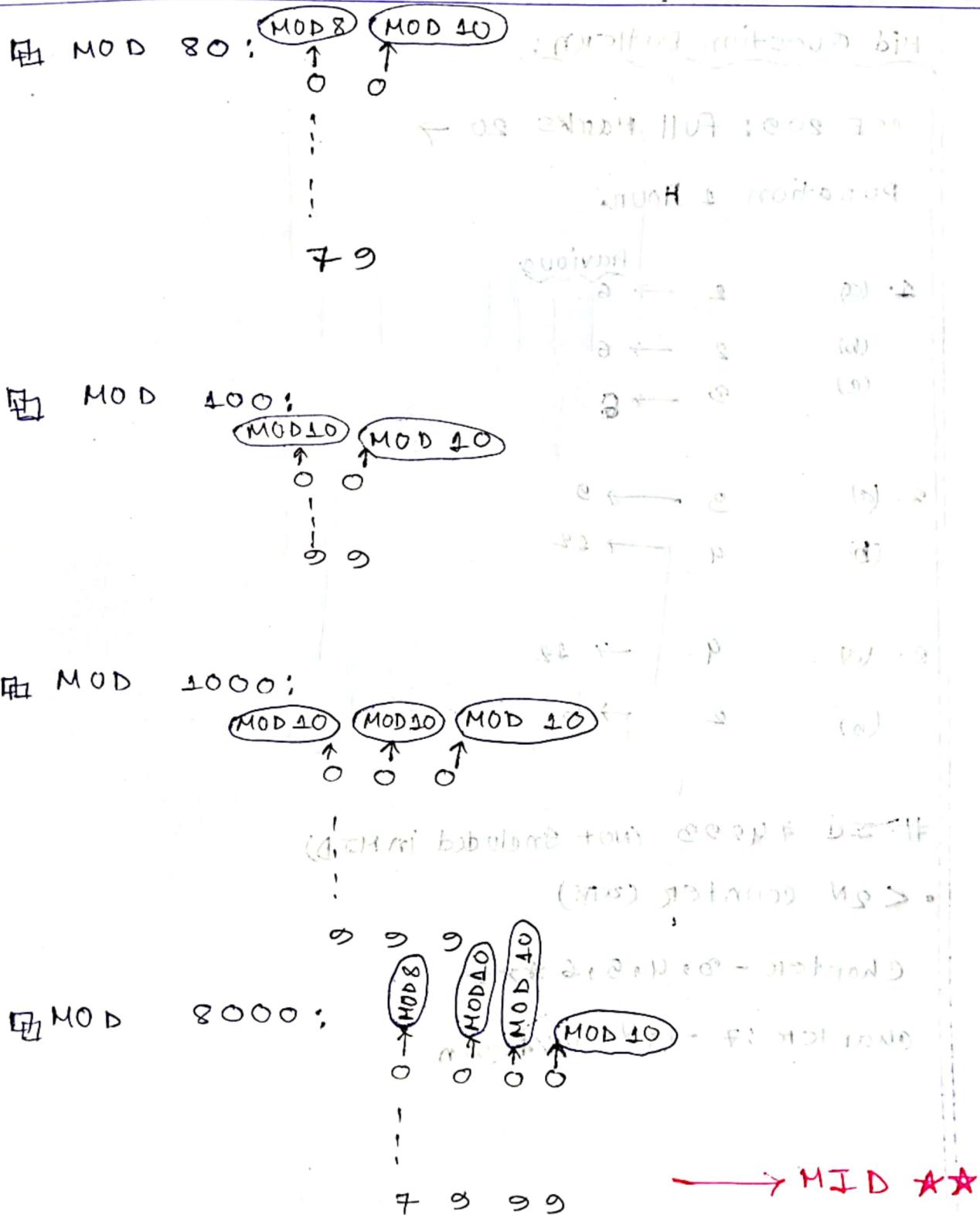
वर्तमान उनके लिए ही

→ Q₃ 1 के लिए 0 को निकल अनुचित, तो Q₃

का Q₂ को जोड़ लिया जाएगा तो उनके लिए ही

NGCT.

ग्राहक को लिए ही तो उनके लिए ही



Mid Question Pattern:

CSE 209: Full Marks 20 →

Puruation 1 Hour.

$$1. (a) \quad 2 \rightarrow \text{Previous}$$

$$(b) \quad 2 \rightarrow 6$$

$$(c) \quad 3 \rightarrow 8$$

$$2. (a) \quad 3 \rightarrow 9$$

$$(b) \quad 4 \rightarrow 12$$

$$3. (a) \quad 9 \rightarrow 12$$

$$(b) \quad 2 \rightarrow 6$$

ID #4293 (NOT included in MID)

• $< 2^N$ Counter (arr)

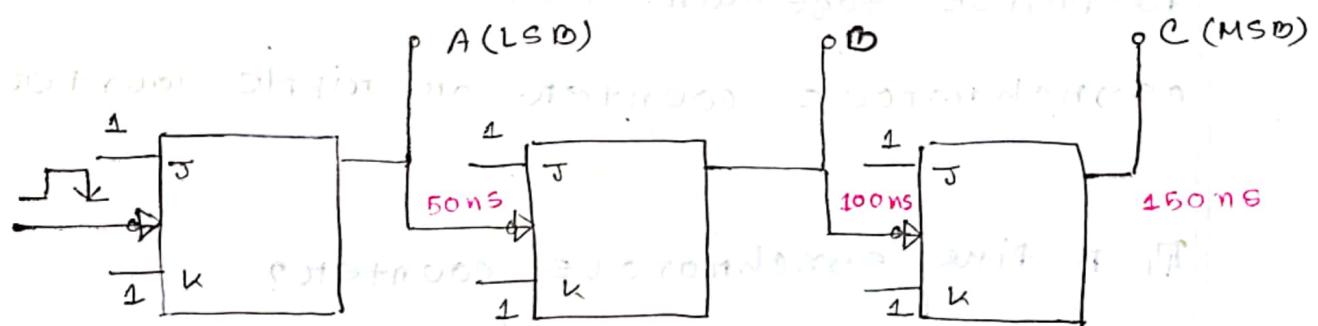
Chapter - 3, 4, 5, 6 ***

Chapter : 7 $\rightarrow 2^N$ UP/Down

A 4 bit Counter

Asynchronous counter/ Ripple counter: (before Mid)

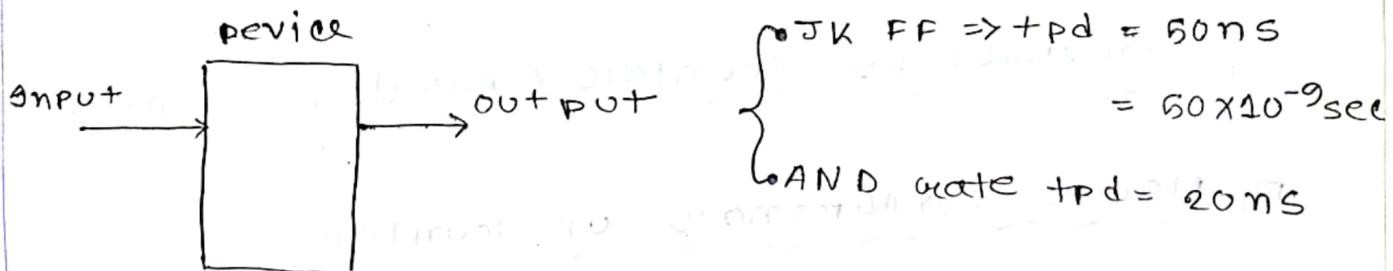
MOD 8 UP ASYNCHRONOUS:



Propagation Delay (t_{pd})

⇒ what is t_{pd} ?

Generally,



for any device, to give the input, and response for outputs, it takes some time, this time is called propagation delay.

Q Define Asynchronous counter?

Ans: The counter where all the outputs do not response together, that counter is called asynchronous counter or ripple counter.

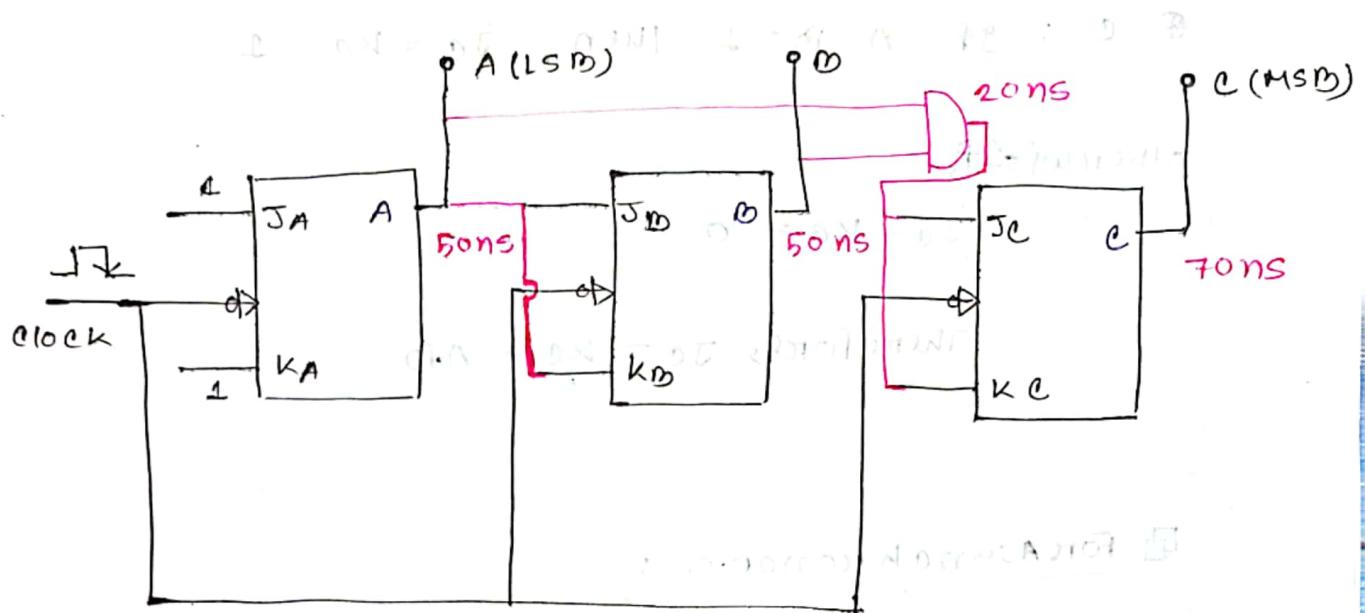
Q Define synchronous counter?

Ans: The counter where all the outputs response together, that counter is called synchronous counter or parallel counter.

Synchronous counter / Parallel counter:

Q MOD 8 synchronous up counter:

(0 to 7)



Circuit diagram of a 3-bit binary counter

JK Truth Table:

J	K	CLK	Output
0	0	↑	N.C
0	1	↑	0
1	0	↑	1
1	1	↑	Toggle

	C	B	A
#1	0	0	0
#2	0	0	1
#3	0	1	0
#4	1	1	0
#5	1	0	1
#6	1	1	0
#7	0	1	1
	0	0	0

Operation:

- ④ A is always Toggle, $J_A, K_A = 1$
- ④ B: If $A=0$ then, $J_B, K_B = 0\ 0$
If $A=1$ then, $J_B, K_B = 1\ 1$
- ④ $J_C = K_C = A$

④ C : If $A = B = 1$ then, $J_C = K_C = 1$

otherwise,

$$J_C = K_C = 0$$

$$\text{Therefore, } J_C = K_C = A \cdot B$$

■ for Asynchronous :

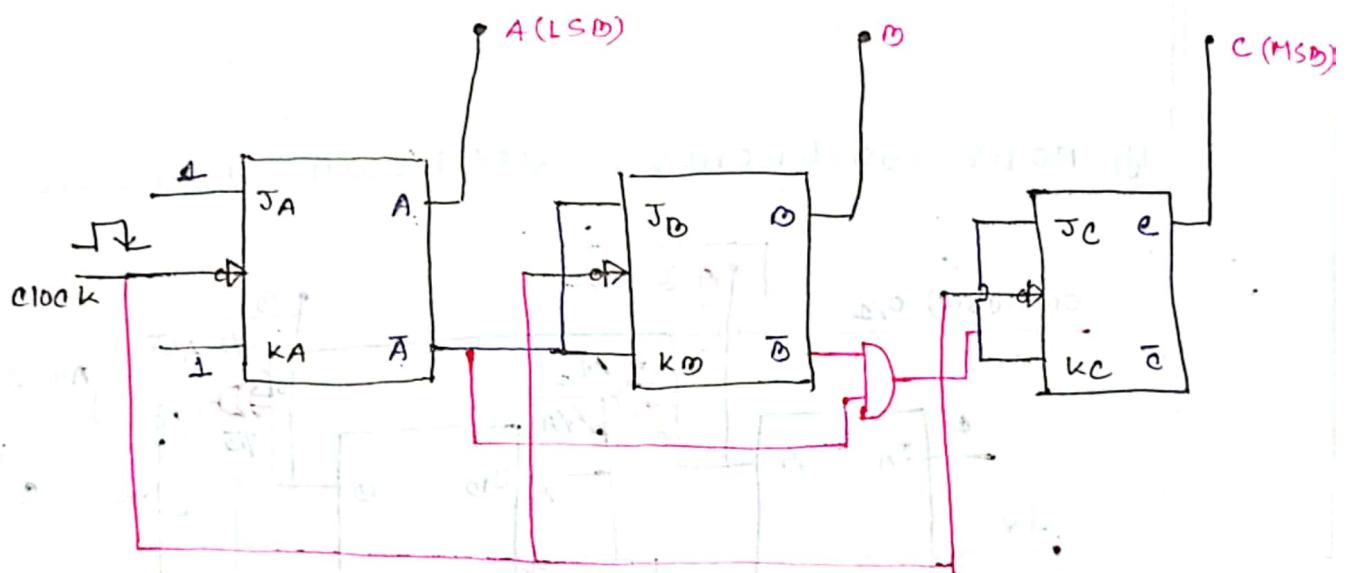
Total $t_{PD} = t_{PD}$ for 1 JKFF \times NO OF FFS.

■ for Synchronous :

Total $t_{PD} = t_{PD}$ for 1 JKFF + t_{PD} for one AND gate
(1)

④ Asynchronous and synchronous Advantage and Disadvantage.

MOD 8 SYNCHRONOUS DOWN - counter:



Target + Truth Table:

	C	B	A
#1	1	1	1
#2	1	1	0
#3	1	0	1
#4	1	0	0
#5	0	1	1
#6	0	1	0
#7	0	0	1
#8	1	1	1

A: Always Toggle

$$J_A = K_A = 1$$

B: when $A=1$ then $J_B = K_B = 0$

$A=0$ then $J_B = K_B = 1$

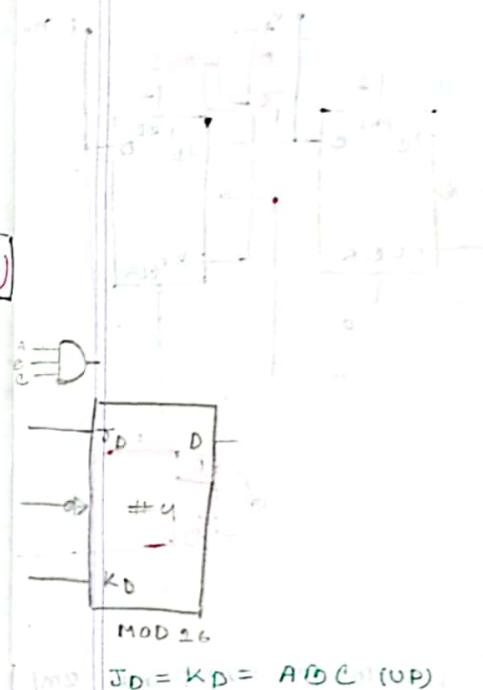
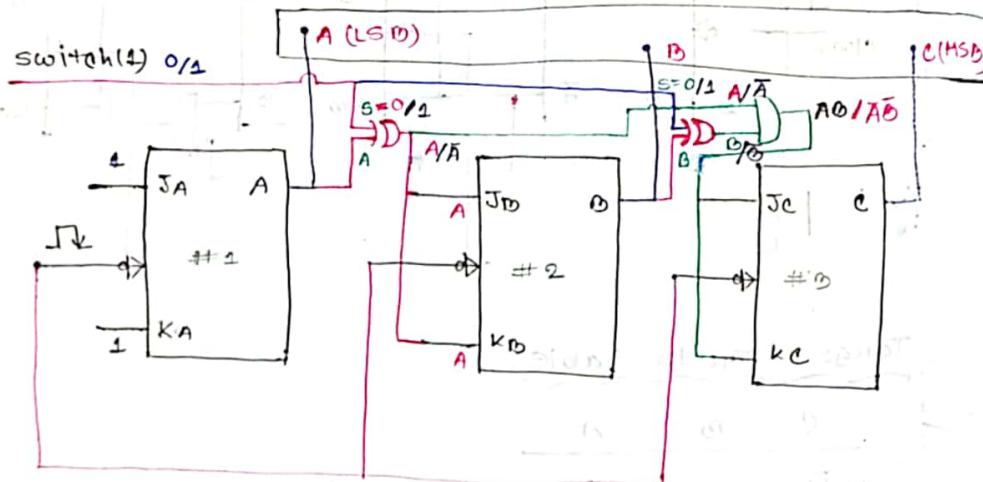
$$\boxed{J_B = K_B = \bar{A}}$$

→ Always Toggle

Q: When $A = B = 0$ then $J_C = 1$ and $K_C = 1$

otherwise, $J_C = 0$ and $K_C = 0$

Q1 MOD8 synchronous UP/ Down counter:



Operation:

$$J_A = K_A = 1$$

If $S = 0$ then $J_B = K_B = A$ and $J_C = K_C = AB$

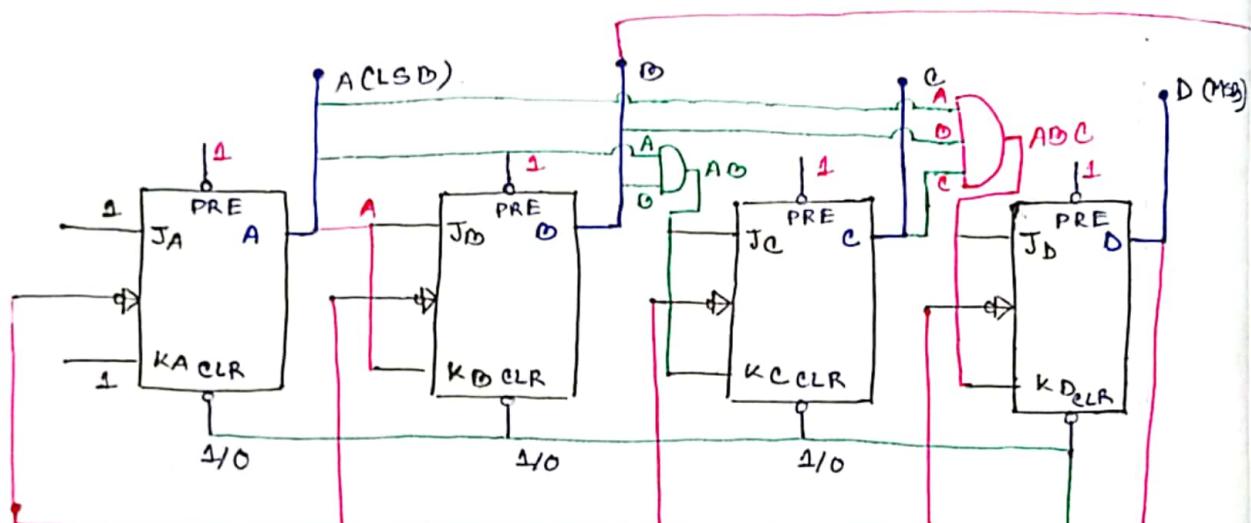
UP counter.

If $S = 1$ then $J_A = K_A = 1$.

$J_B = K_B = \bar{A}$ and $J_C = K_C = \bar{A} \bar{B}$

This is Down counter.

MOD 10 SYNCHRONOUS UP COUNTER:



D	C	B	A	
0	0	0	0	$P = 1$
1	0	0	1	$C = 1$
2	0	1	0	$P = 1$
				$C = 0$

[D B TO NAND Gate 2(a)]

Operation:

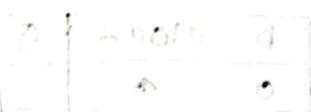
From (0 to 9) PRE = 1; CLR = 1 \Rightarrow Normal clock operation

For 10 PRE 1; CLR = 0 \Rightarrow A = B = C = D = 0

it counts $0000_2 = 0_{10}$

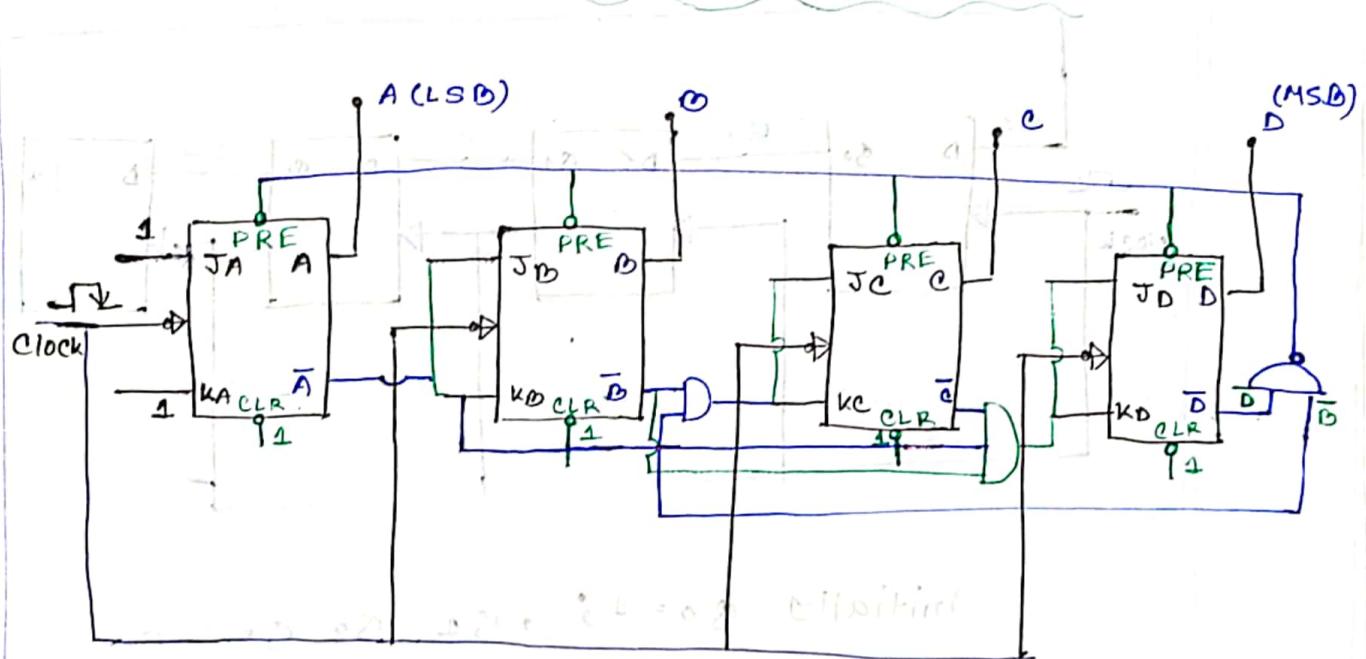
∴ The counter counts from 0 to 9.

This is MOD 10 synchronous up counter.



Instruction part 4

MOD 10 synchronous up down counter:



$$J_B = K_B = \bar{A}$$

$$J_C = K_C = \bar{A} \bar{B} : \text{divide by } +10$$

$$J_D = K_D = \bar{A} \bar{B} \bar{C}$$

shift counter: (Easy topic)

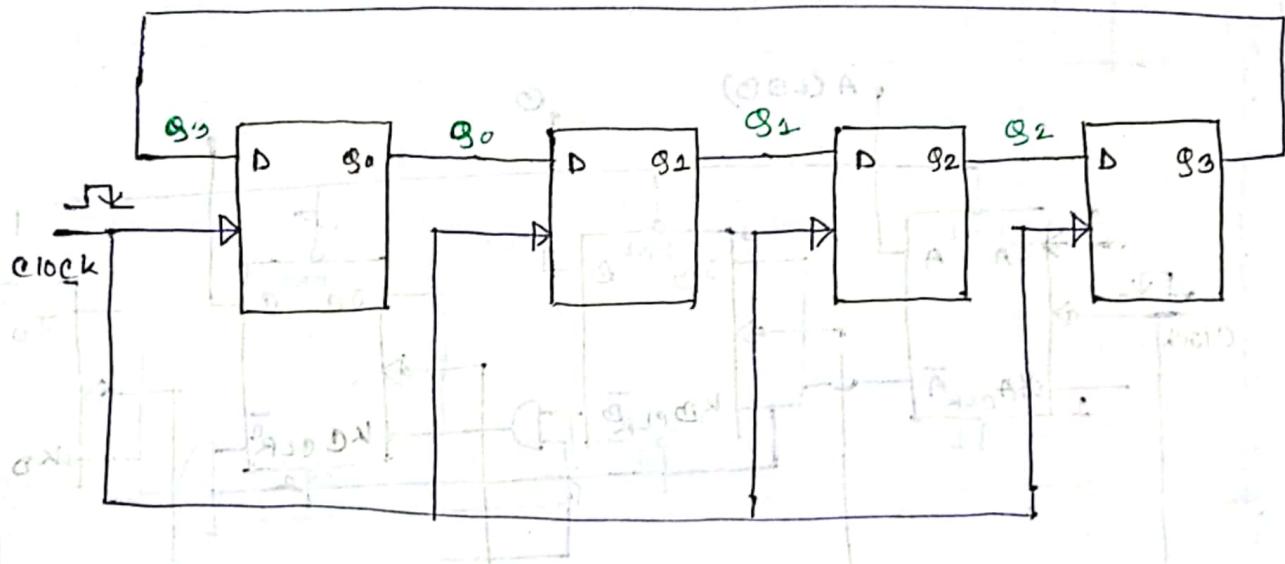
1. Ring counter

2. Johnson counter

1. Ring counter:

D	Clock	Q
0	↑	0
1	↑	1

MOD 4 Ring counter:



Initially $Q_0 = 1$, $Q_1 = Q_2 = Q_3 = 0$.

operation:

After giving the pulse:

$$Q_0 = Q_3$$

$$Q_1 = Q_0$$

$$Q_2 = Q_1$$

$$Q_3 = Q_2$$

STATE TRANSITION DIAGRAM

	Q_0	Q_1	Q_2	Q_3
Initial value	1	0	0	0
#1	0	1	0	0
#2	0	0	1	0
#3	0	0	0	1
#4	1	0	0	0

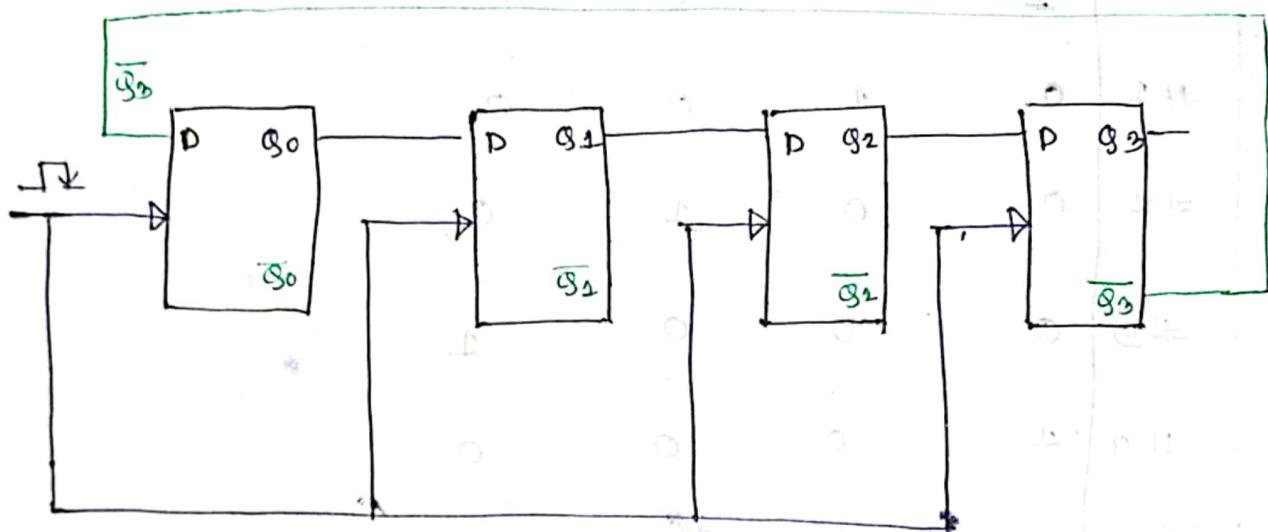
(a) For Ring counter:

(b) MOD Number of Ring counter
= NO of Flip FLOP

Formula

2. Johnson counter:

iii) MOD 8 Johnson counter:



Initially $Q_0 = Q_1 = Q_2 = Q_3 = 0$

operation:

After giving the pulse:

$$Q_0 = \overline{Q_3}$$

$$Q_1 = Q_0$$

$$Q_2 = Q_1$$

$$Q_3 = Q_2$$

Method to find sequence: $Q_3 Q_2 Q_1 Q_0$

Initial value

#1 1 0 0 0

#2 1 1 0 0

#3 1 1 1 0

#4 1 1 1 1

#5 0 1 1 1

#6 0 0 1 1

#7 0 0 0 1

#8 0 0 0 0

Method to find sequence: $Q_3 Q_2 Q_1 Q_0$

(initial state) $\rightarrow 0000 \rightarrow$

Step 1: $0000 + 1000 = 1000$ (Binary)

Step 2: $1000 + 1000 = 0000$ (Binary)

Step 3: $0000 + 1000 = 1000$ (Binary)

Step 4: $1000 + 1000 = 0000$ (Binary)

Step 5: $0000 + 1000 = 1000$ (Binary)

Step 6: $1000 + 1000 = 0000$ (Binary)

Step 7: $0000 + 1000 = 1000$ (Binary)

Step 8: $1000 + 1000 = 0000$ (Binary)

Step 9: $0000 + 1000 = 1000$ (Binary)

Step 10: $1000 + 1000 = 0000$ (Binary)

Step 11: $0000 + 1000 = 1000$ (Binary)

Step 12: $1000 + 1000 = 0000$ (Binary)

Step 13: $0000 + 1000 = 1000$ (Binary)

Step 14: $1000 + 1000 = 0000$ (Binary)

Step 15: $0000 + 1000 = 1000$ (Binary)

Step 16: $1000 + 1000 = 0000$ (Binary)

Step 17: $0000 + 1000 = 1000$ (Binary)

Step 18: $1000 + 1000 = 0000$ (Binary)

Step 19: $0000 + 1000 = 1000$ (Binary)

Step 20: $1000 + 1000 = 0000$ (Binary)

Step 21: $0000 + 1000 = 1000$ (Binary)

Step 22: $1000 + 1000 = 0000$ (Binary)

Step 23: $0000 + 1000 = 1000$ (Binary)

Step 24: $1000 + 1000 = 0000$ (Binary)

Step 25: $0000 + 1000 = 1000$ (Binary)

Step 26: $1000 + 1000 = 0000$ (Binary)

Step 27: $0000 + 1000 = 1000$ (Binary)

Step 28: $1000 + 1000 = 0000$ (Binary)

Step 29: $0000 + 1000 = 1000$ (Binary)

Step 30: $1000 + 1000 = 0000$ (Binary)

Step 31: $0000 + 1000 = 1000$ (Binary)

Step 32: $1000 + 1000 = 0000$ (Binary)

Step 33: $0000 + 1000 = 1000$ (Binary)

Step 34: $1000 + 1000 = 0000$ (Binary)

Step 35: $0000 + 1000 = 1000$ (Binary)

Step 36: $1000 + 1000 = 0000$ (Binary)

for Johnson counter:

$\text{MOD Number} = 2 \times \text{No of flip flop}$

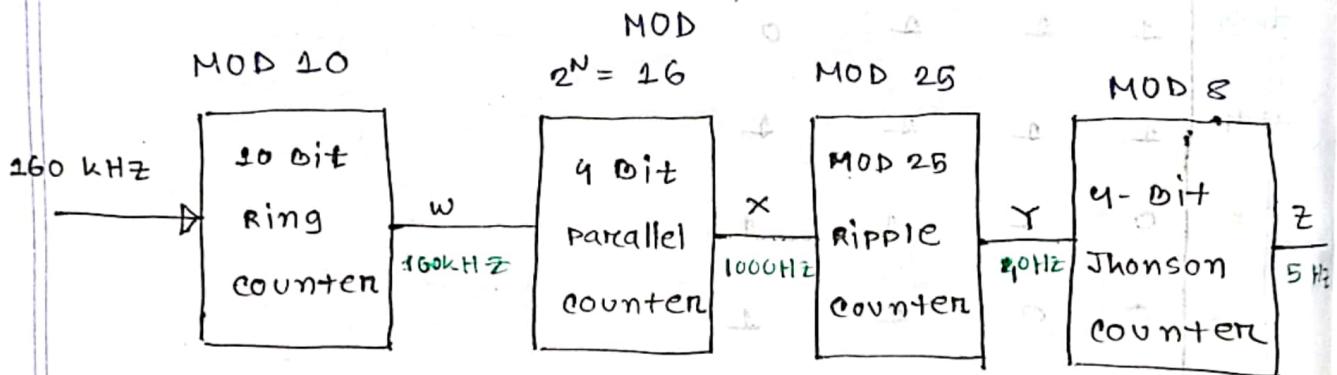
Formula

$= 7$

$\text{SHD} = \frac{1000}{1000} = 1$

CT: sync, $\leq 2N$, #74293, shift + counters.
 → 26.09.2023 → (Estimator)

Q: output frequency = $\frac{\text{input frequency}}{\text{MOD Number}}$



Q: Find values of w, x, y, z?

$$w = \frac{160 \text{ kHz}}{10} = 16 \text{ kHz}$$

$$x = \frac{16 \text{ kHz}}{16} = 1 \text{ kHz} = 1000 \text{ Hz}$$

$$y = \frac{1000 \text{ Hz}}{25} = 40 \text{ Hz}$$

$$z = \frac{40 \text{ Hz}}{8} = 5 \text{ Hz}$$

question Answer:

for each of the following statements, indicate the types of counter being described.

- (i) Each FF is clocked at the same time.
- (ii) Each FF divides the frequency at its clock pulse by two(2).
- (iii) The counter sequence is 111, 110, 101, 100, 011, 010, 001, 00.
- (iv) The counter has ten(10) distinct states.
- (v) The total delay is the sum of the individual FF's delay.
- (vi) The counter can count in either direction.
- (vii) The counter counts from 0 to 9.
- (viii) The MOD number is always twice the number of FF's.
- (ix) The total delay is the sum of one FF's

delay and one AND gate's delay

- (X) The MOD Number is always equal to
the number of bits or number of stages with
number of FF's.

right answer for the following of 11 about (X)

- (i) Ans: synchronous counter / parallel counter

→ (i) Synchronous counter (Ans) (X)

- (ii) Ans: Any counter

- (iii) Ans: MOD 8 down counter

→ (iii) Mod 8 down counter (Ans) (X)

- (iv) Ans: MOD 10 counter

→ (iv) Mod 10 counter (Ans) (X)

- (v) Ans: Asynchronous counter / ripple counter

→ (v) Asynchronous counter (Ans) (X)

- (vi) Ans: UP/DOWN counter

→ (vi) Up/Down counter (Ans) (X)

- (vii) Ans: MOD 10 UP counter

→ (vii) Mod 10 up counter (Ans) (X)

- (viii) Ans: Johnson counter

→ (viii) Johnson counter (Ans) (X)

- (ix) Ans: synchronous counter / parallel counter

→ (ix) Synchronous counter (Ans) (X)

- (x) Ans: Ring counter

→ (x) Ring counter (Ans) (X)

→ End of counter

caden's software

Chapter : 9

MSI, Logic circuit:

MSI → Medium scale integrated logic circuit

SSI → small scale of combinational circuits



(till counter chapter)

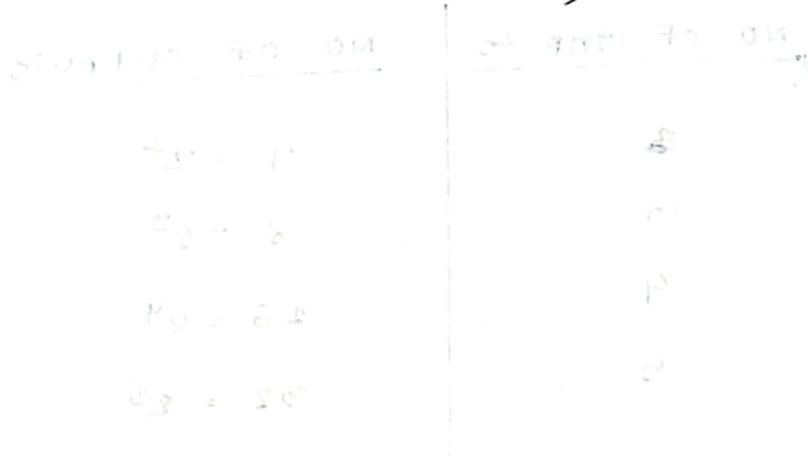
LSI → Large scale

VLSI → very large scale

(a) Decoder

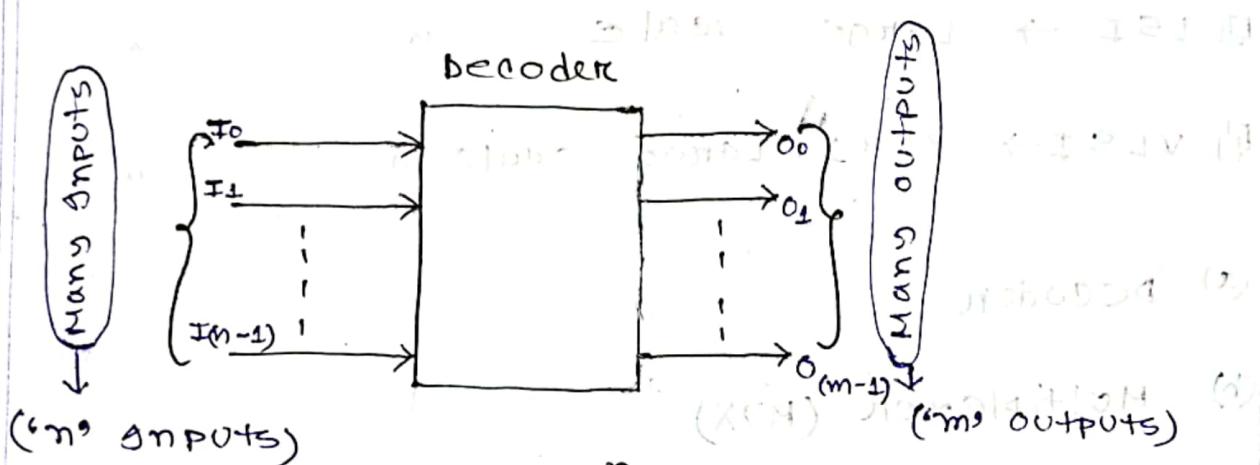
(b) Multiplexer (MUX)

(c) Demultiplexer (DE MUX)



obtain the output configuration for all 16 outputs.

Decoder: Decoder is a device where there are many inputs, also many outputs. And at a time one of the output will be active according to corresponding combination of inputs.



$$\therefore m = 2^n$$

<u>NO OF INPUTS</u>	<u>NO OF OUTPUTS</u>
2	$4 = 2^2$
3	$8 = 2^3$
4	$16 = 2^4$
5	$32 = 2^5$

$$\therefore \text{No of outputs} = 2^{\text{No of inputs}}$$

4) 3 Lines to 8 Lines Decoder :

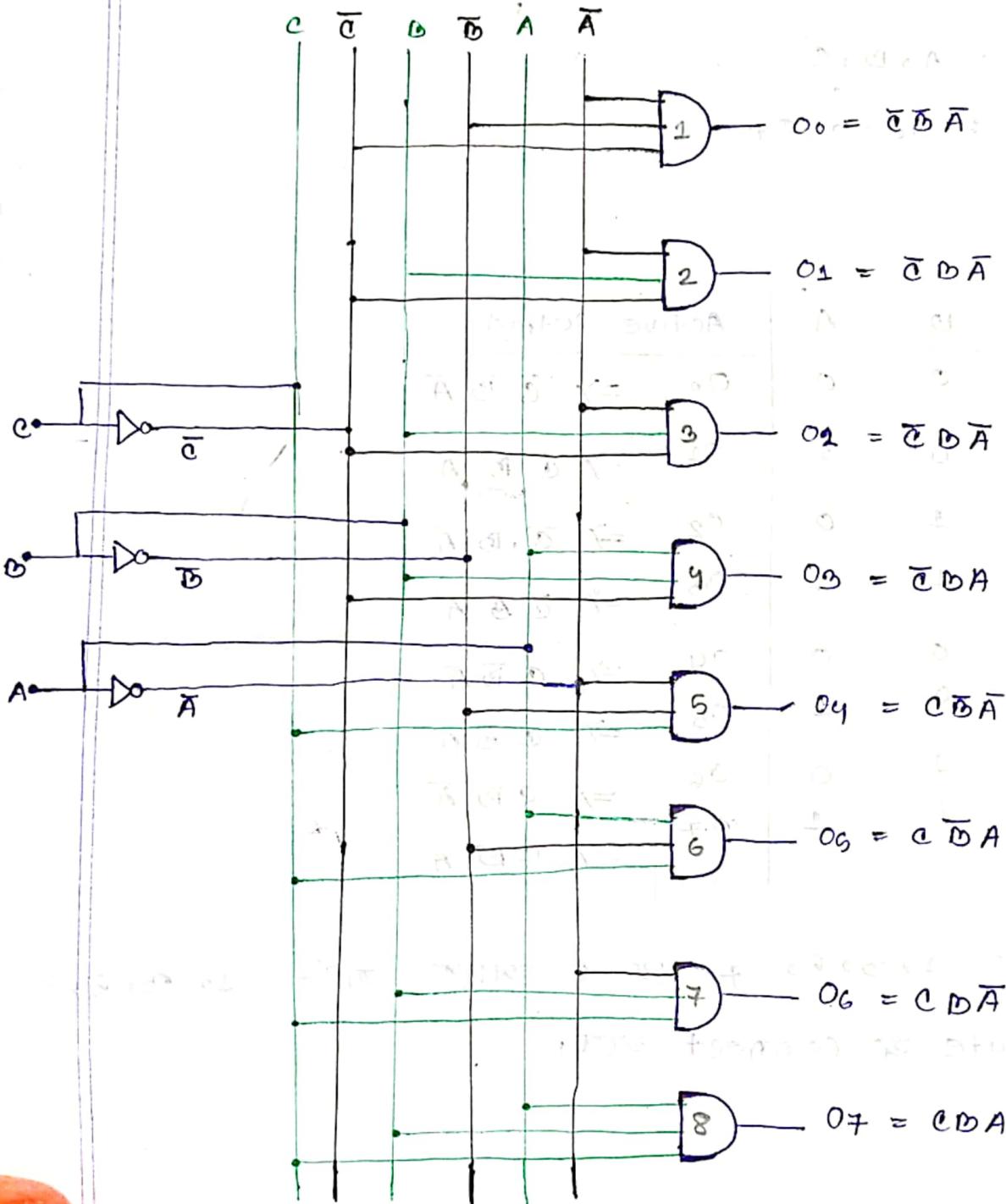
Inputs : A, B, C

Outputs : O₀ to O₇

ABC = 000			Active Output
C	B	A	O ₀ $\Rightarrow \bar{C} \bar{B} \bar{A}$
0	0	1	O ₁ $\Rightarrow \bar{C} \bar{B} A$
0	1	0	O ₂ $\Rightarrow \bar{C} B \bar{A}$
0	1	1	O ₃ $\Rightarrow \bar{C} B A$
1	0	0	O ₄ $\Rightarrow C \bar{B} \bar{A}$
1	0	1	O ₅ $\Rightarrow C \bar{B} A$
1	1	0	O ₆ $\Rightarrow C B \bar{A}$
1	1	1	O ₇ $\Rightarrow C B A$

* A तरे 1, 3, 5, 7 या 0 आवृत्ति असे - 1, 3, 5, 7

AND gate ए- connect झाला.



4 Line to 16 Line Decoder:

Inputs : $A, B, C, D_{(MSB)}$

Outputs : O_0 to O_{15}

AND gate : 16 ($\frac{1}{2}$ to 16) = 16 AND

$\bar{A} \rightarrow 1, 3, 5, 7, 9, 11, 13, 15$

$A \rightarrow 2, 4, 6, 8, 10, 12, 14, 16$

$\bar{B} \rightarrow 1, 2, 5, 6, 9, 10, 13, 14$

$B \rightarrow 3, 4, 7, 8, 11, 12, 15, 16$

$\bar{C} \rightarrow 1 \text{ to } 4, 9 \text{ to } 12$

$C \rightarrow 5 \text{ to } 8, 13 \text{ to } 16$

$\bar{D} \rightarrow 1 \text{ to } 8$

$D \rightarrow 9 \text{ to } 16$

Q) 4 Line to 10-Line Decoder:

Inputs: A, B, C, D

Outputs: O₀ to O₉

AND gate: 1 to 10

$\bar{A} \Rightarrow 4, 3, 5, 7, 9$ = 1's complement of 00001 → \bar{A}

A $\Rightarrow 2, 4, 6, 8, 10$ = 1's complement of 00000 → A

$\bar{B} \Rightarrow 4, 2, 5, 6, 8, 9, 10$ = 1's complement of 00011 → \bar{B}

B $\Rightarrow 3, 4, 7, 8$ = 1's complement of 00000 → B

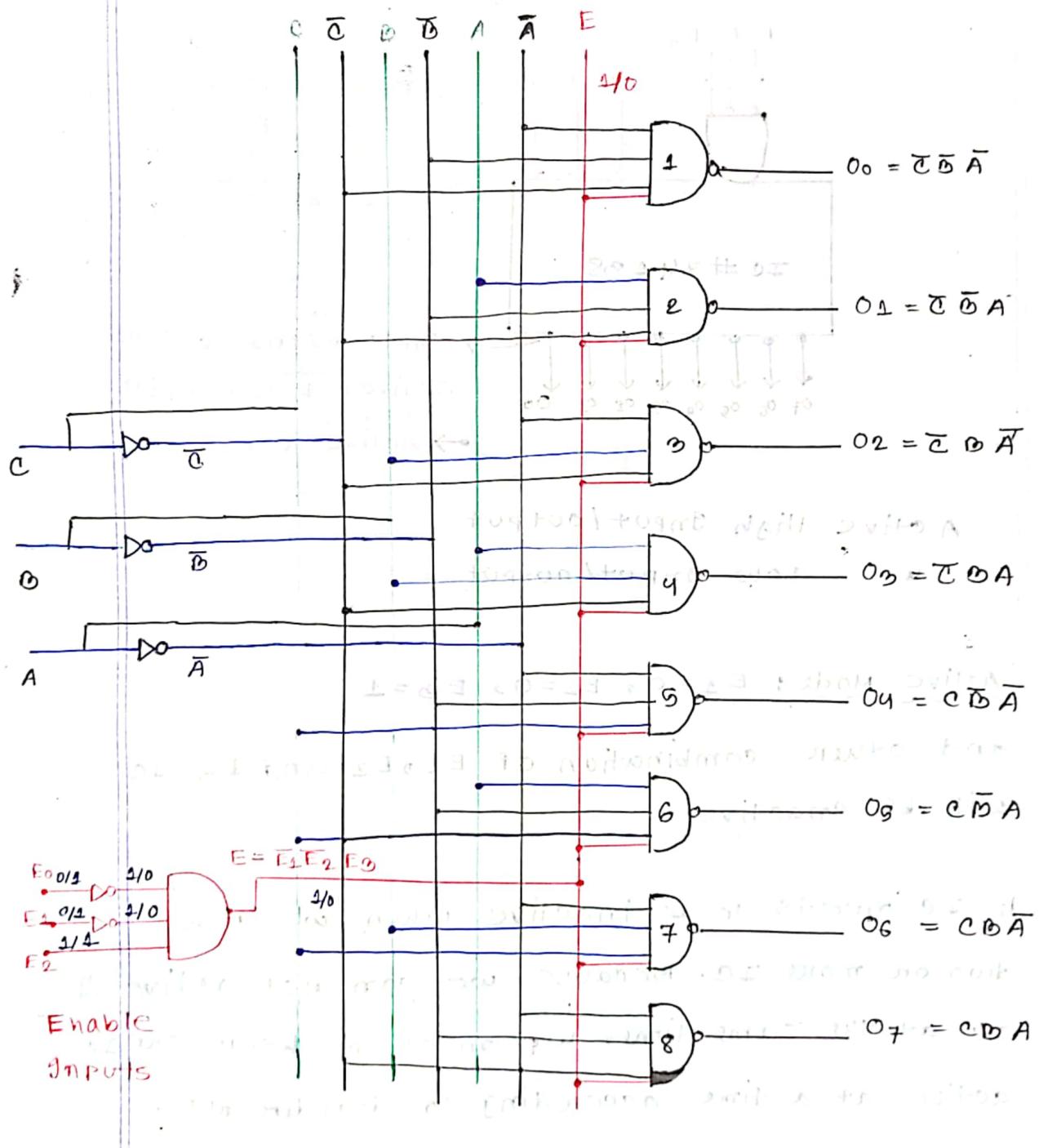
$\bar{C} \Rightarrow 1, 2, 3, 4, 9, 10$ = 1's complement of 00001 → \bar{C}

C $\Rightarrow 5, 6, 7, 8$ = 1's complement of 00010 → C

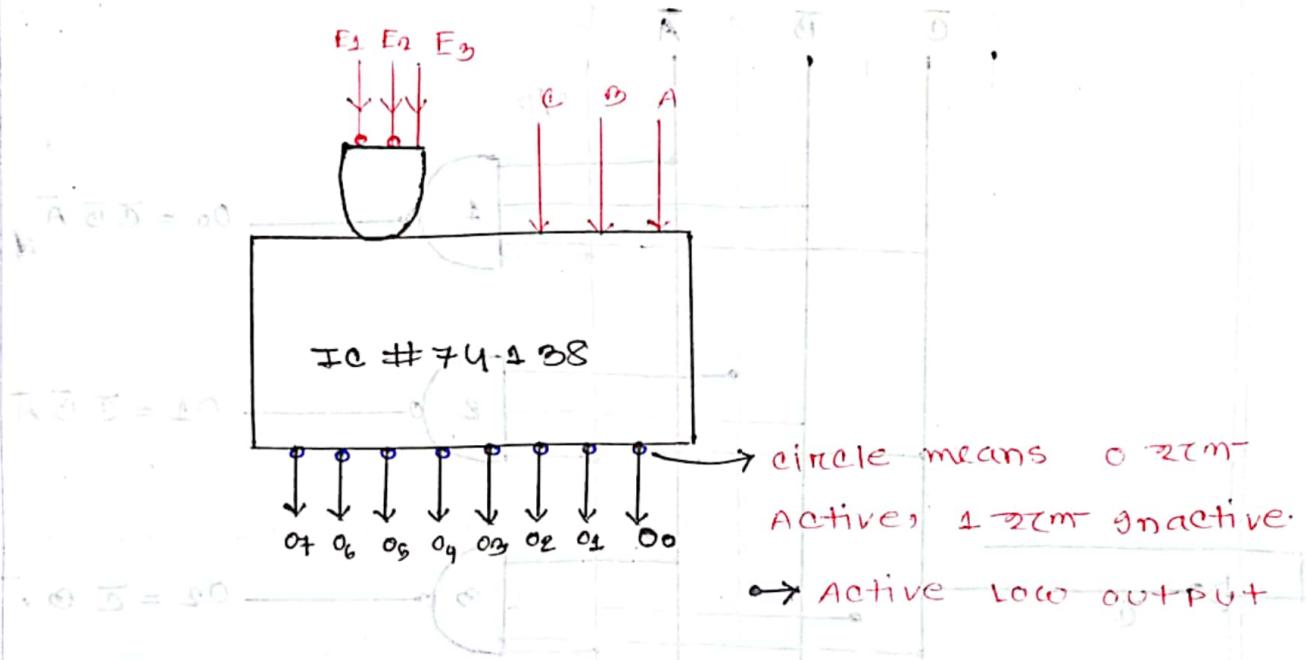
$\bar{D} \Rightarrow 1 \text{ to } 8$ = 1's complement of 00000 → \bar{D}

D $\Rightarrow 9 \text{ to } 10$ = 1's complement of 00011 → D

IC # 74138: Internal circuit



Block diagram of IC # 74138



Active High Input/Output

Active Low Input/Output

Active Mode: E₁ = 0, E₂ = 0, E₃ = 1

and other combination of E₁, E₂ and E₃ IC will be inactive.

⇒ IC needs to be inactive when we use two or more IC. Because we can not active all IC at the same time, we need to keep one IC active at a time according to decoder rule.

Ques: If $E_1 = E_2 = 0$, $E_3 = 1$ then which output will be active?

Sol: $A = 1, B = 1, C = 0$ and $0 \oplus 1 = 1$ & $1 \oplus 0 = 1$

Ans: Which output will be active?

$\frac{C \quad B \quad A}{0 \quad 1 \quad 1} \rightarrow 03$ will be active.

So 03 is the output

Ques: If $E_1 = 0, E_2 = 1, E_3 = 1$ then what will be the output?

$A = 1, B = 0, C = 1$

which output will be active?

Ans: No output will be active.

Input Output

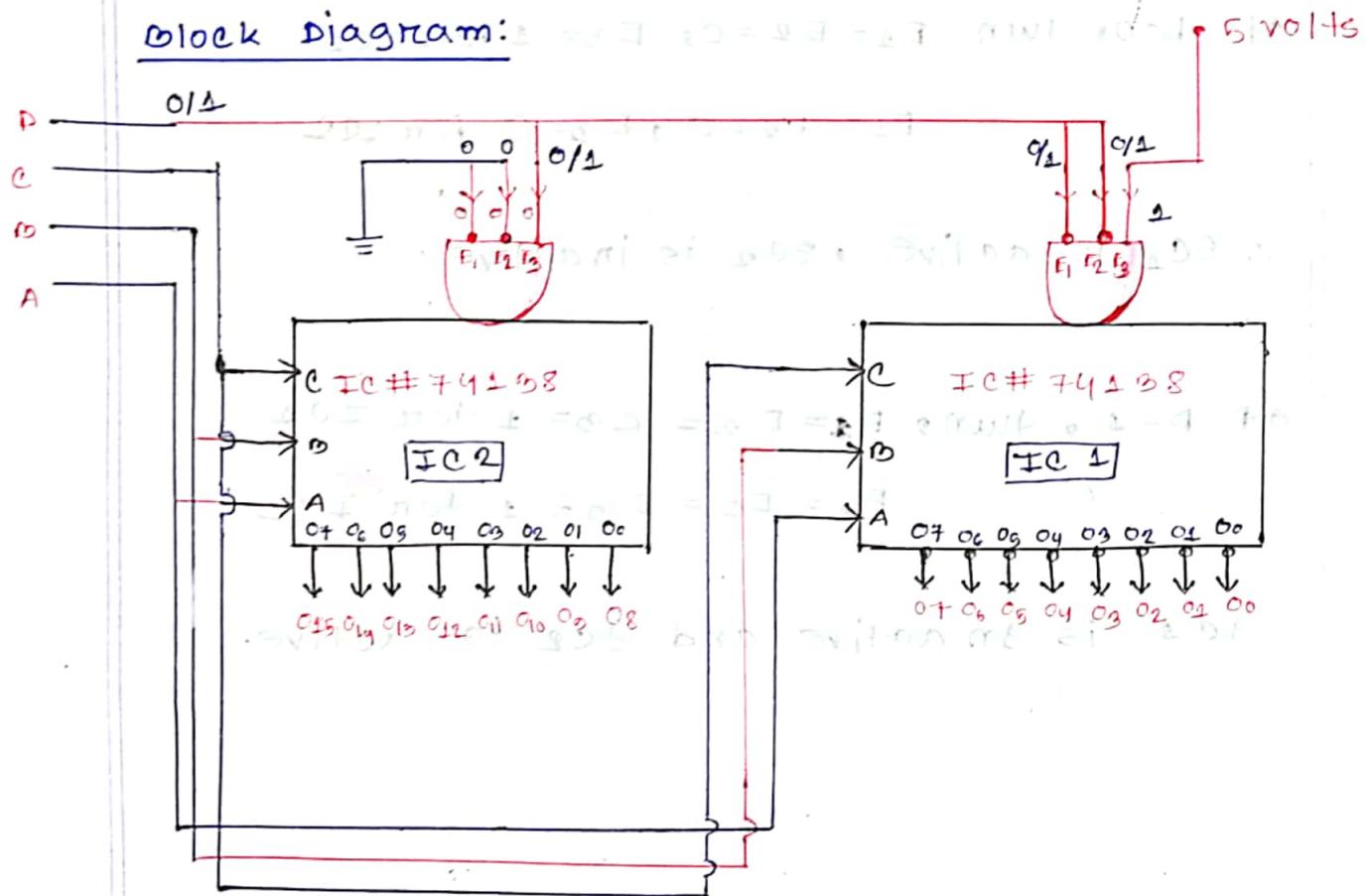
\Rightarrow Ques: Design $\underline{4}$ line to $\underline{16}$ line Decoder using
 IC # 74138. You can use other logic gates
 if necessary.

\Rightarrow Ans: Inputs: D, C, B, A $\frac{A}{B} \frac{C}{D}$
 Outputs: O_0 to O_{15}

$$\text{Number of IC: } \frac{16}{2} = 8$$

D	C	B	A	Active Output	
0	0	0	0	00	
0	0	0	1	01	IC1 Active $(D=0)$
0	0	1	0	02	
0	0	1	1	03	
0	1	0	0	04	
0	1	0	1	05	
0	1	1	0	06	
0	1	1	1	07	
1	0	0	0	08	IC1 Inactive $(D=1)$
1	0	0	1	09	
1	0	1	0	010	
1	0	1	1	011	
1	1	0	0	012	IC2 Active $(D=1)$
1	1	0	1	013	
1	1	1	0	014	
1	1	1	1	015	

Block Diagram:



when $D=0$ then Q_1 Active, Q_2 Inactive.

when $D=1$ then Q_1 Inactive, Q_2 Active.

Operation:

If $P=0$ then IC_1 is active and IC_2 is inactive

If $D=1$ then IC_2 is active and IC_1 is -u.

If $D=0$, then $E_1 = E_2 = 0$, $E_3 = 1$ for I_{C1} is active

$E_1 = E_2 = 0$, $E_3 = 0$ for I_{C2}

$\therefore g_{C1}$ is active, g_{C2} is inactive.

If $D=1$, then, $E_1 = E_2 = E_3 = 1$ for I_{C1}

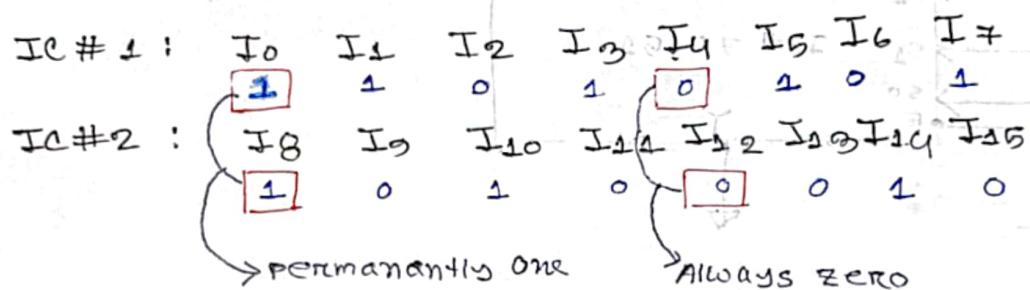
$E_1 = E_2 = E_3 = 1$ for I_{C2}

$\therefore g_{C1}$ is inactive and g_{C2} is active.

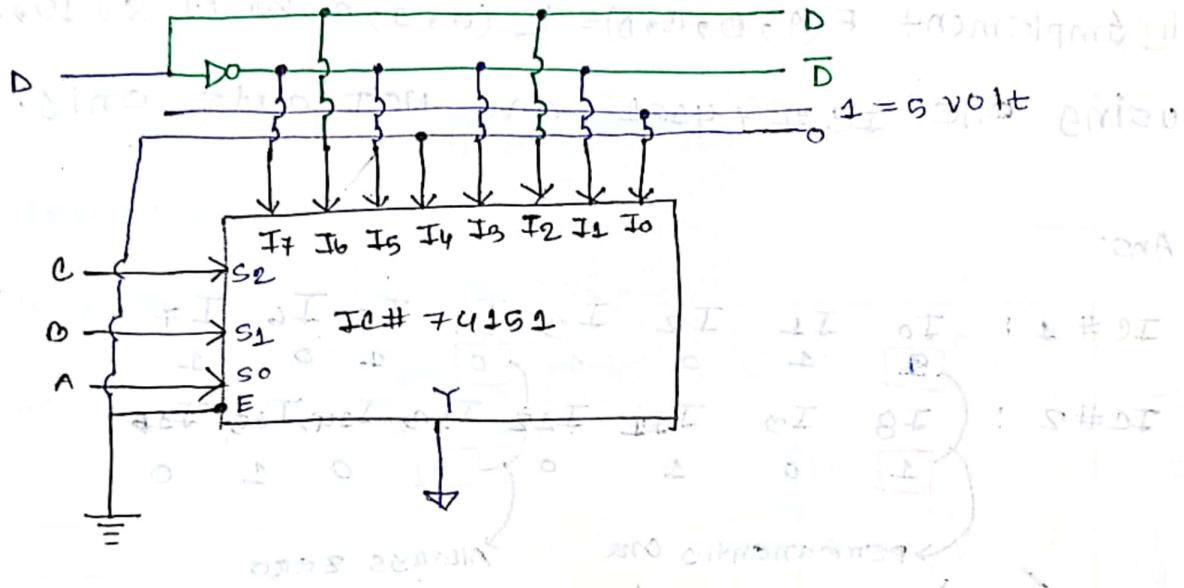
Implement $F(A, B, C, D) = \sum(0, 2, 3, 5, 7, 8, 10, 14)$

using one IC #74151 and NOT gate only.

Ans:



D	C	B	A	Y
0	0	0	0	$I_0 = 1 \rightarrow$
0	0	0	1	$I_1 = 1 \rightarrow$
0	0	1	0	$I_2 = 0$
0	0	1	1	$I_3 = 1 \rightarrow$
0	1	0	0	$I_4 = 0$
0	1	0	1	$I_5 = 1 \rightarrow$
0	1	1	0	$I_6 = 0$
0	1	1	1	$I_7 = 1 \rightarrow$
1	0	0	0	$I_8 = 1 = I_0$
1	0	0	1	$I_9 = 0$
1	0	1	0	$I_{10} = 1 = I_2$
1	0	1	1	$I_{11} = 0$
1	1	0	0	$I_{12} = 0$
1	1	0	1	$I_{13} = 0$
1	1	1	0	$I_{14} = 1 = I_6$
1	1	1	1	$I_{15} = 0$



$$D = I_2, I_6$$

$$\bar{D} = I_1, I_3, I_5, I_7$$

$$I = 5 \text{ volt} = I_0$$

$$O = I_4$$

$$\{ \text{If } D=0 \text{ then } I_1=1 \quad \therefore I_1 = D$$

$$\{ \text{If } D=1 \text{ then } I_1=0 \quad \therefore I_1 = \bar{D}$$

$$\{ \text{If } D=0 \text{ then } I_2=0 \quad \therefore I_2 = D$$

$$\{ \text{If } D=1 \text{ then } I_2=1 \quad \therefore I_2 = \bar{D}$$

	A	B	D	O
$\leftarrow A = 0\right)$	0	0	0	0
$\leftarrow A = 1\right)$	1	0	0	0
$\leftarrow B = 0\right)$	0	1	0	0
$\leftarrow B = 1\right)$	1	1	0	0
$\leftarrow D = 0\right)$	0	0	1	0
$\leftarrow D = 1\right)$	1	0	1	0
$\leftarrow D = 0\right)$	0	1	1	0
$\leftarrow D = 1\right)$	1	1	1	0
$\leftarrow D = 0\right)$	0	0	0	1
$\leftarrow D = 1\right)$	1	0	0	1
$\leftarrow D = 0\right)$	0	1	0	1
$\leftarrow D = 1\right)$	1	1	0	1
$\leftarrow D = 0\right)$	0	0	1	1
$\leftarrow D = 1\right)$	1	0	1	1
$\leftarrow D = 0\right)$	0	1	1	1
$\leftarrow D = 1\right)$	1	1	1	1

I_1

I_2

$$I_3 \begin{cases} \text{if } D = 0 \text{ then } I_3 = 1 \\ \text{if } D = 1 \text{ then } I_3 = 0 \end{cases} \quad \therefore I_3 = \overline{D}$$

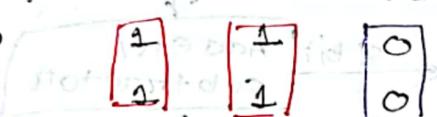
$$\text{Q} F(A, B, C, D) = \sum (0, 1, 2, 4, 8, 9, 15)$$

~~not summing~~

Ans:

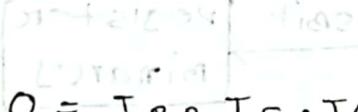
IC#0 : I_0, I_1, I_2

$D = 0$



IC#1 : I_8, I_9, I_{10}

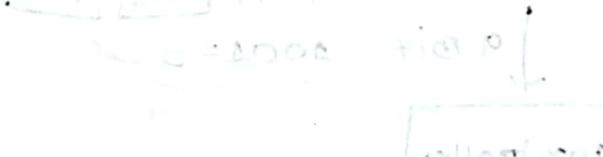
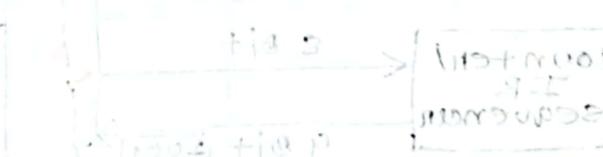
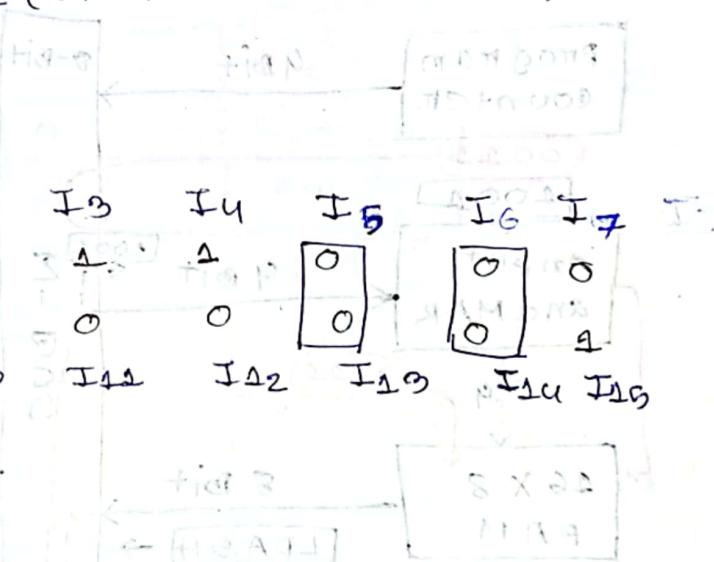
$D = 1$



$$1 = I_0, I_1$$

$$D = I_7$$

$$\overline{D} = I_3, I_9$$



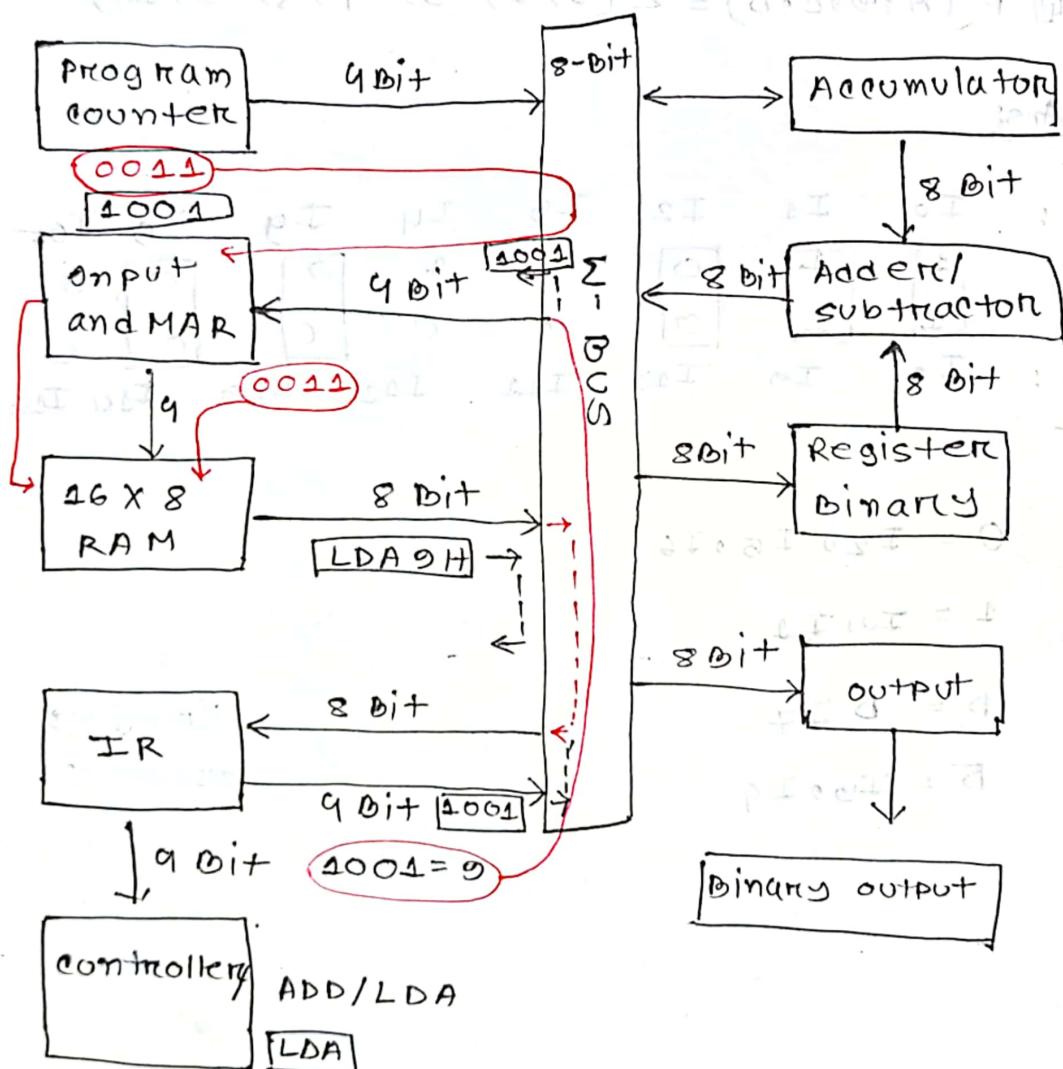
One number of terms in each function is minimum EA

extra terms may be added to obtain a minimum term

can be achieved by

SAP-1 (simple AS possible) computer

प्रोग्राम विकास



□ Program counter \Rightarrow generates Address (4 bit)

MAR (Memory Address Register) \Rightarrow stores into main memory

TTL RAM = Transistor to Transistor load

→ RAM reads bit and performs content.

$16 = 9H$

$= 100000$
 $= 80H$

$110000 = AH$

$= 10100$

$= 10H$

		ADD		9H → Hexa
		0001	1001	
		Data/content		
0	0	0	0	LDA 8H
0	0	0	1	ADD 9H
0	0	1	0	OUT
0	0	1	1	
0	1	0	0	ADD 9H
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	2
1	0	0	1	10
1	0	1	0	9
1	0	1	1	2
1	1	0	0	8
1	1	0	1	7
1	1	1	0	6
1	1	1	1	5

- ④ Load RAM Data into Accumulator \Rightarrow LDA

Q1 Write a code to do the following:

3+5=2 summing b/w the above MAR & code:

L DA 8H

ADD 9H

SUB 7H

OUT

HLT

8085 / 8080

Q2 Fetch cycle : T₆ T₅ T₄ T₃ T₂ T₁ T₀

cycle

1. PC → MAR = Address step (T₁)

EP LM

(T₂)

2. PC → CON = increment step (PC+1)

CP

3. MAR → RAM → IR → CON (T₃)

Fetch from RAM and

store in IR.

T₄ → RAM → Accumulator

LDA \Rightarrow Load RAM data into accumulator

ADD \Rightarrow Add RAM data into accumulator

SUB \Rightarrow Subtract RAM data from accumulator

OUT \Rightarrow Load accumulator data into output register (OUT \leftarrow ACC)

HLT \Rightarrow Stop processing (CLK \leftarrow 0)

④ can perform only arithmetic operation

⑤ Assembly Language

Machine Language

4 Hexadecimal Number

1. 01, 01 01

Binary Number

	OP code
LDA	\Rightarrow 0000
ADD	\Rightarrow 0001
SUB	\Rightarrow 0010
OUT	\Rightarrow 0110
HLT	\Rightarrow 1111

step 1: ACC \leftarrow 10H

step 2: ACC \leftarrow 10H + 18H = 28H X=40H

step 3: ACC \leftarrow 10H + 18H + 20H = 48H X=60H

step 4: ACC \leftarrow 10H + 18H + 20H - 14H = 52H X=70H

step 5: $\boxed{20H + 18H + 20H - 14H}$ X=70H

OUT = FH (0 \rightarrow 110) X=70H

HLT = FH

mostrar o resultado cifra mais alta em 0

$$40H = 1 \times 16^1 + 0 \times 16^0$$

$$16^1 = 16 + 0$$

$$= 16 \rightarrow \underline{\underline{10000}}$$

resultado obtido

$$\boxed{0001} \quad \boxed{0000} \quad H=3$$

resultado obtido

10000 \leftarrow 10H

10000 \leftarrow 40H

10000 \leftarrow 60H

10000 \leftarrow 70H

10000 \leftarrow 80H

10000 \leftarrow 90H

10000 \leftarrow A0H

10000 \leftarrow B0H

10000 \leftarrow C0H

10000 \leftarrow D0H

10000 \leftarrow E0H

10000 \leftarrow F0H

gus:

$$10H + 18H + 20H - 14H$$

10H most abos minimum out stored by

Assembly Language		Machine Language		
Address	contents	Address	contents in binary	contents in hex
0H	LDA FH	10H	10101010	1A
4H	ADD EH	14H	10010010	12
21H	ADD DH	18H	10010001	11
3H	SUB CH	20H	10010010 00000001	12 1
9H	OUT FH	24H	10010010 00000010	12 2
5H	HLT FH	28H	10010010 00000011	12 3
6H	FFH	2AH	10010010 00000101	12 5
7H	FFH	2DH	10010010 00001101	12 9
8H	FFH	30H	10010010 00010000	12 E
9H	FFH	34H	10010010 00010010	12 F
AH	FFH	38H	10010010 00010100	12 10
BH	FFH	3DH	10010010 00011100	12 14
CH	14H	40H	10010010 00100000	12 20
DH	20H	44H	10010010 00100100	12 24
EH	18H	48H	10010010 00100101	12 25
FH	20H	4DH	10010010 00101101	12 29
		50H	10010010 00110000	12 30
		54H	10010010 00110010	12 34
		58H	10010010 00110100	12 38
		5DH	10010010 00111101	12 41
		60H	10010010 01000000	12 40

OPERANDS

Ques: Write the assembly language program and generate the machine code for the following expression:

$$Ans: 52 + 28 - 38 + 72 - 12 \quad \text{Hence}$$

numbers are in decimal form:

$$D = 52 + 28 - 38 + 72 - 12$$

$$H = 34H + 1CH - 26H + 48H - 0C$$

Assembly Language		Machine Language		
Address	contents	Address	contents in binary	contents in Hex
0H	LDA FH	0000	0000 1111	0F
1H	ADD EH	0001	0001 1110	1E
2H	SUB DH	0010	0010 1101	2D
3H	ADD CH	0011	0011 1100	1C
4H	SUB BH	0100	0010 1011	2B
5H	OUT FH	0101	1110 1111	EF
6H	HLT FH	0110	1111 1111	FF
7H	FFH	0111	1111 1111	FF
8H	FFH	1000	1111 1111	FF
9H	FFH	1001	1111 1111	FF
AH	FFH	1010	1111 1111	FF
BH	0C	1011	0000 1100	0C
CH	48H	1100	0100 1000	48
DH	26H	1101	0010 0110	26
EH	1C	1110	0001 1100	1C
FH	34H	1111	0011 1000	34

$$D : 48 - 20 + 35 + 37 - 8$$

$$H : 12H - 14H + 23H + 25H - 08H$$

Qus: write the SAP-1 Assembly language program & ...
 : $48 - 20 + 35 + 37 - 8$.

Address	contents	Address	contents in Binary	contents in Hex
0H	LDA FH	0000	0000 1111	OF
1H	SUB EH	0001	0010 1110	2E
2H	ADD BH	0010	0001 1101	1D
3H	ADD CH	0011	0001 1100	1C
4H	SUB BH	0100	0010 1011	2B
5H	OUT FH	0101	1110 1111	EF
6H	HLT FH	0110	1111 1111	FF
7H	FFH	0111	1111 1111	FF
8H	FFH	1000	1111 1111	FF
9H	FFH	1001	1111 1111	FF
AH	FFH	1010	1111 1111	FF
BH	08H	1011	0000 1000	08
CH	25H	1100	0010 0101	25
DH	23H	1101	0010 0011	23
EH	14H	1110	0001 0100	14
FH	12H	1111	0001 0010	12

$$2+8+60+58-22 = 11$$

$$H_2O \rightarrow H_2S + H_2S + H_2 + H_2S + H$$

Last Topic:

Synchronous counter (Any sequence)

$\rightarrow 0, 1, 3, 5, 7, 0, \dots$

Step 1: Circuit Excitation Table:

Before Pulse	After Pulse			J_C	K_C	J_D	K_D	J_A	K_A
	C	B	A						
0 0 0	0 0 1			0 x	0 x	0 x	0 x	1 x	
0 0 1	0 1 1			0 x	1 x	1 x	1 x	x 0	
* 0 1 0	0 0 0			0 x	0 x	0 x	0 x	x 1	0 x
0 1 1	1 0 1			1 x	1 x	1 x	1 x	x 1	x 0
* 1 0 0	0 0 0			x 1	0 x	0 x	0 x	0 x	0 x
1 0 1	1 1 1			x 0	1 x	1 x	1 x	x 0	
* 1 1 0	0 0 0			x 1	1 x	x 1	x 1	0 x	
1 1 1	0 0 0			x 1	x 1	x 1	x 1	x 1	

Undesired step

If undesired step comes, turn it starts

from 0 0 0.

JK Flip FLOP:

J	K	CLK	Q
0	0	↑	N.C
0	1	↑	0
1	0	↑	1
1	1	↑	Toggle

J	K	Q
0 → 0	0 0	0 - x
0 → 1	1 1	q - x
1 → 1	0 0	x 0
1 → 0	1 1	x 1

Step 2: Simplification using K-MAP:

	$\bar{A}\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$
\bar{C}	0	1	0	2
C	4	5	7	6

	$\bar{A}\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$
\bar{C}	0	0	1	0
C	x	x	x	x

count AS if 0

→ we need to loop every 1, so used x and assumed it 1.

$K_C \Rightarrow$

$\bar{A} + B$

x	x	x	x	x
1	0	1	1	0

2nd row 2nd column

0

A

$J_B \Rightarrow$

A

0	1	x	x
0	1	x	x

A

$K_D \Rightarrow 1$

x	x	1	1
1	1	1	1

Nothing common

$J_A \Rightarrow$

$\bar{B} \bar{C}$

1	x	x	0
0	x	x	0

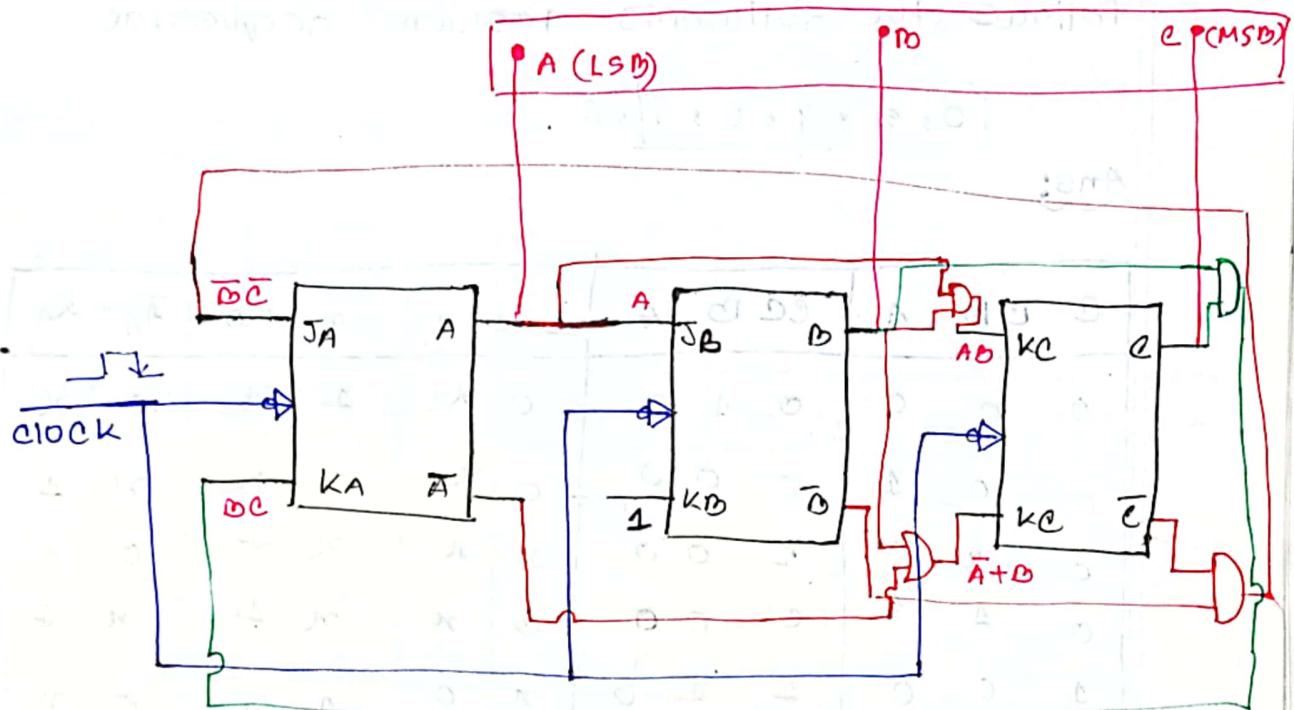
$\bar{B} \bar{C}$

$K_A \Rightarrow B C$

x	0	0	x
x	0	1	x

B C

Step 3 : circuit



$$\left. \begin{array}{l} J_A = K_A = 1 \\ J_A = K_A = A \\ J_C = K_C = A\bar{B} \end{array} \right\} (i)$$

Instead of (i)

$$J_A = \bar{B}\bar{C}$$

$$J_C = A\bar{B}$$

$$K_A = BC$$

$$K_C = \bar{A} + B$$

$$J_B = A$$

$$K_B = 1$$

Ques: Design the synchronous counter that follows the following fashion sequence:

Ans:

$[0, 2, 4, 6, 7, 0]$

C	B	A	C	B	A	J _C	K _C	J _B	K _B	J _A	K _A
0	0	0	0	1	0	0	x	1	x	0	x
0	0	1	0	0	0	0	x	0	x	x	1
0	1	0	1	0	0	1	x	x	1	0	x
0	1	1	0	0	0	0	x	x	1	x	1
1	0	0	1	1	0	x	0	1	x	0	x
1	0	1	0	0	0	x	1	0	x	x	1
1	1	0	1	1	1	x	0	x	0	1	x
1	1	1	0	0	0	x	1	x	1	x	1

Step: 2
Step: 3

$$QA = 96$$

(i) To obtain

$$D_2 = AC$$

$$D_1 = AB$$

$$D_0 = A\bar{B}$$

$$K = AB$$

$$L = \bar{A}B$$

Q) Design the counter of following sequence:

0, 1, 2, 5, 7, 9, 14, 13, 15, 0, ...

Ans: Excitation Table:

Before PULSE	After PULSE	J _D	K _D	J _C	K _C	J _B	K _B	J _A	K _A
0 0 0 0	0 0 0 1	0	x	0	x	0	x	1	x
0 0 0 1	0 0 1 1	0	x	0	x	1	x	x	0
0 0 1 0	0 0 0 0	0	x	0	x	x	1	0	x
0 0 1 1	0 1 0 1	0	x	1	x	x	1	x	0
0 1 0 0	0 0 0 0	0	x	x	1	0	x	0	x
0 1 0 1	0 1 1 1	0	x	x	0	1	x	x	0
0 1 1 0	0 0 0 0	0	x	x	1	x	4	0	x
0 1 1 1	1 0 0 1	1	x	x	4	x	1	x	0
1 0 0 0	0 0 0 0	x	1	0	x	0	x	0	x
1 0 0 1	1 0 1 1	x	0	0	x	1	x	x	0
1 0 1 0	0 0 0 0	x	1	0	x	x	1	0	x
1 0 1 1	1 1 0 1	x	0	1	x	x	1	x	0
1 1 0 0	0 0 0 0	x	1	x	4	0	x	0	x
1 1 0 1	1 1 1 1	x	0	x	0	1	x	x	0
1 1 1 0	0 0 0 0	x	1	x	2	x	1	0	x
1 1 1 1	0 0 0 0	x	4	x	1	x	4	x	1

Step 2: Simulation using K-map: 4×4 K-MAP = 4

$$J_D \Rightarrow$$

$\bar{A}\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$
$\bar{A}B$	0	0	0
$A\bar{B}$	0	0	1
AB	x	x	x
$\bar{A}B$	x	x	x

$$\rightarrow ABC = 101$$

$$K_D \Rightarrow \bar{A} + BC$$

x	x	x	x
x	x	x	x
1	0	1	1
1	0	0	1

$$\text{quad} = BC$$

$$\text{octet} = \bar{A}$$

$$J_C \Rightarrow AD$$

0	0	1	0
x	x	x	x
x	x	x	x
0	0	1	0

$$\text{quad} = AD$$

$$K_0 = B + \bar{A}$$

x	x	x	x
1	0	1	1
1	0	1	1
x	x	x	x

$B \oplus A = K_0$

$B \oplus A$

$$J_B \Rightarrow A$$

0	1	x	x
0	1	x	x
0	1	x	x
0	1	x	x

$J_B \Leftarrow A$

$$J_B \Rightarrow 1$$

x	x	1	1
x	x	1	1
x	x	1	1
x	x	1	1

$J_A \Rightarrow \overline{B} \overline{C} \overline{D}$

α	α	α	0
0	α	α	0
0	α	α	0
0	α	α	0

$K_A \Rightarrow B C D$

α	0	0	α
α	0	0	α
α	0	α	α
α	0	0	α

Step 3: circuit HW to implement logic of 404

Assignment:

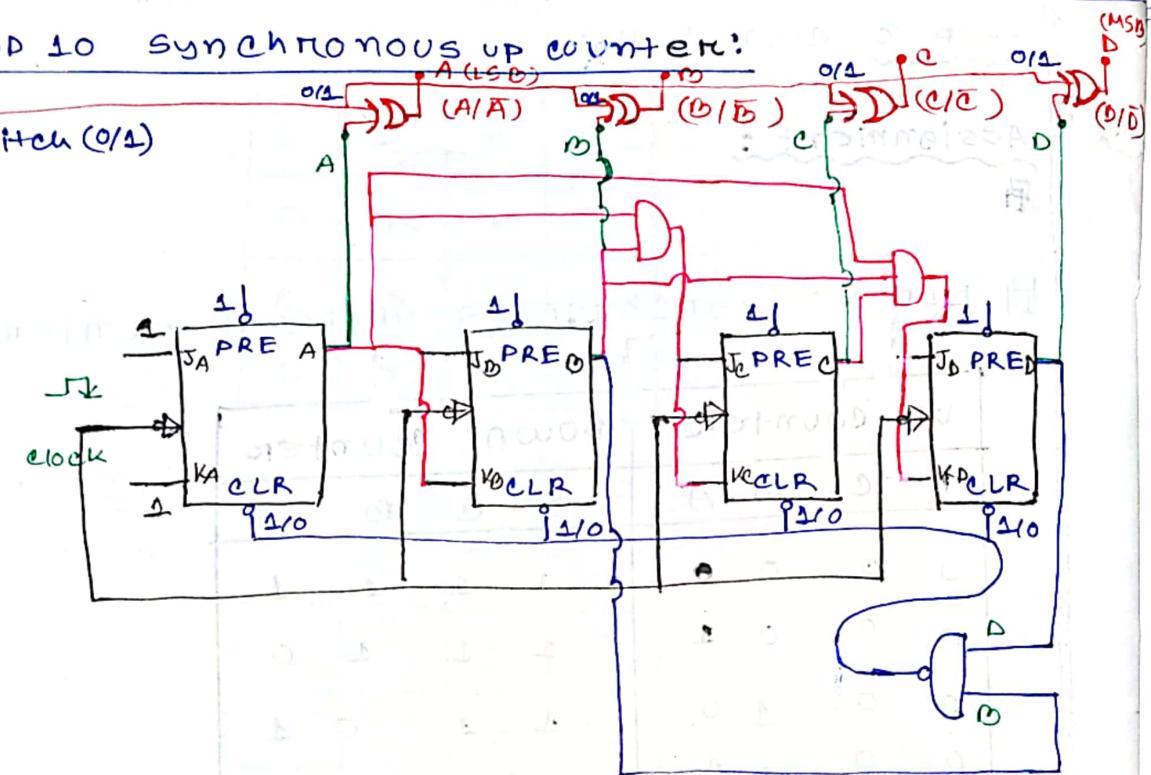


MOD 10 synchronous UP/DOWN counter:

UP Counter	Down Counter
D C B A	D C B A
0 0 0 0	1 1 1 1
0 0 0 1	1 1 1 0
0 0 1 0	1 1 0 1
0 0 1 1	1 1 0 0
0 1 0 0	1 0 1 1
0 1 0 1	1 0 1 0
0 1 1 0	1 0 0 1
0 1 1 1	1 0 0 0
1 0 0 0	0 1 1 1
1 0 0 1	0 1 1 0
0 0 0 0	1 0 0 1
:	:

MOD 10 SYNCHRONOUS UP COUNTER:

switch (0/1)



OPERATION:

if $S=0$ then output are $D C B A$.

\therefore This is UP counter.

if $S=1$ then output are $D \bar{C} \bar{B} \bar{A}$.

\therefore This is DOWN counter.