

2.9.24

(circuit maker)

input \Rightarrow browse \leftarrow for (OFF) AND

switch \rightarrow digital \rightarrow logic switch

Display \rightarrow digital \rightarrow logic display \rightarrow wire

tool (+) \rightarrow simulation \rightarrow digital mode \rightarrow run simulation.

4.9.24

Digital Logic Design (DLD)

Book: Digital Systems by Ronald J. Tocci

Chapter: 1, 2, 3, 4, 5, 6, 7, 8, 9
↓
for reading prog 201

Chapter 3: Logic gates and Boolean Algebra

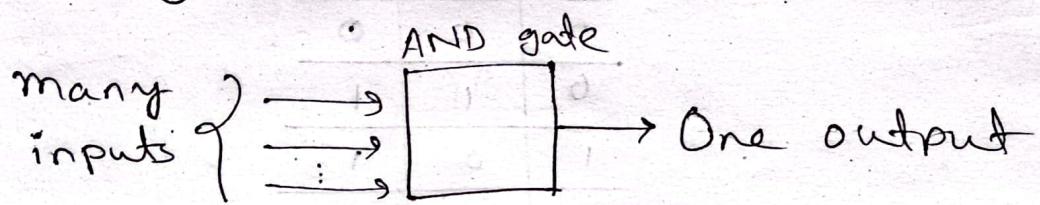
T \rightarrow 1 / HIGH / 5 Volts

F \rightarrow 0 / LOW / 0 Volts

Logic gates:

- ① AND
 - ② OR
 - ③ NOT
- Basic logic gate

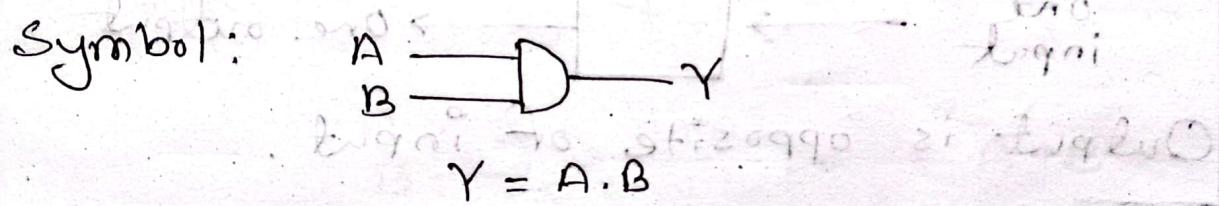
① AND gate:



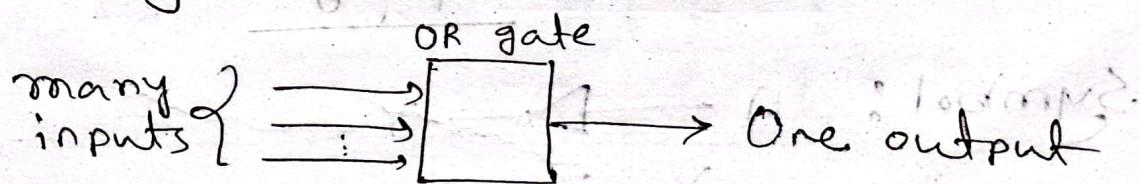
Output will be HIGH when all the inputs are HIGH; otherwise output will be LOW.

Truth Table:

	A	B	Y
0	0	0	0
0	1	0	0
1	0	0	0
1	1	1	1



② OR gate:



Output will be LOW when all the inputs are LOW; otherwise output will be HIGH.

Truth Table:

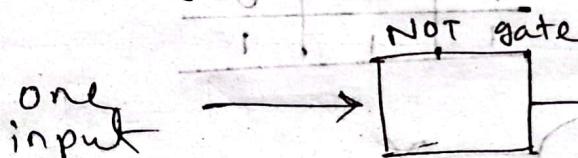
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Symbol:



$$Y = A + B$$

(iii) NOT gate:



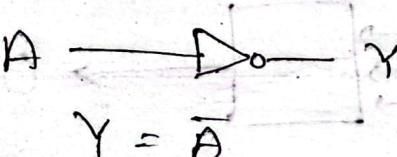
One output

Output is opposite of input.

Truth Table:

A	Y
0	1
1	0

Symbol:



$$Y = \bar{A}$$

Compound logic gates:

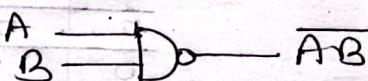
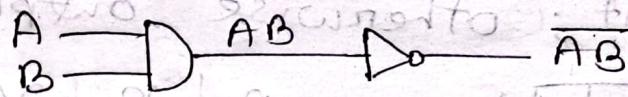
(iv) NAND gate

(v) NOR gate

(vi) Ex-OR gate

(vii) Ex-NOR gate

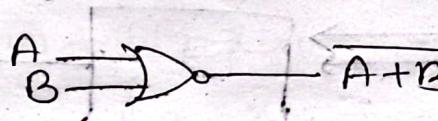
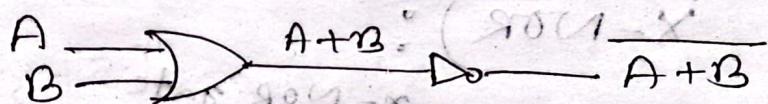
IV) NAND gate: $\text{NOT} \rightarrow \text{NAND}$



Truth Table:

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

V) NOR gate: $\text{NOT} \rightarrow \text{OR} \Rightarrow \text{NOR}$

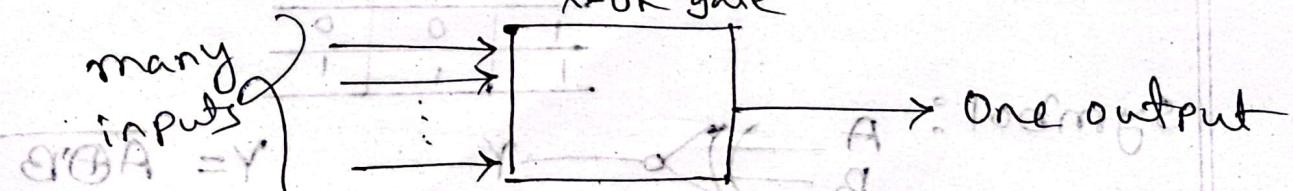


Truth Table:

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

VI) Ex-OR gate (Exclusive OR/Ex-OR/X-OR):

X-OR gate



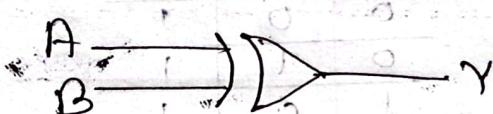
many
inputs
 $A \oplus A = Y$

Output will be HIGH when inputs are different; otherwise output will be LOW.

Truth Table:

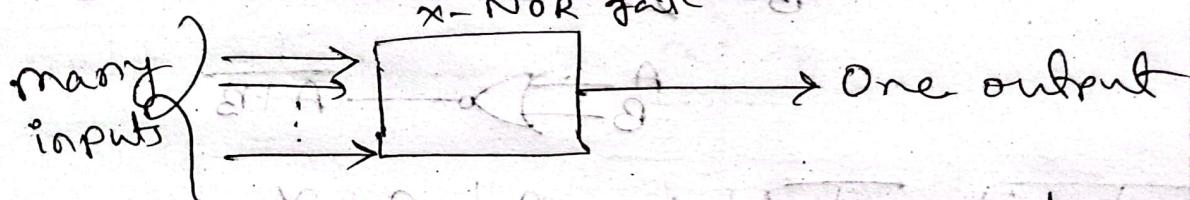
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Symbol:



$$Y = A \oplus B \quad A \oplus B$$

Mn Ex-NOR gate (Exclusive NOR / Ex-NOR / X-NOR)



Output will be HIGH when inputs are same; otherwise output will be LOW.
Opposite of Ex-OR gate.

Truth Table:

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Symbol:



$$Y = \overline{A \oplus B}$$

5.9.24

Simplification of logic expression:

Boolean Algebra

Boolean Algebra:

$$\textcircled{I} \quad x \cdot 0 = 0$$

$$\textcircled{II} \quad x \cdot 1 = x$$

$$\textcircled{III} \quad x \cdot x = x$$

$$\textcircled{IV} \quad x \cdot \bar{x} = 0$$

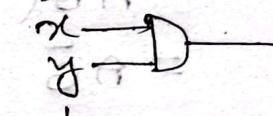
$$\textcircled{V} \quad x + 0 = x$$

$$\textcircled{VI} \quad x + 1 = 1$$

$$\textcircled{VII} \quad x + x = x$$

$$\textcircled{VIII} \quad x + \bar{x} = 1$$

Don't care input



$$\textcircled{IX} \quad x + y = y + x \quad \{ \text{commutative law}$$

$$\textcircled{X} \quad x \cdot y = y \cdot x$$

$$\textcircled{XI} \quad x + (y + z) = (x + y) + z = x + y + z \quad \{ \text{Associative law}$$

$$\textcircled{XII} \quad x \cdot (yz) = (xy) \cdot z = xyz \quad \{ \text{Distributive law}$$

$$\textcircled{XIII} \quad \text{a) } x(y+z) = xy + xz \quad \text{b) } (x+y)(w+z) = xw + xz + yw + yz$$

$$\textcircled{XIV} \quad x + xy = x \quad \| x + xy \Rightarrow x(1+y) \Rightarrow x \cdot 1 = x$$

$$\textcircled{XV} \quad \text{a) } x + \bar{x}y = x + y \quad \text{b) } x + xy = \bar{x} + y$$

$$\textcircled{XVI} \quad \overline{x+y} = \bar{x} \cdot \bar{y} \quad \{ \text{De Morgan's theorem}$$

$$\textcircled{XVII} \quad \overline{xy} = \bar{x} + \bar{y} \quad \{ \text{De Morgan's theorem}$$

$$(x+x) \text{ उपरी } \\ (x+\bar{x}y)$$

1) अनुकूल Term Common
Form 210

Simplification of logic expression using Boolean Algebra:

Q. $y = A\bar{B}D + \bar{A} \cdot A\bar{B}D$: Simplify

$$= A\bar{B}(D + \bar{D})$$

$$= A\bar{B}$$

Q. $y = ACD + \bar{A}BCD$

$$= CD(A + \bar{A}B)$$

$$= CD(A + B)$$

$$= ACD + BCD$$

$y = \overline{(\bar{A}+C)(B+\bar{D})} = \overline{(A+C)} \cdot \overline{(B+\bar{D})}$

$$= \overline{\bar{A}+C} + \overline{B+\bar{D}}$$

$$= \bar{A} \cdot \bar{C} + \bar{B} \cdot \bar{D} = (\bar{A} + \bar{C})(\bar{B} + \bar{D})$$

Q. $y = A\bar{B}\bar{C} + A\bar{B}C + ABC$

$$= AB(\bar{C} + C) + ABC$$

$$= AB + ABC$$

$$= A(B + BC)$$

$$= A(\bar{B} + C)$$

$$\begin{aligned}
 \text{Q3} \quad Y &= \bar{A}C(\bar{A}\bar{B}\bar{D}) + \bar{A}B\bar{C}\bar{D} + A\bar{B}C + 28A = B \\
 &= \bar{A}C(\bar{A} + \bar{B} + \bar{D}) + \bar{A}B\bar{C}\bar{D} + A\bar{B}C \\
 &= \bar{A}C(A + \bar{B} + \bar{D}) + \bar{A}B\bar{C}\bar{D} + A\bar{B}C \\
 &= \bar{A}\bar{B}C + \bar{A}C\bar{D} + \bar{A}B\bar{C}\bar{D} + A\bar{B}C \\
 &= \bar{B}C(\bar{A} + A) + \bar{A}\bar{D}(C + \bar{B}\bar{C}) \\
 &= \bar{B}C + \bar{A}\bar{D}(C + B)
 \end{aligned}$$

$$\begin{aligned}
 \text{Q4} \quad Y &= \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC \\
 &= BC(\bar{A} + A) + A\bar{B}C + A\bar{B}\bar{C} + BA \\
 &= BC + A\bar{B}C + AB\bar{C} \\
 &= C(B + A\bar{B}) + AB\bar{C} \\
 &= C(B + A) + AB\bar{C} \\
 &= CB + CA + AB\bar{C} \\
 &= CB + A(C + B\bar{C}) \\
 &= CB + A(C + B) \\
 &= CB + AC + AB + (\bar{B}A + \bar{B}B) \\
 &= CB + AC + AB + (\bar{B}A + B) \\
 &= CB + AC + AB + B
 \end{aligned}$$

Q

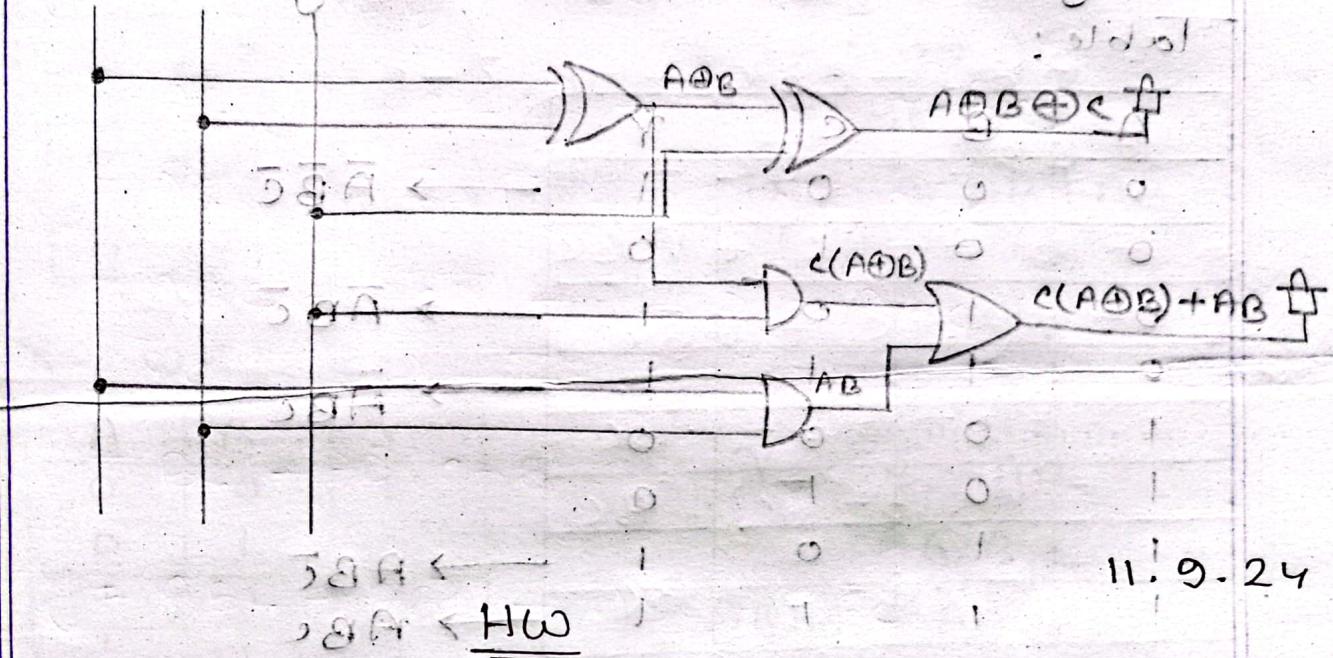
$$\begin{aligned}Y &= \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC \\&= \bar{A}BC + A\bar{B}C + AB(\bar{C} + \bar{C}) \\&= \bar{A}BC + A\bar{B}C + AB \\&= \bar{A}BC + A(B + \bar{B}) \\&= \bar{A}BC + A(B + C) \\&= \bar{A}BC + AB + AC \\&= B(A + \bar{A}C) + AC \\&= B(A + C) + AC \\&= AB + BC + AC\end{aligned}$$

9.9.24

$$\begin{aligned}X &= \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}C + ABC \\&= \bar{A}(\bar{B}C + B\bar{C}) + A(\bar{B}C + BC) \\&= \bar{A}(B \oplus C) + A(\overline{B \oplus C}) \\&= A \oplus B \oplus C\end{aligned}$$

$$\begin{aligned}Y &= \bar{A}Bc + A\bar{B}C + AB\bar{C} + ABC \\&= C(\bar{A}B + A\bar{B}) + AB(\bar{C} + C) \\&= C(A \oplus B) + AB\end{aligned}$$

At B, C is not binary off register



11.9.24

De Morgan's Law: ~~not thinking to me~~

$$\overline{A+B} = \bar{A} \cdot \bar{B}$$

$$\overline{AB} = \bar{A} + \bar{B}$$

A	B	$\bar{A}B$	\bar{B}	$\bar{A} \cdot \bar{B}$	$A+B$	$\overline{A+B}$
0	0	1	1	1	0	1
0	1	1	0	0	1	0
1	0	0	1	0	1	0
1	1	0	0	0	1	0

$$\bar{B}A + \bar{B}A + \bar{A}B$$

A	B	AB	$\bar{A}B$	\bar{A}	\bar{B}	$\overline{A+B}$
0	0	0	1	1	1	1
0	1	0	1	1	0	1
1	0	0	1	0	1	1
1	1	1	0	0	0	0

Design the circuit from a given truth table:

Table:

A	B	C	Y	
0	0	0	1	$\rightarrow \bar{A}\bar{B}\bar{C}$
0	0	1	0	$\rightarrow \bar{A}B\bar{C}$
0	1	0	1	$\rightarrow \bar{A}BC$
0	1	1	1	$\rightarrow \bar{A}BC$
1	0	0	0	
1	0	1	0	
1	1	0	1	$\rightarrow A\bar{B}\bar{C}$
1	1	1	1	$\rightarrow ABC$

Sum of product form:

$$Y = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}BC + AB\bar{C} + ABC$$

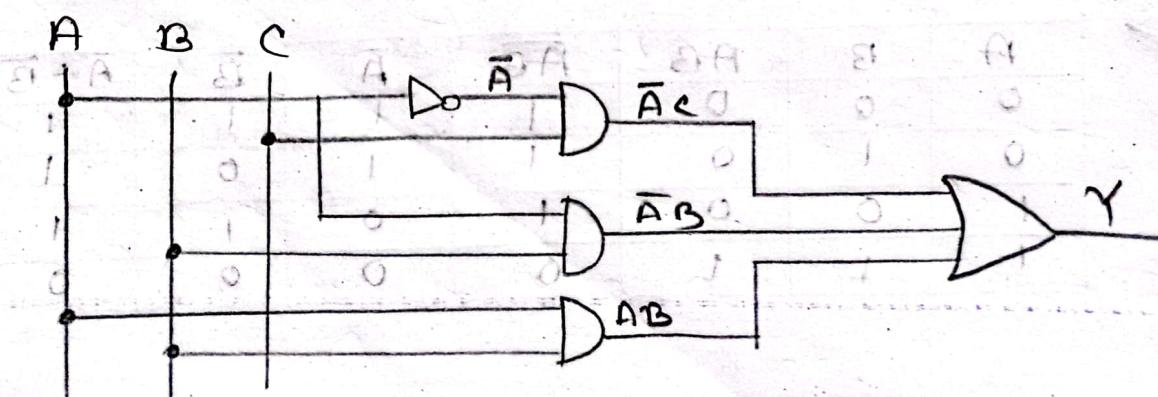
$$= \bar{A}C(\bar{B} + B) + \bar{A}B\bar{C} + AB(\bar{C} + C)$$

$$= \bar{A}C + \bar{A}B\bar{C} + AB$$

$$= \bar{A}(C + B\bar{C}) + AB$$

$$= \bar{A}(C + B) + AB$$

$$= \bar{A}C + \bar{A}B + AB$$



X-OR :

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

$$S\bar{A} + S\bar{B} + S\bar{A}\bar{B} + S\bar{A} = Y$$

$$Y = \bar{A}B + A\bar{B} =$$

$$= A \oplus B$$

$$\bar{S}A + \bar{S}\bar{B} + \bar{S}\bar{A}\bar{B} =$$

$$A \oplus B = \bar{A}B + A\bar{B}$$

$$S\bar{A} + (\bar{S}\bar{A} + A)S =$$

$$S\bar{A} + (S + A)S =$$

$$S\bar{A} + S + AB =$$

$$Y = \bar{A}\bar{B} + A\bar{B} =$$

$$= A \oplus B$$

$$A \oplus B = \bar{A}\bar{B} + A\bar{B}$$

$$S\bar{A} + S + \bar{A}B =$$

X-NOR:

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

$$S\bar{A} + S\bar{B} + AB =$$

$$Y = \bar{A}\bar{B} + A\bar{B} =$$

$$= A \oplus B$$

$$A \oplus B = \bar{A}\bar{B} + A\bar{B}$$

$$S\bar{A} + S + \bar{A}B =$$



Design the logic circuit from a given Statement.

Q) A, B, C are inputs and Y is the output.
Output will be high when majority of inputs are high. Design the circuit.

For circuit draw

Truth Table
②

8 minterms

6 minterms

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

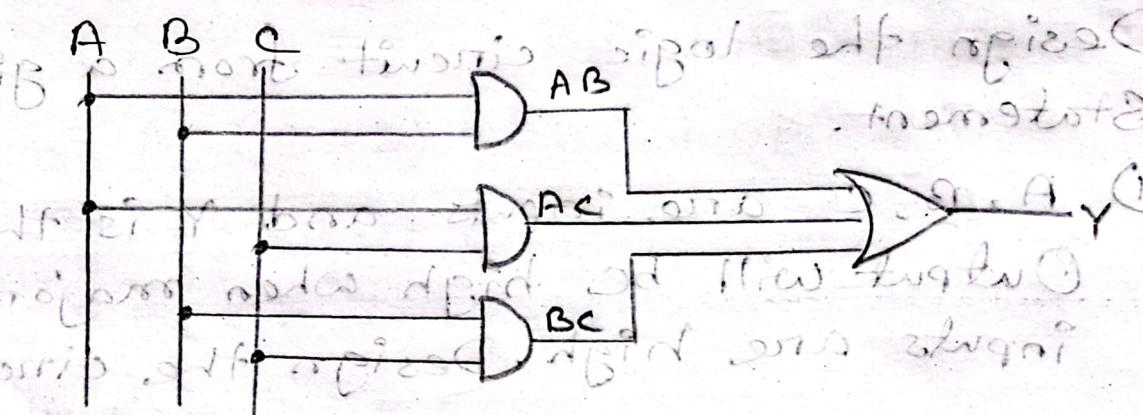
$\rightarrow \bar{A}BC$

$\rightarrow A\bar{B}C$

$\rightarrow ABC\bar{C}$

$\rightarrow ABC$

$$\begin{aligned}
 Y &= \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC \\
 &= \bar{A}BC + A\bar{B}C + AB(C + \bar{C}) \\
 &= \bar{A}BC + A\bar{B}C + AB \\
 &= B(A + \bar{A}C) + A\bar{B}C \\
 &= B(A + C) + A\bar{B}C \\
 &= BA + BC + A\bar{B}C \\
 &= A(B + \bar{B}C) + BC \\
 &= A(B + C) + BC \\
 &\text{Simplifying, } A = AB + AC + BC
 \end{aligned}$$



Q Design the logic circuit that follows the following requirement.

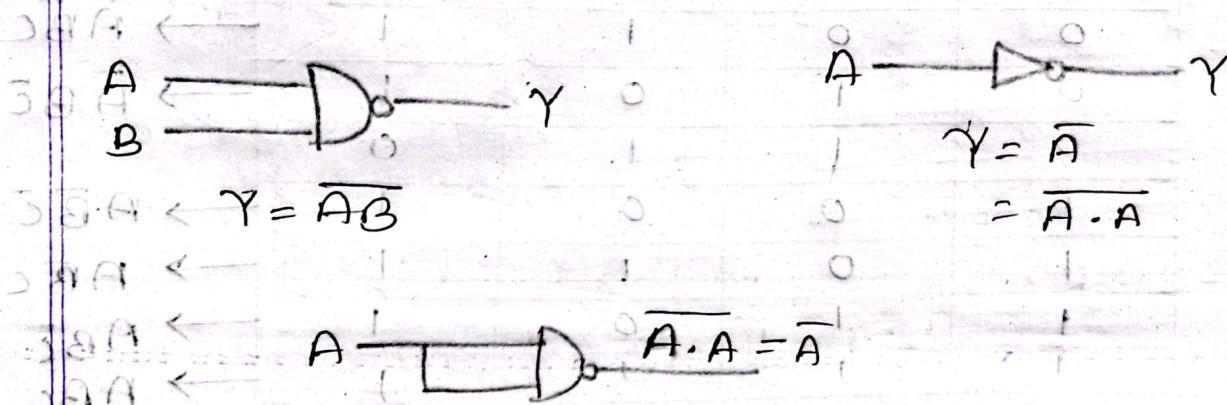
- i) Output x will equal A when B and C are same.
- ii) Output x remain HIGH when B and C are different.

A	B	C	X	
0	0	0	0	$\bar{A}\bar{B}\bar{C}$
0	0	1	1	$\bar{A}B\bar{C}$
0	1	0	1	$A\bar{B}\bar{C}$
0	1	1	0	$A\bar{B}C$
1	0	0	1	$A\bar{B}\bar{C}$
1	0	1	1	$AB\bar{C}$
1	1	0	1	$AB\bar{C}$
1	1	1	1	ABC

$$\begin{aligned}
 Y &= \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}\bar{C} + A\bar{B}C + AB\bar{C} + ABC \\
 &= \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}(\bar{C}+C) + AB(\bar{C}+C) \\
 &= \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B} + AB \\
 &= \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A(B+\bar{B}) \\
 &= \bar{A}\bar{B}\bar{C} + \cancel{\bar{A}B\bar{C}}^X + A \\
 &= \cancel{\bar{A}\bar{B}\bar{C}}^Y + A + B\bar{C} \\
 &= A + \bar{B}\bar{C} + B\bar{C} \\
 &= A + B \oplus C
 \end{aligned}$$

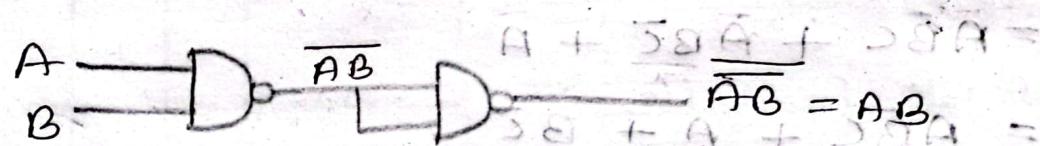
 Universality of NAND gate: NOR 
OR 
AND 

(i) NAND to NOT:

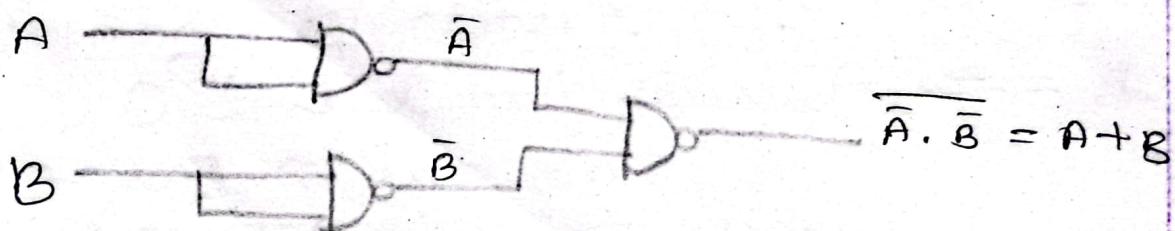
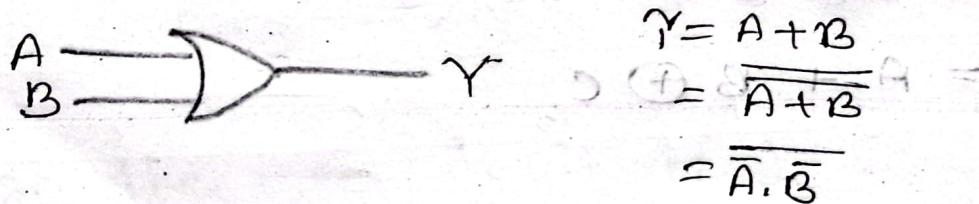


(ii) NAND to AND:

$$\begin{aligned} & \Sigma \bar{A}B + \Sigma \bar{A}B + \Sigma \bar{A}A + \Sigma \bar{A}\bar{A} + \Sigma \bar{B}\bar{A} = Y \\ & (\Sigma \bar{A}B + \Sigma \bar{A}B) + \Sigma \bar{A}A + \Sigma \bar{B}\bar{A} = \\ & Y = AB + \bar{A}A + \Sigma \bar{B}\bar{A} = \\ & (AB) + \bar{A}A + \Sigma \bar{B}\bar{A} = \end{aligned}$$



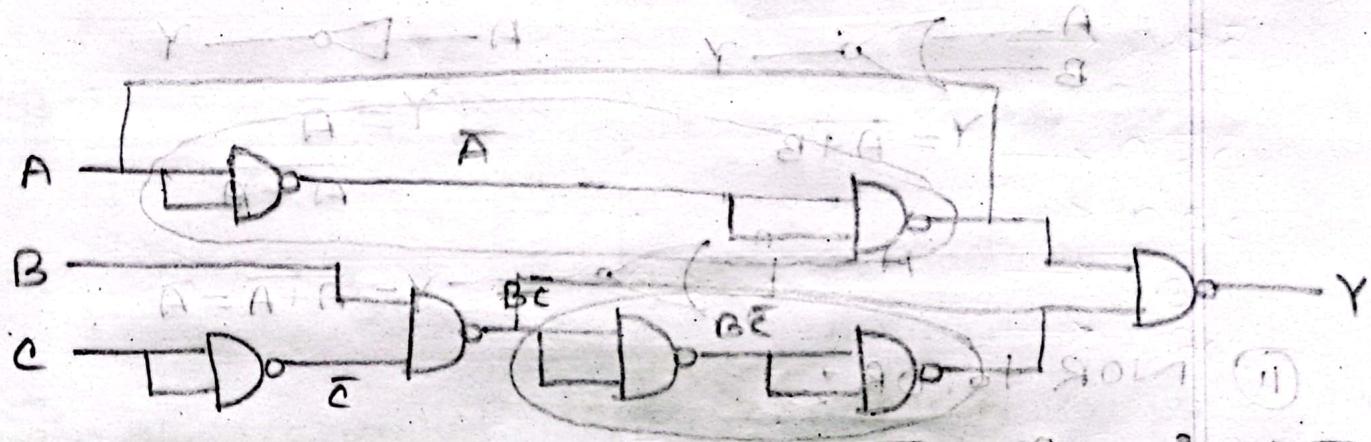
(iii) NAND to OR:



Therefore we can design any basic gate using NAND gate only. So, we can say NAND gate is a

Universal gate.

Q) $Y = \bar{A} + BC \rightarrow$ Using NAND gate only.



Circuits are not

simplified version exists 210.

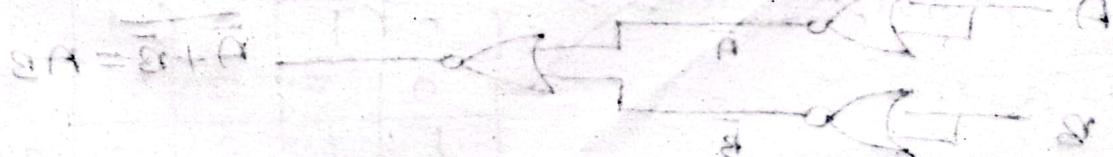
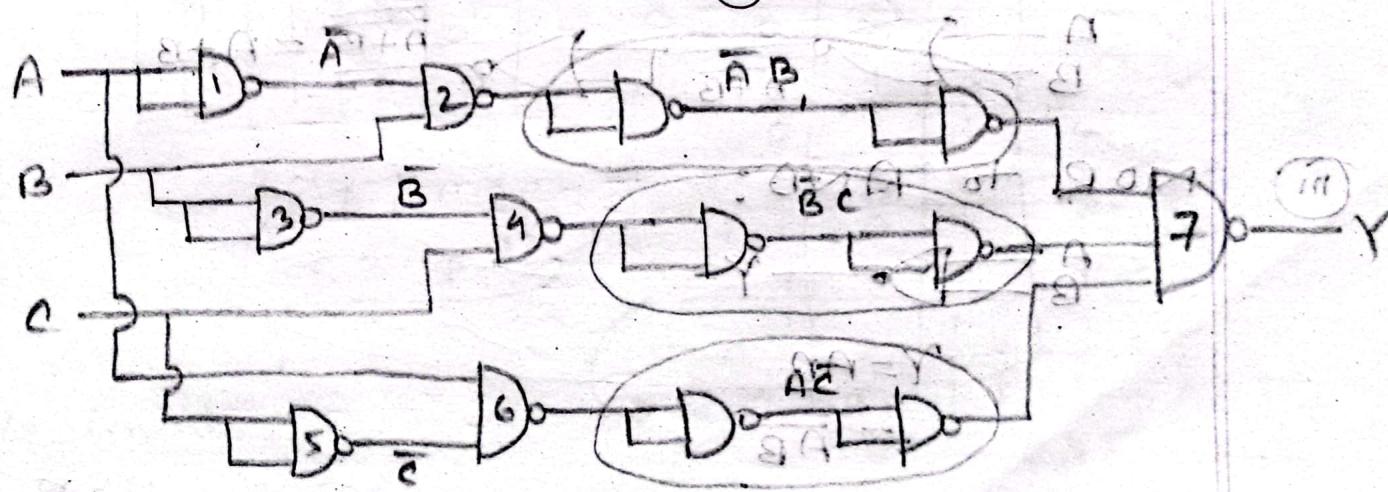
extra 21 NOT

gate circuit short

$$\bar{A} + \bar{B} = Y$$

no. fig 210

Q) $Y = \bar{A}B + \bar{B}C + A\bar{C} \rightarrow$ Using NAND gate.

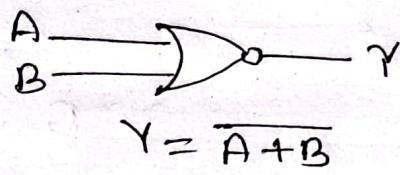


the step needs four apes now we materialized
in the 2011 fig 2 no. 2012 plus step 2011
the 2011 fig 2 no. 2012 plus step 2011
the 2011 fig 2 no. 2012 plus step 2011



Universality of NOR gate:

(i) NOR to NOT:



$$A \rightarrow \text{NOR} \rightarrow Y$$

$$Y = \overline{A}$$

$$= \overline{A+A} = A$$

$$A \rightarrow \text{NOR} \rightarrow Y = \overline{A+A} = A$$

(ii) NOR to OR:

$$A \rightarrow \text{NOR} \rightarrow Y$$

$$Y = A+B$$

~~step circuit = $\overline{\overline{A+B}}$ $\rightarrow \overline{5A+2B+8\bar{A}} = Y$~~

$$A \rightarrow \text{NOR} \rightarrow \overline{A+B} \rightarrow \overline{\overline{A+B}} = A+B$$

(iii) NOR to AND:

$$A \rightarrow \text{NOR} \rightarrow Y$$

$$Y = AB$$

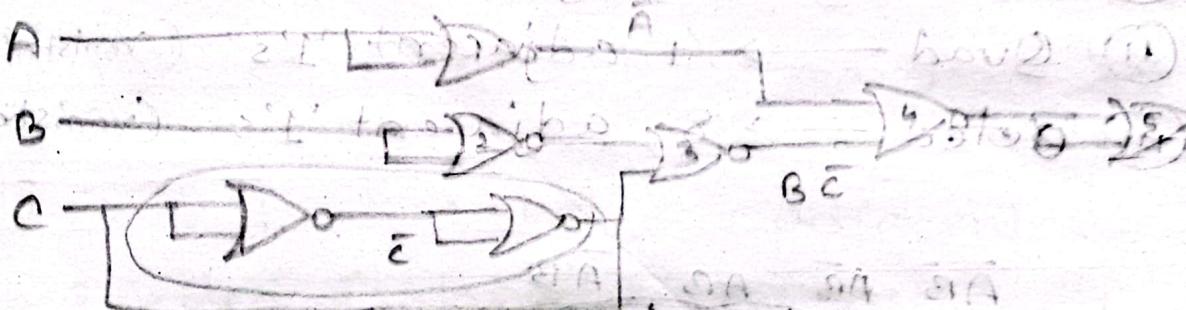
$$= \overline{\overline{AB}}$$

$$= \overline{\overline{A} + \overline{B}}$$

$$A \rightarrow \text{NOR} \rightarrow \overline{A} \rightarrow \text{NOR} \rightarrow \overline{\overline{A} + \overline{B}} = AB$$

Therefore we can design any basic gate using NOR gate only. So, we can say NOR gate is a Universal gate.

Q) $Y = \bar{A} + BC$ → using NOR gate only.



Q) Simplification of logic expression using K-map.

What is K-map?

*

	$\bar{A}\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$
\bar{C}	0	1	1	1
C	1	1	1	0

2x4 K-map
(for 3 inputs)

*

4 inputs

4x4 K-map

	$\bar{A}\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$
$\bar{C}\bar{D}$	1	0	1	0
$C\bar{D}$	0	0	0	0
$C\bar{D}$	1	0	1	1
$\bar{C}D$	1	1	0	0

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

$$Y = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} + A\bar{B}\bar{C} + AB\bar{C} + AB\bar{C} + ABC$$

$$Y = \bar{A}\bar{B}\bar{C}D + A\bar{B}CD$$

$$+ \bar{A}\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}D \\ + AB\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D} \\ + \bar{A}\bar{B}CD$$

Looping

- ① Pair \rightarrow 2 adjacent '1's (vanished 1 var)
 - ② Quad \rightarrow 4 adjacent '1's (Vanished 2 var)
 - ③ Octec \rightarrow 8 adjacent '1's (vanished 3 var)
- start count ←

	$A\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$	
\bar{C}	0 1 1 1	1 0 1 0			$\rightarrow BC$
	1 1 1 0				$\downarrow A$
					$\downarrow BC$

	$A\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$	$\bar{B}\bar{D}$	
$\bar{C}\bar{D}$	1 1 0 0	0 1 0 0	1 0 1 1	1 1 1 1	0 1 0 1	$\rightarrow BC$
$C\bar{D}$	1 0 1 1	0 0 1 1	1 1 1 1	1 1 1 1	1 0 1 1	$\rightarrow D$
$\bar{C}D$	1 1 1 1		1 1 1 1	1 1 1 1		$\downarrow B\bar{C}D$

$$Q_2 Q_1 + Q_2 \bar{Q}_1 = Y$$

$Q_2 Q_1 + Q_2 \bar{Q}_1 > \text{Octec} > \text{Quad} > \text{Pair} > \text{nothing}$

$$Q_2 Q_1 + \bar{Q}_2 Q_1 +$$

$$Q_2 \bar{Q}_1 +$$

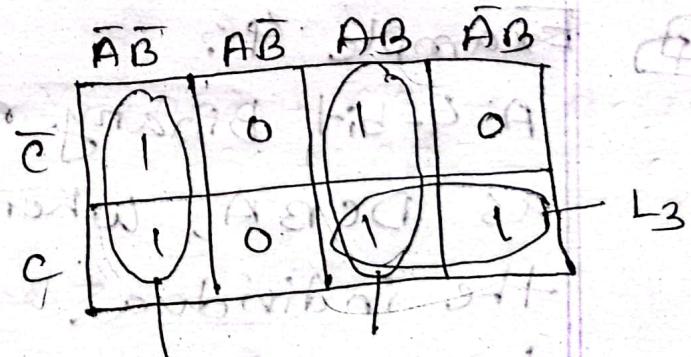
	0	0	0	0	0	0
	1	1	0	1	0	1
	1	0	1	1	1	0
	0	1	1	0	1	1
	1	1	1	1	1	1

Algorithm is of K-map:

- i) Draw the K-map according to number of inputs and hence input inject 1's in appropriate position.
- ii) find '1's that has no adjacent 1. That 1 is called isolated 1. If so then loop itself.
- iii) find '1's that has exactly one adjacent 1; if so then pair them.
- iv) Find octet ; if any
- v) find Quad ; if any
- vi) Find Pair ; if any
- vii) Write down sum form for each of the loops result. $\bar{A}B + \bar{B}\bar{A} = Y$

Example:

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1



$$\begin{aligned}
 Y &= \bar{A}\bar{B} + \bar{A}B + BC \\
 &= \overline{A \oplus B} + BC
 \end{aligned}$$

PS. 5 81

Q

4.11

$\bar{A}\bar{B}$ $A\bar{B}$ AB $\bar{A}B$

$\bar{C}\bar{D}$	1	1	1	1	L_2
$C\bar{D}$	1	1	0	0	
CD	0	0	0	1	L_3
$\bar{C}D$	0	0	1	1	

$$Y = \bar{A}BD + BC + \bar{B}\bar{D}$$

Q

$\bar{C}\bar{D}$	0	1	1	1	L_2
$C\bar{D}$	1	0	0	1	L_3
CD	0	0	0	0	
$\bar{C}D$	1	0	1	1	

$$Y = \bar{A}\bar{D} + BC + \bar{A}\bar{C}$$

B

Example 4:

A 4-bit binary number is represented as D_CBA , where D, C, B, A represent the individual bits and A is equal to LSB. Design the circuit that will produce a HIGH output whenever the binary number is greater than 0010 and less than 1010.

D	C	B	A	Y
0	0	0	0	101
0	0	0	1	001
0	0	1	0	000
0	0	1	1	111
0	1	0	0	111
0	1	0	1	111
0	1	1	0	111
0	1	1	1	111
1	0	0	0	111
1	0	0	1	111
1	0	1	0	111
1	0	1	1	111
1	1	0	0	111
1	1	0	1	111
1	1	1	0	111
1	1	1	1	111

$\bar{A}\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$
0	0	1	0
1	1	1	1
0	0	0	0
1	1	0	0

$$Y = ABD + \bar{B}\bar{C}D + CD$$

25.9.24

Ex 5: A 4-bit binary number is represented as DCBA where D is MSB. Design a logic circuit that will produce a HIGH output whenever (The binary number is greater than 0011 and less than 1011) or (all the inputs are low) or (all the inputs are HIGH).

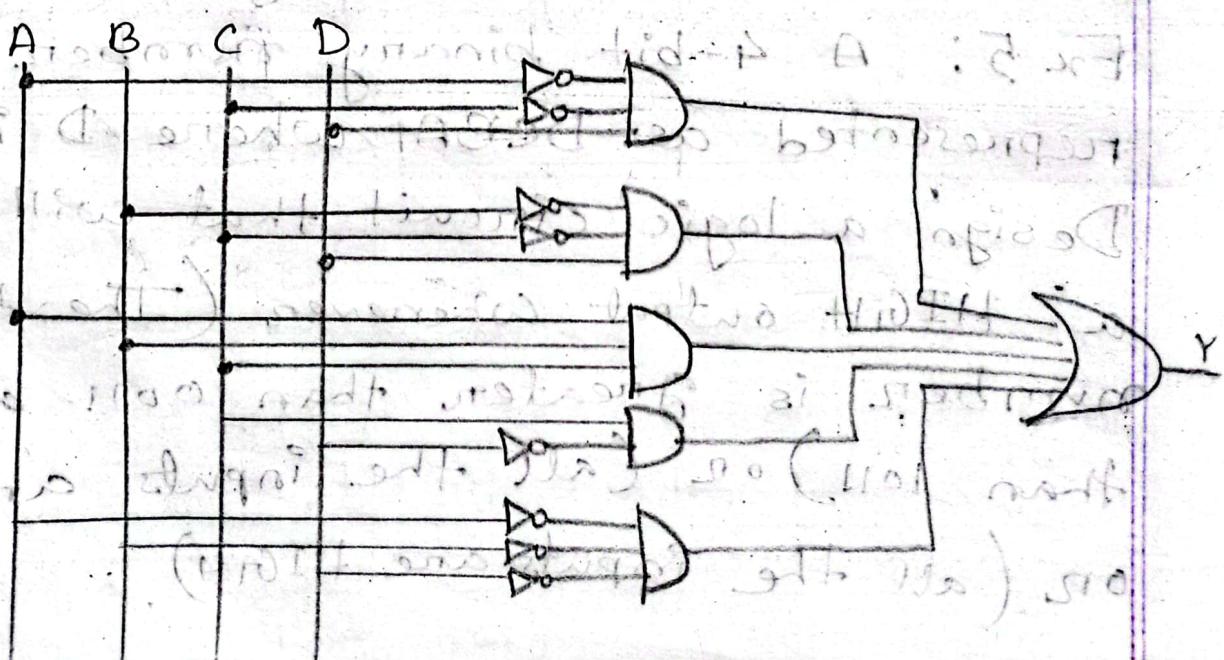
D	C	B	A	Y'
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

VS

	A	B	C	D	
	$\bar{A}\bar{B}$	$\bar{A}B$	AB	$A\bar{B}$	
	1	0	0	0	
	1	1	1	1	
	0	0	1	1	
	0	1	1	0	
	1	1	0	1	
	1	0	1	0	
	0	1	0	0	
	1	0	0	1	
	0	0	1	0	
	0	1	1	1	

$$\begin{aligned}
 Y &= \bar{A}\bar{C}D + \bar{B}\bar{C}D \\
 &\quad + A\bar{B}C + C\bar{D} \\
 &\quad + \bar{A}\bar{B}\bar{D}
 \end{aligned}$$

Draw the circuit



Ex

Implement $F(A, B, C) = \sum(0, 1, 4, 6, 7)$ using K-map

C	B	A	Y
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

msb ↑

$\bar{A}\bar{B}$	$\bar{A}B$	AB	$A\bar{B}$
1	1	0	0
0	1	0	1

$$Y = \bar{B}\bar{C} + \bar{A}\bar{B} + BC$$

$$= \bar{A}\bar{B} + \overline{B \oplus C}$$

0	1	3	2
4	5	7	6
12	13	15	14

Ex 7:

Implement $F(A, B, C, D) = \sum(0, 1, 2, 3, 6, 7, 9, 11, 14, 15)$ using K-map.

D	C	B	A	Y
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

msb ↑

$\bar{A}\bar{B}$	$\bar{A}B$	AB	$A\bar{B}$
1	1	1	1
0	0	1	1
0	0	0	0
1	0	1	0
0	1	1	0

$$Y = \bar{C}\bar{D} + BC + A\bar{C}$$

0	1	3	2
4	5	7	6
12	13	15	14
8	9	11	10

Ex 8: $F(A, B, C, D) = \sum(0, 2, 3, 4, 8, 9, 12, 13, 14, 15)$

	$\bar{A}\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$			
$\bar{C}\bar{D}$	1	0	1	1		L_1	
$\bar{C}D$	0	0	0	0			
$C\bar{D}$	1	1	1	1			
CD	1	1	0	0			
$\bar{C}\bar{D}$	1	1	0	0		L_3	
					L_4	L_2	

$$Y = B\bar{C}\bar{D} + \bar{B}D + CD + \bar{A}\bar{B}$$

Ques. $Y = \bar{A}\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}D + ABC + BCD + CD$

	$\bar{A}\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$			
$\bar{C}\bar{D}$	1	0	1	0		L_3	
$\bar{C}D$	0	0	1	0			
$C\bar{D}$	1	1	1	1			
CD	0	0	1	0		L_4	
$\bar{C}\bar{D}$	0	1	0	1			
					L_2		

$$= \bar{A}\bar{B}\bar{C}\bar{D} + A\bar{B}D + AB\bar{D} + CD$$

$$= 34 + 28 + 33 = Y$$

Mid term : Chapter 3, 4, 5, 6, 8 & 7 (part)

Chapter 6: Digital Arithmetics :

Operations and Circuits

Binary addition:

$$\begin{array}{r} 0 \\ + 1 \\ \hline 1 \end{array}
 \quad
 \begin{array}{r} 1 \\ + 0 \\ \hline 1 \end{array}
 \quad
 \begin{array}{r} 0 \\ + 0 \\ \hline 0 \end{array}
 \quad
 \begin{array}{r} 1 \\ + 1 \\ \hline 10 \end{array}$$

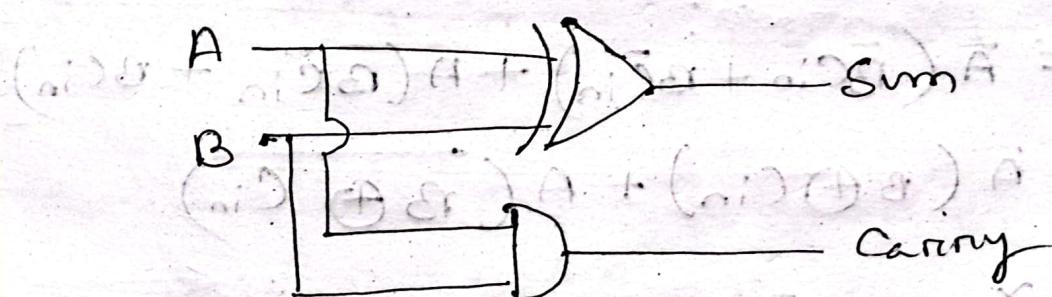
carry sum carry sum sum carry sum

Half Adder:

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	10	01
1	1	01	10

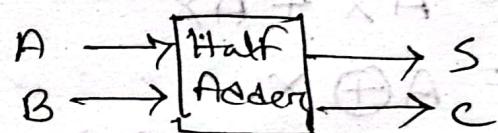
$\text{Sum} = \bar{A}\bar{B} + A\bar{B} + \bar{A}B = A \oplus B$
 $\text{Carry} = AB$

$$\text{Sum} = (\bar{A} \oplus B)A + (\bar{A} \oplus B)\bar{B} + (\bar{A} \oplus B)A\bar{B}$$



$$\begin{array}{r}
 11 \\
 + 13 \\
 \hline
 11000
 \end{array}$$

Block diagram:



Full adder:

A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Cin = Carry input

Cout = Carry output

	$\bar{A}\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$
Sum	0	1	0	1
Cin	1	0	1	0

$$\begin{aligned}
 \text{Sum} &= \bar{A}\bar{B}\text{Cin} + \bar{A}B\bar{\text{Cin}} + A\bar{B}\bar{\text{Cin}} + AB\text{Cin} \\
 &= \bar{A}(\bar{B}\text{Cin} + B\bar{\text{Cin}}) + A(\bar{B}\bar{\text{Cin}} + B\text{Cin}) \\
 &= \bar{A}(B \oplus \text{Cin}) + A(\bar{B} \oplus \text{Cin})
 \end{aligned}$$

$$\text{Let, } X = B \oplus \text{Cin}$$

$$= \bar{A}X + A\bar{X}$$

$$= A \oplus X$$

$$\text{Sum} = A \oplus B \oplus \text{Cin}$$

Q. 1.2

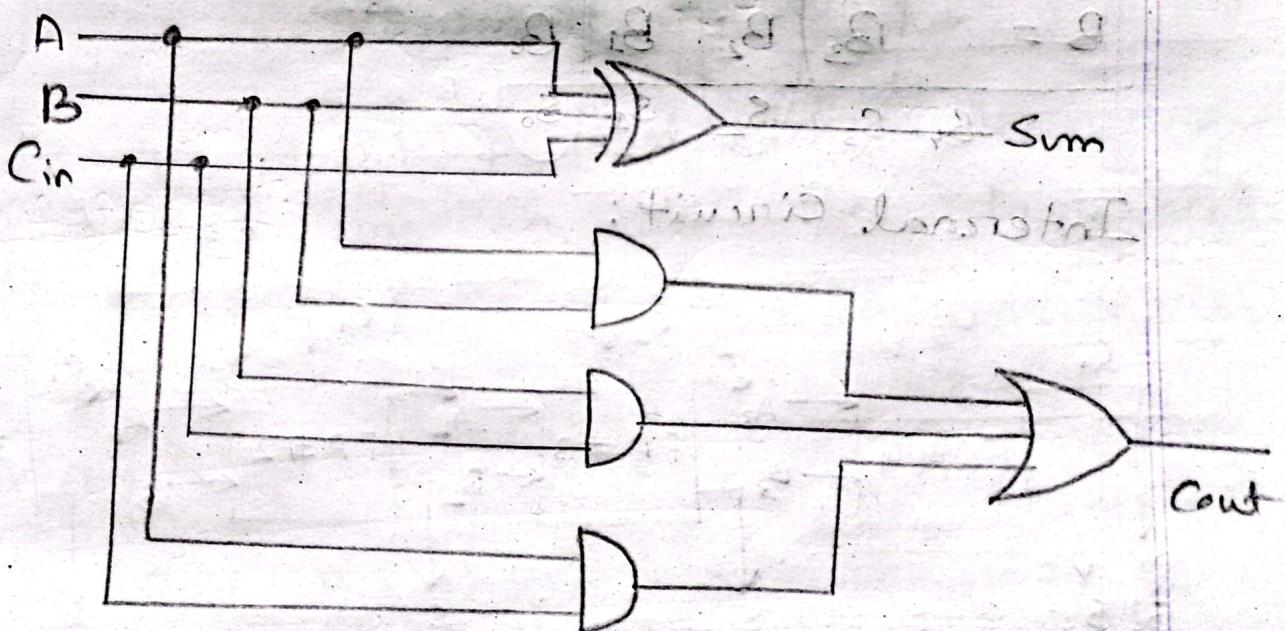
Classmate

Cout:

$\bar{A}\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$
\bar{C}_{in}	0 1 0 0	1 0 1 0	0 0 0 1
C_{in}	0 1 1 0	1 0 1 1	0 1 1 1

$$Cout = AB + BC_{in} + AC_{in}$$

Diagram:



Block diagram:



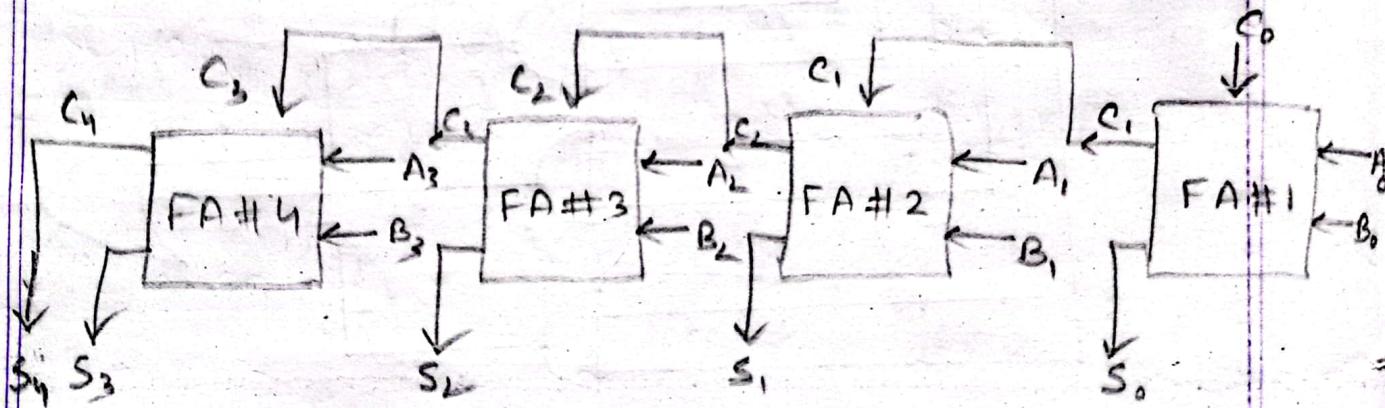
4-bit parallel adder : (IC # 7483 / 74283)

$$\begin{array}{r}
 13 = \begin{smallmatrix} 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 0 \end{smallmatrix} \\
 + 11 = \begin{smallmatrix} 1 & 1 & 0 & 1 \\ 1 & 1 & 0 & 1 \end{smallmatrix} \\
 \hline
 24 = \begin{smallmatrix} 1 & 1 & 0 & 0 \\ 1 & 1 & 0 & 0 \end{smallmatrix}
 \end{array}$$

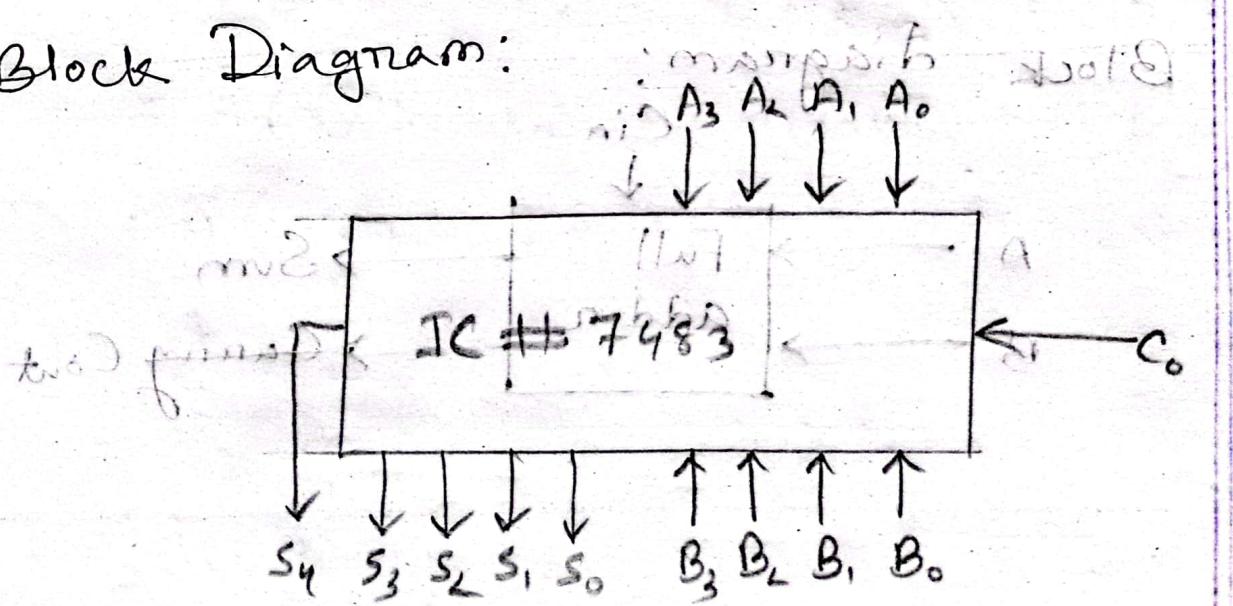
FA₄ FA₃ FA₂ FA₁
 C₄ C₃ C₂ C₁ C₀
 A = A₃ A₂ A₁ A₀
 B = B₃ B₂ B₁ B₀
 S₄ S₃ S₂ S₁ S₀

4-bit full Adder
MISCO

Internal Circuit:

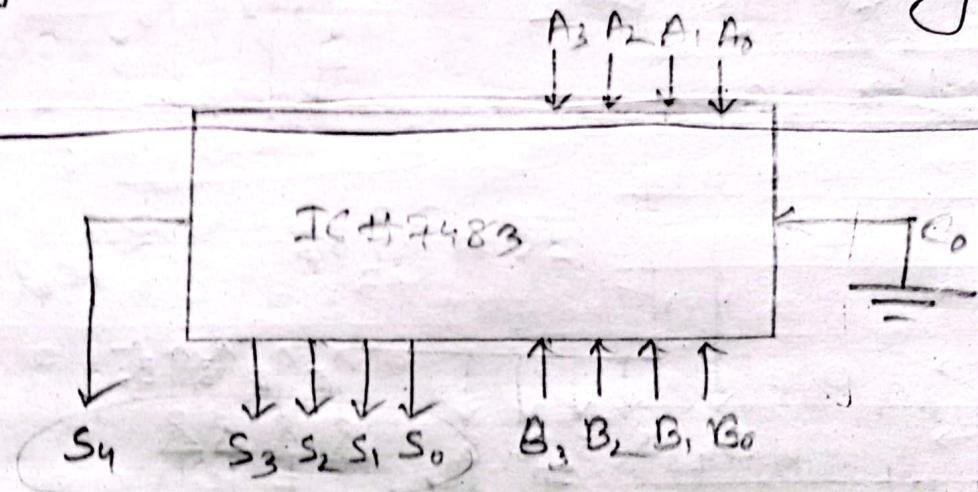


Block Diagram:



→ Addition AT 5EN⁻ C₀ = 0 2(5)

D) Design 4-bit parallel Adder using IC #7483



II) Design 4-bit parallel subtractor using IC #7483. You can use other logic gates, if necessary.

$$A - B \\ = A + (-B)$$

$$0 \ 1 \ 0 \ 1 \Rightarrow 5$$

$$1 \ 0 \ 1 \ 0 \Rightarrow 1\text{'s complement}$$

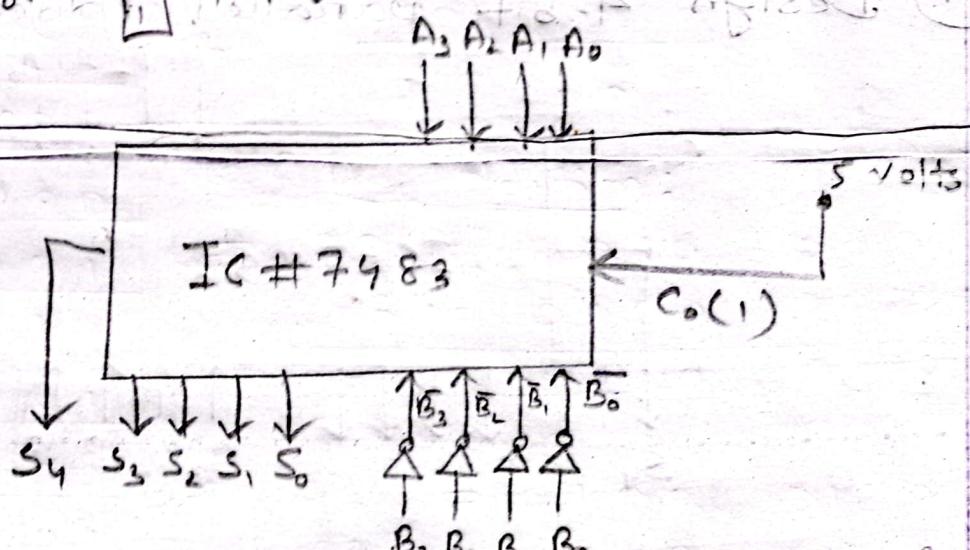
$$\begin{array}{r} 0 \ 1 \ 0 \ 1 \\ 1 \ 0 \ 1 \ 0 \\ \hline 1 \ 0 \ 1 \ 1 \end{array} \Rightarrow 2\text{'s complement} \\ (-5)$$

$$B \Rightarrow B_3, B_2, B_1, B_0$$

$$\begin{array}{r} \overline{B_3} \ \overline{B_2} \ \overline{B_1} \ \overline{B_0} \\ + \ 1 \\ \hline -B \end{array}$$

XOR	\rightarrow	A	B		Y
2's complement input	\leftarrow	0	0		0
0 2's input	\leftarrow	0	1		1

if $s=0$, then $C_0=0$
 if $s=1$, then $C_0=1$
 $\therefore s=C_0$



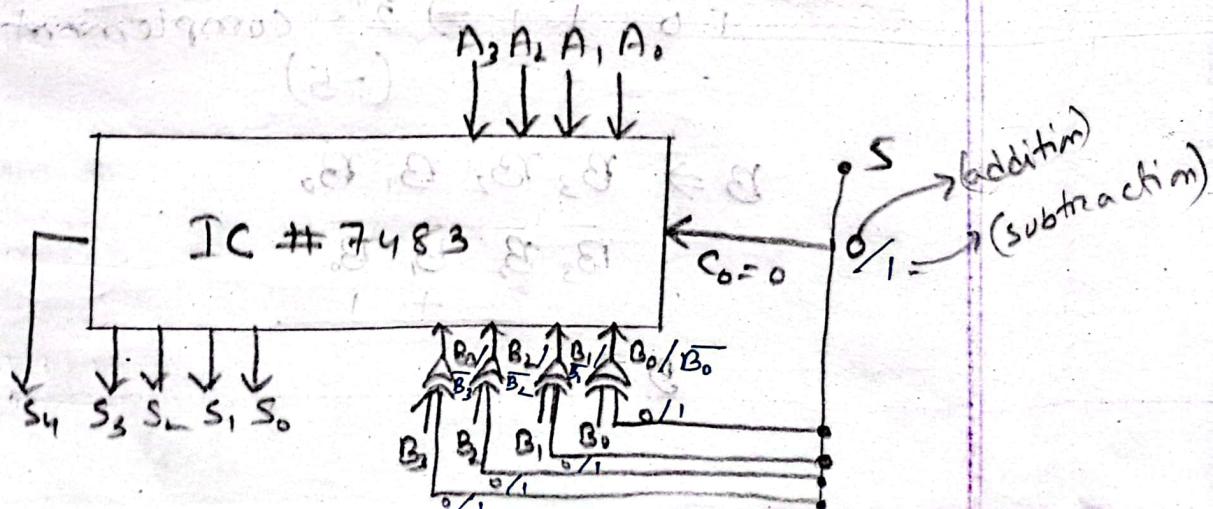
III) Design 4-bit parallel adder/

Subtractor using IC # 7483. You can use other logic gates if necessary.

Switch (s)

If $s=0$ then Adder $(A+B)$

If $s=1$ Then Subtractor $(A-B)$



Operation:

If $s=0$ Then first inputs are $A_3 A_2 A_1 A_0$

Second inputs are $\bar{B}_3 \bar{B}_2 \bar{B}_1 \bar{B}_0$

and $C_0 = s$

This is addition.

If $s=1$ Then first inputs are $A_3 A_2 A_1 A_0$

Second inputs are $\bar{B}_3 \bar{B}_2 \bar{B}_1 \bar{B}_0$

and $C_0 = 1$

This is Subtraction.

BCD Adder:

3.10.24

Q What is BCD?

BCD stands for Binary-Coded Decimal.

It's a way to represent decimal numbers using binary. In BCD, each digit of a decimal number is converted into its own binary code. Each decimal digit (0-9) is represented by a 4-bit binary number. It is useful because it allows for straight-forward conversion between binary and decimal formats while keeping each digit separate.

if sum > 9 and final carry = 0 ; then $(6)_{10} = 0110$ (Ans 2nd)

if sum ≤ 9 and final carry = 1 ; then $(6)_{10} = 0110$ (Ans 2nd)

if sum ≤ 9 and final carry = 0 ; 670 (Ans 1st) & 1970 (Ans 2nd)

$$(10)_{10} = (1010)_2 = \begin{array}{r} 0001 \\ + 0000 \\ \hline 0001 \end{array}$$

Decimal → BCD
0 → 0 0 0 0
1 → 0 0 0 1
2 → 0 0 1 0
3 → 0 0 1 1
4 → 0 1 0 0
5 → 0 1 0 1
6 → 0 1 1 0
7 → 0 1 1 1
8 → 1 0 0 0
9 → 1 0 0 1

BCD Addition:

$$\begin{array}{r} \# 23 = 0010 \quad 0011 \\ 43 = 0100 \quad 0011 \\ \hline 66 = 0110 \quad 0110 \end{array}$$

$$\begin{array}{r} \# 46 = 0100 \quad 0110 \\ 67 = 0110 \quad 0111 \\ \hline 1079 \quad 1010 \quad 1101 \\ 50, \quad 0110 \quad 0110 \\ \hline 1000 \quad 80011 \end{array}$$

$$\begin{array}{r} 0001 \quad 0001 \quad 0011 \\ \downarrow \quad \downarrow \quad \downarrow \\ (1 \quad 1 \quad 3)_{10} \end{array}$$

Here

Sum = 1, which is less than 9, and final carry = 1.

So we have to add $(6)_{10} = 0110$.

Now, $\begin{array}{r} 10001 \\ + 0001 \\ \hline 10100 \end{array}$

final carry $1 < 9$

Now,

$$\begin{array}{r} 0001 \quad 01101 \\ \downarrow \quad \downarrow \\ 17 \end{array}$$

$(17)_{10}$

Q

Design BCD adder using IC #7483. You can use other logic gates if necessary.

$$A \rightarrow A_3 \ A_2 \ A_1 \ A_0 \leq 9$$

$$B \rightarrow B_3 \ B_2 \ B_1 \ B_0 \leq 9$$

$$\underline{S_4 \ S_3 \ S_2 \ S_1 \ S_0 \leq 18}$$

S_4	S_3	S_2	S_1	S_0	
0	0	0	0	0	
0	0	0	0	1	
0	0	0	1	0	
0	0	0	1	1	
0	0	1	0	0	add '0'
0	0	1	0	1	$X = '0'$
0	0	1	1	0	when, $X = 1$
0	0	1	1	1	If, $S_4 = 1$ or $S_3 = 1$
0	1	0	0	0	AND
0	1	0	0	1	(either $S_2 = 1$ or $S_1 = 1$)
0	1	0	1	0	
0	1	0	1	0	
0	1	1	0	0	$X = S_4 + S_3(S_2 + S_1)$
0	1	1	0	1	
0	1	1	1	0	
0	1	1	1	1	
0	1	1	1	0	$X = '1'$
0	0	0	0	0	
0	0	0	0	1	
0	0	0	1	0	
0	0	0	1	1	
0	0	1	0	0	
0	0	1	0	1	
0	0	1	1	0	
0	0	1	1	1	
0	1	0	0	0	
0	1	0	0	1	
0	1	0	1	0	
0	1	0	1	1	
0	1	1	0	0	
0	1	1	0	1	
0	1	1	1	0	
0	1	1	1	1	

Condition:

* If sum > 9 , then $X = 1$

* If sum ≤ 9 , then $X = 0$

$X = '0'$ when, $X = 1$

If, $S_4 = 1$ or $S_3 = 1$

AND

(either $S_2 = 1$ or $S_1 = 1$)

$$X = S_4 + S_3(S_2 + S_1)$$

$X = '1'$ if $S_4 = 1$ or $S_3 = 1$

$X = '0'$ Logic output

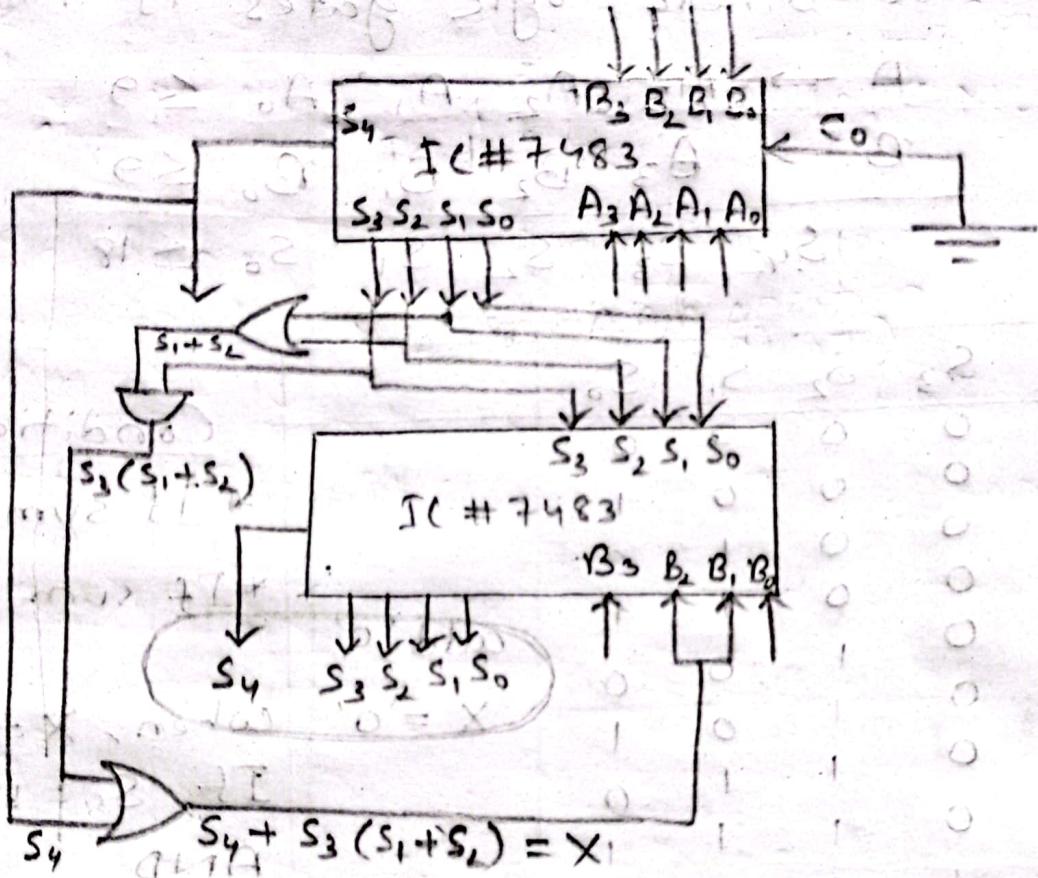
Invert S4 S3 S2 S1 High or

1 2 3 4 5 sum > 9

2 3 4 5 sum > 9

Carry 5 & string goes to 90

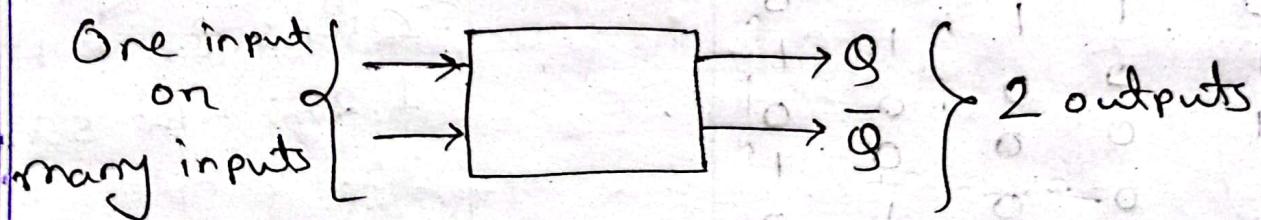
Carry 5 & string goes to 90



9.10.24

Chapter 5: flip flop

What is flip flop?

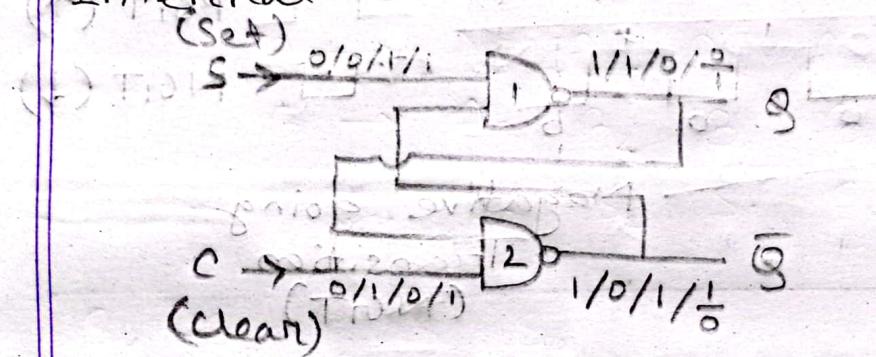


One or many inputs & 2 outputs.

One output is opposite of other output.

NAND Latch : ~~gold gift to do b37303~~

Internal Circuit :



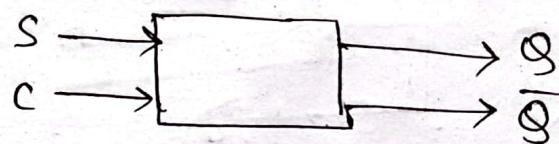
Operation & Truth Table:

S	C	Q
0	0	Invalid
0	1	1
1	0	0
1	1	No change

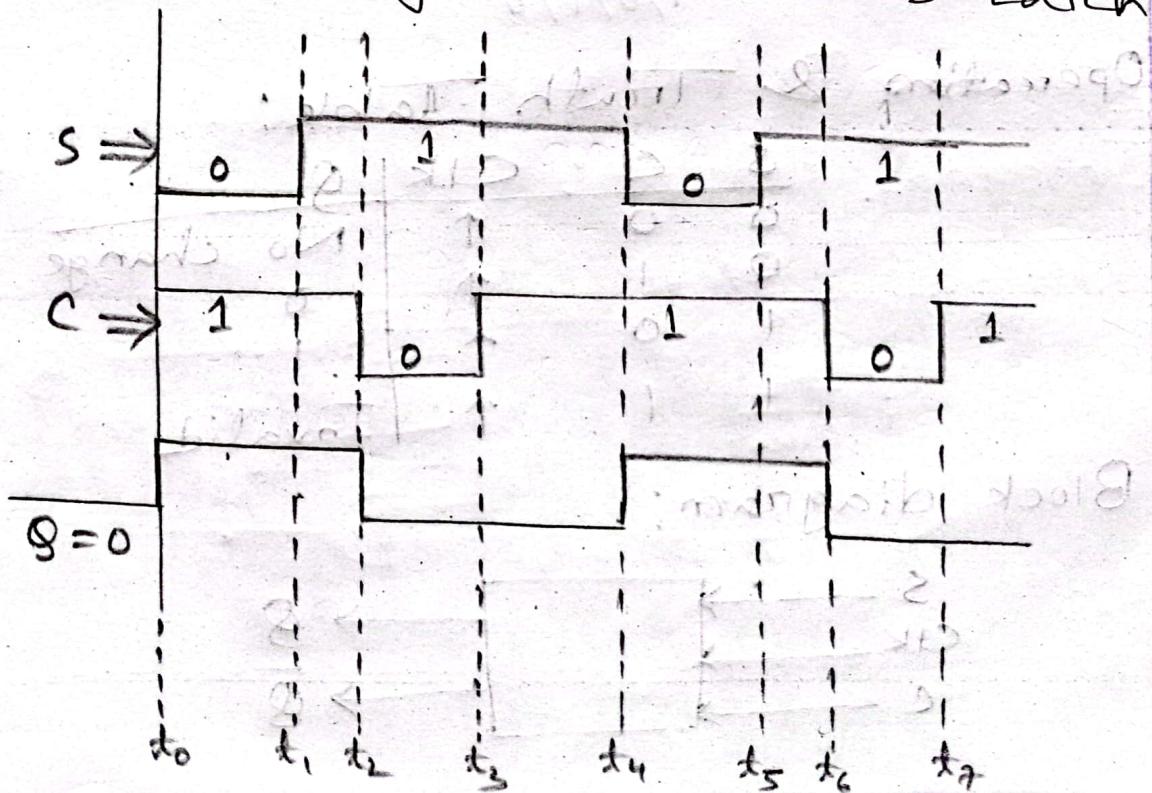
If initially $Q=0$, then finally $Q=0$

If initially $Q=1$, then finally $Q=1$.

Block diagram :

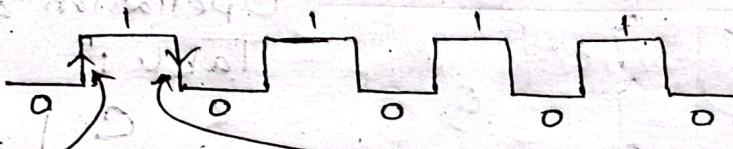


Waveform diagram of NAND Latch :



Clocked SC Flip Flop:

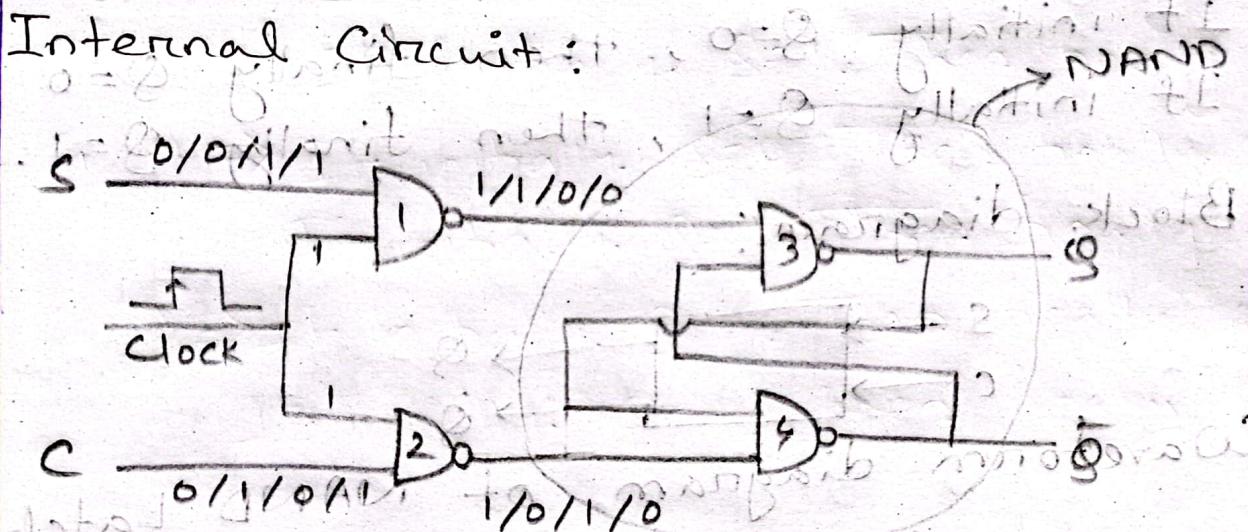
Clock



Positive going
Transition
(PGT)

Negative going
Transition
(NGT)

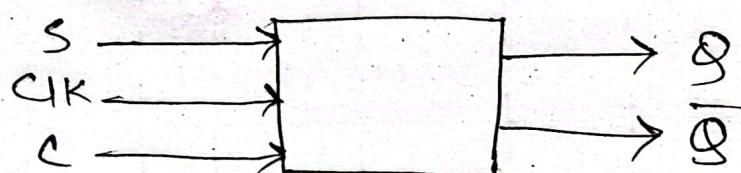
Internal Circuit:



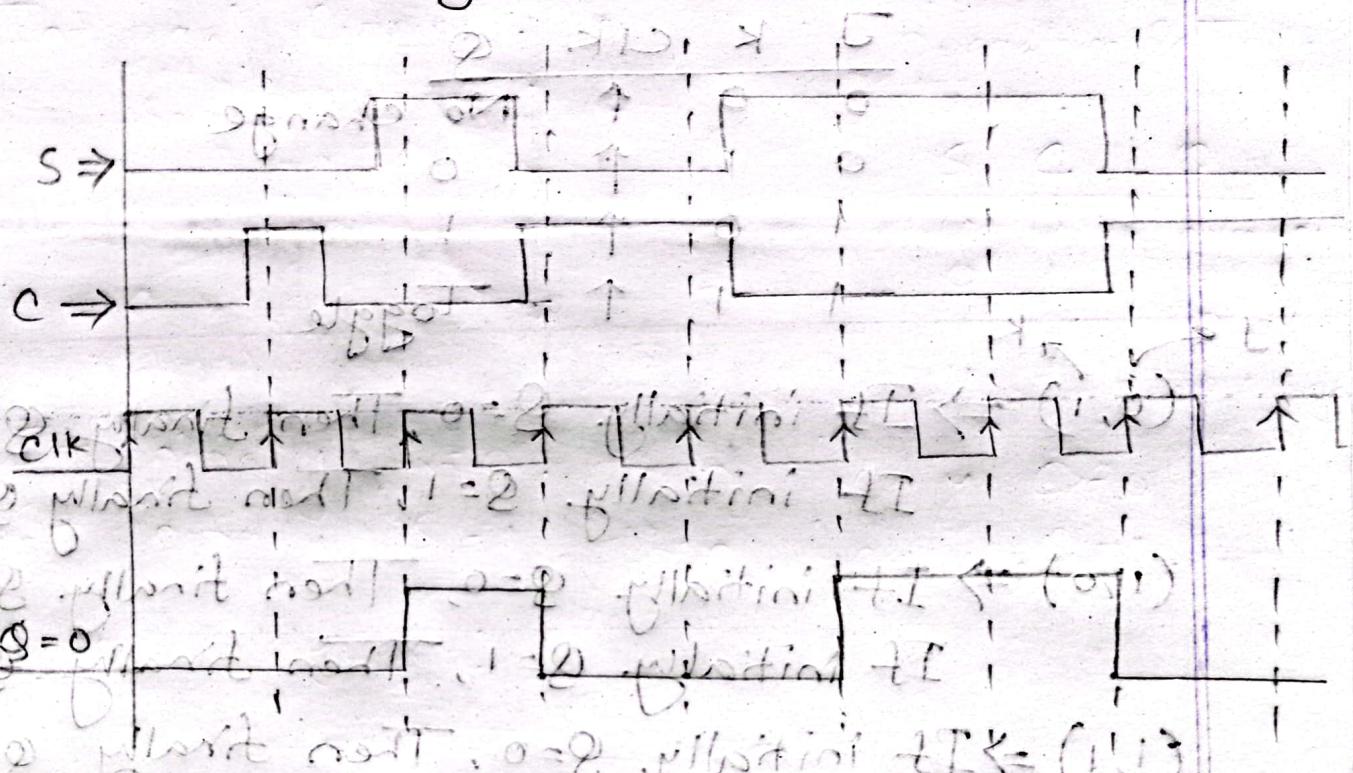
Operation & Truth Table:

S	C	CK	Q
0	0	↑	No change
0	1	↑	0
1	0	↑	1
1	1	↑	Invalid

Block diagram:

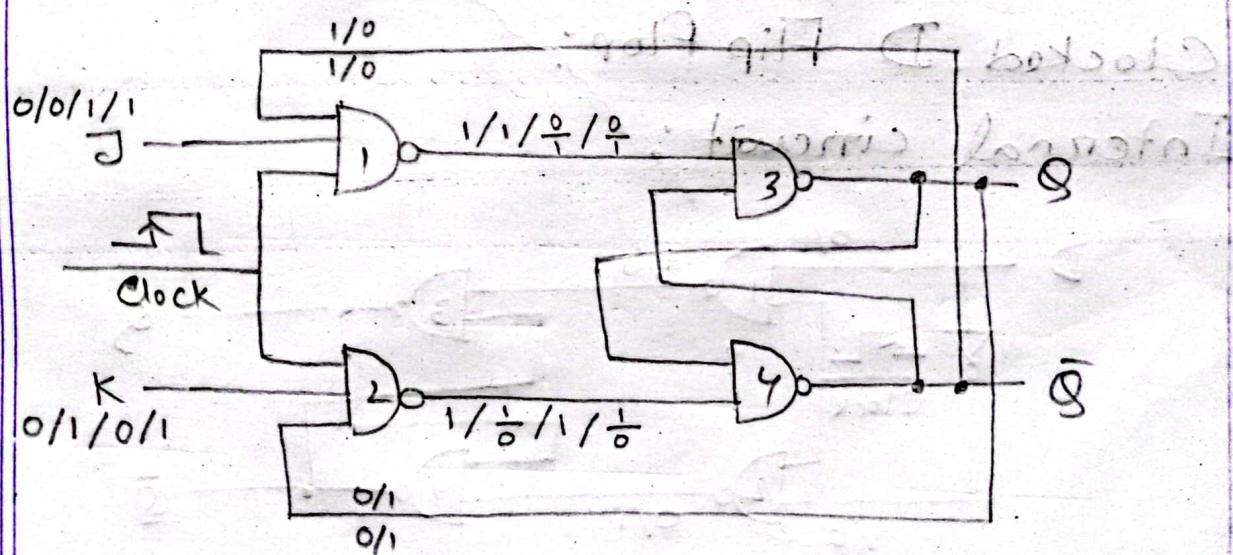


Waveform diagram of clocked SRFF:



Clocked JK flip flop:

Internal Circuit:



Operations & Truth Table:

J	K	CK	Q
0	0	↑	No change
0	1	↑	0
1	0	↑	1
1	1	↑	Toggle

J ↙ K ↘

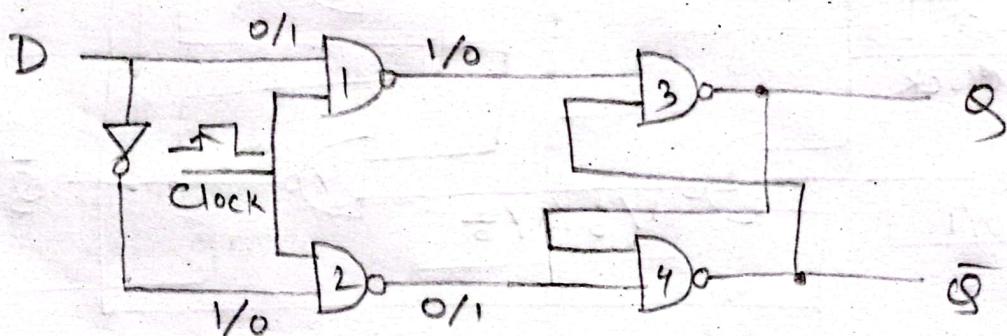
(0, 0) \Rightarrow If initially $Q=0$, Then finally $Q=0$
 If initially $Q=1$, Then finally $Q=0$

(1, 0) \Rightarrow If initially $Q=0$, Then finally $Q=1$
 If initially $Q=1$, Then finally $Q=1$

(1, 1) \Rightarrow If initially $Q=0$, Then finally $Q=1$
 If initially $Q=1$, Then finally $Q=0$

Clocked D Flip Flop:

Internal circuit:



Operation & Truth Table:

D	CK		Q
0	↑		0
1	↑		1

Block diagram:

