BRAC University | CSE-460: VLSI Design | Spring 25 | Faculty: YAP

Assignment - 01 | Total Marks - **80**

Due - 11.59 PM, March 05, 2025 | Submission link:

ID:	Sec:	Name:

Instructions:

- **Print the question paper** and start writing your answers as instructed.
- **Do not print the questions on both sides of the pages**. You can **use the opposite side of the page** for writing your answers.
- You can add additional pages if required, but you **must write your ID, Section and Name at the top of each additional page.**
- Please note, **Collaboration =/= copying.** You are allowed to discuss the questions and clear confusions you might have, but you have to write your solutions independently and distinctively.
- **Scan** your answers, make a single PDF file by renaming "A2_StudentID_Fullname_CSE460.pdf" and **upload** it in the submission link.
- **Any findings of plagiarism will** result in a **Zero** mark. It may also hamper your future grading!
- **You must submit the online copy by the deadline.**

Q1. [CO2] - Marks 10 (5+5)

a) **Complete** the truth table shown in Figure 2, for the circuit shown in Figure 1.

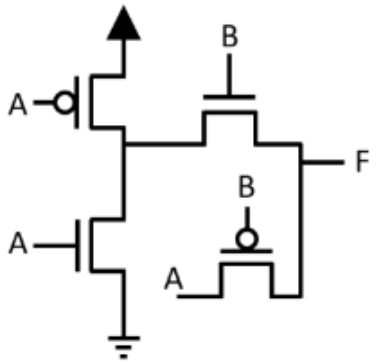

Figure 1: A logic circuit

A	B	F
0	0	
0	1	
1	0	
1	1	

Figure 2: Truth table

b) A D flip-flop is made by cascading two D latches as shown in Fig. 1. **Draw the waveforms** for $\mathbf{Q_m}$ **and** $\mathbf{Q_{out}}$. (Use a pencil to draw the signals and draw on the question paper, no need to draw the diagram in your answer script separately)

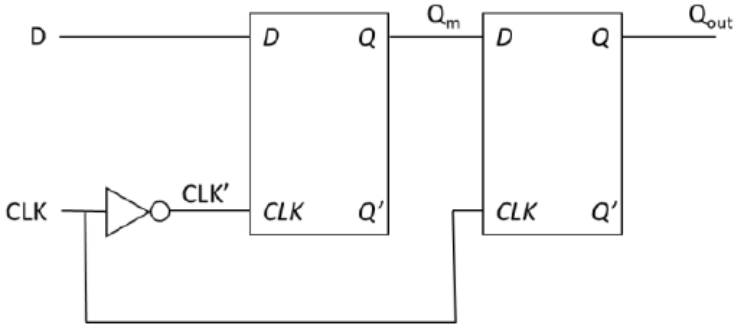

Fig. 1

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Q2. [CO2] - Marks 10 (5+5)

a) **Design a 4 to 1** multiplexer that will pass either input A, B, C, or D to the output F depending on the logic state of the control pin S. Implement your design using basic logic gates (AND, OR, INVERT). Also, implement it using CMOS to determine the total number of nMOS and pMOS transistors required to implement the multiplexer.

b) **Design** the same multiplexer described in (a) using **transmission gates** only and calculate the total number of nMOS and pMOS transistors required to implement your design. Is this design restoring or non-restoring? Why?

Q3. [CO2] - Marks 10 (2+4+4)

The timing diagram of an edge triggered sequential circuit element is shown in **Figure 1**

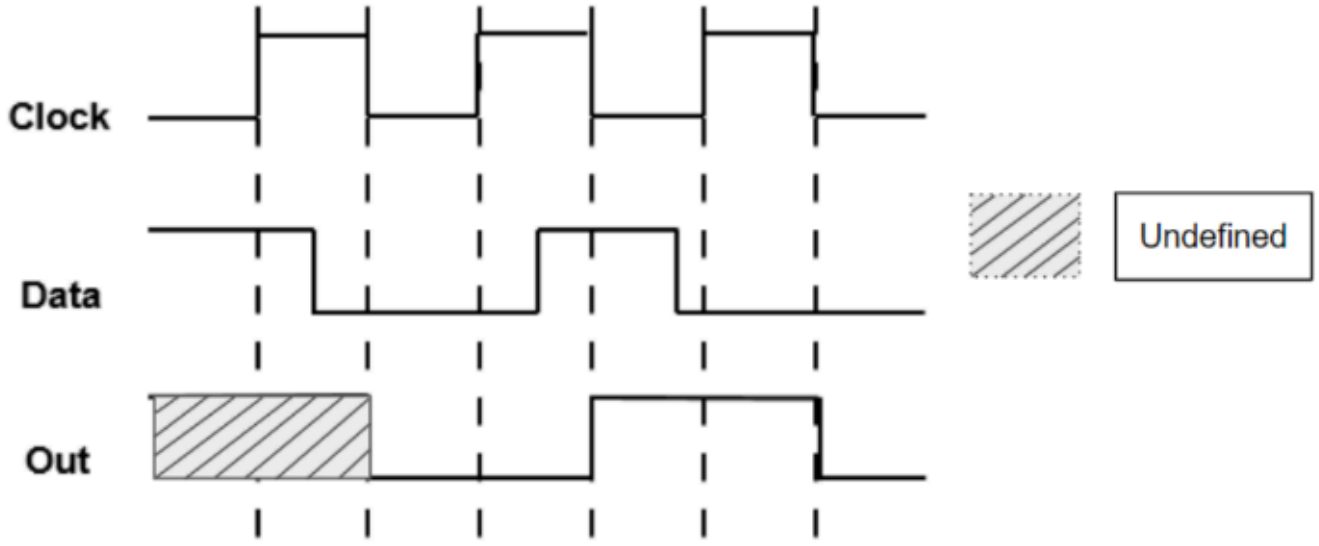

Figure 1

a) **Identify** the type of the edge triggered circuit element shown in **Figure 1**.

b) **Justify** if it is possible to build the circuit element as shown in **Figure 1** using **level triggered** sequential circuit elements only. **Draw** the appropriate **block diagrams**.

c) **Draw** the appropriate circuit diagrams corresponding to the block diagrams of (b) using **transmission gates**.

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Q4. [CO1] - Marks 10 (2+2+3+3)

a) **Draw** the circuit diagram of "X" using **transmission gates**. **[2]**

"X" is a circuit element that produces output **Qx** from input **Dx** with a clock signal, **CLKx**, as shown in Figure 2 :

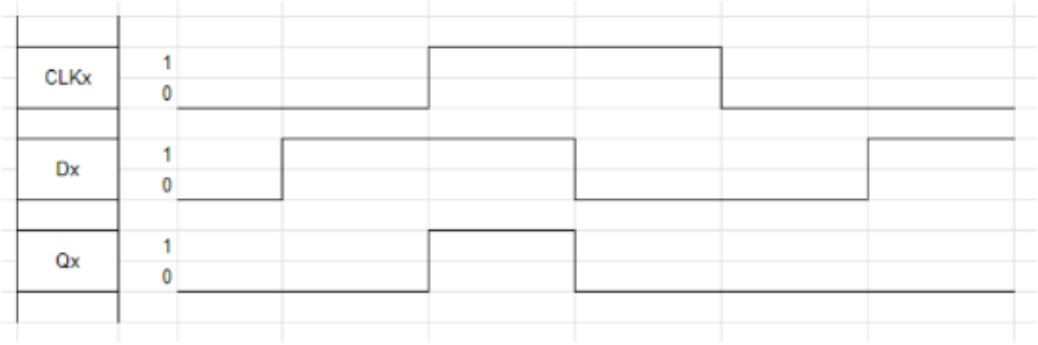

Figure 2: Timing Diagram for circuit element "X"

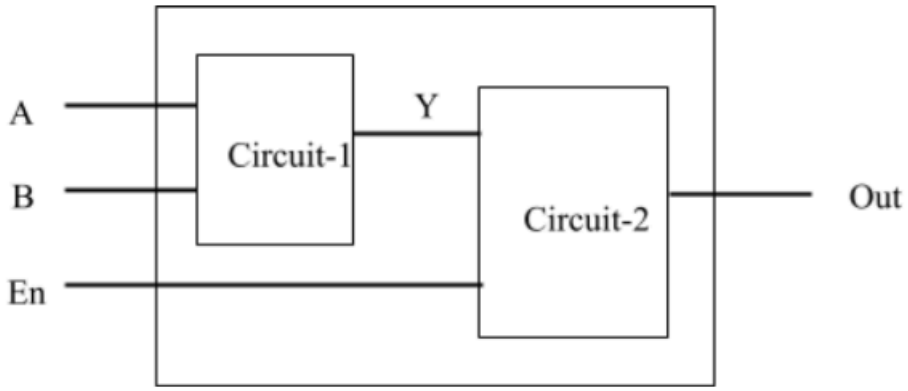

Figure 3: Tri-state circuit

The truth tables for both Circuit-1 and Circuit-2 are given below:

Truth table for Circuit-1

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Truth table for Circuit-2

En	Out
0	z
1	$\overline{Y}$

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b) Consider the Tri-state circuit shown in Figure 3 with **inputs: A, B, En** and **output: Out**. The Tri-state circuit further consists of two sub-circuits: Circuit-1 and Circuit-2.
   i) **Determine** the boolean expression of Y **[2]**
   ii) **Draw** the CMOS circuit diagram for Circuit-1 **[3]**
   iii) **Draw** the circuit diagram for Circuit-2 **[3]**

Q5. [CO1] - Marks 15 (3+5+7)

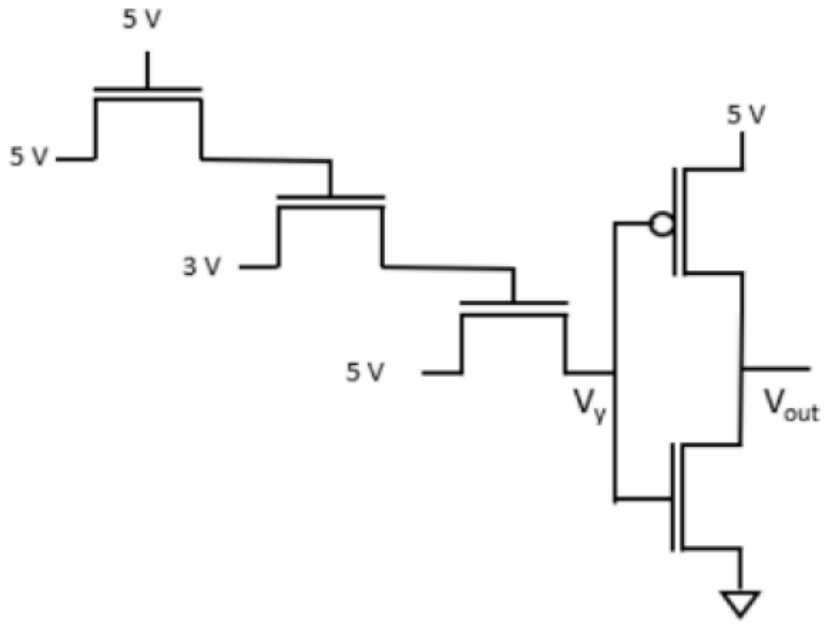

Figure 4: Circuit Diagram for Q.3

(a) Find the value of the voltage marked at Vy and Vout.

(b) Implement the following expressions using a single MUX:
   1. A'B + C'
   2. A' + BC

Hints: Try to write down the truth table of the logic expression

(c) Implement a 9:1 MUX using a minimum number of 4:1 MUX.

Q6. [CO2] - Marks 10 (4+6)

a) **Complete** Figure 04 by drawing the **waveform of Q_M and Q [4]**
b) **Draw** and **implement** the circuit in Figure 03 using **transmission gate [6]**

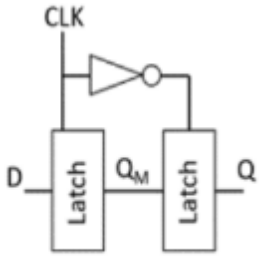

Figure 3

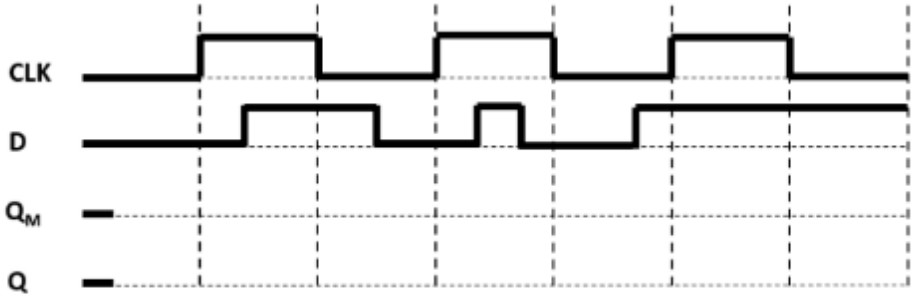

Figure 4

Q7. [CO1]: 15 Marks

We have to implement an exam cheat detector. We have 4 sensors (A, B, C). Their functions are as follows:

A: High when a person has AirPods hidden in his/her ears.
B: High when a person has something written on his/her arms.
C: High when a person has a cheatsheet in his/her pocket

The output of the system will be high if the student should be expelled. The system is lenient enough to not expel if a student commits only offense **A** or only offense **B**. In any other case, the student will be expelled.

(a) **Write** down the truth table for the system, describing all possible states of the sensors (A, B, C) and their corresponding output states. **2**

(b) **Draw** the Karnaugh map (K-map) for the system based on the truth table in part (a). Derive the logical expression that governs the system from the K-map. **4**

(c) **Draw** the CMOS logic circuit for the logical expression derived in part (b). Specify the number of MOSFETs required to implement your design. **3**

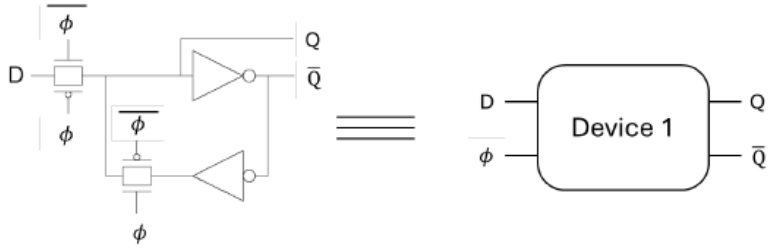

Figure 1: Circuit on the left is represented by the block - **Device 1**

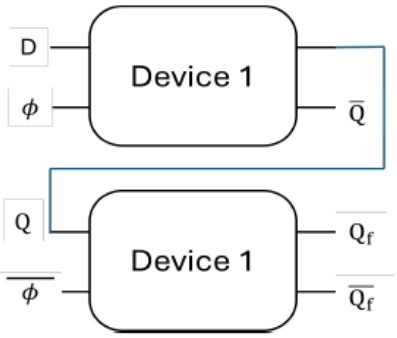

Figure 2: A circuit made up of two **Device 1** blocks **from Fig. 1**

(d) **Analyze** the circuit in **Fig. 1** and write the truth table of the block **Device 1**. **Represent Q as a logic function of D when $\phi = 0$.** **3**

(e) The table represents the time-dependent logical values (0 or 1) for each node in the circuit depicted in **Fig. 2**, which is constructed using two Device 1 blocks. The Φ and D values are provided in the table. **3**

Node ↓ / Time →	5 ns	10 ns	15 ns	20 ns	25 ns
ϕ	0	1	0	1	0
D	0	1	1	1	0
Q					
Q_f	1				

Determine the values of **Q** and Q_f for the specified time intervals (5 ns, 10 ns, etc.). **Determine** if the circuit in **Fig. 2** functions as a **negative**-edge/level-triggered or **positive**-edge/level-triggered flip-flop/latch?