PESD5V0S1BA

Transient Voltage Suppression Diode

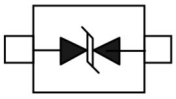
Features

100Watts peak pulse power (tp = 8/20μs)
Bidirectional configurations
Solid-state silicon-avalanche technology
Low clamping voltage
Low leakage current
IEC 61000-4-2 ±30kV contact ±30kV air
IEC 61000-4-4 (EFT) 40A (5/50ns)
IEC 61000-4-5 (Lightning) 9A (8/20μs)

Applications

Microprocessor based equipment
Personal Digital Assistants (PDA's)
Notebooks, Desktops, and Servers
Portable Instrumentation
Pagers Peripherals

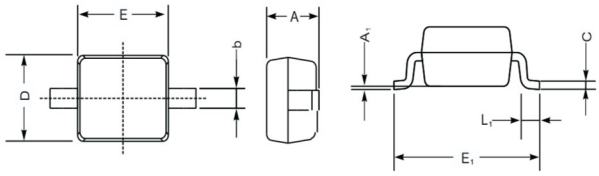
Schematic & PIN Configuration



Mechanical Data

SOD-323 package
Molding compound flammability rating: UL 94V-0
Packaging: Tape and Reel
RoHS/WEEE Compliant

SOD323



UNIT		A	C	D	E	E_1	b	L_1	A_1
mm	max	1.1	0.15	1.4	1.8	2.75	0.4	0.45	0.2
	min	0.8	0.08	1.2	1.4	2.55	0.25	0.2	—
mil	max	43	5.9	55	70	108	16	16	8
	min	32	3.1	47	63	100	9.8	7.9	—

Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (t_p =8/20μs)	P_{PP}	100	Watts
Peak Pulse Current (t_p =8/20μs) (note1)	I_{pp}	9	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	30 30	kV
Lead Soldering Temperature	T_L	260(10seconds)	℃
Junction Temperature	T_J	-55 to + 125	℃
Storage Temperature	T_{stg}	-55 to + 150	℃

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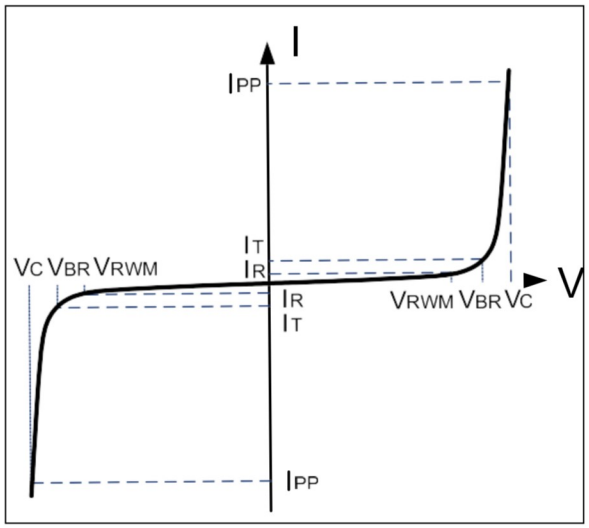
Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{RWM}				5.0	V
Reverse Breakdown Voltage	V_{BR}	I_T=1mA	5.6			V
Reverse Leakage Current	I_R	V_{RWM}=5.0V,T=25℃			1	uA
Clamping Voltage	V_C	I_{PP}=9A,t_p=8/20μs		10		V
Junction Capacitance	C_j	V_R = 0V, f = 1MHz		20		pF

Electrical Parameters (TA = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current



Note:. 8/20μs pulse waveform.

RATING AND CHARACTERISTIC CURVES (PESD5V0S1BA)

Figure 1: Peak Pulse Power vs. Pulse Time

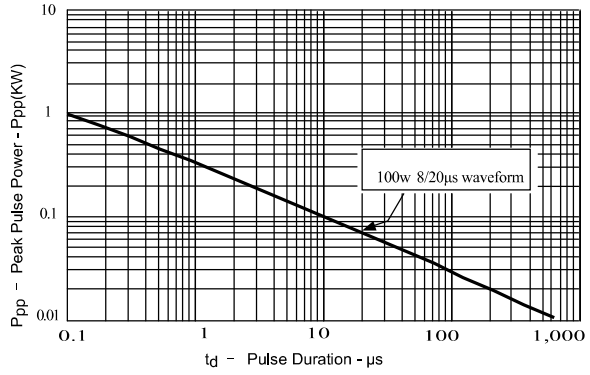


Figure 2: Power Derating Curve

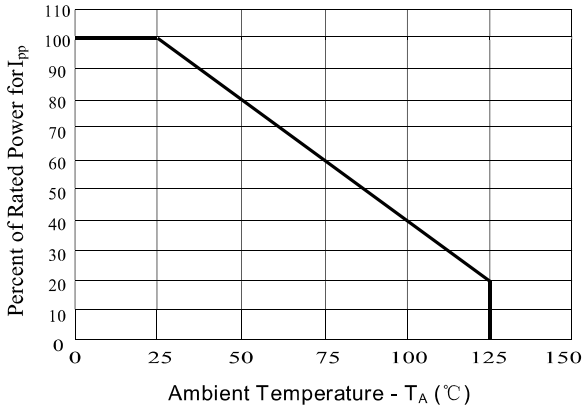


Figure3: Pulse Waveform

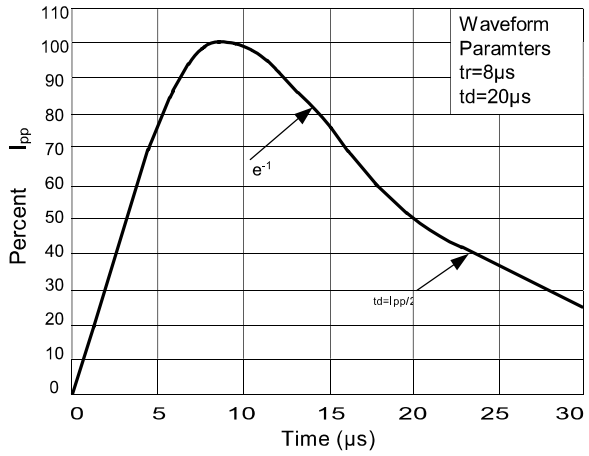


Figure 4: Clamping Voltage vs.Ipp