COMP22111

Two hours

UNIVERSITY OF MANCHESTER
SCHOOL OF COMPUTER SCIENCE

VLSI System Design

Date: Tuesday 17th January 2012

Time: 09:45 - 11:45

Please answer any THREE questions from the FOUR questions provided

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This is a CLOSED book examination

The use of electronic calculators is permitted provided they are not programmable and do not store text.

[PTO]

1.

a) The STUMP processor has a limited instruction set of only 8 instructions. Why is this? Explain how instructions such as MOV and NOP, which are not supported by the STUMP instruction set, may be implemented, giving examples of equivalent STUMP instructions for implementing MOV and NOP.

(3 marks)

b) Figure 1 illustrates a code fragment for the STUMP processor, along with the status of the registers at the current value of the program counter (PC) (in binary, hexidecimal and decimal). Identify the new value of any registers that have changed (in decimal) when the instructions at each of the following addresses in memory have been executed in full assuming a non-pipelined STUMP processor.

i. 8
ii. 9
iii. 11
iv. 12
v. 13

(5 marks)

c) The RTL datapath design for the STUMP processor is already suited for use in a pipelined design. What modification to the non-pipelined STUMP datapath is required for the pipelined design and why is it necessary?

(2 marks)

d) Discuss three types of hazards in pipeline designs using diagrams where appropriate. State a potential solution to each hazard.

(7 marks)

e) For the code listing given in Figure 1 identify the instructions that will be affected by the hazards discussed in part d).

(3 marks)

[PTO]

```
initial state for current value for PC:
CC:         0000                  0x0000     0
r0:         0000000000000000      0x0000     0
r1:         0000000000000011      0x0003     3
r2:         1111111111100010      0xFFE2     -30
r3:         0000000000011110      0x001E     30
r4:         0000000001100100      0x0064     100
r5:         0000000001111100      0x007C     124
r6:         0000000000000000      0x0000     0
r7:         0000000000000100      0x0004     4

code:

memory:           content:

3           loop: add r3, r3, #30
4                 add r5, r0, #15
5                 add r5, r5, #1
6                 sub r5, r4, r1
7                 and r6, r3, #0
8                 ld r4, [r0, #15]
9                 adds r2, r3, r2
10                beq jump
11                add r2, r2, #100
12          jump: sub r0, r6, r4
13                subs r4, r4, #25

15                #24
16                #10
```

Figure 1

[PTO]

2.

a) Apart from the control block, four other functional blocks can be identified in the architecture of the STUMP processor. State what these are and explain the purpose of each block.

(4 marks)

b) Using the register transfer level (RTL) design for the STUMP processor shown in Figure 2 explain how the STUMP processor performs the operations for:

i. a Type 1 instruction
ii. a Type 2 instruction
iii. load and store instructions
iv. branch instructions

(10 marks)

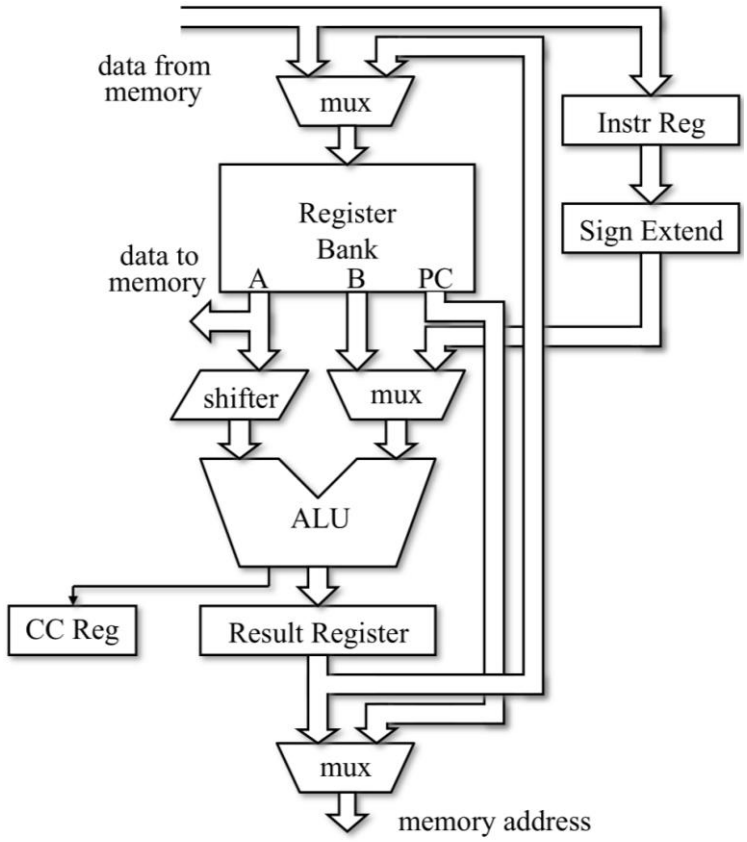

Figure 2

Register Transfer Level (RTL) design for the datapath in the STUMP processor.

(Question 2 continues on the following page)

(Question 2 continues from the previous page)

c) Control of the operation of the STUMP processor is determined using a state machine. Figure 3 illustrates the RTL Verilog code for the state machine in the STUMP processor. Explain the Verilog constructs in this code, in particular the use of the *always* block and the use of the assignment <=. In your explanation identify what these do in terms of the example code shown.

(6 marks)

```
reg[1:0] state;

always @(posedge clock)
begin
      if (Reset == 1) state <= 0;
      else if (state == 3) state <= 1;
      else state <= state+1;
end
```

Figure 3

[PTO]

3.

a) What does the 'C' in 'CMOS' stand for and why is this term appropriate in terms of the gate structure?

(2 marks)

b) Sketch a 2-input CMOS NOR gate showing the serial and parallel transistor stacks and the type of each transistor.

(8 marks)

c) Describe the operation of your NOR gate, in terms of which transistors are 'on' and 'off', when:

i. both inputs are ‘low’ (2 marks)
ii. the inputs are indifferent logic states (2 marks)

d) The carrier mobility in PMOS channels is about half that on NMOS channels, so their impedance is correspondingly higher. If your NOR gate is to deliver roughly equal output rise and fall times suggest - and justify - an appropriate transistor width for the PMOS transistors if the NMOS devices are 250 nm wide

(6 marks)

4.

Some form of 'testing' is used throughout the VLSI design and production process.

a) Explain what is meant by 'regression tests' and say when they are used.

(2 marks)

b) Why are tests needed on manufactured chips if the design is known to work?

(2 marks)

c) How might verification test patterns, used during the design phase, differ in test coverage from post-production tests

(6 marks)

d) Draw a sketch to illustrate what is meant by a 'scan path'. (6 marks)

e) How may a scan path simplify the chip testing process? (2 marks)

f) Suggest a use for a scan path other than for testing on a complex SoC.

(2 marks)

END OF EXAMINATION