COMP22111

Two hours

An additional answersheet is provided for Question 1.
Please remember to complete the additional answersheet
with your University ID number and attach it to your answerbook(s).

UNIVERSITY OF MANCHESTER
SCHOOL OF COMPUTER SCIENCE

Processor Microarchitecture

Date: Monday 13th January 2014

Time: 14:00 - 16:00

Please answer any THREE Questions from the FOUR Questions provided

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This is a CLOSED book examination

The use of electronic calculators is permitted provided they are not programmable and do not store text.

[PTO]

1. a) Figure 1 illustrates an RTL representation of a Stump datapath. Discuss the features that identify it as a load/store architecture. (2 marks)

   b) The Stump uses two common addressing modes: immediate and register. Briefly discuss these two addressing modes and identify how they are used in the Stump. (2 marks)

   c) Explain the operation of the Stump datapath (referring to the key components in the RTL representation of Figure 1) during the following:

      i) an instruction fetch
      ii) the execute phase of a Type 1 instruction
      iii) the execute phase of a Type 2 instruction
      iv) the memory phase of a load/store instruction (8 marks)

   d) For the RTL representation of the Stump datapath in Figure 1 produce signal usage charts using the additional answer sheet provided, depicting the status of the datapath control signals for

      i) the fetch phase of the instruction

      ADD R0, R2, #5

      ii) the execute phase of the instruction

      ORS R1, R2, R3, ROR

      iii) the execute phase of the instruction

      ST PC, [R5, #-3]

      iv) the memory phase of the load instruction

      LD R5, [R1, R2] (8 marks)

      You may assume the design of this Stump is the same as the design covered in the lectures and laboratory. A list of operations for this design of the Stump ALU is given in table 1. Table 2 lists the shift operations.

      Please write your University ID clearly on the additional answer sheet and attach it securely to your answer booklet.

(Question 1 continues on the following page)

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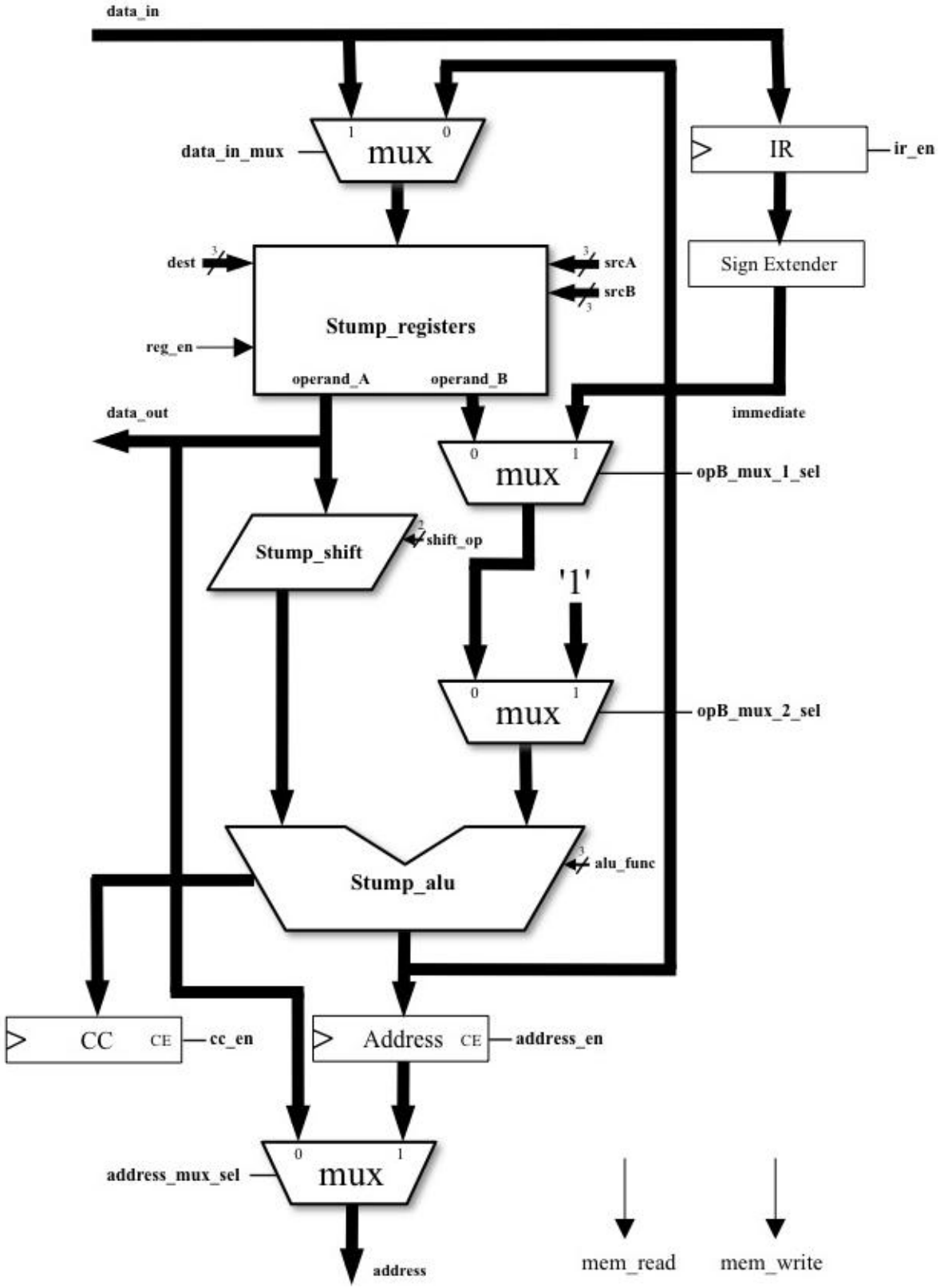

Figure 1

(Question 1 continues on the following page)

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ALU operation	alu_func
ADD	000
ADC	001
SUB	010
SBC	011
AND	100
OR	101

Table 1

Shift operation	shift_op
No Shift	00
ASR	01
ROR	10
RRC	11

Table 2

[PTO]

2. a) In Verilog we can use blocking and non-blocking assignments to assign values to variables. Discuss how these two methods of assigning values differ. (2 marks)

b) For the Verilog code given in Figure 2, when will the assignments be evaluated? Describe, with the aid of a suitable diagram, how the simulator will handle the events created by the Verilog code given in Figure 2. (7 marks)

```
assign signald = signala + signalc;

always @(negedge clock)
  signala <= 1;

always @(negedge clock)
  signalb <= 2;

always @(negedge clock)
  signalc  <= 3;
```

Figure 2

c) The Verilog module given in Figure 3 is used to represent a design in structural Verilog. Sketch an equivalent circuit diagram of this module, clearly labelling the internal wires declared in the Verilog description. What common device is being implemented in this code? (5 marks)

The modules `not` (inverter), `nand3` (3-input NAND gate), and `nand4` (4-input NAND gate) are provided for you with interfaces defined below.

```
module not(output    Y,
           input     X);

module nand3(output    Y,
             input     X1, X2, X3);

module nand4(output    Y,
             input     X1, X2, X3, X4);
```

d) The Stump processor has a simple Finite State Machine (FSM) to control its operation, as illustrated in Figure 4. Select appropriate state codes for each state and produce a Verilog module for the Stump FSM. The interface to the module should include the inputs `Clock`, `Reset` and `LDST` (which is high for a load/store instruction), and the output `State`. (6 marks)

(Question 2 continues on the following page)

(Question 2 continues from the previous page)

```
module circuit_design(input         D0, D1, D2, D3,
                      input   [1:0] sel,
                      output        Q);

wire   nsel0, nsel1, N0, N1, N2, N3;

not   not0(.Y(nsel0), .X(sel[0]));
not   not1(.X(sel[1]), .Y(nsel1));

nand3  nandg0(.X1(nsel0), .X2(nsel1), .X3(D0), .Y(N0));
nand3  nandg1(.X1(sel[0]), .X2(nsel1), .X3(D1), .Y(N1));
nand3  nandg2(.X1(nsel0), .X2(sel[1]), .X3(D2), .Y(N2));
nand3  nandg3(.X1(sel[0]), .X2(sel[1]), .X3(D3), .Y(N3),);

nand4  nandg4(.Y(Q), .X1(N0), .X2(N1), .X3(N2), .X4(N3));

endmodule
```

Figure 3

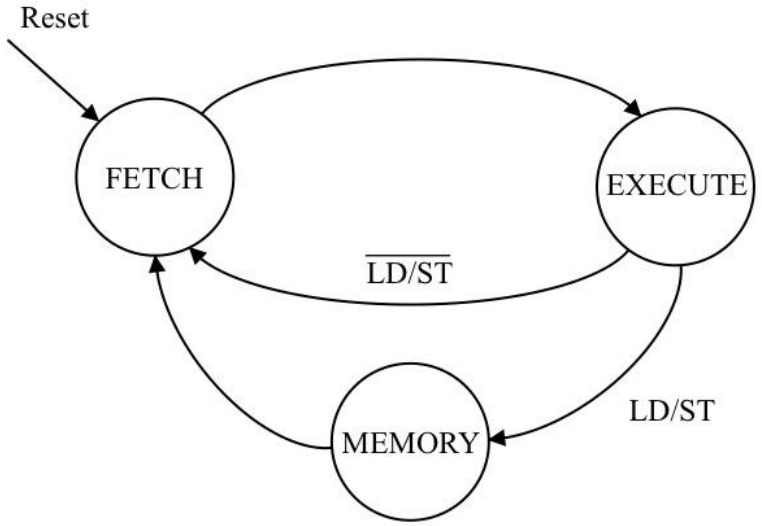

Figure 4

[PTO]

3. a) A contemporary leading edge VLSI process is labelled as "21 nm". Next year the same fab. plant promises a "14 nm" process. **Estimate** how many more transistors will be available on a chip of the same size. (3 marks)

   b) Describe the characteristics of a 'standard cell' on a VLSI device. (4 marks)

   c) During the VLSI design process, simulation will normally be done at the behavioural, pre-layout and post-layout stages. Briefly describe what is meant by each of these terms. (3 marks)

   d) What **timing** information can be obtained through each of the three types of simulation mentioned above? (6 marks)

   e) Outline two different challenges which currently threaten to limit Moore's Law, making it clear why these are contemporary problems. (4 marks)

4. a) What is meant by 'pipelining' a processor's execution path? (2 marks)

   b) State reasons why a processor implementation pipelined in three stages will not be three times faster than an unpipelined version:

      i) because of the implementation detail
      ii) because of the instruction mixture constituting a program. (6 marks)

   Both ARM and Stump processors allow a shift operation before an arithmetic or logical operation, within the same instruction. In a simple implementation this places the shifter and ALU *in series* on the datapath.

   c) What effect does this choice have on the critical path in an unpipelined implementation? (2 marks)

   d) Why is the 'problem' more severe with the ARM's barrel shifter than the Stump's single-place shift? (3 marks)

   e) Describe a microarchitectural solution to the shifter-ALU inefficiency in an ARM. Highlight any further problems that your solution may introduce and suggest solutions to these which facilitate a performance increase overall. (7 marks)

END OF EXAMINATION