DIGITAL LOGIC DESIGN CEP REPORT (CS-220)

Course Code: CS 220, Course Title: Digital Logic Design
Evaluation Rubric

Group Members:

Student No.	Name	Roll No.	Batch
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CRITERIA AND SCALES

Criterion 1: To what level has the student understood the problem? [CPA 1]

0 - 2	3 - 4	5
Problem understanding is minimal.	Problem is understood partially	Problem is completely understood

Criterion 2: To what extent the student implemented the solution? [CPA 1]

0	1-3	4-5
The solution has not been implemented	The solution is incomplete. The outputs are erroneous	The solution is complete. Desired outputs have been achieved

Criterion 3: What level of creativity is evident in the proposed design? [CPA 2]

0 - 1	2-3	4-5
No / Poor design	The design is run of the mill	The design is innovative

Criterion 4: What is the student's level of confidence with the Simulation Tool Interface? [CPA 3]

0	1-2	3-4	5
The student is unfamiliar with the tool	The student is familiar with the visible features of the tool	The student is familiar with the unexposed features of the tool	The student is proficient with the tool

Criterion 5: How well has the student interconnected the circuit components / hardware resources?

0	1-3	4-5
Student has no idea how to connect the circuit components / hardware resources	Circuit components / hardware resources are not connected properly	Circuit components / hardware resources are properly connected

Criterion 6: Answer to questions related to the design (Hardware part)

0	1-2	3-4	5
The student did not answer any question	Few questions were answered	The student answered most of the questions	The student answered all the questions

Criterion 7: Answer to questions related to the design (Simulation Part)

0	1-4	5-8	9-10
The student did not answer any question	The student answered a few questions	The student answered most of the questions	The student answered all the questions

Unlock Combination Pair Selected:

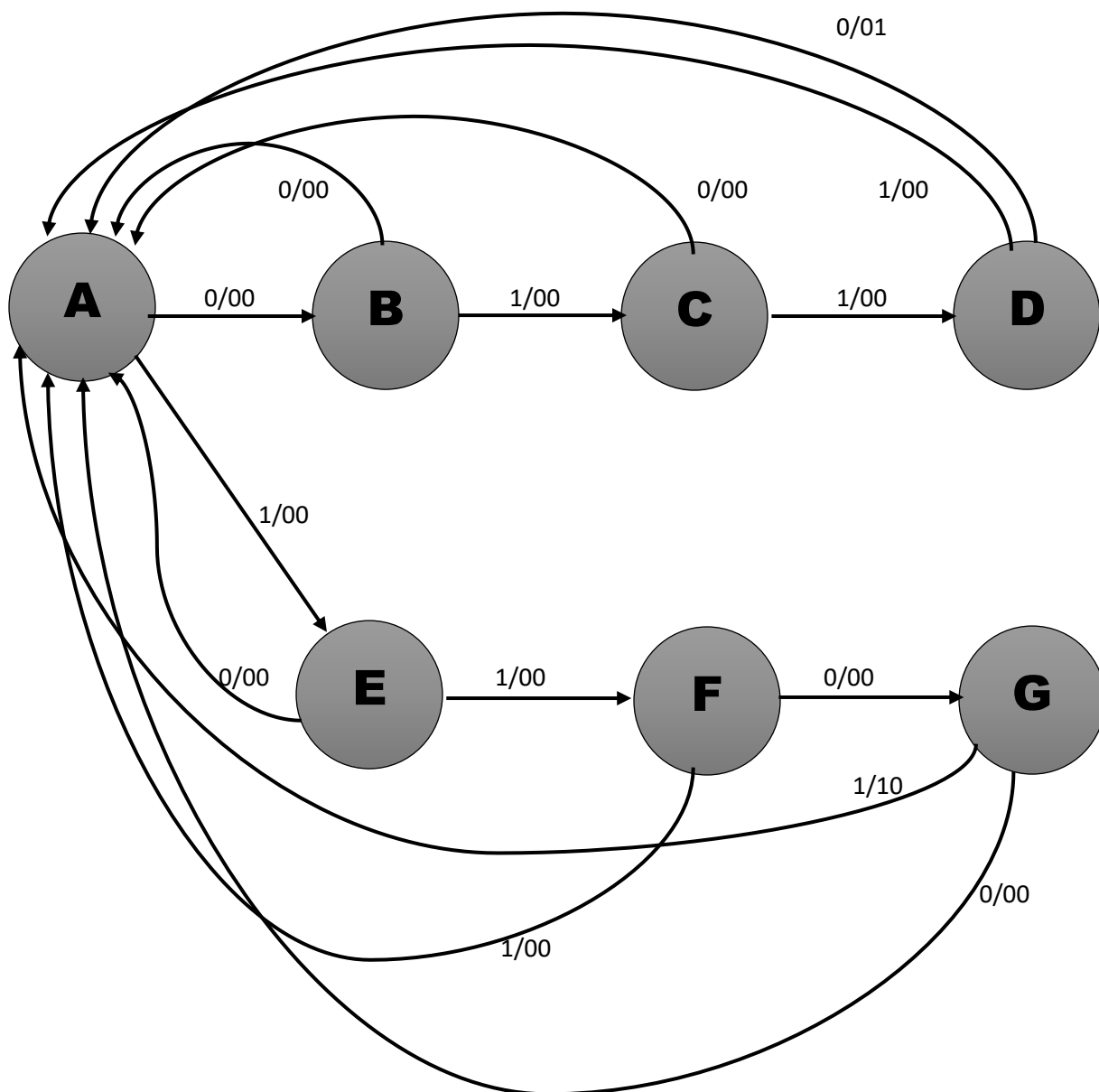As the 1st Roll No is 31 and the 2nd Roll No is 10, so 31+10=41. According to the Rule, as our least significant digit of 41 is 1, so the Unlock Combination Pairs are:

1. 1101

2. 0110

➲ In our project, we have used NO OVERLAPPING design.

State Diagram:

State Assignment:

No. of States = 7

No. of Flipflops needed = $\lceil Log_2 N \rceil$ = $\lceil Log_2 7 \rceil$ = 3

So, 3 D-FFs will be needed for the design.

A = 000

B = 001

C = 010

D = 011

E = 100

F = 101

G = 110

State Minimization:

	0	1
A	B,00	E,00
B	A,00	C,00
C	A,00	D,00
D	A,01	A,00
E	A,00	F,00
F	G,00	A,00
G	A,00	A,10

Pair Implication Chart:

	A	B	C	D	E	F
B	A B / C E ✖					
C	A B / D E ✖	C D ✖				
D	✖	✖	✖			
E	A B / E F ✖	C F ✖	D F ✖	✖		
F	B G / A E ✖	A G / A C ✖	A G / A D ✖	✖	A G / A F ✖	
G	✖	✖	✖	✖	✖	✖

➲ As no state is compatible to each other, so it is concluded that states will remain same.

State Table:

Present State			Input	Next State			Output		Flipflop Inputs		
Q2(t)	Q1(t)	Q0(t)	X	Q2(t+1)	Q1(t+1)	Q0(t+1)	Y1	Y0	D2	D1	D0
0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	1	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	0	0	0	1	0
0	1	0	0	0	0	0	0	0	0	0	0
0	1	0	1	0	1	1	0	0	0	1	1
0	1	1	0	0	0	0	0	1	0	0	0
0	1	1	1	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	1	0	1	0	0	1	0	1
1	0	1	0	1	1	0	0	0	1	1	0
1	0	1	1	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	1	0	0	0
1	1	1	0	X	X	X	X	X	X	X	X
1	1	1	1	X	X	X	X	X	X	X	X

Deriving Equations:

D2 Q0 X

Q2 Q1

	00	01	11	10
00		1		
01				
11			✗	✗
10		1		1

$$D2 = Q1\ 'Q0'\ X + Q2\ Q0\ X'$$

D1 Q0 X

Q2 Q1

	00	01	11	10
00			1	
01		1		
11			✗	✗
10				1

$$D1 = Q2\ Q0\ X' + Q2'\ Q1\ Q0'\ X + Q2'\ Q1'\ Q0\ X$$

D0 Q0 X

Q2 Q1

	00	01	11	10
00	(1)			
01		(1)		
11			✗	✗
10		(1)		

$$D0 = Q2' \ Q1' \ Q0' \ X' + Q2' \ Q1 \ Q0' \ X + Q2 \ Q1' \ Q0' \ X$$

Y0 Q0 X

Q2 Q1

	00	01	11	10
00				
01				1
11			✗	✗
10				

$$Y0 = Q1 \ Q0 \ X'$$

Y1   Q0 X

Q2 Q1   00   01   11   10

	00	01	11	10
00				
01				
11		1	✗	✗
10				

$$Y1 = Q2\,Q1\,X$$

Circuit Diagram: