A Wearable Auto-Patient Adaptive ECG Processor for Shockable Cardiac Arrhythmia

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Abstract— **A non-machine learning patient-specific shockable cardiac arrhythmia (SCA) classification processor based on single lead electrocardiogram (ECG) is presented. The proposed SCA detection processor integrates a hardware-efficient reduced-set-of-five (RSF5) feature extraction engine to extract SCA and non-SCA, self-adaptive patient-specific threshold engine for the peak and interval detection from the ECG, and simplified decision logic to discriminate the arrhythmia in real-time. The SCAD processor consumes 0.89µJ/classification while classifying with an average sensitivity, and specificity of 98.66%, and 99.75%, respectively.**

Keywords— cardiac arrhythmia, defibrillator, ecg processor, feature extraction, FPGA, wearable

I. Introduction

Wearable Electrocardiogram (ECG) devices are essential nowadays for personalized, preemptive, participatory, and precautionary medical practice adapted especially for the cardiovascular disorders [1]. Ventricular tachycardia (VT) and ventricular fibrillation (VF) are the leading cause of sudden cardiac deaths in the USA [2]. Timely detection of VT and VF is very crucial in delivering an electric shock therapy; continuous 24/7 monitoring with the on-sensor processing of ECG to detect shockable cardiac arrhythmias (SCA) and non-SCAs (NSCAs) along with defibrillators is very crucial [3]. [1], [4] presents single-lead on-sensor processor with high classification accuracy but targeting NSCA without defibrillation. [5], [6] presents wearable cardiac monitoring system but lacks patient adaptability whereas [3] implements a closed-loop arrhythmia diagnosis SoC but targeting implantable environment.

This paper presents a patient-adaptive ultra-low power single-channel "reduced feature set, non-machine learning" early ECG rhythm detection for SCAs targeting a wearable defibrillator with immediate response time (<20s). The system employs the reduced feature set of five (RFS5) feature extractor (FE) for both SCAs and NSCAs while utilizing non-machine learning patient adjustable threshold for proposed decision tree classifier (DTC) to achieve hardware-efficient implementation.

Fig. 1 shows the proposed SCA detection (SCAD) SoC with wearable defibrillator (WD); composed of single-lead ECG front-end, followed by an 11b SAR ADC, SCAD processor implemented on FPGA, and an external WD. For timely defibrillation, the SCAD performs auto-patient-adaptive detection to trigger WD for a short duration [biphasic shock energy: ~75J].

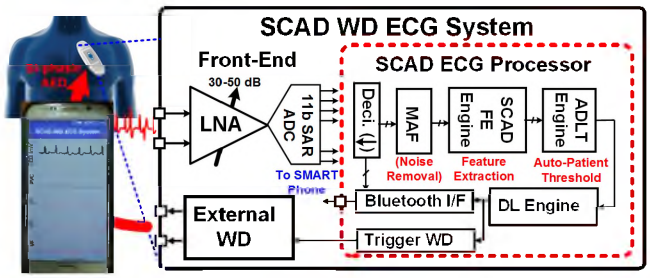


Fig. 1. Proposed wearable ECG SoC for Cardiac Arrhythmia Detection

II. Shockabale Cardiac Arrhthmia Processor

To integrate ECG processor on-sensor including all necessary SCA (VT, VF) and NSCA (Sinus rhythm, Premature Ventricular Contraction (PVC), Supra VT (SVT)), minimizing the hardware cost while maintaining the reliability is crucial [7][8]. The implemented SCAD ECG processor filters high frequency noise, baseline wandering and dc component while utilizing proposed moving average filter (MAF) which consumer 29% and 80% less area and power, respectively, compared to the conventional BPF. The feature extraction (FE) engine is based on proposed reduced set of five (RSF5) to extract the discriminatory features with minimal hardware requirement along with adaptive threshold value for R and T wave detection, to be used in the decision logic (DL) engine. Fig. 2 shows the implementation of SCAD FE engine; 2-sec filtered ECG data is stored in RAM which is further divided into respective P wave (PW), T wave (TW), Q wave (QW) and S wave (SW) window RAMs.

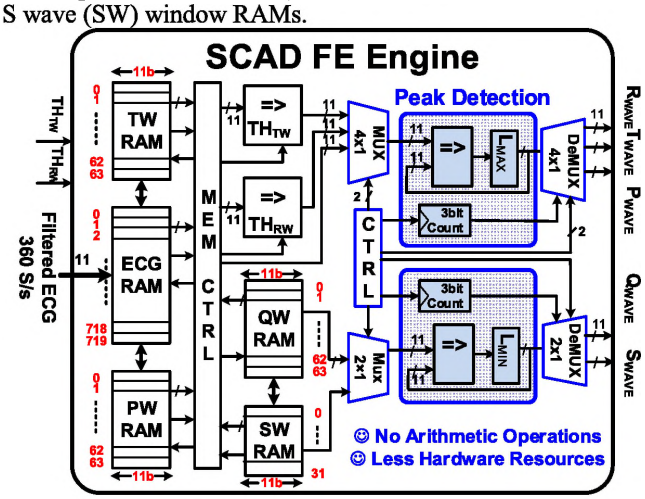


Fig. 2. Architecture of SCAD FE Engine

Peak detection is utilized to detect R-R interval based on R wave threshold which get updated automatically based on the slope change variation in the local maxima. To ensure the robustness and discard the abrupt glitch events, counter based cross check is utilized for 8-consecutive samples. Q and S wave detection will be done relative to the R-peak detection using same slope change principle. The proposed implementation achieves the comparable performance without utilization of any multiplier/divider and floating-point arithmetic blocks.

Fig. 3 shows the proposed adaptive decision logic threshold (ADTL) engine along with conventional implementation; proposed achieves an area reduction of >65% with a minimal overhead of increased processing speed and power. The RSF5 features detected by the FE update decision logic thresholds in ADTL. One feature out of RSF5 features are selected by the multiplexer (MUX) to save the value in on-chip RAM. First in first out (FIFO) based moving average of 4 values is utilized to compute/update the thresholds in a multiplexed way and decision logic thresholds are updated one by one in round-robin fashion.

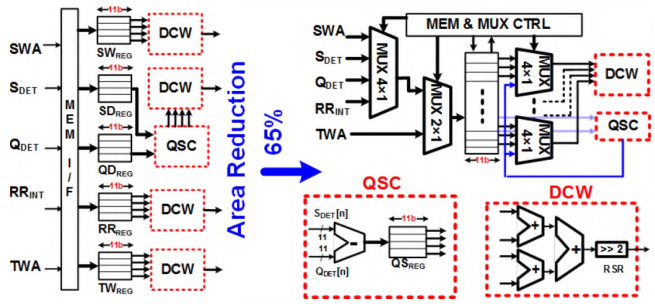


Fig. 3. Conventional vs. proposed automatic decision threshold logic.

III. MEASUREMENT RESUTLS

Fig. 4 is the FPGA measurement results with ECG-ID [9] and MIT-arrhythmia ECG database [10] that contains VF, VFL and PVC, VT cases respectively. Each ECG beat is classified using ADTL and corresponding flag is raised. Results shown are for a sinusoidal rhythm appears with amplitude equal to that of normal rhythm at a heart rate > 250 bpm, VFL rhythm is detected and VFL flag goes high. VFL rhythm may turn into VF when the amplitude of the rhythm is reduced significantly which results in shock delivery by the system and VF flag goes high.

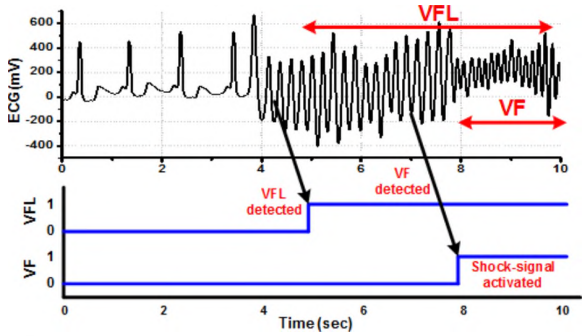
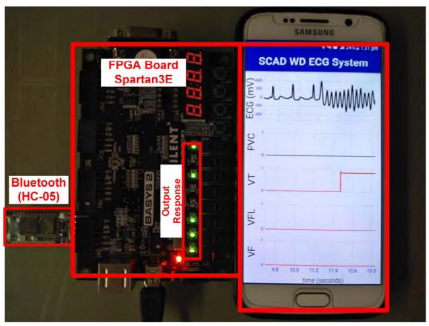


Fig. 4. Measurement results by storing the ECG data [10] on FPGA and classifying through SCAD ECG processor.

Fig. 5 shows the FPGA implementation and its performance summary based on P&R results from 180nm CMOS process. The proposed system achieves high sensitivity and specificity for both SCA and NSCA, with proposed RFS5 approach, while consuming 0.89µJ/Classification to continuously track SCA and NSCA. Table I shows the comparison of proposed with state-of-the-art works.



Implemented Results	
Process*	0.18µm 1P6M CMOS
Area*	0.375 x 0.375 mm
Supply Voltage	1.0V
No. of Feature	5
Classifier	Simple Threshold
Energy Efficiency*	0.89µJ/Class.
Sensitivity**	98.66%
Specificity**	99.75%

* PnR Results
** FPGA verification results

Fig. 5. FPGA implementation and performance summary.

Table 1. Comparison with state of the art works

	S. Abubakar DATE'18 [2]	D. Jeon ISSCC'14 [3]	X. Liu A-SSCC'13 [5]	S. Yin VLSI'17 [6]	This Work
Arrhythmia Detection	O	O	X	O	O
Defibrillation Shock	X	X	X	O	O
Technology	-	65 nm	180 nm	65 nm	180 nm
Supply Voltage	1.0 V	0.4 V	1.8 V	0.55V	1.0 V
Frequency	2 KHz	10 KHz	6 K Hz	2KHz	2 KHz
Classifier	ANN	Thresholds	N/A	ANN	ADLT
Power	5.94uW	45nW	0.435uW	1.06uW	115.8nW

REFERENCES

[1] W. Saadeh, *et al.*, "A 1.1mW Hybrid OFDM Ground Effect-Resilient Body Coupled Communication Transceiver for Head and Body Area Network," *in Proc. IEEE ASSCC*, Nov. 2016, pp. 201-204.

[2] S. Abubakar, *et al.*, "A wearable long-term single-lead ECG processor for early detection of cardiac arrhythmia," in *Proc. IEEE/ACM DATE*, pp. 961-966, Mar. 2018.

[3] D. Jeon, *et al.*, "An Implantable 64nW ECG-Monitoring Mixed-Signal SoC for Arrhythmia Diagnosis," in *IEEE ISSCC Dig. Tech. Papers, pp. 416-417, Feb. 2014.*

[4] S. Izumi, *et al.*, "A 14uA ECG Processor with Robust Heart Rate Monitor for a Wearable Healthcare System," in *Proc. IEEE ESSCIRC*, pp. 145-148, Sep. 2013.

[5] X. Lin, *et al.*, "A 457-nW Cognitive Multi-Functional ECG Processor," in *Proc. IEEE ASSCC*, pp. 141-144, Nov. 2013.

[6] S. Yin, *et al.*, "A 1.06 uW Smart ECG Processor in 65 nm CMOS for Real-Time Biometric Authentication and Personal Cardiac Monitoring," *IEEE Symp.VLSI Cir. Dig. Tech. Papers*, pp. 102-103, May. 2017.

[7] W. Saadeh, *et al.*, "A > 89% efficient LED driver with 0.5V supply voltage for applications requiring low average current," in *Proc. IEEE A-SSCC*, Nov. 2013, pp.273-276.

[8] W. Saadeh, *et al.*, "A High Accuracy and Low Latency Patient-Specific Wearable Fall Detection System," *in Proc. IEEE Biomedical and Health Informatics (BHI)*, 2017, pp. 441-444.

[9] Creighton University Ventricular Tachyarrhythmia database [Online], Available: https://physionet.org/physiobank/database/cudb/

[10] MIT-BIH arrhythmia database [Online], Available: https://www.physionet.org/physiobank/database/mitdb.