Chip Support Library

Release Notes

Applies to Product Release: 3.3.0.5
Publication Date: December 2, 2016

Contributors to this document

Texas Instruments, Incorporated
20450 Century Boulevard
Germantown, MD 20874 USA

Contents

Release Notes

Chip Support Library version 3.3.0.5

Overview

This release of CSL contains peripheral programming (functional and register level) APIs. The list of modules supported in this release is listed in later sections. This set of APIs provides peripheral abstraction that can be used by higher layers of software.

This release includes:

- Compiled library of supported CSL modules for AM571x and AM572x SOCs
- Source
- API reference guide

New and Updated Features

- This is the first release supporting AM571x and AM572x SOCs

The following is the naming convention for the various CSL prebuilt library files:

Default Directory	Library Name	Description
`ti\csl\lib\<soc>\c66`	`ti.csl.ae66`	66 ELF Little Endian Library
`ti\csl\lib\<soc>\c66`	`ti.csl.intc.ae66`	66 ELF Interrupt Controller Little Endian
`ti\csl\lib\<soc>\armv7`	`ti.csl.aa15fg`	A15 ELF Little Endian Library
`ti\csl\lib\<soc>\m4`	`ti.csl.aem4`	M4(IPU) ELF Little Endian Library

Resolved IRs

IR Parent/ Child Number	Severity Level	IR Description
PRSDK-839	Major	klocwork bug introduced due to version update from 10.2.1 to 11.1.0
PRSDK-781	Major	Klocwork report for IPs : UART, I2C, SPI, McASP and MMCSD
PRSDK-851	Major	Edma example code fails when tcc is above 32
PRSDK-954	Major	CSL: EDMA V1 API EDMA3RequestChannel enabling the wrong interrupt
PRSDK-1074	Major	Memory Barrier implementation in HW_ macros is ineffective when compiling with TI's ARM compiler
PRSDK-1078	Major	Remove unwanted waits in TI RTOS Driver IPs - I2C, UART
PRSDK-1086	Major	K2G I2C LLD Slave mode support
PRSDK-1316	Major	Wrong Regster Macros in K2G GPIO CSL-R
PRSDK-1447	Major	Update V1 version of csl_mdioAux.h with missing functions.
PRSDK-1545	Major	CSL: csl ARM GIC Aux implementation does not work with csl init library
PRSDK-1624	Major	CSL: Add Timer IP to AM3/AM4 CSL library

Release 3.3.0.5 Updates

- Resolved IRs for this release is listed under Resolved IRs section.

Release 3.3.0.4 Updates

- Resolved IRs for this release is listed as below.

IR Parent/ Child Number	Severity Level	IR Description
PRSDK-1052	Major	Renamed csl_a15init to csl_init
PRSDK-960	Major	Am572x a15 interrupt is triggered only the first time

IR Parent/ Child Number	Severity Level	IR Description
PRSDK-961	Major	armgic interrupt line 16,17,18,19 do not trigger after csl armgic initialization
PRSDK-966	Major	am57xx m4 interrupt line 48 triggers even after disabling it
PRSDK-948	Major	Enabling CSL-FL for McASP on K2G
PRSDK-1075	Major	CSL A15 interrupt code is wrongly using Intc line no as GIC id
PRSDK-1101	Major	CSL: API to get ARM GIC ID for a given IRQ Input Line
PRSDK-685	Major	PDK ICSS CSL organization/naming does not reflect ICSS IP revision changes
PRSDK-996	Major	TI RTOS: UART - Number of byte read incase of timeout
PRSDK-865	Major	CSL: Baremetal Cache & AMMU routines for Cortex-M4 as a part of CSL

-

Release 3.3.0.3 Updates

- CSL bare-metal examples for AM572x and AM571x
- CSL to support i2c, spi, gpio, uart version speficic layers.
- Resolved IRs for this release are listed as below:

IR Parent/ Child Number	Severity Level	IR Description
PRSDK-818	Major	software and the TRM definition of the QSPI word length in the QSPI_SPI_CMD_REG register doesn`t match
PRSDK-539	Major	CSL_a15ReadCoreId returns incorrect results

Release 3.3.0.2 Updates

- K2G merge to Common CSL to support
- Resolved IRs for this release are listed as below.

IR Parent/ Child Number	Severity Level	IR Description
SDOCM00119536	Major	Incorrect PCIE outbound register overlay in Keystone I/II devices CSL code
SDOCM00121249	Major	SEC_MGR register definitions (cslr_sec_mgr.h) in CSL package needs to be removed from the PDK package
SDOCM00120885	Major	Wrong definitions of CSL_CGEM_IDMA1_COUNT_COUNT_SHIFT and CSL_CGEM_IDMA1_COUNT_COUNT_MASK

Release 3.3.0.1 Updates:

- Common CSL to support AM571x, AM572x and KeyStone devices.
- Resolved IRs for this release are listed as below.

IR Parent/ Child Number	Severity Level	IR Description
SDOCM00117947	Major	CSL code accesses DRAEH register in EDMA CC0 and causes memory protection exception on Keystone 1
SDOCM00117869	Major	Keystone II A15 CSL library is not supported
SDOCM00102018	Minor	C6657 CSL CHIP_PIN_CONTROL_0 address is wrong
SDOCM00100228	Major	CSL cache APIs does not include workaround for advisory 6.
SDOCM00097896	Minor	Update CSL cache APIs to support write through functionality
SDOCM00094196	Minor	Problem to enable HW prefetch perf counters with CSL
SDOCM00119865	Major	Update CSL Serdes restore default API for PHY-A
SDOCM00118436	Major	tap offsets are not initialized before passing to CSL_Serdes_DLEV_Patch() in CSL_SerdesLaneEnable

Migration:

- Migration information for CSL from BIOS-MCSDK 2.1.2 release
  - SOC_C6657 needs to be defined for including CSL header files for C6657 PDK
  - SOC_C6678 needs to be defined for including CSL header files for C6678 PDK
  - Top level cslr_pcie*.h needs to be changed to include cslr_pcie.h

- cslr_sgmii.h, csl_sgmii.h renamed to cslr_cpsgmii.h and csl_cpsgmii.h respectively.
- following files are not supported from the top level CSL folder (ti/csl)
  - csl_mpuAux.h
  - csl_memprot.h
  - csl_memprotAux.h
  - csl_pllcAux.h
  - csl_cp_tracer.h
  - cslr_cpsw_3gf.h and cslr_cpsw_3gfss_s.h
  - csl_cpsw_3gf.h, csl_cpsw_3gfAux.h, csl_cpsw_3gfssAux.h, csl_cpsw_3gfss_s.h
- Top level csl_cpsw_3gfAux.h files are substituted with csl_cpswAux.h and csl_cpsw_3gfssAux.h files are substituted with csl_cpswAux.h
- Top level csl(r)_cpsw_3gf*.h files are substituted with csl(r)_cpsw.h and csl(r)_cpsw_ss_s.h files respectively and also all the definitions regarding 3gf are renamed as below.
  - Rename CSL_CPSW_3GF_XXXXXX to CSL_CPSW_XXXXXX

o Migration information for CSL from MCSDK 3.1.4 release

- Renamed “ti/csl/device” folder to “ti/csl/soc” – hence any include header files as “ti/csl/device/k2?/src/xxxx.h” needs to be changed to “ti/csl/soc/k2?/src/xxxx.h”
- Top level include files for “bcp” are moved under “ti/csl/src/ip/bcp/V0” folder, except for cslr_bcp.h
- Top level include files for “iqn2” are moved under “ti/csl/src/ip/bcp/V0” folder, except for cslr_iqn2.h
- Top level include files for “rac” are moved under “ti/csl/src/ip/rac/V0” folder, except for csl_rac.h
- Top level include files for “tac2” are moved under “ti/csl/src/ip/tac2/V0” folder, except for csl_tac2.h
- Top level include files for “aif2” are moved under “ti/csl/src/ip/aif2/V0” folder, except for csl_aif2.h and cslr_aif2.h
- Deprecated top level cslr_cpsw_5gf*.h files which was there for backwards compatibility and also all the definitions regarding 5gf are renamed as below.
  - Rename CSL_CPSW_5GF_XXXXXX to CSL_CPSW_XXXXXX
- Top level cslr_pcie*.h needs to be changed to include cslr_pcie.h

        - Removed support for wiz8b8sb header files.
    - Migration information for CSL from Processor SDK 2.0.0 release
        - None

Release 3.3.0.0 Updates:

- First Release to support AM571x and AM572x SOCs
- Resolved IRs for this release are listed as below.

IR Parent/ Child Number	Severity Level	IR Description
SDOCM00114000	Major	Updated csl serdes flow for all serdes K2 peripherals

Known Issues / Limitations

The release has undergone limited testing on simulator. Current Known issues at the time of release include:

IR Parent/ Child Number	Severity Level	IR Description

Licensing

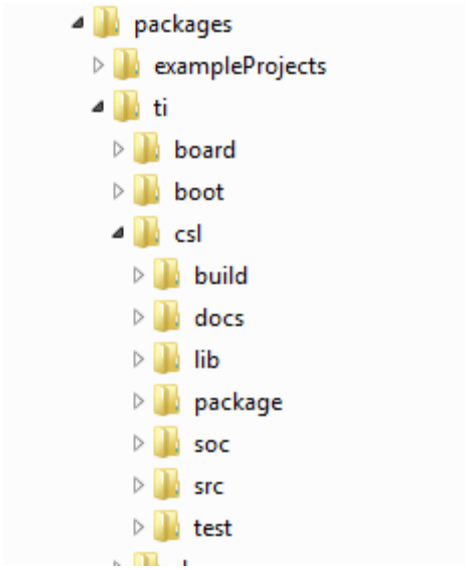
BSD Licensing

Delivery Package

Package is delivered as full source release in tar format.

Directory Structure

Following is the directory structure after CSL tar package is extracted.



Instruction for RTSC getLibs

In order to retrieve CSL library for a device using getLibs following line would be required in RTSC configuration file.

```
/* Load and use the CSL package */
var Csl = xdc.loadPackage('ti.csl.device.am572x.c66');
```

Replace k2k with the appropriate device name for the library being included

Customer Documentation List

Table 1 lists the documents that are accessible through the **/docs** folder on the product installation CD or in the delivery package.

Table 1 Product Documentation included with this Release

Document #	Document Title	File Name
1	API documentation (generated by Doxygen)	csl/docs/csldocs.chm