385L / 5585 - Laboratory 7 - Latches and Level Conditioners 17 APR 2017 (Due 01 MAY 2017)

Objectives:

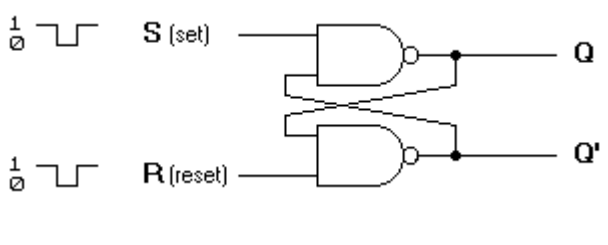
1. Determine the truth table for basic latches and flip-flops
2. Construct and understand a Schmitt trigger using UA-741 Op-Amp
3. Generate pulses using a timer circuit

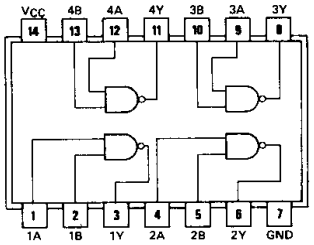
Equipment and Parts:

1. Oscilloscope with probes
2. UA 741 Op-amp
3. Function generator
4. Gates - **verify the basic logic of each gate works before constructing flip-flops/latches**
5. Resistors
6. Capacitors
7. 555-timer

7-1 Building a "Set-Reset" Latch with NAND gates

The **S**et-**R**eset latch is a bistable device, capable of providing one bit (binary digit) of memory. This "transparent" or "simple" device is constructed by crossing the outputs of two inverting (i.e. NAND) elements. Construct the latch below using the 7400 NAND gate. Determine the value of Q and Q`, for given inputs to S and R (use ground or 5 V for input). Go through the S and R inputs in the order given below to determine when Q, Q` are HI or LO (add a 300 Ω resistor to prevent overvoltage or use the voltage division principle to approximate the resistor required to prevent overvoltage if needed). Discuss why S=1, R=1 can give different Q, Q` (hint: history). How can this be used for memory?





S	R	Q	Q`
1	0		
1	1		
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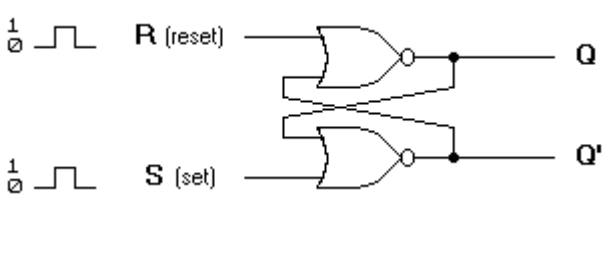
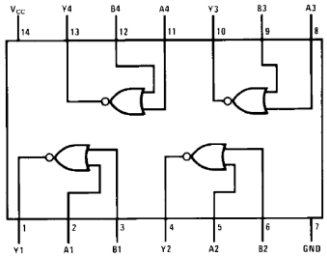
0	1		
1	1		

7-2 Building a "Set-Reset" Latch with NOR gates

Repeat the procedure for 7-1, but for the 7402 NOR gate and inputs below. Discuss the difference between the NOR and NAND latches from the information obtained in constructing the truth tables.





S	R	Q	Q`
1	0		
0	0		
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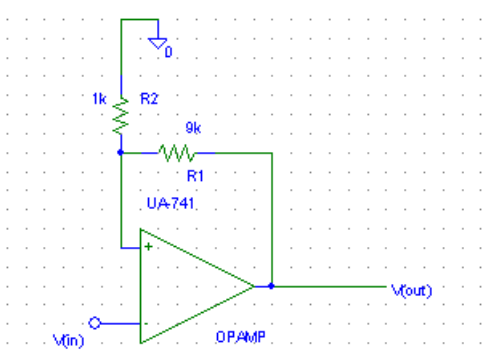
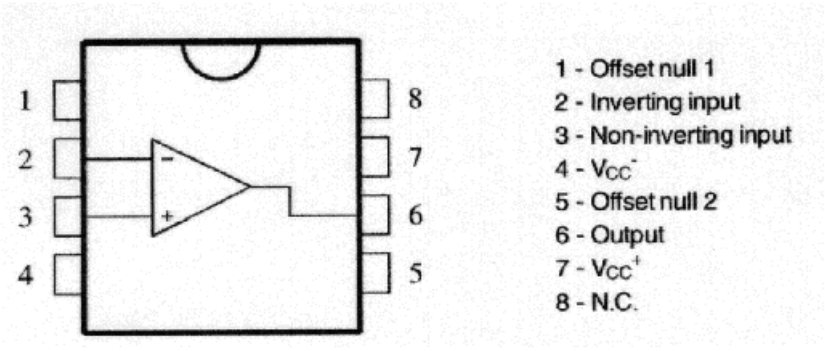
0	1		
0	0		

7-3 Level Conditioning

The Schmidt trigger may be built using the UA741 Op-amp (which is closely related to a comparator). The only difference in the Schmidt trigger is the presence of hysteresis in the switching level or threshold; that is, the level at which the output switches from low to high is different from the level at which the output switches from high to low. This characteristic is useful when working with noise signals where the threshold is not well defined (discretization level). The circuit will use a positive feedback to drive the op-amp UA741 to saturation (amplifies to V_{cc} but inverted). Start by setting $V_{cc}^{+/-}$ = +/-15V (pin diagram below). Now, suppose the output of the op-amp is 15V at this moment. What must the voltage at the non-inverting input be if R_2=1kΩ and R_1= 9 kΩ. Then, what must be the voltage at the inverting input to invert the output to -15V? Verify your predictions by inputting a 6V sine wave at 400 Hz and sketch the input and output on the same graph. What is the threshold input voltage that causes the output voltage to invert? Also, does this threshold voltage for inversion change with frequency?....and, if so, why?





7-4 555 Timer Circuit

The 555 Timer consists of a pair of comparators, a S-R flip-flop (latch from 7-2), and a transistor switch. If a HI voltage pulse is applied to the S input, the Q output is set to the HI state. Another HI pulse to the S input will not cause the voltage to toggle back to the LO state; rather a HI pulse to R input resets the output to a LO state. The second flip-flop Q` does the opposite of Q.

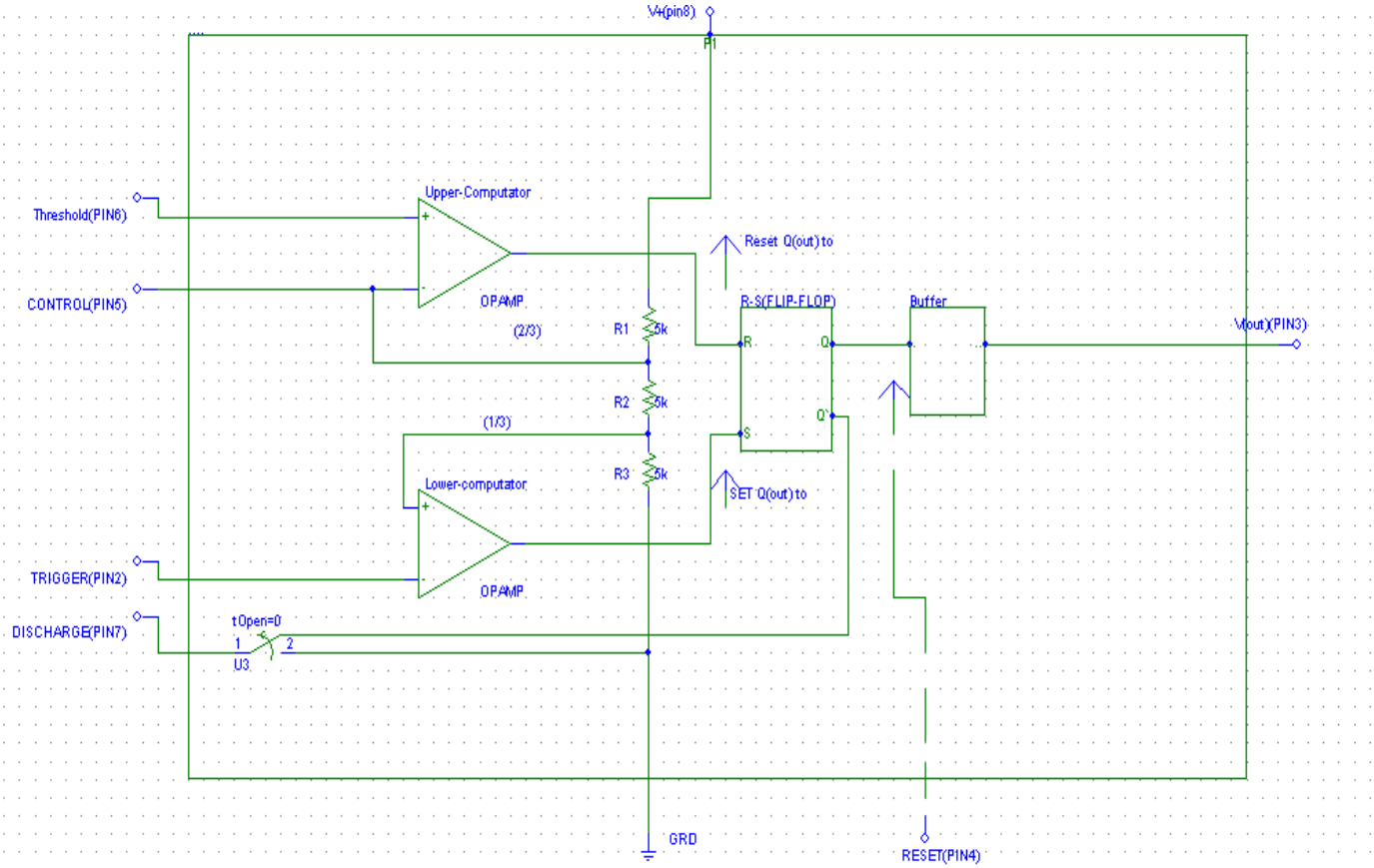
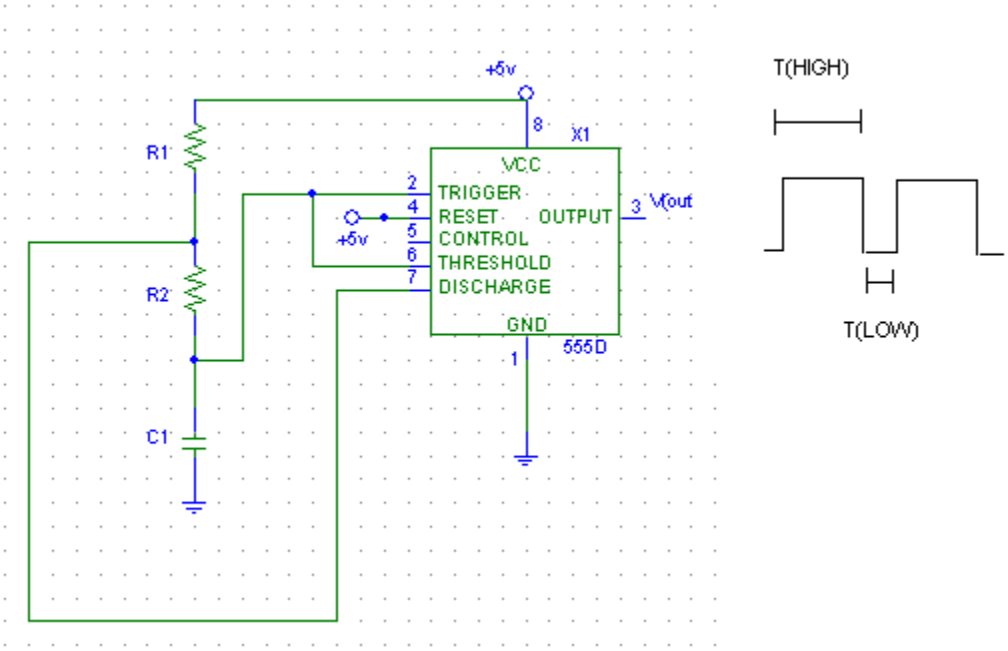


Figure A. Block diagram of interior of 555 Timer IC. Now the task in the experiment is to design an output clock signal (a pulse that occurs in a time sequence). The schematic diagram of what you are to wire up is given below.



The upper and lower comparators are connected to the top of capacitor "C" (see Fig. A). The discharge switch connects the junction between resistors R_1 and R_2 which are in series with capacitor "C". If switch S is opened (see Fig. A) the capacitor charges through R_1 and R_2 towards V+ (pin 8). But if the switch S is closed, the capacitor discharges through R_2 towards ground. If S is closed then any charge on C will leak off through R_2 to ground with time constant R_2*C. However when the voltage across capacitor "C" gets down to 1/3 of V+ (5V), the lower comparator sets the flip-flop; this causes the output to go HI and also opens the discharge switch "S". Now capacitor "C" charges through R_1 and R_2 towards V+ with time constant (R_1+R_2)*C. However when the voltage on C reaches 2/3 of V+, the upper comparator resets the flip-flop to low. Simultaneously the output goes low and the discharge switch closes so that C begins discharging again, and the cycle repeats. Since capacitor C charges through R_1+R_2 but discharges through R_2, the time constant for the output to be HI is different (see pulse diagram above). *This is now the basis for the clocking action!* First, build a simple circuit to blink an LED; you will then, translate this to the oscilloscope (only for the output) to experimentally determine the period (try for 0.5 sec as the period, with 0.3 sec HI and 0.2 sec LO).

The output to be high T_H (time to be HI) is given by T_H=0.7(R_1+R_2) C

While the time to low T_L is given by T_L = 0.7R_2C

Analytically determine the equation for the period of a square wave.

HINT: The period of a square wave is the sum of T_H and T_L.

Note: Set capacitance in μF and resistance in $k\Omega$