ECE 220 Computer Systems & Programming

Lecture 1 – Course Overview & LC-3 Review August 29, 2017



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Course Wiki: https://wiki.illinois.edu/wiki/display/ece220/Home

ECE ILLINOIS

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Course Logistics

- 4 Lectures to choose from (Borisov, Patel, Chen, Mitra)
- Programming Studio on Fridays (10 makeup pts/week towards MPs)
- MPs: due every Thursday @ 10pm (100 pts each, late penalty 2pts/hour)
- Quizzes: 6 programming quizzes, lowest score dropped
- Exams: 2 midterms and a final Exam (paper format)

Textbook: Patt & Patel, Introduction to Computing Systems: from bits to

gates to C and beyond, 2nd Edition.

Academic Integrity

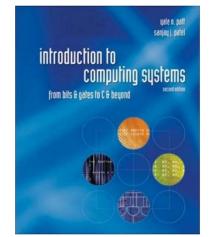
Grading Mechanics:

MPs: 20%

Quizzes: 15%

Midterms: 20% x 2

Final Exam: 25%

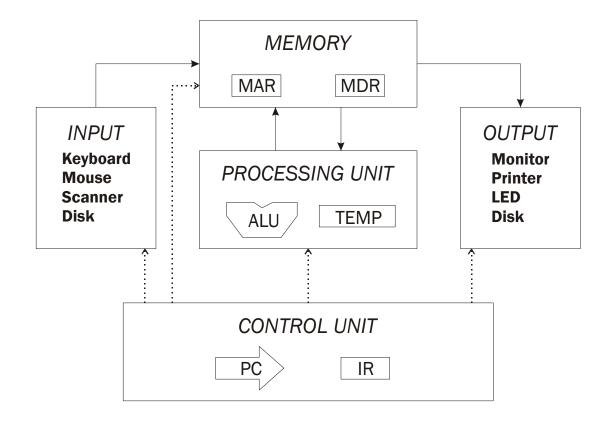


Tools & Resources

- Course Wiki course info, MP write-up, exam info, etc.
- SVN MP release, programming studio, etc.
- Piazza discussion board monitored by TAs
- Compass online grade book
- CBTF facility for taking programming quizzes, reserve your seat 2 weeks in advance at https://cbtf.engr.illinois.edu
- Emergency Response
- Resources: CARE, counseling center, DRES

LC-3 Review – The von Neumann Model

- 1. Memory
- 2. Processing Unit
- 3. Input
- 4. Output
- 5. Control Unit



LC-3 Review - Memory

Load and Store Using

- MAR: Memory Address Register (______ -bit)
- MDR: Memory Data Register (_______ -bit)

Load Data from Memory Address X

Step 1:

Step 2:

Step 3:

Store Data to Memory Address Y

Step 1:

Step 2:

Step 3:

LC-3 Review - Processing Unit, Input/Output, Control Unit

Processing Unit

- The Arithmetic and Logic Unit (ALU) only has _____, ____, ____, ____ operations
- Temporary Storage general-purpose registers:

Input – Keyboard (use 2 registers)

- 1.
- 2.

Output – Monitor (use 2 registers)

- 1.
- 2.

Control Unit

IR: instruction register –

PC: program counter –

LC-3 Review – ISA (Instruction Set Architecture)

Memory Organization

- Address space (# of distinct memory locations): _____
- Addressability (# of bits stored in each memory location): ______

Register Set

- 8 16-bit general-purpose registers: R0, R1, ...R7
- special-purpose register: ______, _______

LC-3 Review – ISA (Instruction Set Architecture)

Instruction Set

Data Types: 16-bit 2's complement integers

Addressing Modes (how the location of operand is specified):

Non-memory addresses – immediate (part of instruction), register

Memory address – PC-relative, base+offset, indirect

Opcodes (16-bit, bits 12-15 used to specify the opcode):

Operate instructions: ADD, AND, NOT

Data movement instructions: LD, LDI, LDR, LEA, ST, STR, STI

Control instructions: BR, JSR/JSRR, JMP, RET, TRAP, RTI

Condition codes: N (negative), Z (zero), P (positive)

Using LD, LDI, LDR, LEA

```
.ORIG x3000
LD R6, LABEL
LDI R6, LABEL
LDR R2, R6, #0
LEA R2, LABEL
LABEL .FILL x4000
.END
; Assume the following
; Address
            Content
; x4000
            x5000
; x5000
            x6000
```

LC-3 Exercise

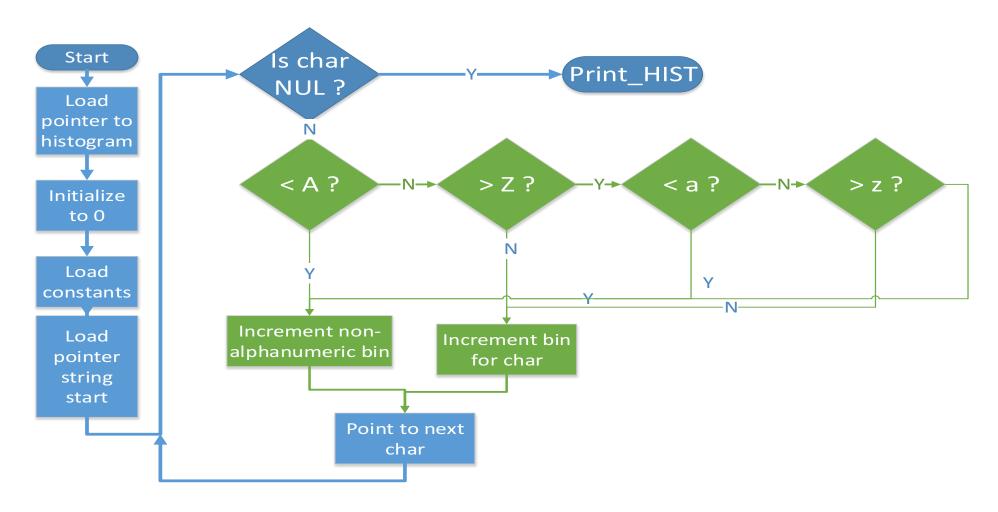
1. Initialize a register

2. Copy from one register to another

3. Compute 5 - 3

4. Compute 4 x 3

MP1 – Computing a Histogram



ASCII Table

11