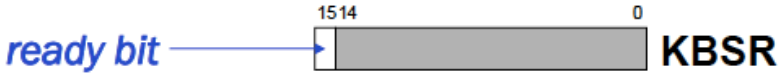
ECE 220 Computer Systems & Programming

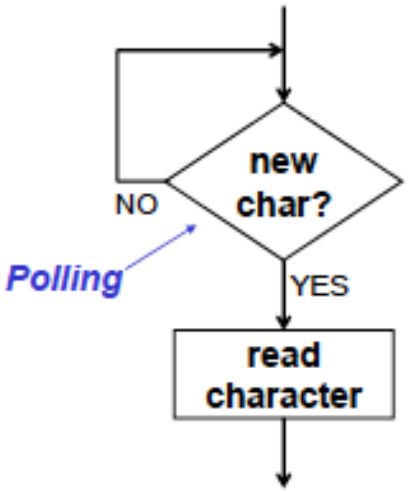
Lecture 6 – Interrupts & Exceptions

September 14, 2017

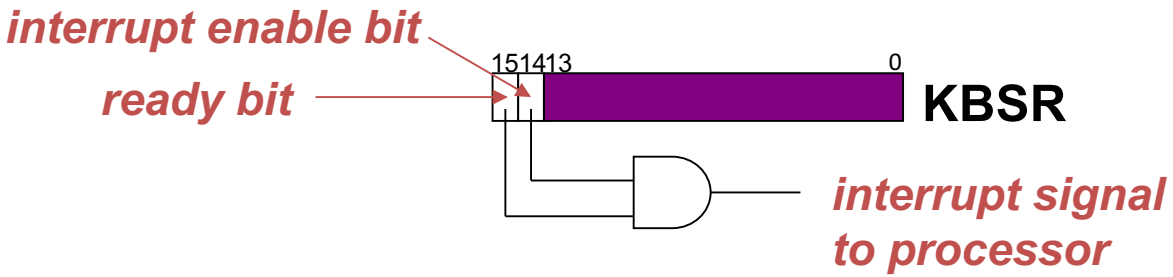
- Quiz 1 next week (practice questions posted)
- Midterm 1 conflict sign-up due 9/21 at 10pm

Polling v.s. Interrupt-Driven I/O






```
POLL   LDI  R0, KBSR
       BRzp POLL
       LDI  R0, KBDR
       ...
KBSR .FILL xFE00
KBDR .FILL xFE02
```

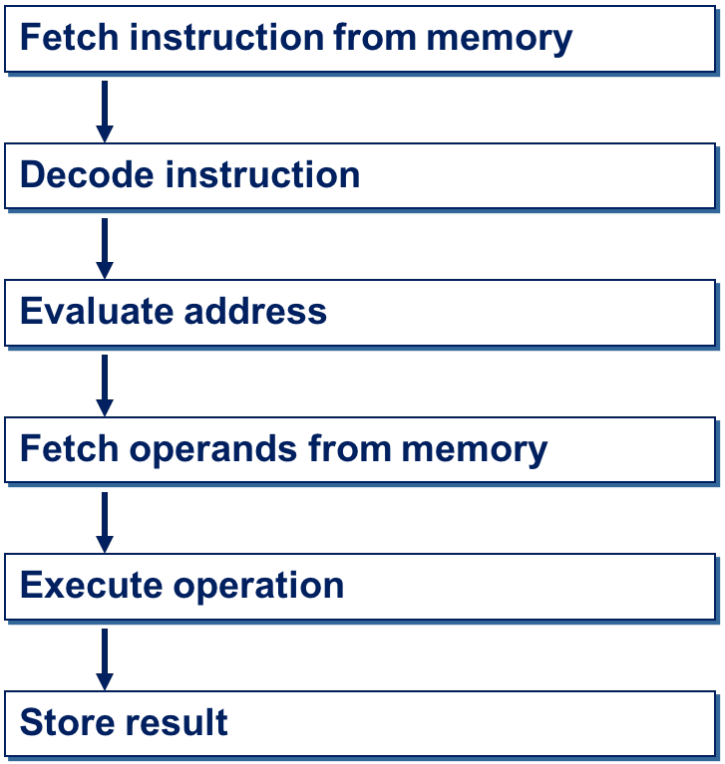


- Software sets “interrupt enable” bit in device register
- When Ready bit and IE bit are both set, interrupt is signaled

Interrupt-Driven I/O

An I/O device can:

1. **Force currently executing program to stop**
2. **Have the processor carry out the need of the I/O device**
3. **Resume the stopped program as if nothing had happened**



- **If INT is not asserted**
- **If INT is asserted**

Two Parts of Interrupt-Driven I/O

1. The mechanism to interrupt the processor
   - A way for the I/O device to _____ the CPU that an interesting event has occurred
   - A way for the CPU to _____ whether the interrupt signal is set and whether its priority is higher than the current program.

2. The process that manages the transfer of the I/O data
   - Initiate the interrupt (saving the state of the interrupted program & loading the state of the Interrupt Service Routine)
   - Service the interrupt
   - Return from interrupt

Processor State

- Enough state info saved for interrupted program to resume later
- Enough state info loaded for the interrupt service routine to begin service

State of a Program (snapshot of the system):

-
-
- PSR (processor status register)

PSR[15] – privileged (supervisor - 0) or unprivileged (user - 1) mode

PSR[10:8] – priority level, PSR[2:0] – condition code

Where to save state information?

Supervisor Stack

A special region of memory used as the stack for interrupt service routines.

- Initial Supervisor Stack Pointer (SSP) stored in _____
- Another register for storing User Stack Pointer (USP) - _____

Want to use R6 as _____, so that our PUSH/POP routines still work.

When switching from User mode to Supervisor mode (as result of interrupt), save R6 to _____.

Invoking the Service Routine

I/O device transmits Interrupt Vector (INTV, 8-bit) along with interrupt signal and priority level. When an interrupt is taken:

1. If Priv = 1 (user),
   Saved.USP = R6, then R6 = Saved.SSP.
2. Push PC and PSR to Supervisor Stack.
3. Set PSR[15] = 0 (supervisor mode).
4. Set PSR[10:8] = priority of interrupt being serviced.
5. Set PSR[2:0] = 0.
6. Set MAR = x01vv, where vv = 8-bit interrupt vector
   provided by interrupting device (e.g., keyboard = x80).
7. Load memory location (M[x01vv]) into MDR.
8. Set PC = MDR; now first instruction of ISR will be fetched.

Returning from interrupt

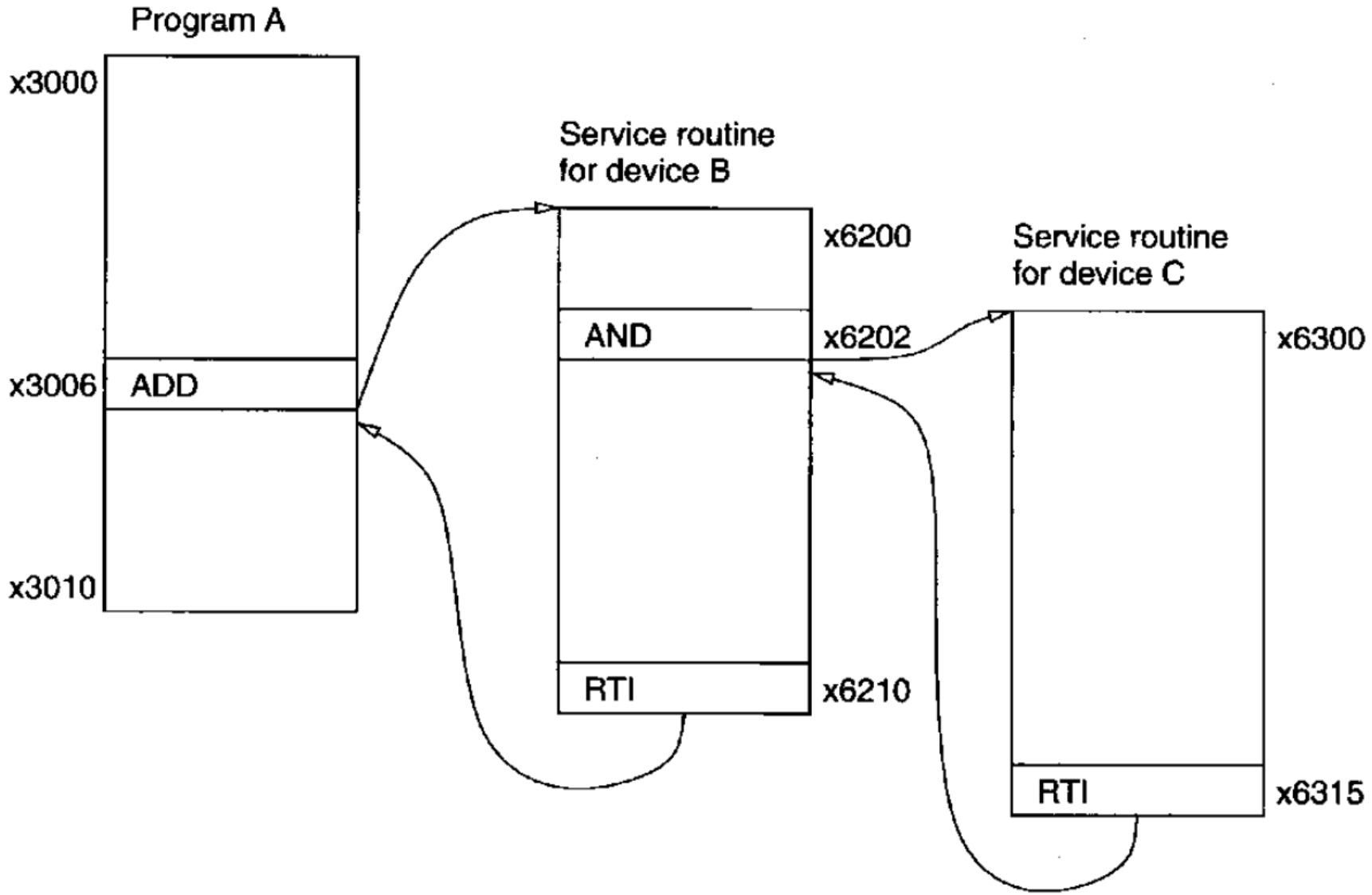
Special instruction (RTI) – restores state

1. Pop PSR from supervisor stack. (PSR = M[R6]; R6 = R6 + 1)
2. Pop PC from supervisor stack. (PC = M[R6]; R6 = R6 + 1)
3. If PSR[15] = 1, R6 = Saved.USP.
   (If going back to user mode, need to restore User Stack Pointer.)

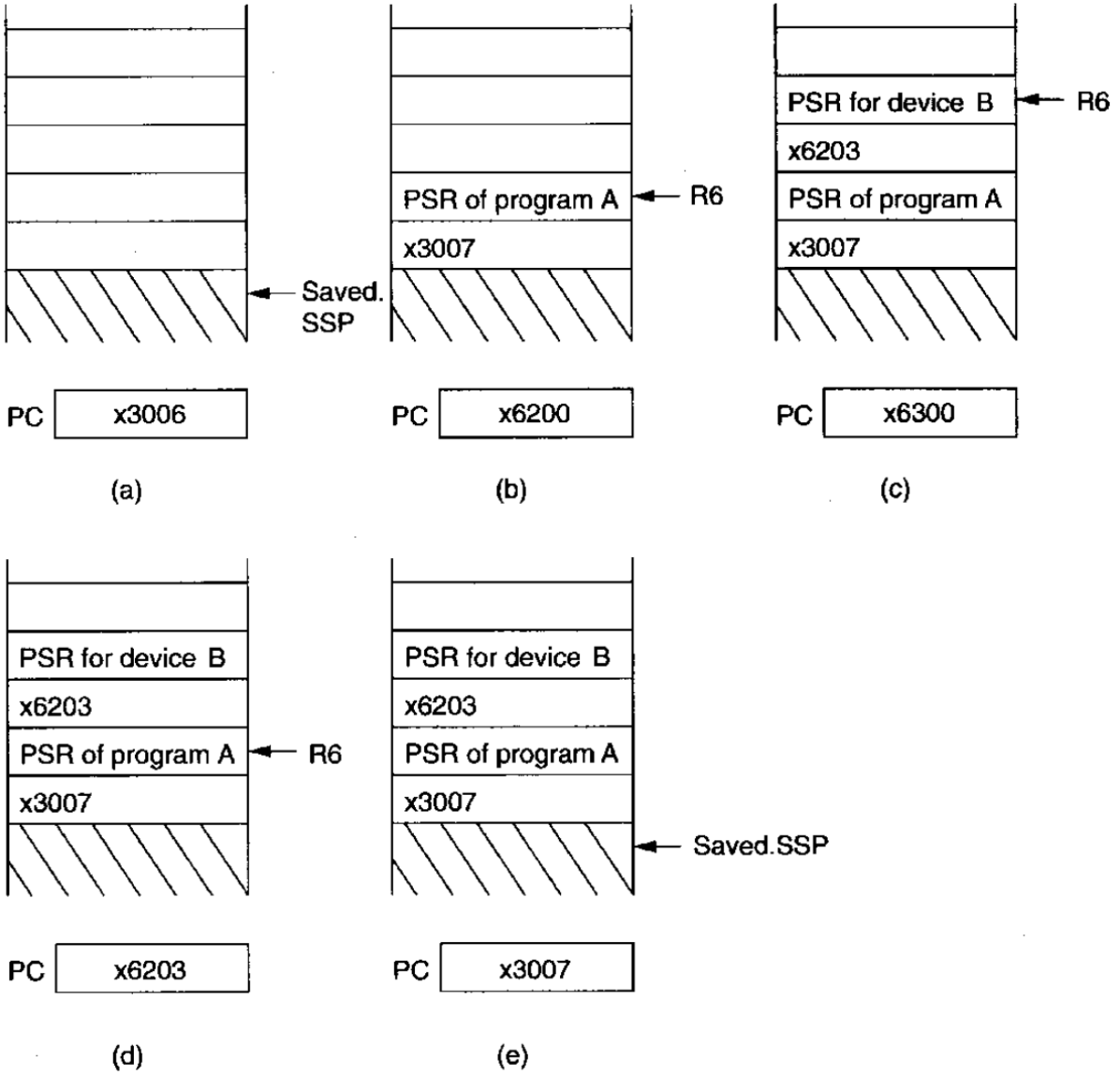
RTI is a privileged instruction.

- Can only be executed in Supervisor Mode.
- If executed in User Mode, causes an exception.

Nested Interrupt



Supervisor Stack During Nested Interrupt Execution



Exceptions: Internal Interrupt

When something unexpected happens *inside* the processor, it may cause an exception.

Examples of Exception in LC-3:

- **Privileged operation (e.g., RTI in user mode)**
- **Executing an illegal opcode (Bits[15:12] = 1101)**

Handled just like an interrupt

- **Vector is determined internally by type of exception**
- **Priority is the same as running program**

Interrupt Vector Table

Exception Service Routines – x0100 to x017F

Interrupt Service Routines – x0180 to 01FF

LC-3 Memory Map