Introduction:

Arithmetic Logic Unit (**ALU**) is an embedded system within a computer's central processing unit (**CPU**) which performs mathematical and logical operations using gateways made of electrical transistors. In some processors, the **ALU** is divided into two units: an arithmetic unit (**AU**) and a logic unit (**LU**). Some processors contain more than one **AU** . For example, one for fixed-point operations and another for floating-point operations. An **ALU** has a number of selection lines for different operations. If there are n selection lines, then there are 2^n distinct operations. In general, there are Eight Arithmetic Operations and Four Logical Operations.

If two operands are A and B in **ALU** then , Eight Arithmetic Operations are Addition, Addition with carry, A plus 1's Complement of B, Subtraction ,Transfer A or Transfer B, Increment A , Decrement A. Four Logical Operations are OR operation (**A + B**) , XOR operation (**A ^ B**) , AND operation(**AB)** and NOT operation (**A'**).

The steps involved in the design of an **ALU** are as follows :

1. Design the arithmetic section independent of the logic section.

2. Determine the logic operations obtained from the arithmetic circuit in step 1, assuming that the input carries to all stages are 0.

3. Modify the arithmetic circuit to obtain the required logic operations.

In some operations, mainly Arithmetic Operations, it should be stored the sign of the result, a zero indication, overflow conditions and so on. For these purposes, status register is used along with **ALU** . These status-bit conditions are sometimes called condition-code bits or flag bits.

Four status registers are carry (**C**), sign(**S**), zero(**Z**) and overflow(**V**).

1. If output carry is 1 in **ALU**, then **C** is set 1 . Otherwise, **C** is set 0.
2. If MSB is 1 in **ALU**, then **S** is set 1. Otherwise, **S** is set 0
3. If output of **ALU** contains all 0's, then **Z** is set 1. Otherwise, **Z** is set 0 or cleared
4. Bit **V** is set 1 if the **XOR** operation of last two carries is 1. Otherwise, **V** is cleared.