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ע"ש איבי ואלדר פליישמן
אוניברסיטת תל-אביב

Clock And Data Recovery

Project Number: **22-1-1-2576**

Project Report

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Project Carried Out at: University, Electronics lab.

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Abstract

This project focuses on designing and implementing a Clock and Data Recovery (CDR) system for 10GHz data transmission. The CDR system plays a crucial role in ensuring accurate reception of digital signals in high-speed data communication systems such as Ethernet, data center communication, wireless communication etc.

Clock and Data Recovery involves recovering the clock signal and extracting the accompanying data from the received digital signal. As data transmission speeds increase, maintaining clock integrity and accurately recovering data become more challenging due to signal distortions, noise, and timing variations. The project deliverable is a fully functional 10Gb Clock and Data Recovery (CDR) system meeting performance specifications.

The following scheme describes the block diagram of the circuit on which we will explain in the next sections.
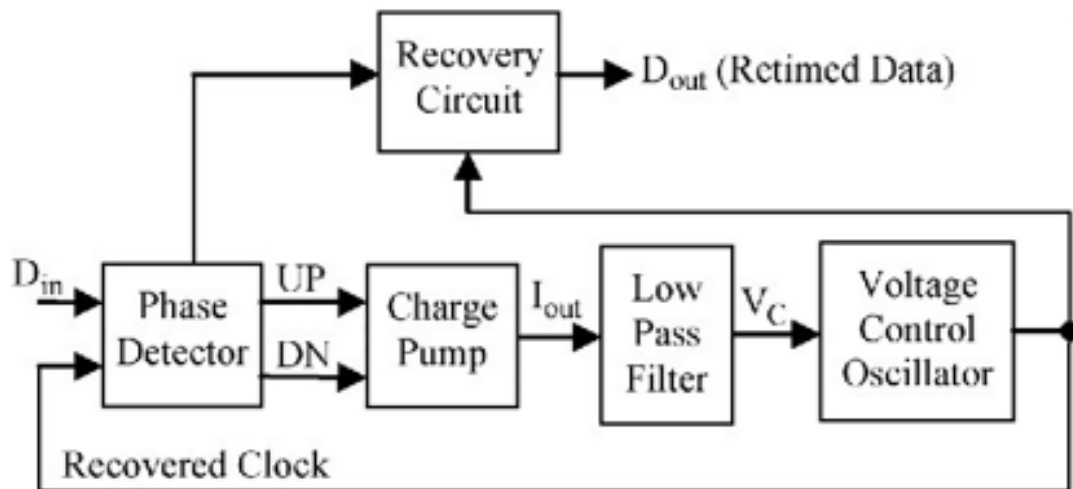

Figure 1:CDR Block Diagram

1 Introduction

As described earlier, the CDR plays a significant role in the digital communication world. And as data transmission speeds increase it becomes increasingly elaborated to design an efficient CDR.

As for today, the existing circuits are more complex, and each has its own advantages and disadvantages. Some of the existing CDRs are described in the following table:

Technology	Frequency	Power	Jitter Tolerance	Jitter Generation	Area	BER (Bit Error Rate)	Supply Voltage
SiGe BiCMOS 3.3-V	12.5Gb/s	420 mW at 3.3 V	exceeded with 50% margin – approx. 2 UI	1.65 ps rms	2X3 mm	less than 10^{-12}	1.2V
deep submicron CMOS - 14nm tri-gate CMOS	10Gb/s	59mW/lane	Approx. 0.1 UI	Approx. 0.3 UI	Each TX/RX lane occupies 0.0 65mm2(0.13 ×0.5mm2)	Less than 10^{-12}	0.9V
65nm CMOS	8.675Gb/s - 11Gb/s	37.2mW	Approx. 0.2 UI	-	$350 \times 400 \mu m^2$	Less than 10^{-12}	1.2V
0.13μm CMOS	10Gb/s	140mW	-	30ps (p-p)	$1.2x1.2$ mm^2	Less than 10^{-12}	VCO differential voltage range of −200mV to 150mV

Table 1: Comparison of existing CDR types

As we can see, some are more efficient considering space, some have better power consumption and each one of them uses different technologies.

The project is divided into 3 parts – the first part is conducting a literature review which will supply the basic knowledge about the circuit, the function of each sub-circuit and the theory behind the circuit. The second part is building the circuit in Cadence Virtuoso, using library components. The goal of this part is to apply the theory from the first part, learn about working with Virtuoso and get the results of an ideal CDR in order to compare them with the third part's results. The third part is building the VCO (Voltage Controlled Oscillator) in transistor level. This part includes more theory background, and a better understanding of the circuit in general and the VCO in particular. The goal is to design a CDR that meets the design requirements (will be presented and explained later on).

2   Theoretical background

Generally, clock and data recovery (CDR) implementations can be roughly divided into three types: phase-locked loop (PLL)-based, phase interpolator (PI)-based, and injection-locked. Our project focuses on phase-locked loop. The general block diagram of the CDR is presented above Figure 1 and from the block diagram we can see that the circuit consists of three main components – Phase Detector, LPF (along with the charge pump), and VCO:

<u>Phase Detector</u> – The function of the phase detector is to measure the phase difference between two incoming signals. Various topologies and designs for phase detectors already exist, such as the Alexander Phase Detector, the Hogge Phase Detector, the Quad-rate Phase Detector, the Octant-rate Phase Detector, etc. The phase detector is an essential element of the phase-locked loop (PLL). The detecting phase difference is important in applications such as motor control, radar,   and telecommunication systems, servo-mechanisms, and demodulators.

<u>Charge Pump (CP) and Low Pass Filter (LPF)</u> - The function of the charge pump is to convert the output voltage of the phase detector to current. This current is then fed to a low pass filter, where the capacitor is either charged or discharged depending on the phase detector output. The function of the low pass filter (LPF) is to convert the charge pump current into control voltage. To minimize the ripples on the control voltage it is possible to use a resistor.

<u>VCO</u> – A voltage-controlled oscillator (VCO) is an oscillator whose oscillation frequency is controlled by a voltage input. The function of the voltage control oscillator is to generate the clock signal at its output, the frequency of which can be changed by varying the input control voltage - the applied input voltage determines the instantaneous oscillation frequency

<u>Jitter-</u> Jitter is defined as the amount of variation in the waveform from their ideal position at zero crossing on the time axis. The Jitter transfer function is - Jitter transfer =| jitter(out)(f) / jitter(in)(f)|.

Existing circuits of the CDR parts: In the next section, we will present the circuits we worked with for the different parts of the CDR.

In appendix 9.4 we present different types of circuits which we didn't use.

Phase Detector - Alexander Phase Detector

The Alexander PD is a binary phase detector, which Only provides sign information of phase error (not magnitude). The Alexander PD is used in the high-speed CDR circuits that operate at GHz speed. It consists of four DFFs and two XOR gates. The scheme and output characteristic of the circuit:
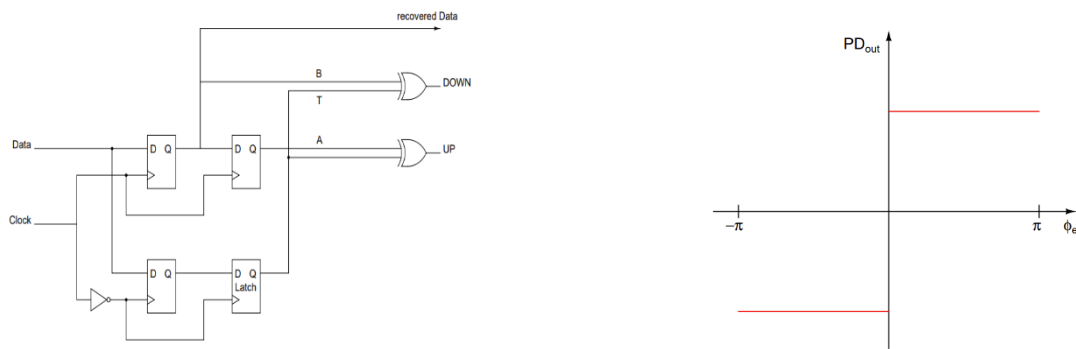

Figure 2:Alexander Phase detector

We can see that the output has two levels (binary PD). The Alexander PD performs two functions: 1) Determines, whether there is any transition in the input data, and 2) Whether the clock is earlier or later than the input data.

Charge Pump and Low Pass Filter:
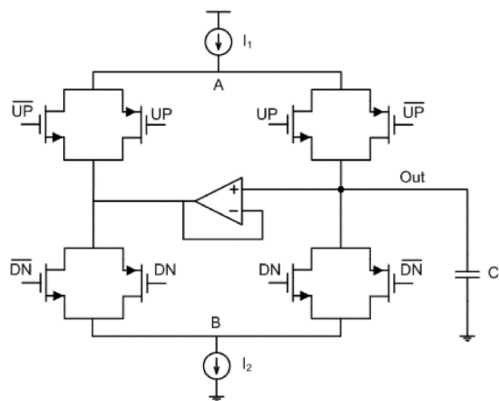
The Charge Pump presented in the next picture:

Figure 3:Charge Pump diagram
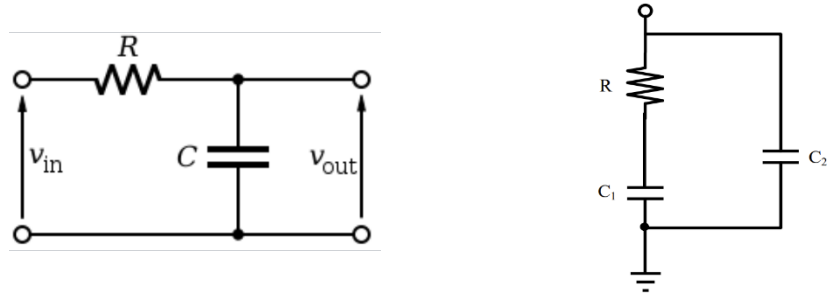
The LPF presented in the next pictures:

Figure 4:first and second order LPF

As we said earlier the function of the low pass filter (LPF) is to convert the charge pump current into control voltage. The Type-I LPF Figure 4(left) is replaced by Type-II LPF Figure 4(right) due to trade-offs between the settling time, ripple on the control voltage, and the phase error and stability.

VCO – LC VCO:

A differential LC VCO topology is suitable for low voltage operation satisfying the phase noise requirement. Differential tuning is obtained by cascading the varactors with fixed capacitors and applying a differential control voltage. The choice of inductance value plays a critical role in phase noise performance of an LC VCO. For better phase noise performance, a smaller inductance value is preferred.

An example for the circuit:
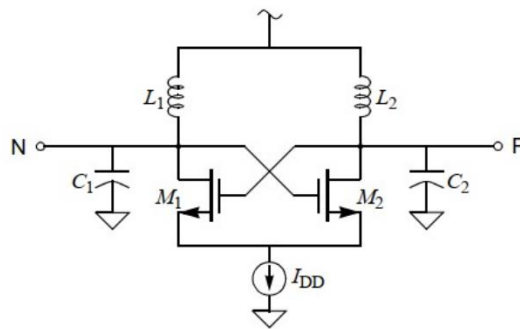
Figure 5:VCO diagram

After covering the existing parts of the CDR, we can choose the circuits we will work with according to the parameters presented above. For a PD we will choose Alexander Phase Detector due to its compatibility for high frequencies. The Charge pump and LPF are presented above and for a VCO we will work with is LC VCO because it is suitable for low voltage operation satisfying the phase noise requirement.

The transfer function of the whole circuit is:

$$T = \frac{T_{PD} \cdot T_{charge-pump} \cdot T_{LPF} \cdot T_{VCO}}{1 + T_{PD} \cdot T_{charge-pump} \cdot T_{LPF} \cdot T_{VCO}}$$

Equation 1:CDR Transfer Function

$$T_{PD} = \frac{2}{\pi} \cdot (TD), TD - transition\ density, we\ will\ assume\ TD$$

$$= 0.5\ and\ adjust\ during\ simulations\ if\ needed$$

$$T_{PD} = \frac{1}{\pi}$$

Equation 2:Phase Detector Transfer Function

$$T_{VCO} = \frac{K_0}{s}$$

Equation 3:VCO Transfer Function

$$T_{LPF+CHARGE\ PUMP} = I_{charge-pump} \cdot Z(RC\ impedance)$$

$$= I_{charge-pump} \cdot \left[(R + \frac{1}{sC_1}) | \left| \frac{1}{sC_2} \right| \right]$$

$$= I_{charge-pump} \cdot \frac{\left[\frac{1}{C_2} + \frac{1}{sC_1 C_2 R} \right]}{\left[s + \frac{1}{RC_1} + \frac{1}{RC_2} \right]}$$

Equation 4:Charge Pump Transfer Function

Also, an important transfer function is the Jitter transfer function:

$$Jitter\ transfer\ = | jitter(out)(f) / jitter(in)(f) |.$$

Equation 5:Jitter Transfer Function

By expressing the transfer function of the whole circuit, we can see that there might be a stability problem, and from our research we can say that the unknown constants in the transfer function will determine the circuits stability. That part will be examined and shown in the next part of our project.

3 Simulation

The simulation environment is Virtuoso by Cadence. We have created a scheme of the part we tested (if needed) and then created a test bench on which we simulated our circuit. In order to design and build our CDR we simulated each part separately first. We will present the different test benches and simulations; all results will be explained in section 5.

At this stage we have simulated the sub circuits of the ideal CDR, the simulations are presented in appendix A.

After testing each component separately, we have built the whole circuit -
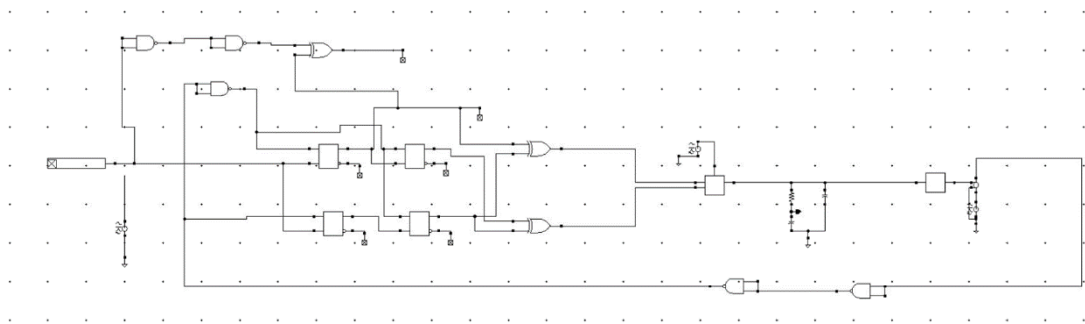
The full circuit scheme:

Figure 6:Full circuit scheme

Zoomed in circuit appear in appendix 9.1

Simulations result:

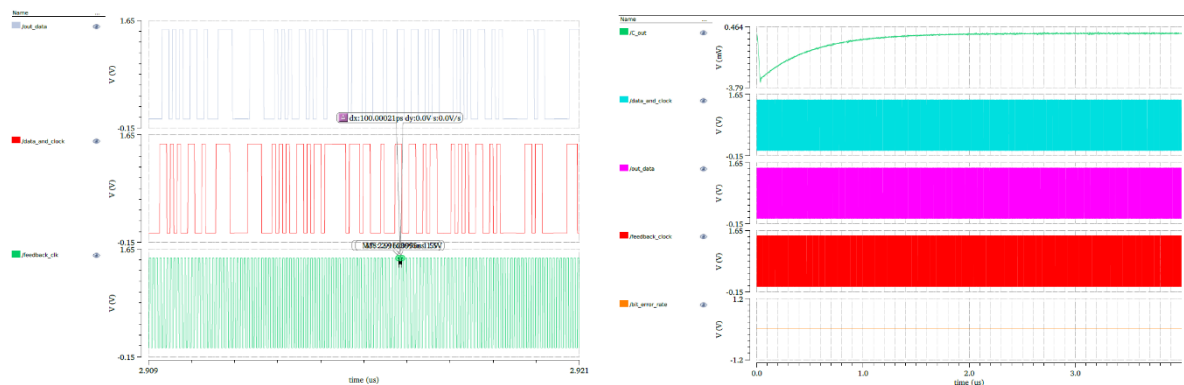**The first simulation shows the important signals waveforms:**

Figure 7:Ideal CDR Simulation result - 10GHz

On the left we can see the zoomed in waves and on the right, we have the full simulation. Next, we can see the eye diagrams of the data and feedback clock:

Figure 8:Ideal CDR Simulation result - 10GHz eye diagram

In red we can see the clock's diagram and in yellow we can see the data diagram.

The next simulation is of the 10GHz +250MHz data. We have the same pictures as well –

Relevant waveforms:

Figure 9:Ideal CDR Simulation result - 10GHz+250MHz

On the left we can see the zoomed in waves and on the right, we have the full simulation.

Eye diagram:

Figure 10:Ideal CDR Simulation result - 10GHz+250MHz eye diagram

In red we can see the clock's diagram and in yellow we can see the data diagram.

The next simulation is of the 10GHz -250MHz data. We have the same pictures as well –

Relevant waveforms:

Figure 11: Ideal CDR Simulation result - 10GHz-250MHz

On the left we can see the zoomed in waves and on the right, we have the full simulation.
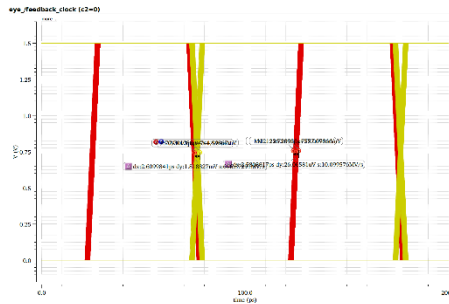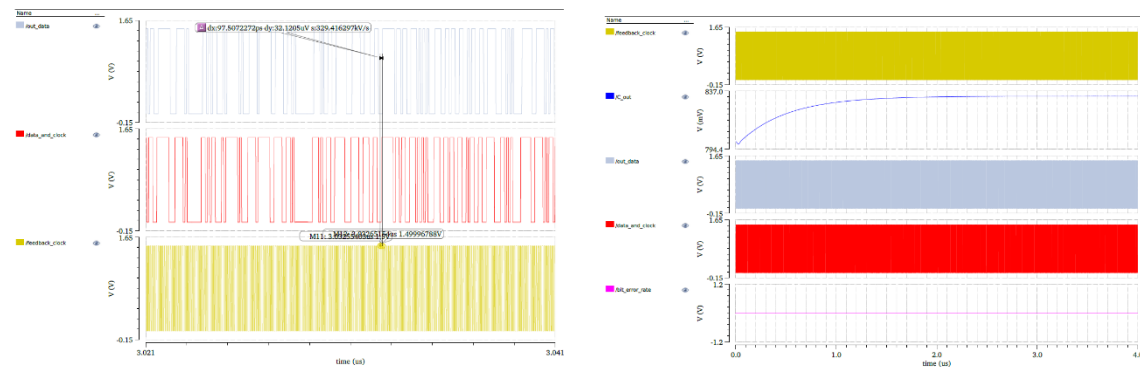
Eye diagram:

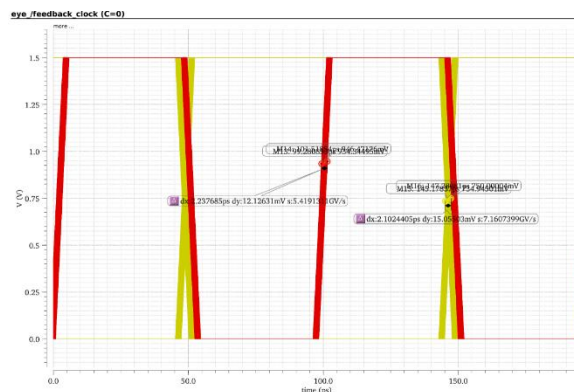**Figure 12:Ideal CDR Simulation result - 10GHz-250MHz eye diagram**

In red we can see the clock's diagram and in yellow we can see the data diagram.

Jitter tolerance simulations:

We have inputted an input with changing frequencies and simulated our CDR.

The results show the eye diagram of the feedback clock and the output data, for each simulation we have the required results:
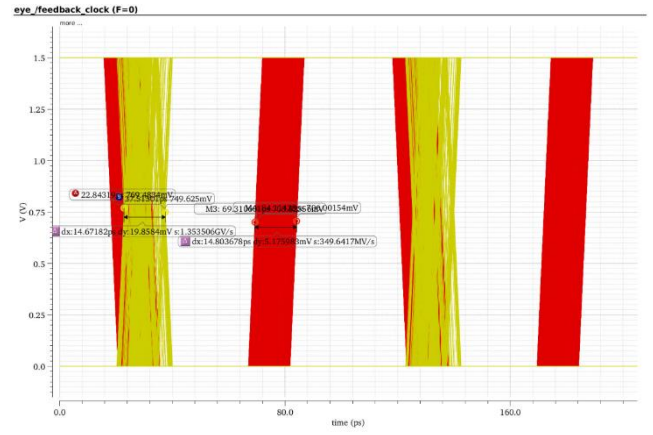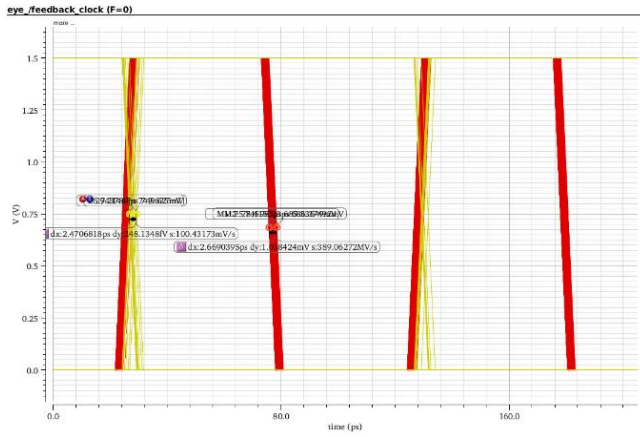
Figure 13: Jitter tolerance - Eye diagram 100Mhz/0.25UI(Left) 4Mhz/0.75UI(Right)
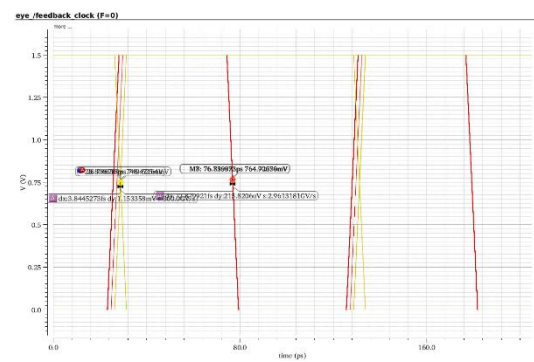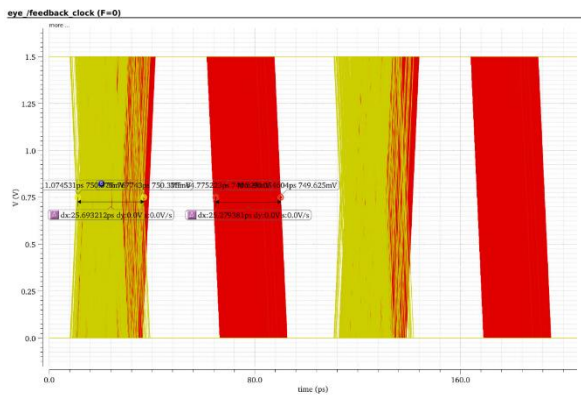
Figure 14:Jitter tolerance - Eye diagram 0.4Mhz/3UI(Left) 400Mhz/0-17ps(Right)

After testing the "ideal" CDR we have built our VCO on transistor level. The scheme of the non-ideal VCO:
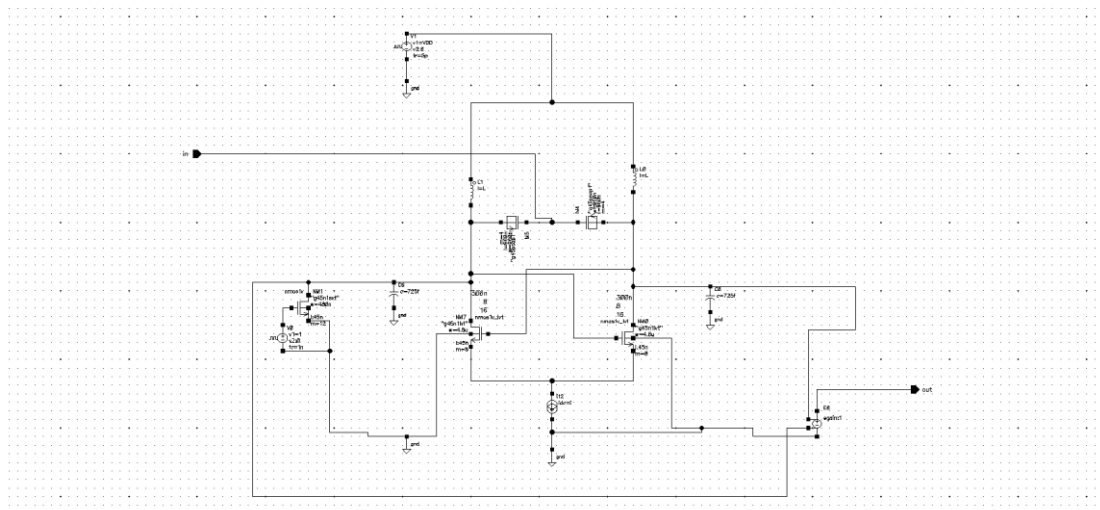
Figure 15:Nonideal VCO diagram

The testbench and the Simulation:
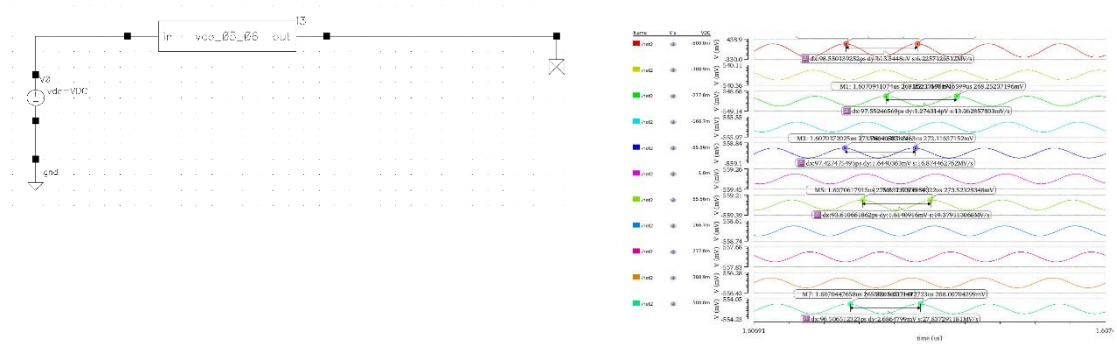
Figure 16:Test and Simulation of Nonideal VCO

After testing the nonideal VCO, we have placed it in our CDR.
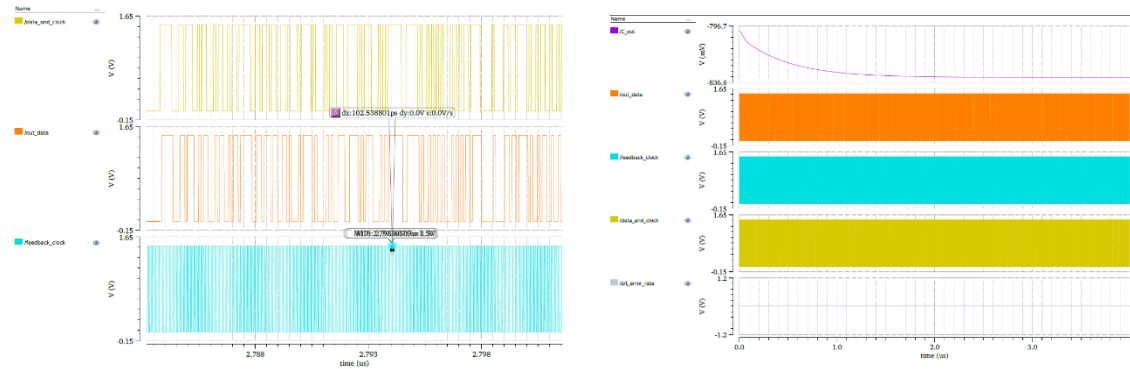
The simulations:

Relevant waveforms:
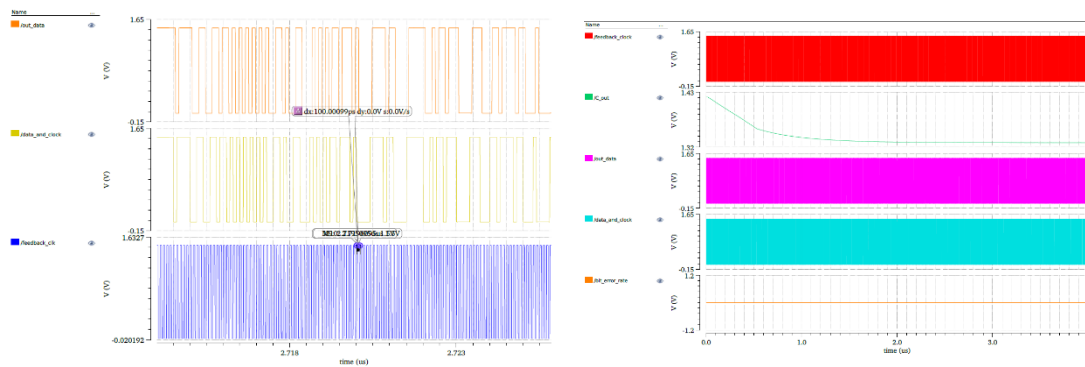
Figure 17:Nonideal Simulation result - 10GHz

On the left we can see the zoomed in waves and on the right we have the full simulation. Eye diagram data and clock at 10 GHz:
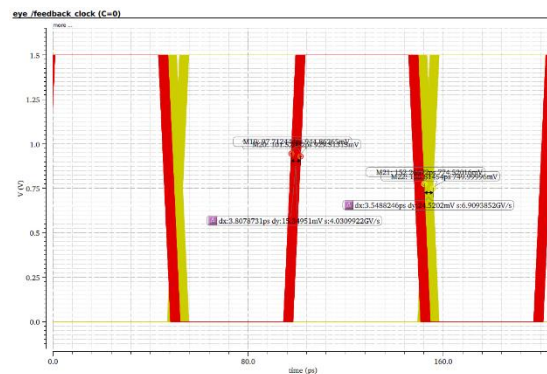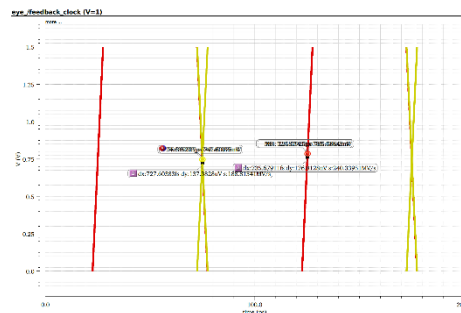

Figure 18:Nonideal Simulation result - 10GHz eye diagram

The clock diagram is in red and the data in yellow.

4 Implementation

We will first present a detailed block diagram of the circuit:

Block Diagram
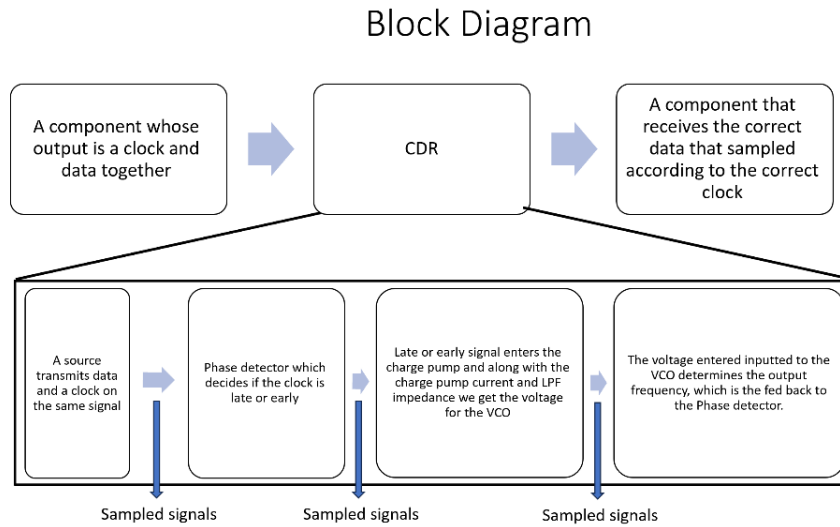
Figure 19: Implementation diagram

4.1 Hardware Description

In order to implement our CDR, we have used Virtuoso by Cadence. The libraries we have used are the following: analoglib, basic, ahdllib, gpdk045 which all use the technology of 45nm.

In the first part of our project, we have set some reasonable parameters to the library components such as delays for the D-FFs, NAND gates for example. But some of the parameters needed to be calculated or carefully set. Such parameters are the LPF components, CP current, VDD – source voltage and VCO gain. Those parameters effect the stability of the circuit (as presented in the theoretical background).After simulation the circuit and getting the desired results, we have designed the nonideal VCO. At first, we have designed an oscillator – LC oscillator with no sensitivity to voltage input. That oscillator had the desired oscillation frequency of 10G. The oscillator's scheme:
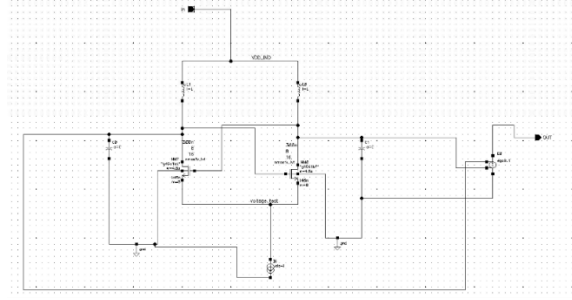
Figure 20: Oscillator scheme - 10G

Where the input voltage is VDD and there is no control voltage. We have started using an inductor of 300pHy (a standard size for a VCO), and using the formula for a simple LC circuit we have calculated the needed capacitor –

$$f = \frac{1}{2\pi\sqrt{LC}} \rightarrow c = \frac{1}{4\pi f^2 L}$$

The value of the capacitor we calculated was slightly adjusted according to simulations.

After getting the desired frequency we have added varactors (pmos varactors), which will change the capacitance of the VCO according to the input voltage and as a result will change the frequency. The full VCO scheme, including the varactors as we cans see in Figure 15.

As can be seen from the scheme pictures, all components are taken from gpdk045 and analoglib, meaning there are no premade parts.

5 Analysis of results

We will start by explaining the simulation results presented in section 3 in the same order.

Phase Detector: From Figure 2 we can see the following behavior:

Q_up_2	Q_down_1	Q_up_1	Q_up_2 xor Q_down_1	Q_down_1 xor Q_up_1	Action
0	0	0	0	0	-
0	0	1	0	1	Early
0	1	0	1	1	-
0	1	1	1	0	Late
1	0	0	1	0	Late
1	0	1	1	1	-
1	1	0	0	1	Early
1	1	1	0	0	-

Table 2:Phase Detector truth table

This is the behavior we expect to get from that PD – we would like the PD to sample exactly in the middle of the data, in that situation the PD will do nothing. Otherwise, if the samples are too fast, we will get an early signal and if the samples are too slow, we will get a late signal. That signal is then sent to the CP, which in turn will produce a current to create an appropriate control voltage to the VCO.

Charge Pump: From Figure 26Figure 26 we can see that according to the two inputs of the CP it produces a current. The current's absolute value is the same for early and late, but it differs in its sign. Early signal will produce a minus sign and late will produce plus sign. After multiplying the current in the LPF impedance we will get the VCO input voltage.

VCO: From Figure 29 we can see that different voltages produce different frequencies. At approx. 0 volts, the frequency id 10 GHz, for lower voltages we get a higher period which means lower frequency and for higher voltages we get lower period which corresponds to higher frequencies.

Ideal CDR: From Figure 7 we can see a few important pieces of information: first of all we can see the correct frequency – 10 GHz, secondly we can see that the samples are at the middle of the data, which means that the PD samples the data correctly and we get the correct data we also see that the output data and the input data are similar which is one indication of 0 BER. Another proof of 0 BER is on the right picture, we have a signal called BER – which is a XOR between both signals (input and output data). The output data has a slight shift due to delays in the circuit, so we have added to invertors in order to be able to

compare the signals correctly. Another important signal is the voltage on the capacitor C – the capacitor's voltage is stable which means that our CDR is locked on the correct frequency. From Figure 8 we can see the eye diagrams of the feedback clock and the output data (after being samples with the feedback clock). From that figure we can see that the Jitter, which is marked with two point is low and that we get a Jitter that is less then 0.25UI (UI = 100ps). We can see that the Jitter for the clock is 2.58ps and the Jitter for the data is 2.6ps – meaning that the total jitter of the data, clock, and setup of the FF (which is 10ps) is less than 50ps (half of the period time) – another proof of 0 BER. From Figure 9 we can see the simulation for 10GHz+250MHz. Same as for the 10GHz simulation we can see that- the capacitor sets on a stable value, the samples are in the middle of the input data and we have 0-bit error rate. From Figure 10 which shows the jitter we can see again that the Jitter is lower than 0.25UI. The clock's Jitter is 2.23ps and the data Jitter is 2.1ps – as before, the total jitter and setup time is less than 50ps.

From Figure 11 and Figure 12 we can see the simulation for 10GHz-250MHz – same simulations and results as for the 10GHz +250MHz.

From Figure 13 we can see the eye diagram with 100MHz shifting input, the Jitter is approx. 2.5ps which is less than 0.25UI and we can see an input that is shifted by 4MHz and the jitter is 15ps which is less then 0.75UI..

From Figure 14 we can see an input that is shifted by 0.4MHz and the jitter is 25ps which is less then 3UI and we can see an input with sine wave at 400MHz and the jitter is 72fs which is within the required range (less then 17ps).

All four simulations show that the Jitter tolerance requirement is met.

Nonideal VCO: Figure 15 shows the simulation of the nonideal VCO. We can see that similar to the ideal VCO (from ahdllib) we get different frequencies for different input voltages. The main difference is the voltage range – in the nonideal VCO the voltage range in the simulation is smaller due to the fact that the voltage range produced from the CP and LPF is lower, and we needed to test only for that range.

Nonideal CDR: Figure 17 shows the simulation result for the nonideal CDR at 10GHz – same signals as for the ideal CDR. From that simulation we can see the following – the clock samples in the middle of the clock, the sampled data

is similar to the input data (again from the BER signal and also the transient simulation) and the voltage on the capacitor is stable. That simulation insures us that the CDR is locked on the correct frequency, and we have 0-bit error rate. From Figure 18 we can see that the Jitter of the data and the clock (both) is 0.7ps which is less than 0.25UI – meaning that the total jitter of the data, clock and setup of the FF (which is 10ps) is less than 50ps (half of the period time) – another proof of 0 BER. If we compare our results to the existing CDRs (which are presented in Table 1 we can see that: our voltage (VDD) is similar to the supply voltages used in other circuits, the 0-bit error rate is achieved in all circuits, and we have a very low Jitter, less than all the circuits listed in the table.The circuits presented in the table were all tested in "real life" and not only in simulations so in order to compare the real results we will have to test the circuit in the lab.

6 Conclusions and further work

Pre decided goals:

Upon the beginning of our work, we have set the main goals and results we expect to achieve. Those goals were set by our project's instructor. The goals describe the 3 parts of our project and the expected results on each part:

We have 3 main parts:

1. Literature review – the first part was to conduct a literature review in which we will learn about the circuit, about each part of it and its function. The result had to include a comparison between existing circuits and their parameters.

2. The second part is building the CDR using library components. The purpose of this stage was to understand how each part works in simulation and that the quantitative requirements are realistic. The results of this part are the simulations proving that the circuit is working, and the requirements are met.

3. Once the second part is finished, the next step is building some of the main parts of the circuit in transistor level. The goal was to build one or two parts in transistor level ad the results of this sage are the same simulations we made for the ideal CDR.

Results after finishing the project:

We have completed all 3 parts of our project - the literature review was submitted on time to our instructor, the main conclusions of our review are explained in the theoretical background and the rest will be documented and submitted as well. The simulations of our ideal circuit are presented in section 3, the requirements are met and the circuit functions properly. Since we have not used only library components in the second part of the project, the parts that we have built 2 full sub-circuits which are the VCO and the LPF. We have also built the Phase Detector but not in transistor level – we have used D-FFs and XOR gates from library but not the full component. The simulations of the nonideal CDR are also presented in section 3. We have a functioning CDR that can recover data from 10GHz data input.

Suggestions to improve and possibilities for future:

In order to complete the design and built a functioning CDR which is not using ideal components, one can design a Charge Pump and Phase detector on a transistor level. The Phase detector is composed of D-FFs and XOR gates and

should not be complicated to design. The Charge Pump is a bit more complicated and includes current sources and MOSFETs which needs to be designed and simulated. An obvious suggestion to improve the performance is reducing the supply voltage. In the theoretical background we have presented a circuit that has a lower supply voltage which might lead to lower power consumption. Power consumption is important in such circuits because they are usually a small part on the chip.

Another aspect that can be tested is the area consumption of the circuit. In our work we did not consider the area of the circuit (the layout size) which is one of the most important considerations when manufacturing chips. The last improvement we can suggest is improving the tolerance of the CDR to different frequencies. We have designed our CDR to withstand changes of 1MHz in frequency, by changing the varactor's size we can set a wider range of frequencies that our VCO can lock on. The main problem here might be the gain of the VCO – which as we described earlier has a key role in determining whether the CDR is stable or not.

7 Project Documentation

We have created a Git repository which contains all our assignments and results. We have also included files explaining how to create the circuits and test them. The repository includes important articles and information in order to understand the circuit. The files are listed in the following table:

File name	Description
Work Plan - Tal Kahlon and Shahar Zarkovsky (CDR)	Work plan with timelines
Literature review – CDR	Theoretical background on the circuit
Poster - Tal Kahlon and Shahar Zarkovsky	Powerpoint poster of the project
Ideal CDR - scheme and simulation	Scheme and simulations description with pictures
LC VCO - scheme and simulations	Scheme and simulations of the VCO - description with pictures
CDR_Final_Project.rar	Virtuoso tar file

Table 3:Project Documentation

GitHub link to our repository:

https://github.com/ShaharZarkovsky/Final-Project-CDR-/tree/main

8   References

[1]   K. A. Clark ,"Modeling the Performance of the Clock Phase Caching Approach to Clock and Data Recovery", Journal of Lightwave Technology, Vol. 40, March 2022.

[2]   Miao-Shan Li, Yen-Kuei Lu,"PLL-Based Clock and Data Recovery for SSC Embedded Clock Systems",2019 International SoC Design Conference (ISOCC), 06-09 October 2019.

[3]   Ryan Helinski, Thomas LeBoeuf," A linear digital VCO for Clock Data Recovery (CDR) applications", 2010 17th IEEE International Conference on Electronics, Circuits and Systems, 12-15 December 2010.

[4]   Alireza Sharif Bakhtiar," A charge-pump with a high output swing for PLL and CDR applications", Proceedings of the 8th IEEE International NEWCAS Conference 2010, 20-23 June 2010.

[5]   M. Meghelli," SiGe BiCMOS 3.3-V clock and data recovery circuits for 10-Gb/s serial transmission systems", IEEE Journal of Solid-State Circuits, Vol. 35, December 2000.

[6]   Rajeev Dokania, Alexandra Kern," 10.5 A 5.9pJ/b 10Gb/s serial link with unequalized MM-CDR in 14nm tri-gate CMOS", 2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers, 22-26 February 2015.

[7]   Ravi Shivnaraine," An 8mW frequency detector for 10Gb/s half-rate CDR using clock phase selection", Proceedings of the IEEE 2013 Custom Integrated Circuits Conference, 22-25 September 2013.

[8]   M. Ramezani," A 10Gb/s CDR with a half-rate bang-bang phase detector",Proceedings of the 2003 International Symposium on Circuits and Systems, 2003. ISCAS '03. 25-28 May 2003.

[9]   Dr. Phillip E. Allen, "ECE 6440 Frequency Sythesizers", https://pallen.ece.gatech.edu/Academic/ECE_6440/Summer_2003/ece_6440_su2003.htm.

9   Appendix

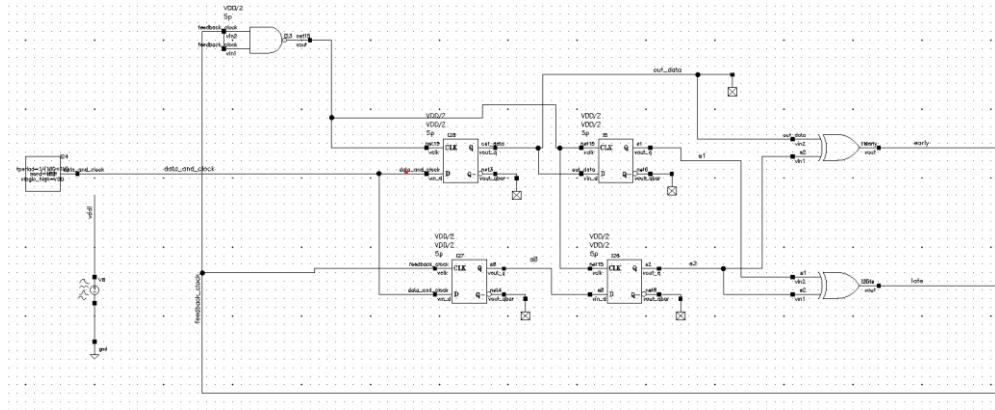## 9.1   Simulations of sub circuits

Zoom in on the left part:

Figure 21:CDR scheme - left part (zoomed in)
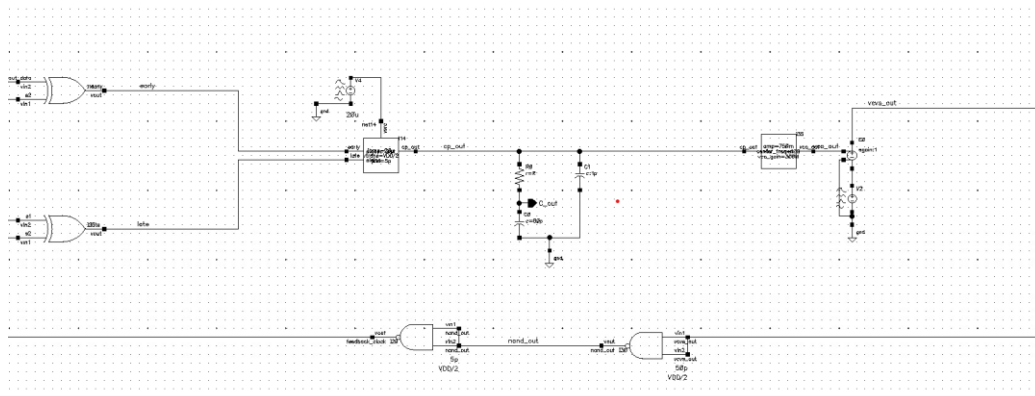
Zoom in on the right part:

Figure 22:CDR scheme - right part (zoomed in)

For the second part of our project, we have simulated the sub circuits of the ideal CDR in order to check correct behavior. The simulations are presented in this section.

Phase Detector: As described earlier, the first part of the project was building the circuit with library components. As for the Phase Detector, we didn't have a premade library component, so we have created a testbench using the description in In order to test it we have created the following testbench:
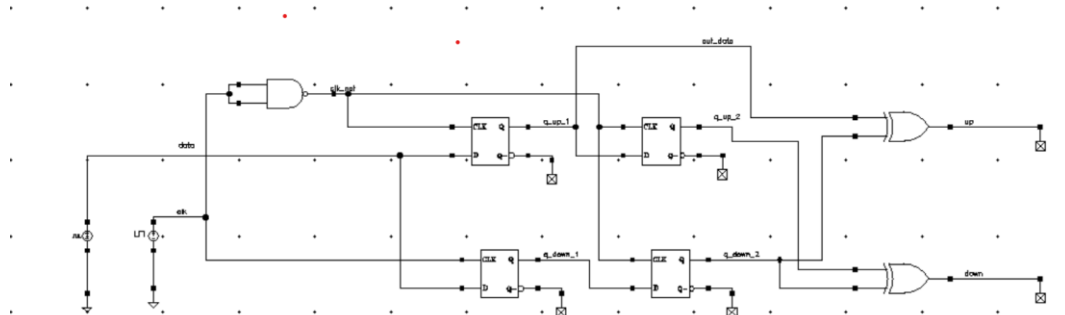

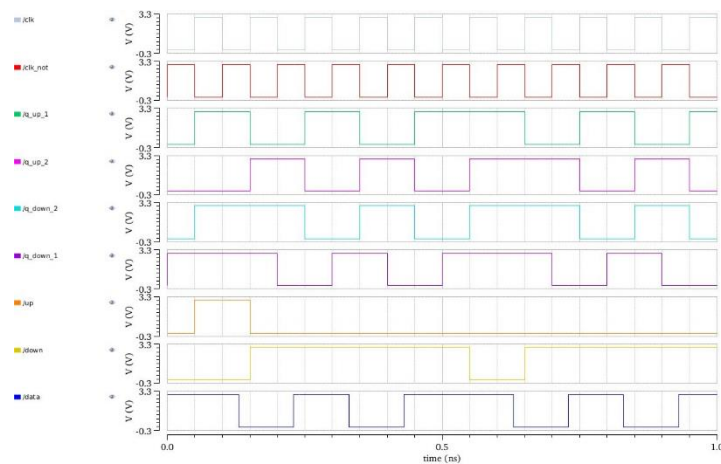**Figure 23:Phase detector scheme**

The simulation results:

Figure 24:Phase detector simulation

Charge Pump:

The charge pump was taken from a library (which will be presented in the next chapter), and so we have built the test bench:
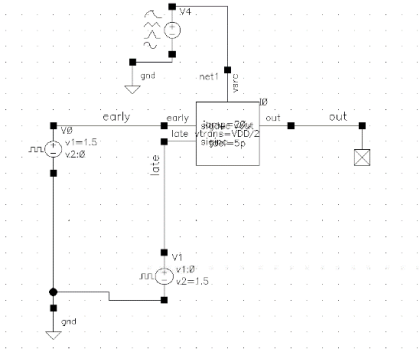
Figure 25:Charge Pump scheme
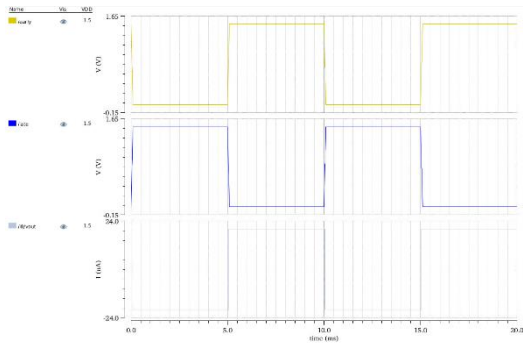
The simulation result:

Figure 26:Charge Pump simulation

<u>Low Pass Filter</u>: The LPF was not a library component. The scheme of the LPF was built according to the theoretical background:
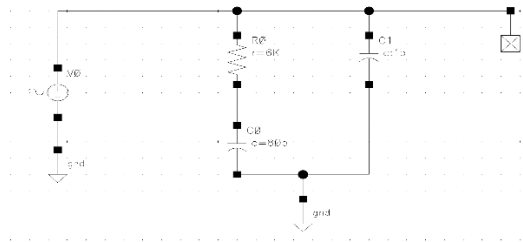

Figure 27:Second order LPF scheme

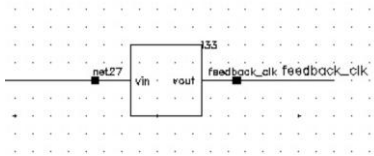<u>Voltage Controlled Oscillator</u>: The VCO was taken from a library. The testbench:

Figure 28: Ideal VCO scheme
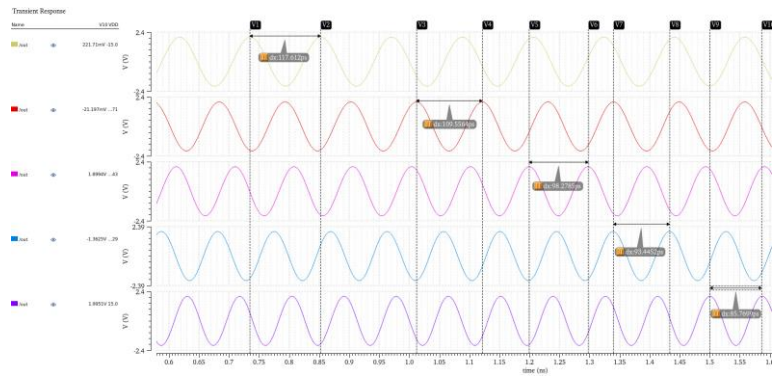
The simulation result:

Figure 29: Ideal VCO simulation

9.2 Calculations of the LPF parameters

Transfer function:

$$G(s) = \left(\frac{K_{VCO}}{s}\right) \cdot I_{CP} \cdot F(s)$$

Where F(s) is the loop filter transfer function in (Volt/Amps).

$$F(s) = \frac{1 + src_1}{s\left((c_1 + c_2) + (src_1c_2)\right)}$$

The loop filter transfer function is:

$$H(s) = \frac{\left(\omega_n^2\left(1 + \frac{s}{\omega_z}\right)\right)}{s^2 + 2s\xi\omega_n + \omega_n^2}$$

Where:

$$\omega_n \text{ is the underdamped natural frequency } \left(\frac{rad}{s}\right)$$

$$\omega_z \text{ is a stabilizing zero} = \frac{1}{rc_1}\left(\frac{rad}{s}\right)$$

$$\xi \text{ is the damping factor}$$

In total we have 2 poles and one zero, but the 2nd order ignores c2 and the feedback delay.

Also,

$$\omega_n = \sqrt{K_{VCO} \cdot \frac{I_{CP}}{c_1}}\left(\frac{rad}{s}\right)$$

For stability we need:

$$\frac{\omega_n}{2\pi} < \frac{1}{15}(reference\ frequency)$$

Damping factor:

$$\xi = \frac{RC_1\omega_n}{2}, usually\ 0.45 < \xi < 2$$

Lower damping factor means low period jitter and higher means accurate ref phase tracking.

Lower end of range for low period jitter

$$\phi_m(degrees) = \left(\frac{180}{\pi}\right) * (\text{atan}(\omega_c * RC_1) - \text{atan}(\omega_c * RC_2) - \omega_c * T_{dly})$$

$$\omega_c = crossover\ frequency, \text{frequency where } open - loop\ gain\ G(s) = 0\text{dB}$$

For stability: 1/RC1 (zero) < ωc < 1/RC2 (parasitic pole)

Typical Range: $1.2 * \omega_n < \omega_c < 2.5 * \omega_n$

Phase margin degradation due to PFD phase error sampling

$$-\phi = \omega_c * T_{ref} / 2$$

z-domain analysis is more accurate.

Phase margin:

$$B\phi_m \sim 100 * \xi \ (for \ \xi < 0.5)$$

Usually, 45° < PM < 70°

Phase Response vs. Damping

$$C_2 = 10\% * C_1 \ (high \ end \ of \ C_2 \ range \ requires \ lower \ \zeta)$$

$$Less \ ringing \ and \ overshoot \ as \ \zeta \to 1$$

Our LPF parameters:

$$\omega_n = \sqrt{K_{PD} \cdot K_{VCO} \cdot \frac{I_{CP}}{c_1}} \left(\frac{rad}{s}\right) = \sqrt{\frac{1.5}{2\pi} \cdot 10 \cdot 10^7 \cdot \frac{5 \cdot 10^{-3}}{c_1}} < 2\pi \cdot \frac{1}{15} \cdot 10 \cdot 10^9$$

$$\sqrt{C_1} > \frac{\sqrt{\frac{1.5}{2\pi} \cdot 10 \cdot 10^7 \cdot 5 \cdot 10^{-3}}}{2\pi \cdot \frac{1}{15} \cdot 10 \cdot 10^9}$$

We will choose $C_1 = 80pF$

Moreover:

$$R = \frac{2}{C_1 \omega_n} \approx 6 \ kohm$$

C2:

$$C_2 = 0.01 \cdot C_1 = 1pF$$

9.3   Stability considerations – bandwidth

To calculate the CDRs bandwidth we will use the following formula:

$$bandwidth = \omega_{-3dB} = \sqrt{\omega_{LPF} \cdot K}$$

Where $K = K_{PD} \cdot K_{VCO}$

We know that in our case:

$$K_{PD} = \frac{2}{\pi} , K_{VCO} = 300 \cdot 10^6$$

We also know the $\omega_{LPF} = \frac{1}{RC} = 62.9 \cdot 10^6 \left[\frac{rad}{sec}\right]$

Hence

$$bandwidth = \sqrt{62.9 \cdot 10^6 \cdot \frac{2}{\pi} \cdot 300 \cdot 10^6} = 110 \ MHz$$

The Phase Margin is given by –

$$PM = \tan^{-1}\left(\frac{K}{\omega_z}\right) - \tan^{-1}\left(\frac{K}{\omega_p}\right)$$

Where $\omega_z \ and \ \omega_p$ are the pole and zero of the LPF.

$$\omega_z = \frac{1}{RC} , \omega_p = \frac{2C}{RC^2}$$

$$\omega_z = \frac{1}{RC} = 62.9 \cdot 10^6 , \omega_p = 40 \cdot 10^9$$

Then,

$$PM = \tan^{-1}\left(\frac{K}{\omega_z}\right) - \tan^{-1}\left(\frac{K}{\omega_p}\right) = \tan^{-1}\left(\frac{127.3 \cdot 10^6}{62.9 \cdot 10^6}\right) - \tan^{-1}\left(\frac{127.3 \cdot 10^6}{40 \cdot 10^9}\right)$$

$$= 63.5 \ deg$$

9.4   Existing CDR sub circuits

Phase Detector:

1. **Hogge detector** - A linear phase detector, linear phase detectors provide both sign and magnitude information regarding the sampling phase error. For a certain input D_{in} we get two outputs Late and Early. The Late output is XOR between the input and the output of the left FF, the Early output is XOR between both the FF output. The main problem with the HPD is that the output terminals do not assume fixed states even in the condition of phase matching of the two inputs to it.

2. **XOR Phase Detector** - The exclusive OR XOR phase detector circuit can provide a very useful simple phase detector for some applications. It comprises of a logic exclusive OR circuit. The scheme and output characteristic of the circuit:
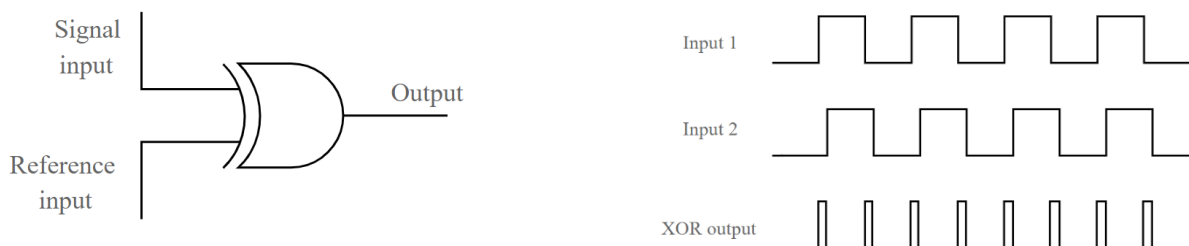

Figure 30: XOR Phase Detector

The problems of this Phase Detector are:
- It is sensitive to the clock duty cycle - a steady duty cycle should be used. It will lock with a phase error if the input duty cycles are not 50%.
- The output characteristic of the XOR phase detector show repetitions and gain changes. This means that if there is a frequency difference between the input reference and PLL feedback signals the phase detector can jump between regions of different gain.

VCO:

Ring Oscillator: consists of an odd number of gain stages in a loop. It has a high frequency tuning range and small area consumption, and it produces less jitter.