CPU Architecture

LAB4 assignment

FPGA based Digital Design

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12.05.2025

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1. Aim of the Laboratory

- Understanding of digital system synthesis.
- FPGA design as a target HW.

2. Assignment definition

In this laboratory you will have to synthesize a Synchronous Digital System based on ***LAB1 assignment*** for the Cyclone II FPGA with impact on performance and logic usage.

Performance Test Case

In this test case, you must test the performance, area, and functionality of a **digital system**. Generally, Quartus is used to evaluate design timing (as explained in detail in the guidance files on Moodle). To perform timing analysis on a digital system, the design must contain registers that confine the logic paths (explained in guidance files).

Note: in synchronous digital system this requirement is obeyed inherently.

In case of pure logic design (for example as ALU), to perform timing analysis, we need to confine the DUT between two synchronous registers (DFF based) operating from the same clock as described in the diagram below to estimate performance.

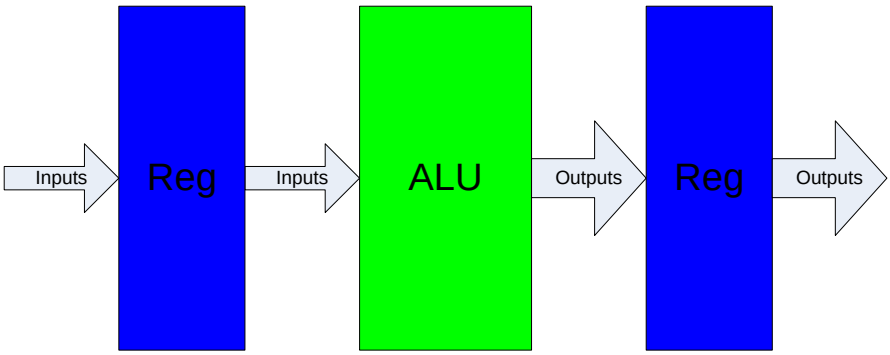


Figure 1 : Test Case in case of pure logic system as ALU

You must do the following tasks:

- ModelSim Simulation with maximal coverage (done in LAB1 assignment).
- Quartus Compilation **without** pin assignments and design loading to check the design synthesis performance.
- Find the maximal operating clock f_{max} , set the clock to constrain the possible maximum value.
- Analyze the logic usage (***based on the compilation report***).
- Analyze the critical path and its location in system. Show the longest (critical) and the shortest paths and explain why.
- Find the frequency limiting operation and explain why it is happening.

The following must be presented in the report:

- RTL Viewer results ***for each logic block*** (of the level underneath top).
- Logic usage for each block (Combinational and Flip-Flops) based on Logic usage report from Quartus II.
- Critical path for each logic block and overall system critical path.
- Optimizations that you have done on the code for the FPGA.

Hardware Test Case

In the hardware test case, you will have to test an **ALU digital system** onto D10-Standard FPGA board.

- Board ***ten*** switches (SW9-SW0) and push ***four*** debounced pushbuttons (KEY3-KEY0) will be used as ***Input interface***.
- Board ***ten*** red LEDs (LEDR9-LEDR0) and ***six*** 7-segment displays (HEX5-HEX0) used as ***Output interface***.
- Connections between the 2x20 GPIO Expansion Header and Cyclone V SoC FPGA

Figure 2a: I/O interface of the DE10-Standard FPGA board

Figure 2b: I/O interface of the DE2-115 FPGA board

Figure 2 : I/O interface of the DE10-Standard and the DE2-115 FPGA boards

The digital system is composed of two concurrent parts, combinatorial and synchronous, as shown in Figures 3 and 4.

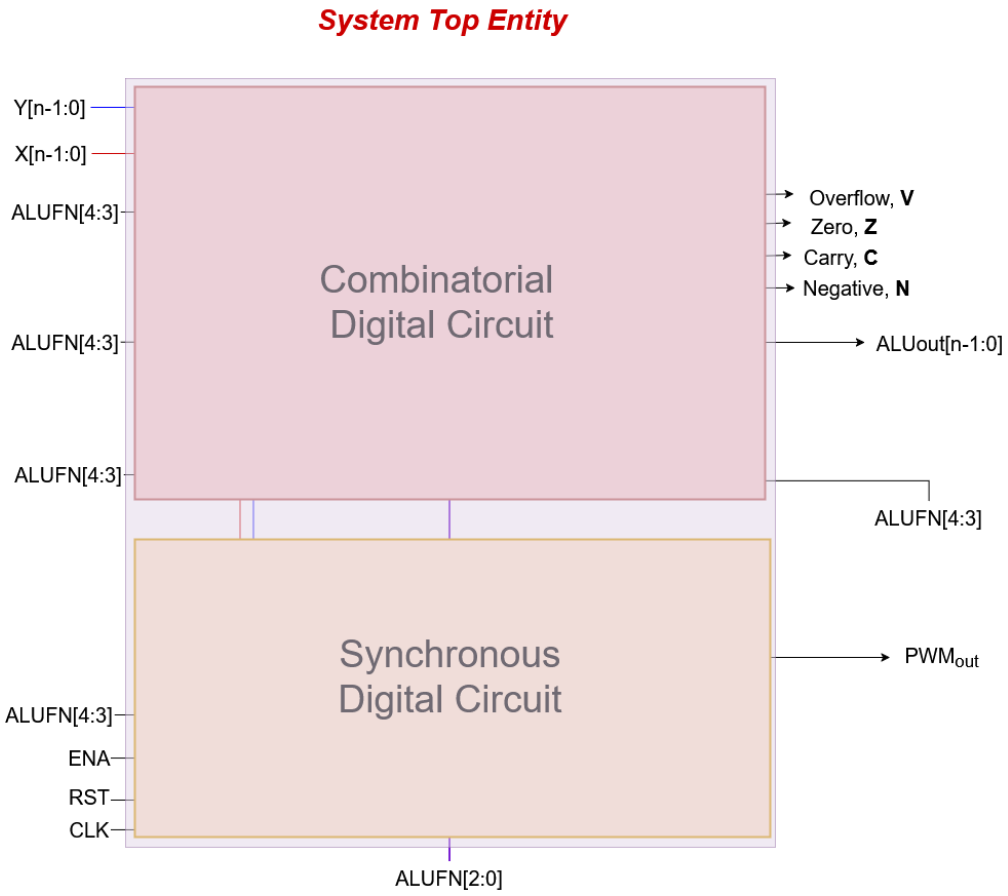


Figure 3: Digital System subparts

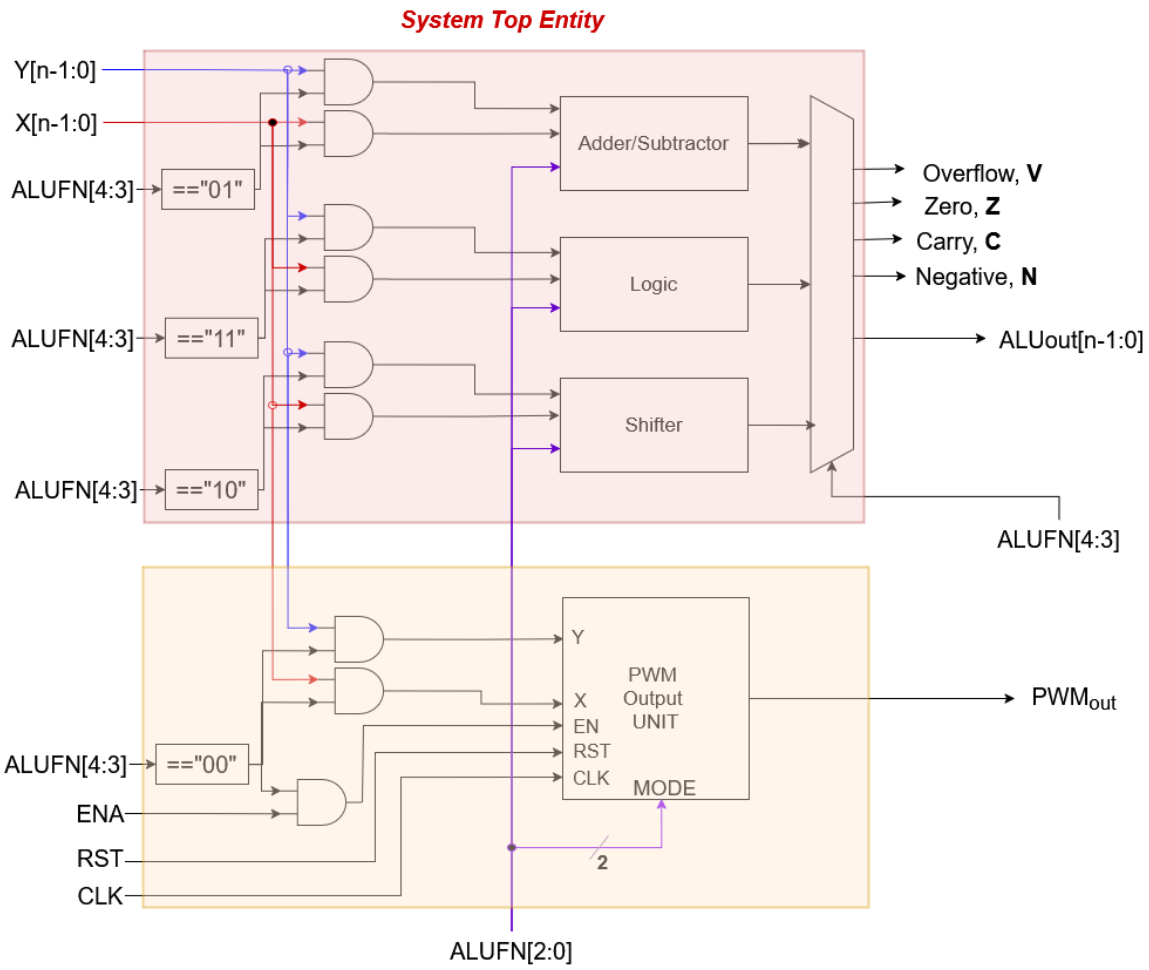


Figure 4: Digital System subparts architecture

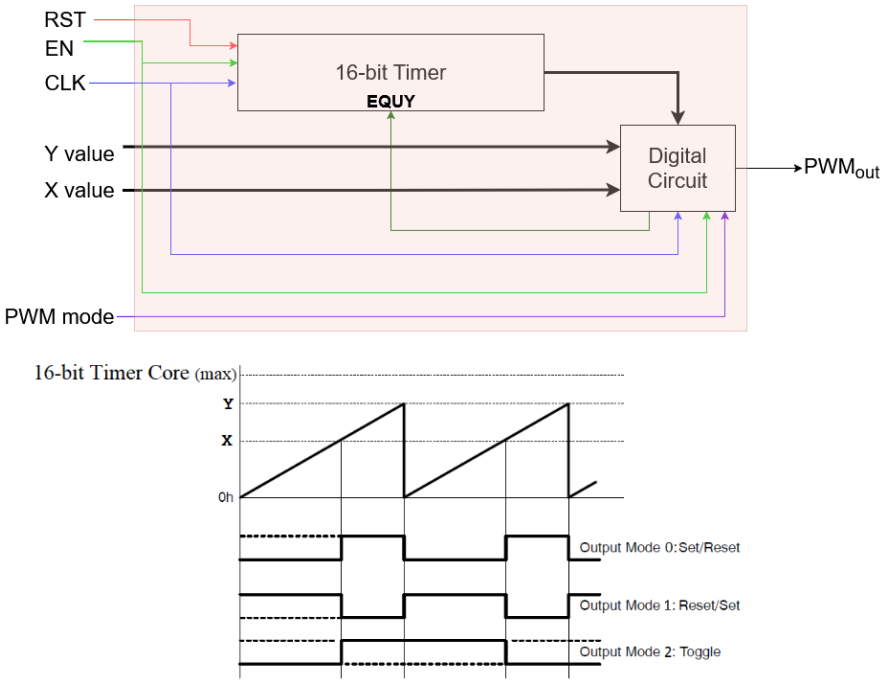
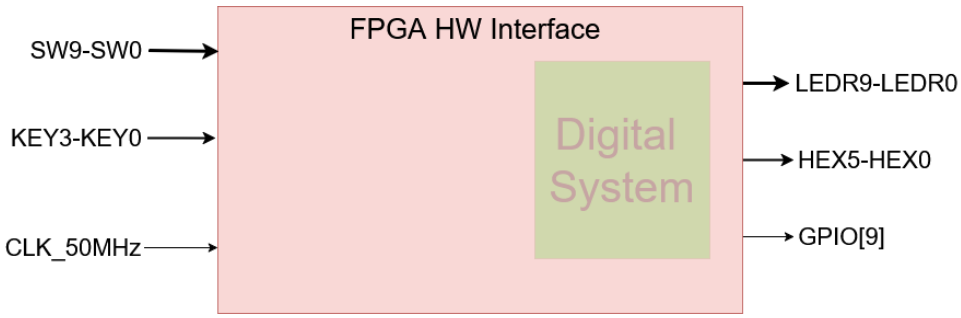


Figure 5: PWM output unit architecture

The whole system must be connected to the Altera board interfaces according to the following diagram:



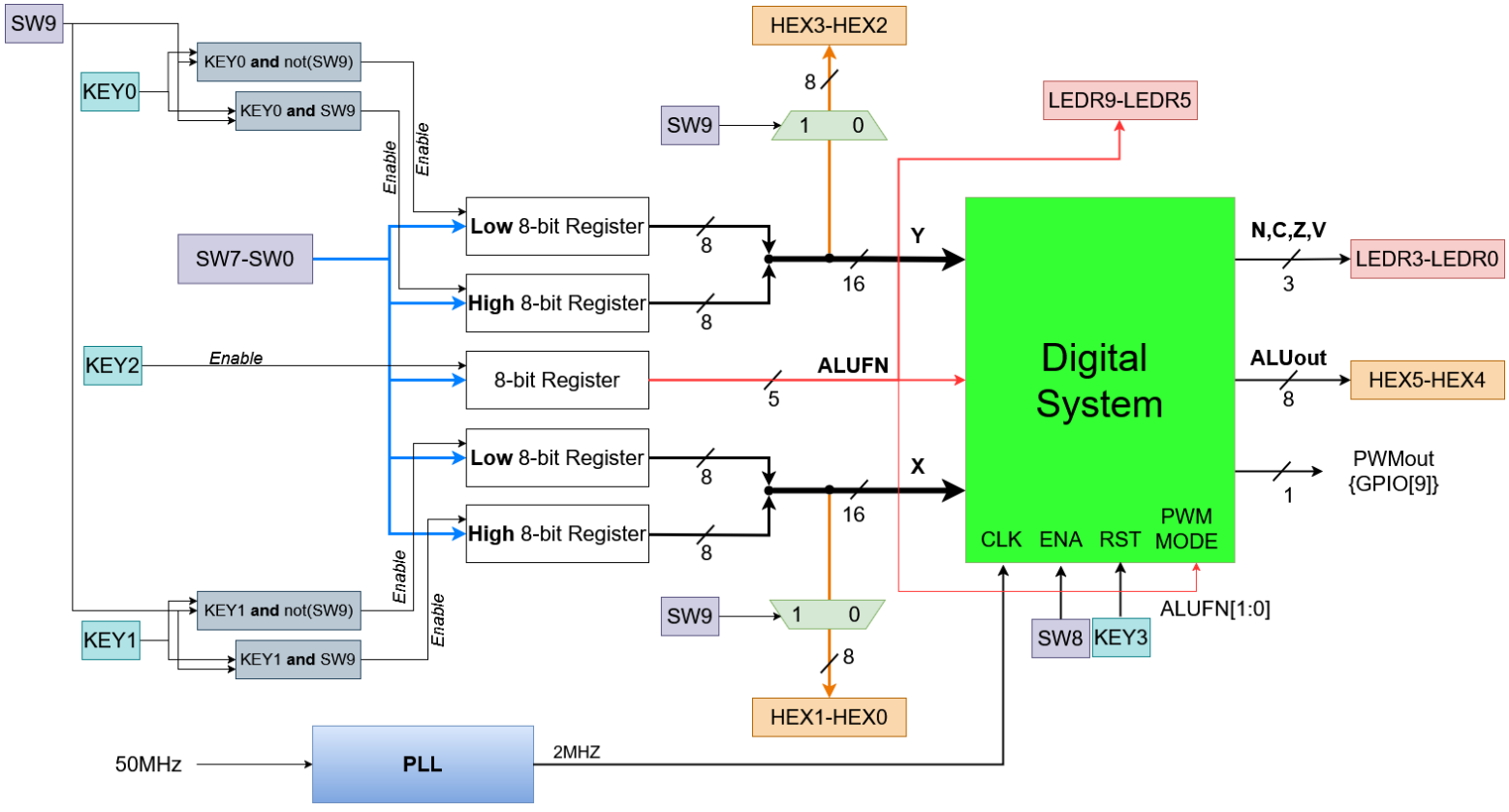


Figure 6: Digital system with I/O interface

The ISA of the combinatorial subpart is given in Figure 7, which is associated with the LAB1 task.

Function Type	Decimal value	ALUFN	Operation	Note
PWM Output (*Y and X are 16-bit width*)	0	**00**000	PWM MODE0	PWM Mode is Set/Reset
	1	**00**001	PWM MODE1	PWM Mode is Reset/Set
	2	**00**010	PWM MODE2	PWM Mode is Toggle
Arithmetic (*Y and X are 8-bit width*)	8	**01**000	Res=Y+X	
	9	**01**001	Res=Y-X	Used also for comparison operation
	10	**01**010	Res=neg(X)	
	11	**01**011	Res=Y+1	Increment of Y in one
	12	**01**100	Res=Y-1	Decrement of Y in one
	13	**01**101	Res=swap(Y)	Res=(Y_{LSHW}, Y_{MSHW})
Shift (*Y and X are 8-bit width*)	16	**10**000	Res=SHL Y,X(k-1 to 0)	Shift Left Y of q≙X(k-1 ..0) times Res=Y(n-1-q…0)#(q@0) ***When*** $k = log_2 n$
	17	**10**001	Res=SHR Y,X(k-1 to 0)	Shift Right Y of q≙X(k-1 ..0) times Res=(q@0)#Y(n-1...q) ***When*** $k = log_2 n$
Boolean (*Y and X are 8-bit width*)	24	**11**000	Res=not(Y)	
	25	**11**001	Res=Y or X	
	26	**11**010	Res=Y and X	
	27	**11**011	Res=Y xor X	
	28	**11**100	Res=Y nor X	
	29	**11**101	Res=Y nand X	
	30	**11**110	Res=Y xnor X	

Figure 7: ISA of the combinatorial subpart of digital design

3. Requirements

1. The report file (LAB4.pdf) content should include page numbers.
2. Images and tables will be numbered. The caption of an image and a table below the image or table. The top-level design must be structural; all other modules can be structural/ behavioral or mixed modeling (structural and behavioral).
3. The behavioral parts of the design (except the test bench) must be synthesized, pay attention to the logic that you are describing.
4. Block diagrams for the behavioral parts of the design that describe the logic behind the behavioral code can be taken from Quartus RTL Viewer
5. The design must be well commented.
6. Elaborated analysis and waveforms:
    - Remove irrelevant signals.
    - Zoom in on regions of interest.
    - Draw clouds on the waveform with explanations of what is happening.
    - Change the waveform colors in ModelSim for clear documentation (*Tools->Edit Preferences->Wave Windows*).
    - Resource Usage from Quartus.
    - **Maximal Frequency and critical paths *of the DUT design* from the Timing Analyzer (for each subpart, in addition to the whole digital system design)**
    - **Proof of work using Signal Tap is mandatory**.
7. Conclusions
8. A ZIP file in the form of **id1_id2.zip** (where id1 and id2 are the identification number of the submitters, and id1 < id2) *must be upload to Moodle only by student with id1* (any of these rule's violation disqualifies the task submission).
9. The **ZIP** file will contain the next five subdirectories (***only the exact next sub folders***):

Directory	Contains	Comments
VHDL	Project VHDL files	Only VHDL files, excluding test bench **Note: your project files must be well compiled (in ModelSim and Quartus separately) without errors as a basic condition before submission**
TB	VHDL files that are used for test bench	Only one **tb.vhd** for the overall DUT
SIM	ModelSim DO files	Only for **tb.vhd** of the overall DUT
DOC	Project documentation	**Readme.txt** and **Lab4.pdf** report file
Quartus	• Signal Tap files used in project verification (for one Arithmetic and one Shift operations) • Project SOF file • Project SDC file	Do not place files that are not relevant for compilation or is a result of compilation

Table 1: Directory Structure

4. Grading Policy

Weight	Task	Description
10%	Documentation	The "clear" way in which you presented the requirements and the analysis and conclusions on the work you have done.
90%	Analysis and Test	The correct analysis of the system (under the requirements)

Table 1 : Grading

Under the above policy, you will be also evaluated using common sense:

- Your files will be compiled and checked; the system must work.
- Your design and architecture must be intelligent, minimal, effective and well organized.

5. References

[1] Altera Cyclone II data book on http://www.altera.com./literature/lit-cyc2.jsp
[2] Quartus II manuals : http://www.altera.com/support/software/sof-quartus.html
[3] DE1 User Manual on http://hl2.bgu.ac.il – Course Library=>FPGA
[4] Cyclone II Technical information http://www.altera.com./literature/lit-cyc2.jsp