UNIVERSITY OF JORDAN

Computer Engineering Department

Digital Electronics Laboratory Project

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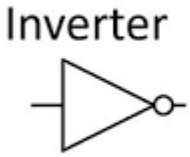
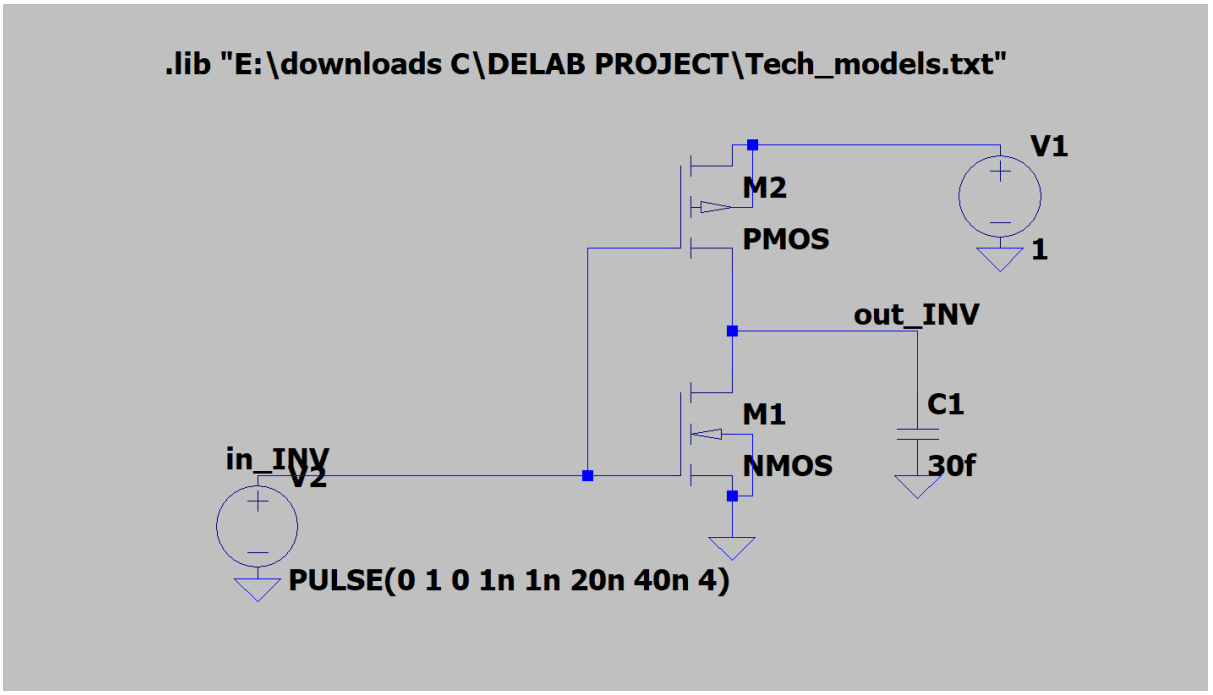
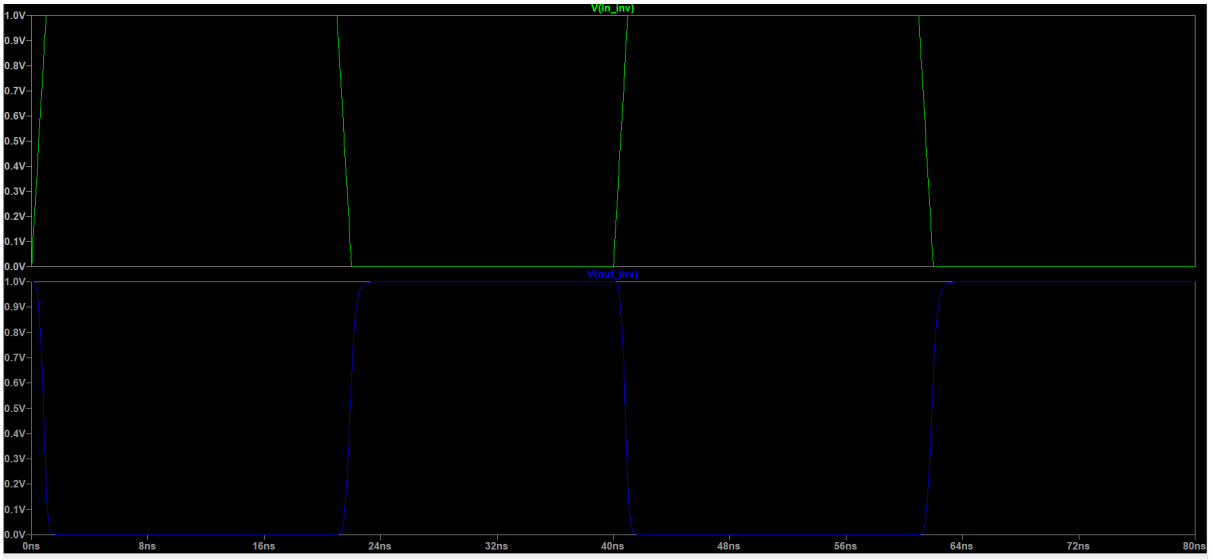
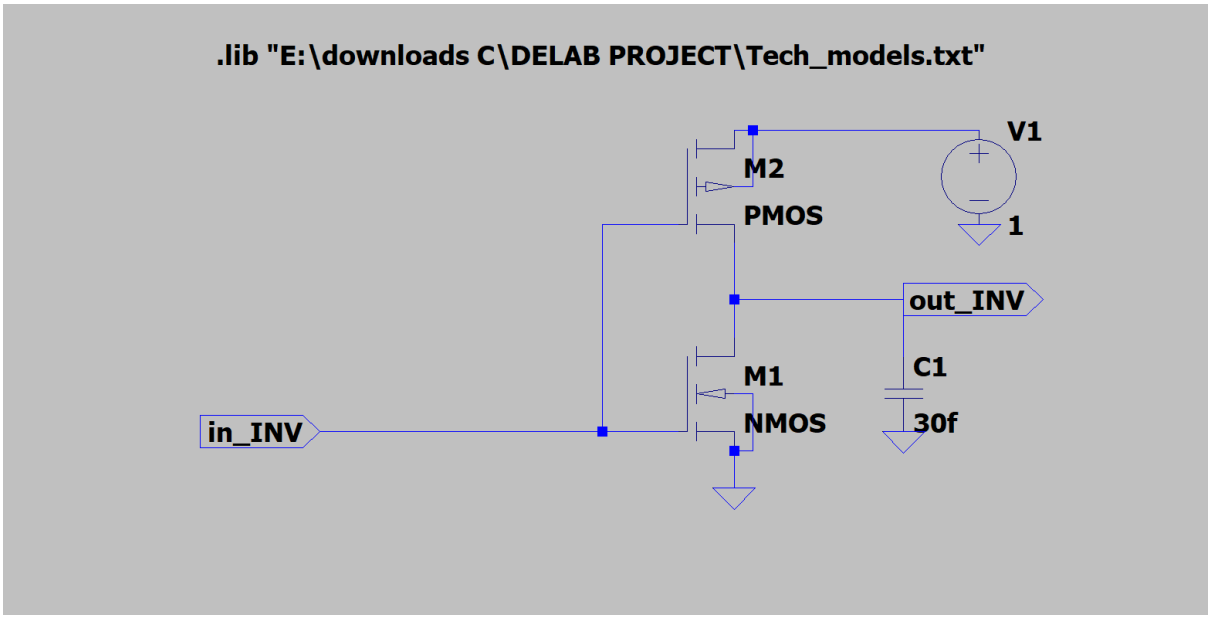
Inverter Gate:

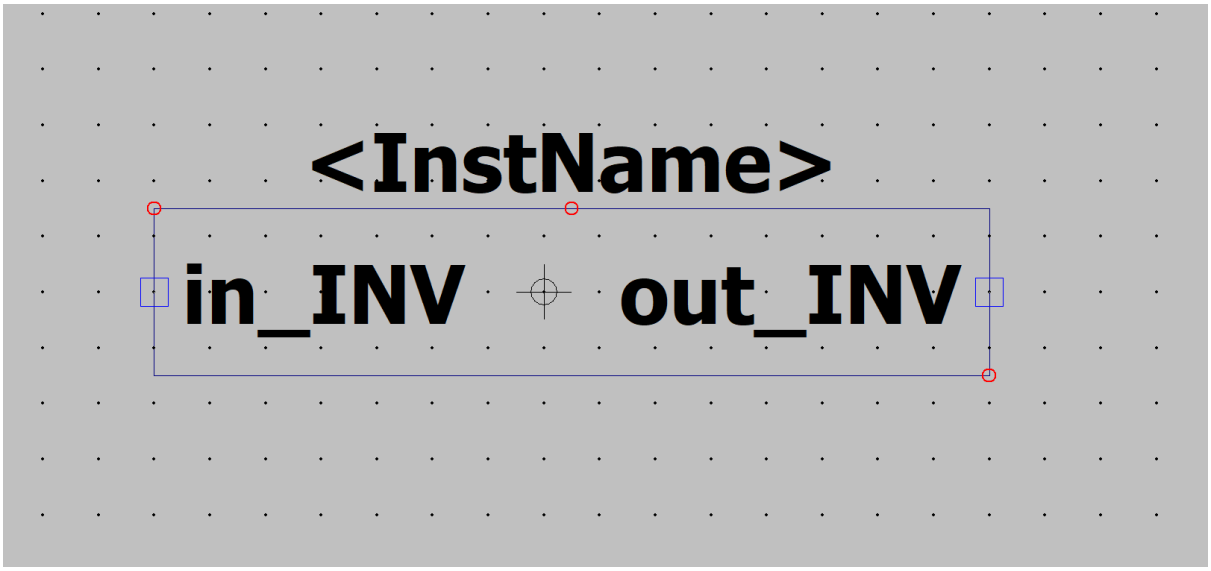


Input	Output
0	1
1	0



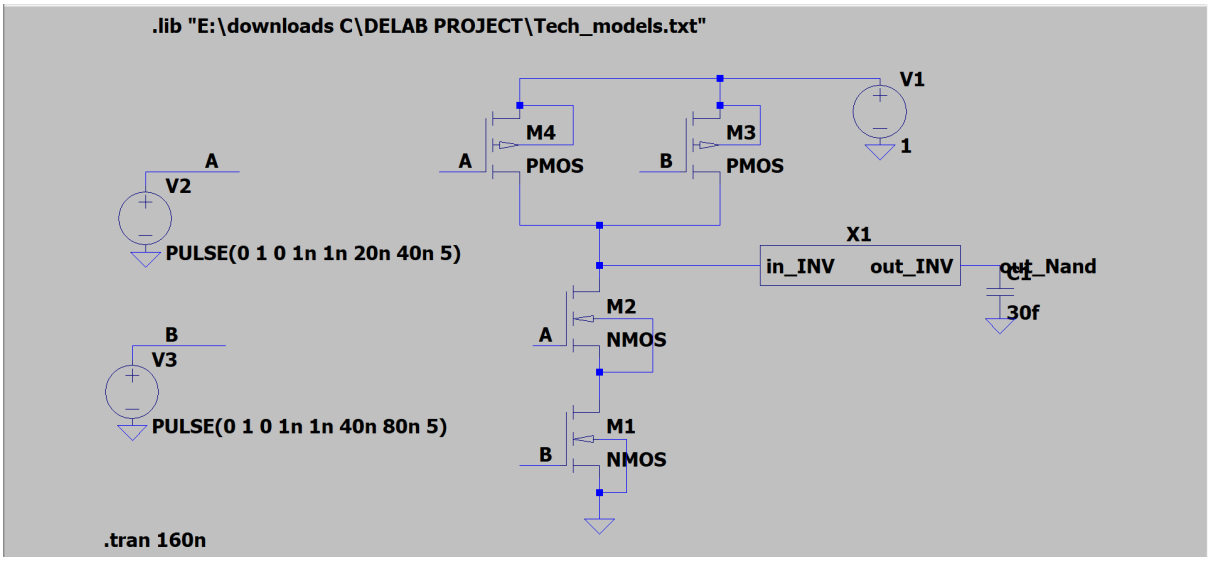


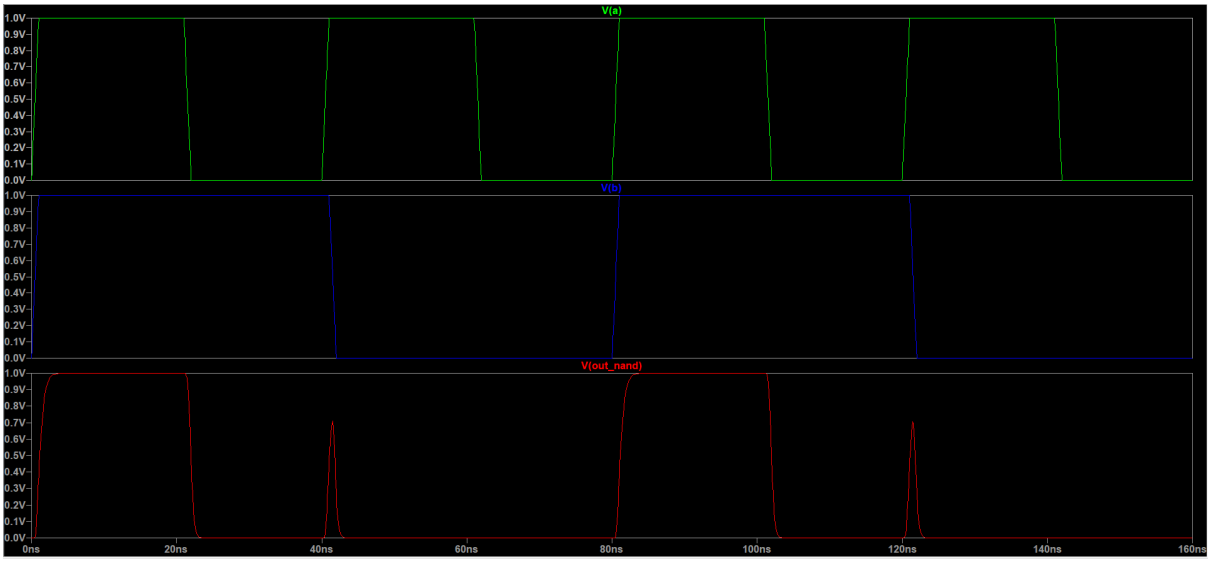

.lib "E:\downloads C\DELAB PROJECT\Tech_models.txt"
V1
M2
PMOS
1
out_INV
C1
M1
NMOS
30f
in_INV

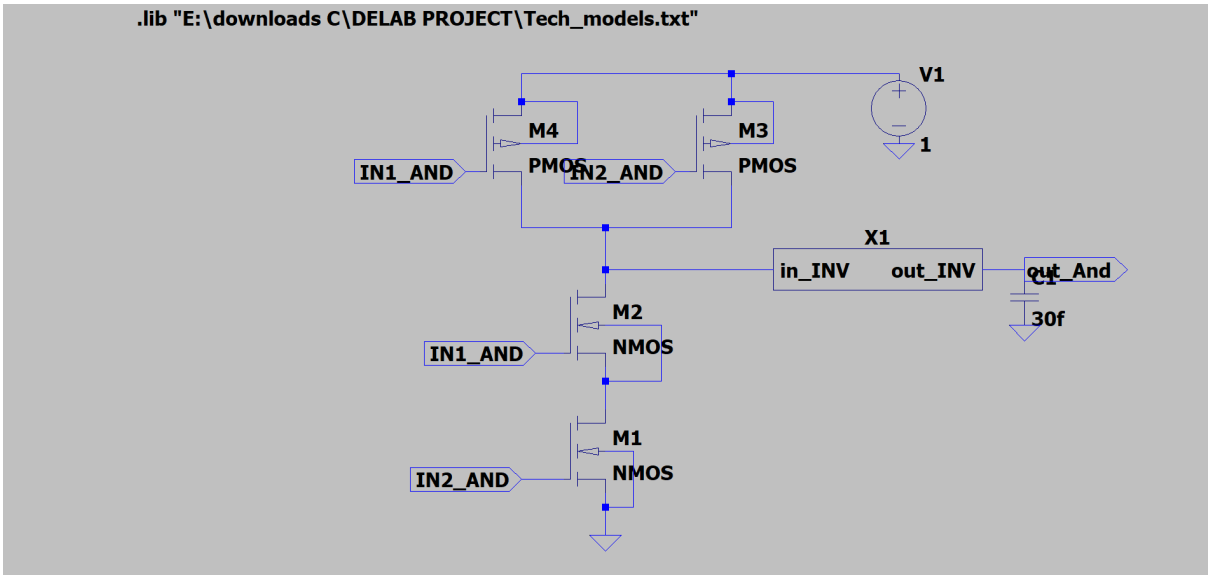

<InstName>
in_INV
out_INV

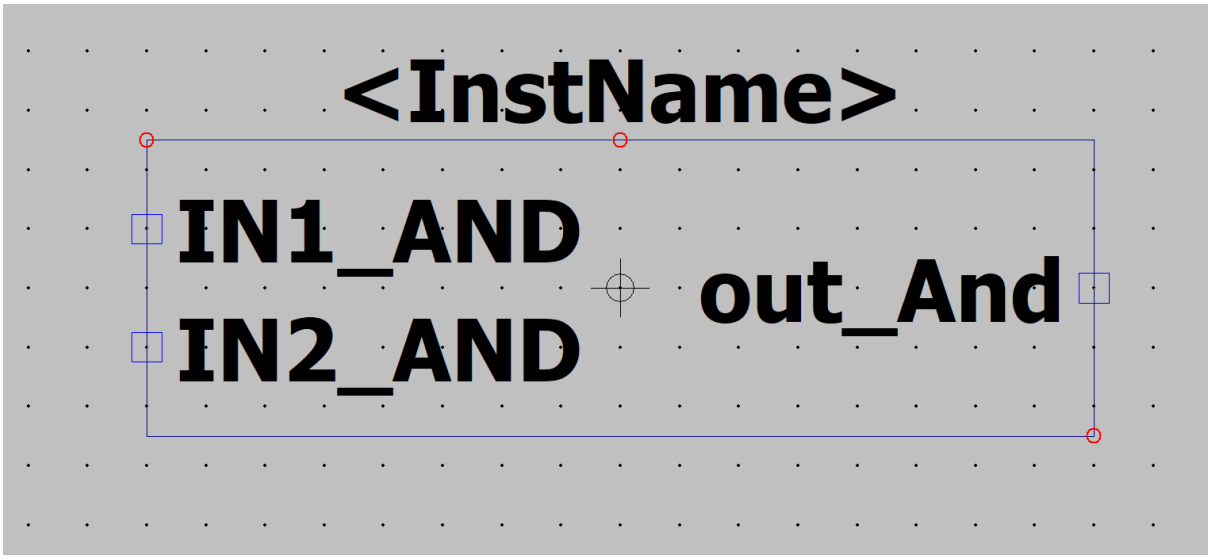
AND Gate:

Symbol	Truth Table		
	A	B	Q
	0	0	0
	0	1	0
	1	0	0
	1	1	1
Boolean Expression Q = A. B, A AND B			

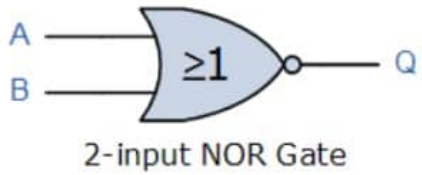


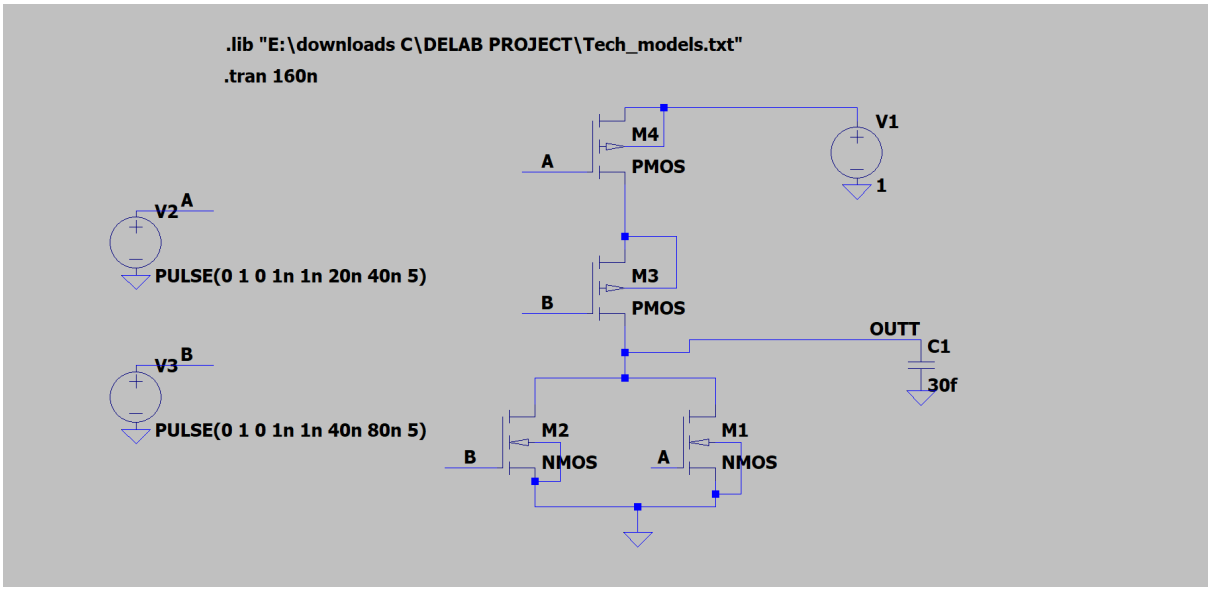


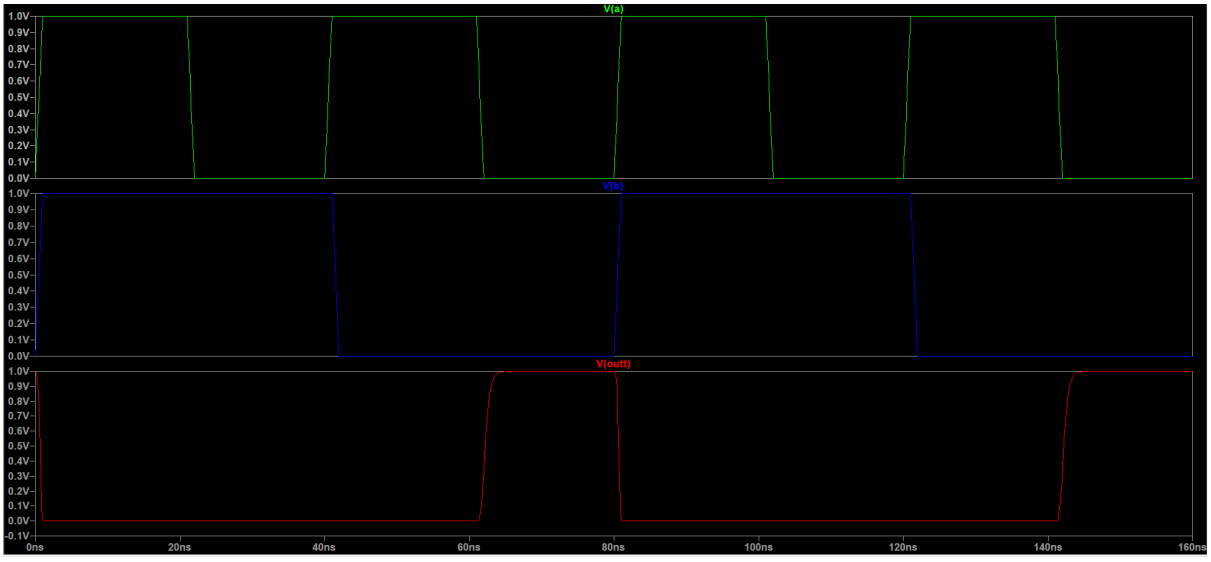

.lib "E:\downloads C\DELAB PROJECT\Tech_models.txt"
V1
1
M4
PMOS
M3
PMOS
IN1_AND
IN2_AND
X1
in_INV
out_INV
out_And
C1
30f
M2
NMOS
IN1_AND
M1
NMOS
IN2_AND

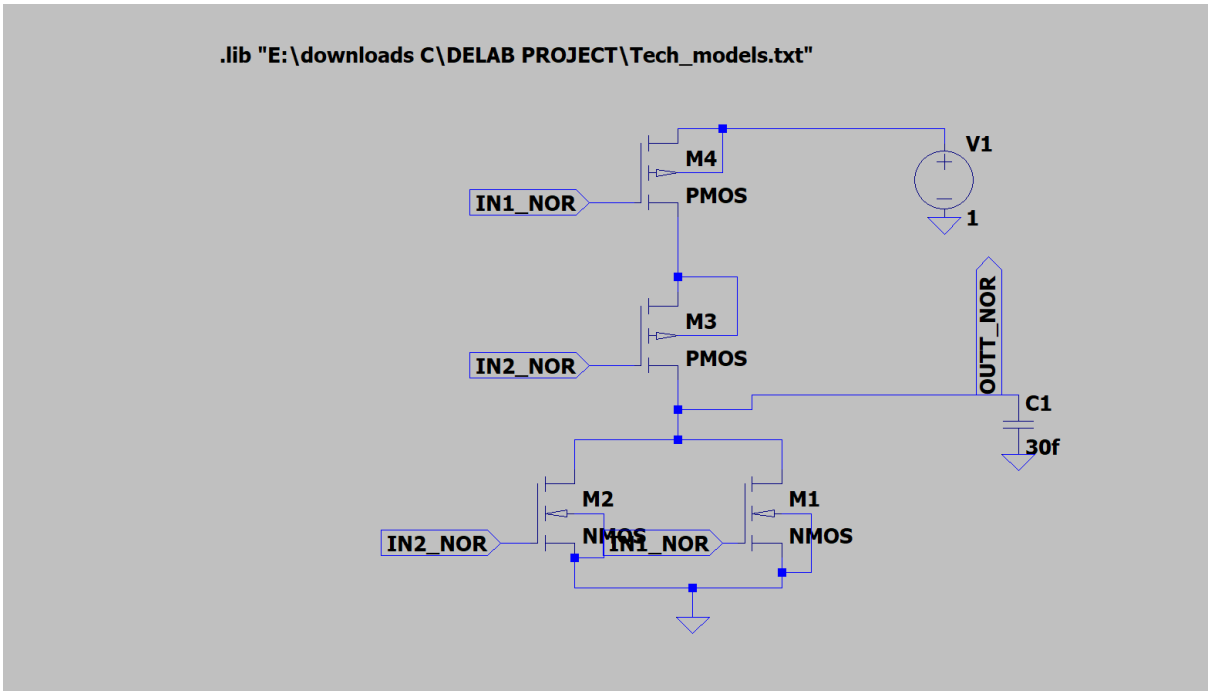

<InstName>
IN1_AND
IN2_AND
out_And

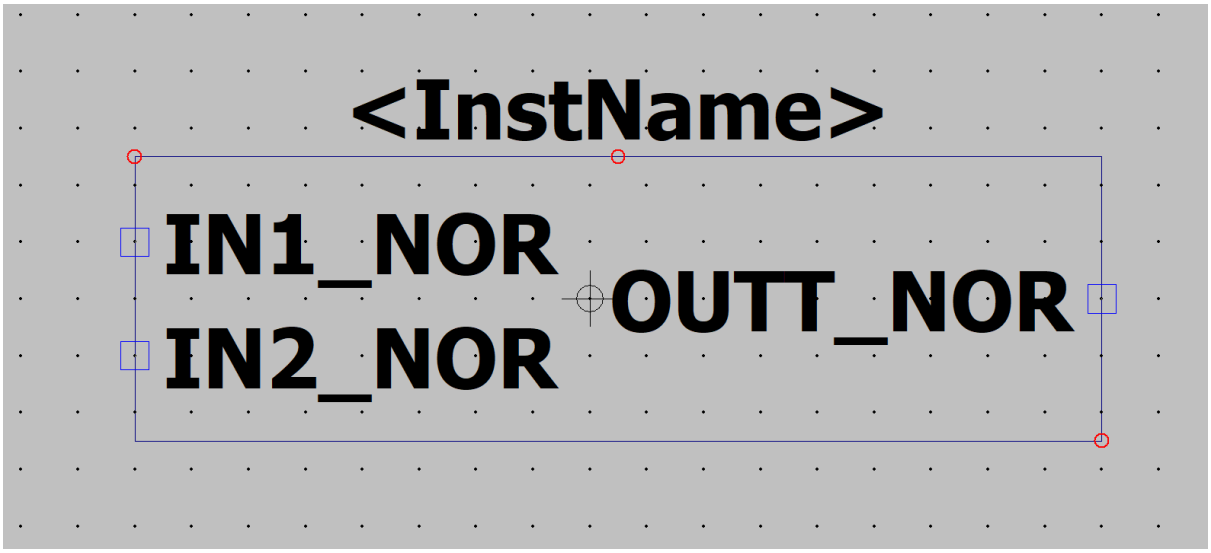
NOR Gate:

Symbol	Truth Table		
 2-input NOR Gate	A	B	Q
	0	0	1
	0	1	0
	1	0	0
	1	1	0
Boolean Expression Q = A NOR B			



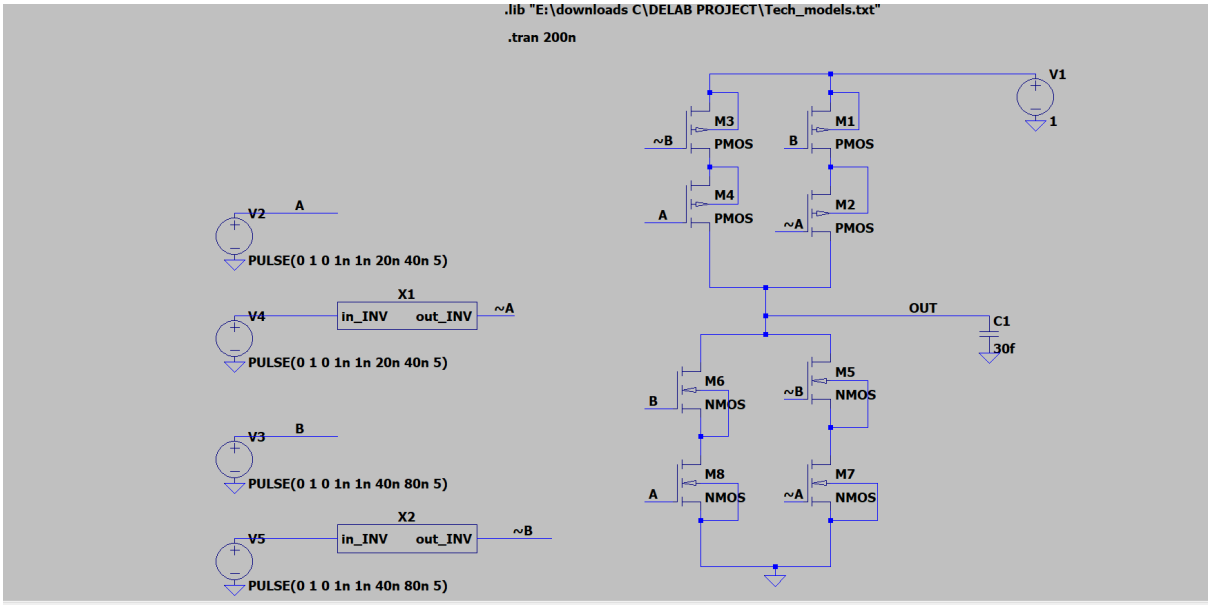


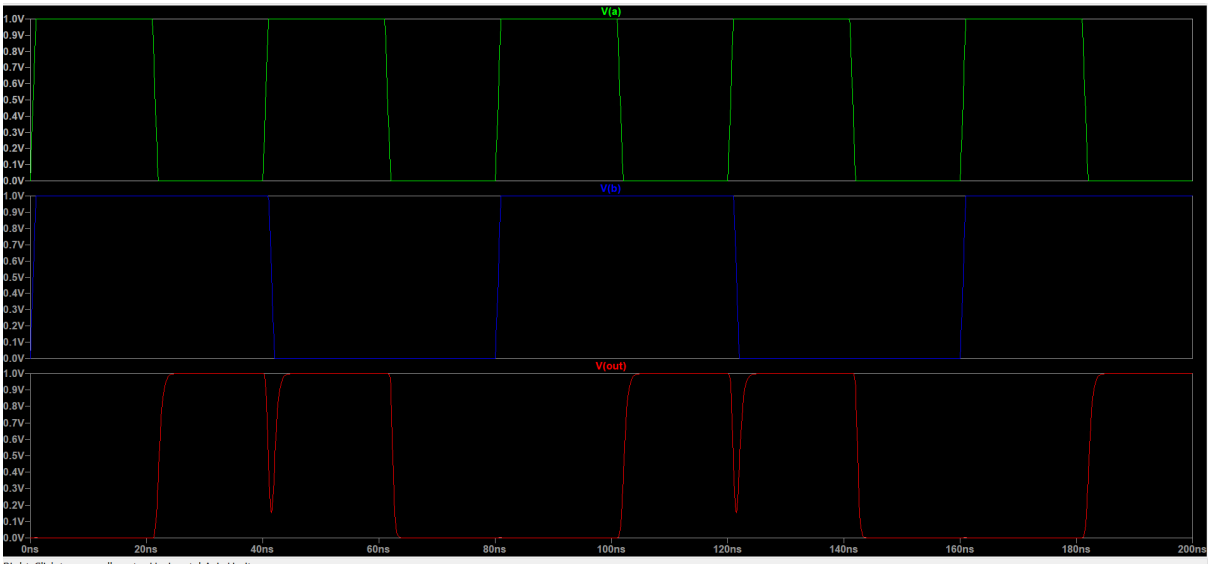

.lib "E:\downloads C\DELAB PROJECT\Tech_models.txt"
M4
PMOS
IN1_NOR
V1
1
M3
PMOS
IN2_NOR
OUTT_NOR
C1
30f
M2
NMOS
IN2_NOR
M1
NMOS
IN1_NOR

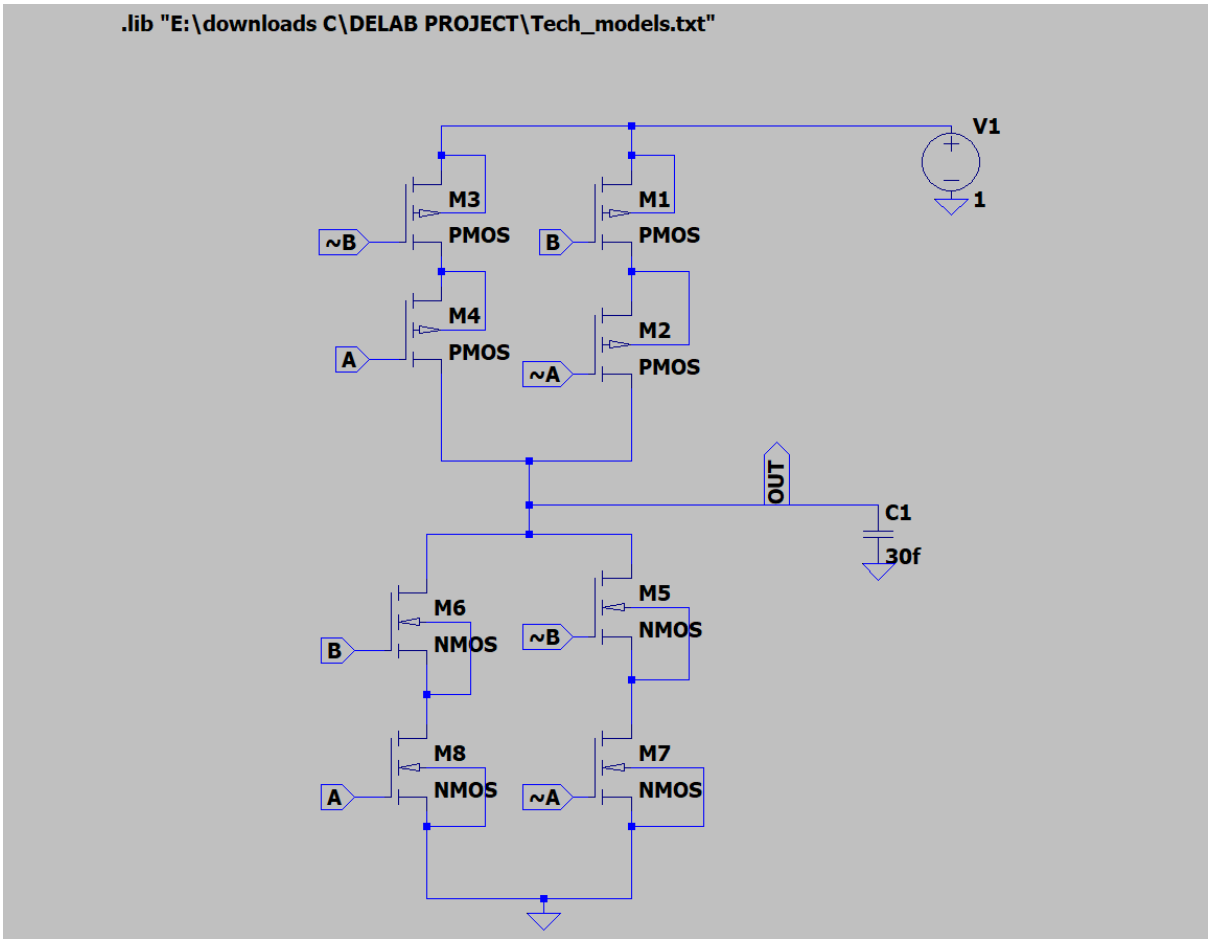

<InstName>
IN1_NOR
IN2_NOR
OUTT_NOR

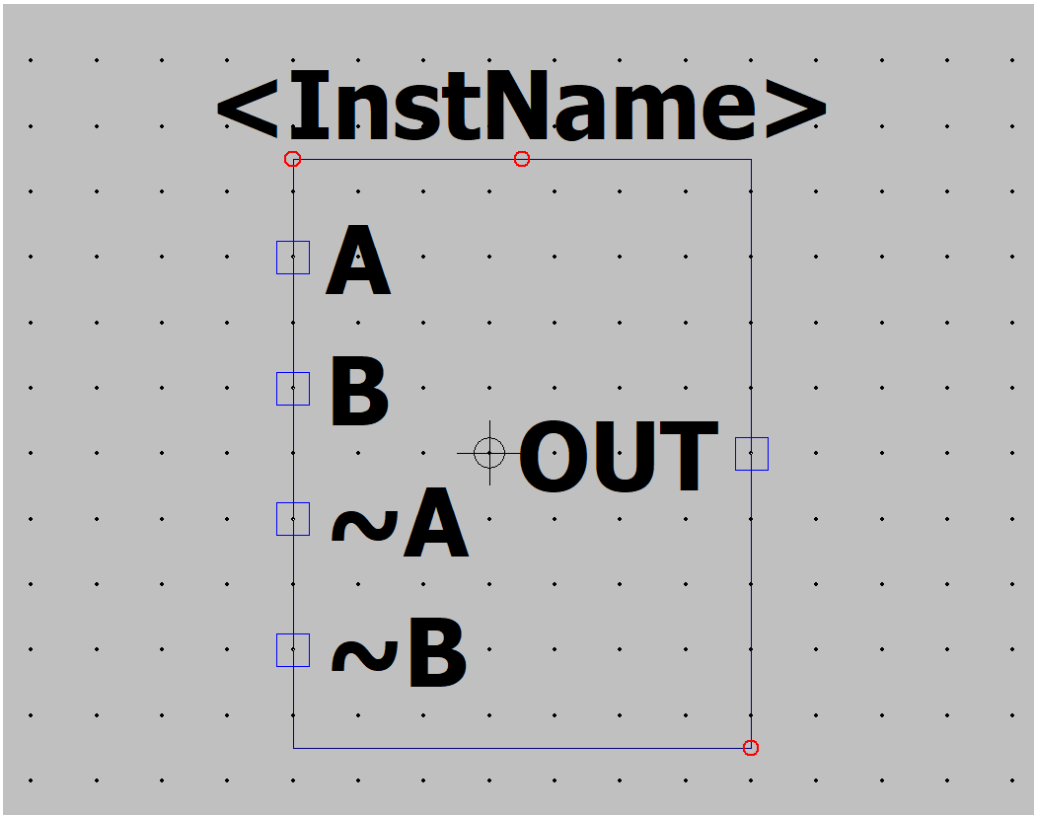
XOR Gate:

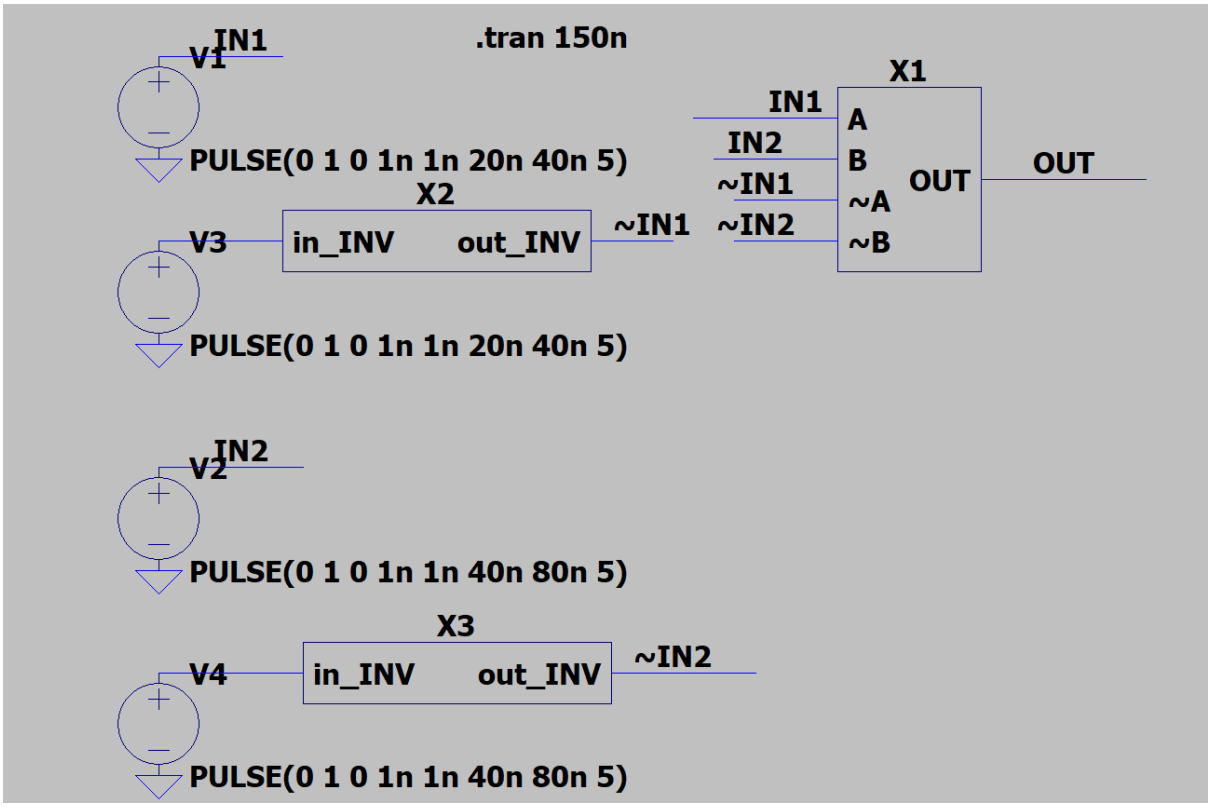
Symbol	Truth Table		
	A	B	Q
	0	0	0
	0	1	1
	1	0	1
	1	1	0
Boolean Expression Q = A XOR B			

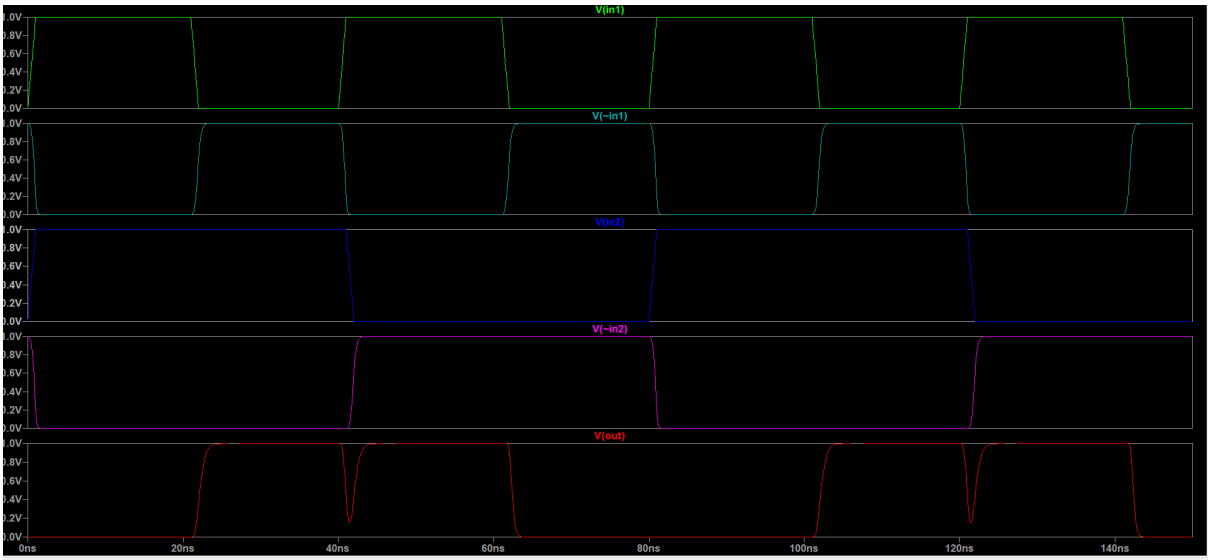




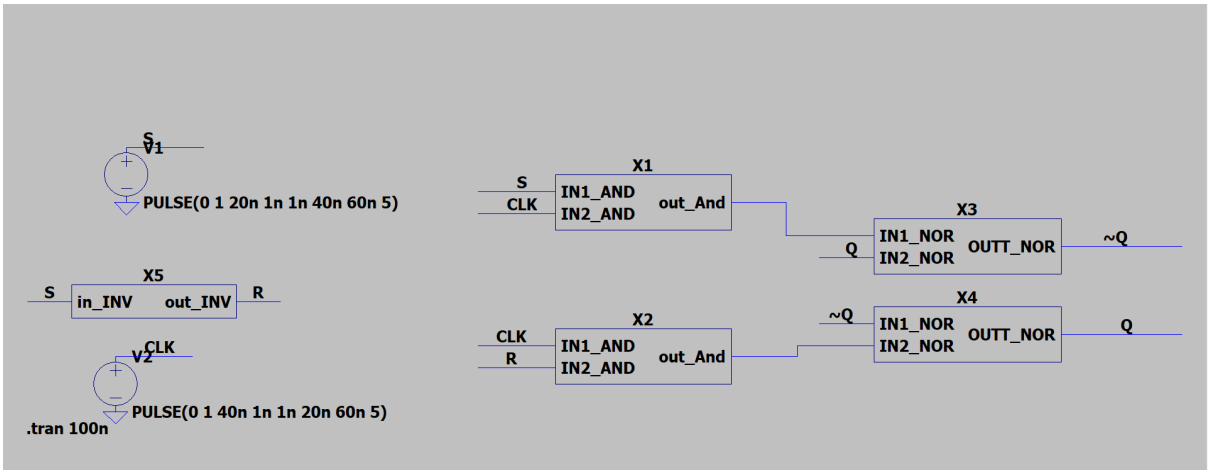

.lib "E:\downloads C\DELAB PROJECT\Tech_models.txt"
V1
1
M3
PMOS
~B
M1
PMOS
B
M4
PMOS
A
M2
PMOS
~A
OUT
C1
30f
M6
NMOS
B
M5
NMOS
~B
M8
NMOS
A
M7
NMOS
~A

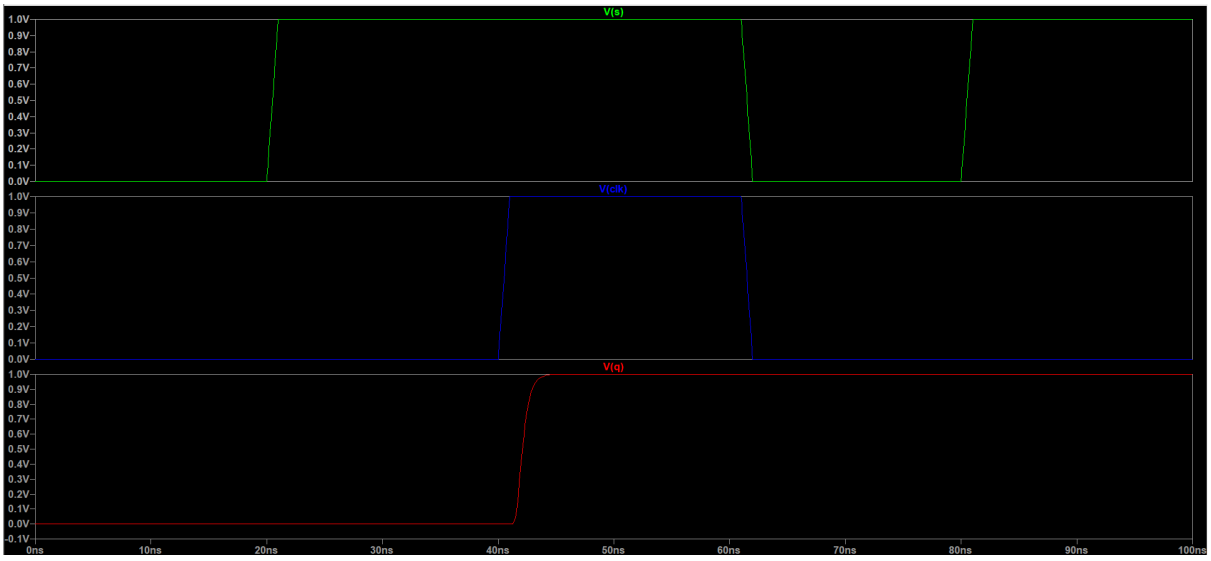

<InstName>
A
B
~A
~B
OUT


IN1
V1
.tran 150n
PULSE(0 1 0 1n 1n 20n 40n 5)
X1
IN1
IN2
~IN1
~IN2
A
B
~A
~B
OUT
OUT
X2
V3
in_INV
out_INV
~IN1
PULSE(0 1 0 1n 1n 20n 40n 5)
IN2
V2
PULSE(0 1 0 1n 1n 40n 80n 5)
X3
V4
in_INV
out_INV
~IN2
PULSE(0 1 0 1n 1n 40n 80n 5)

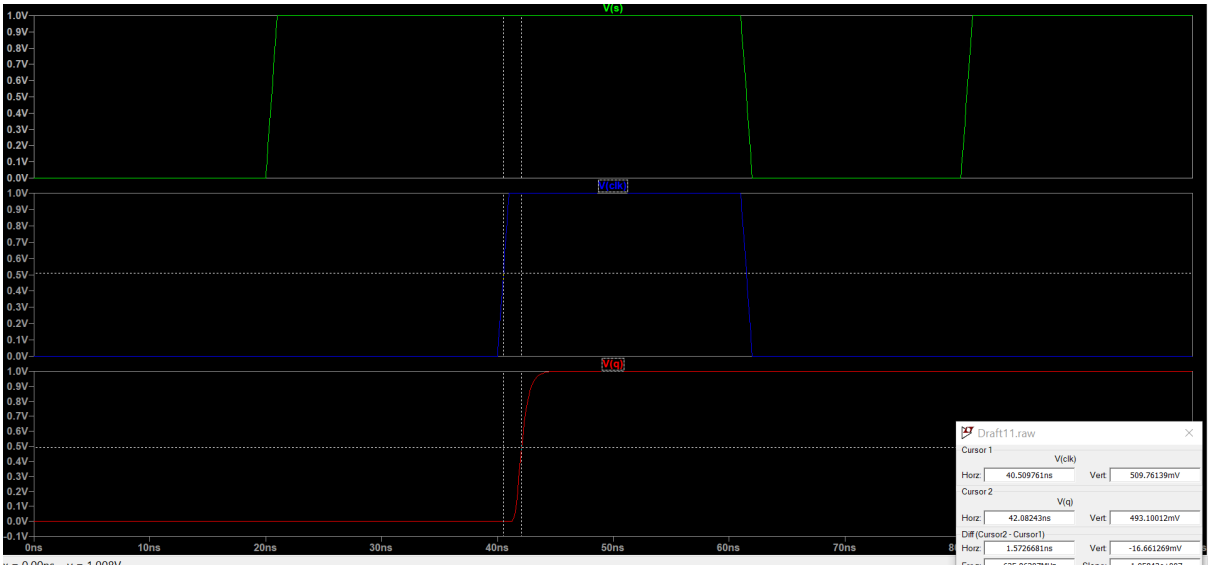

V(in1)
V(~in1)
V(in2)
V(~in2)
V(out)
0ns
20ns
40ns
60ns
80ns
100ns
120ns
140ns

SR LATCH:

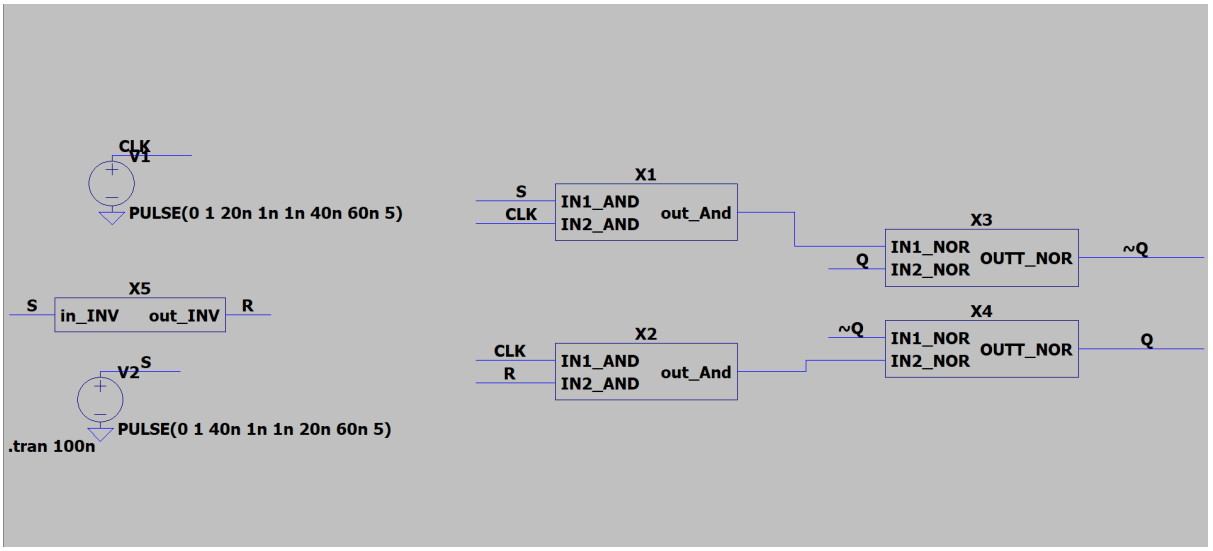


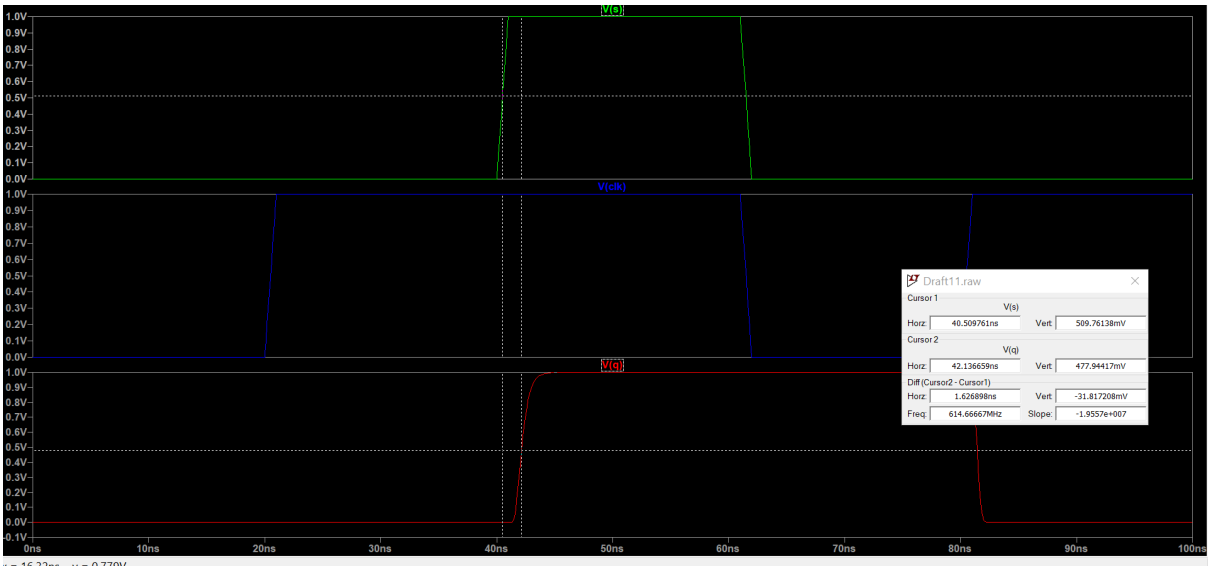


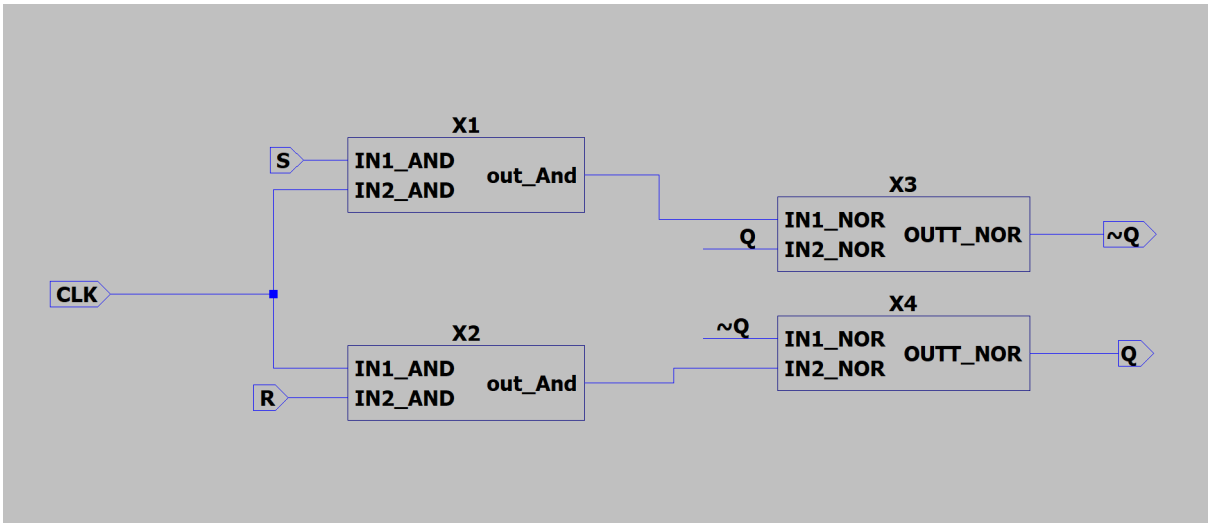
CLK To Q:

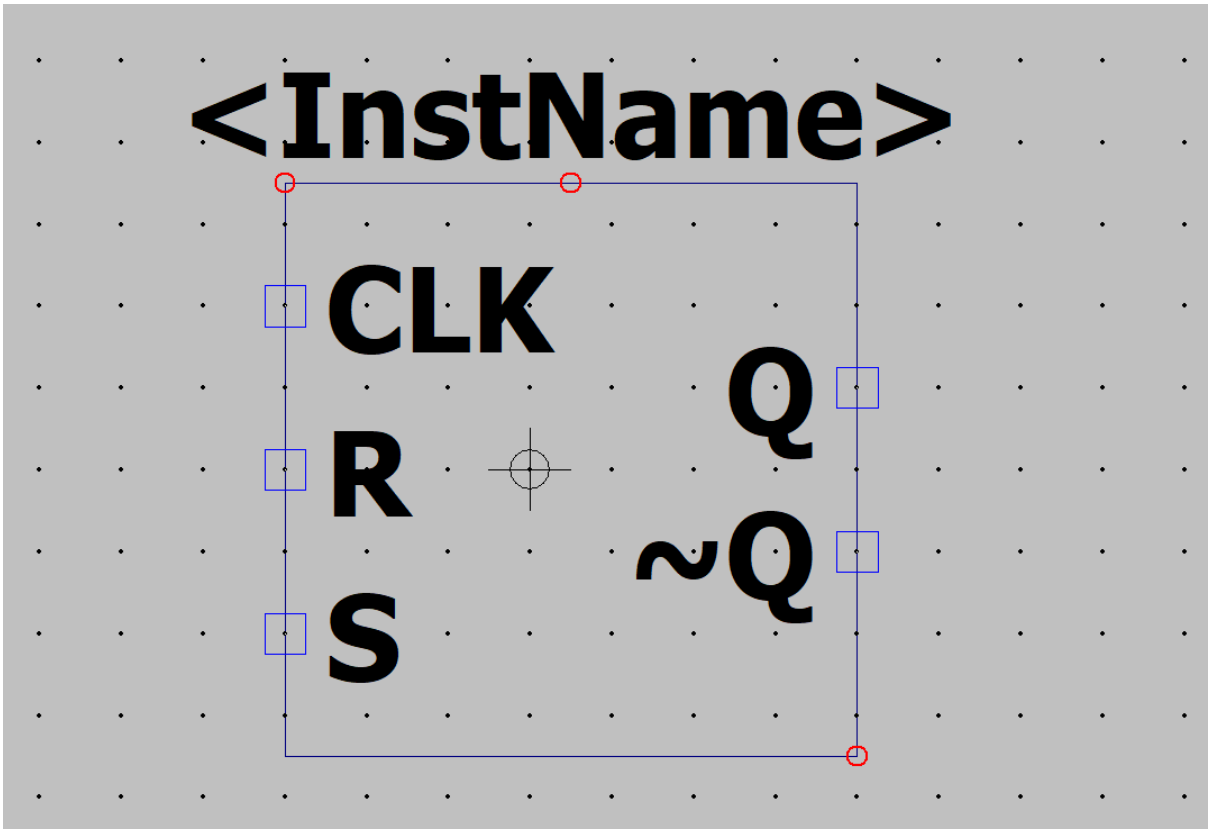


D To Q:

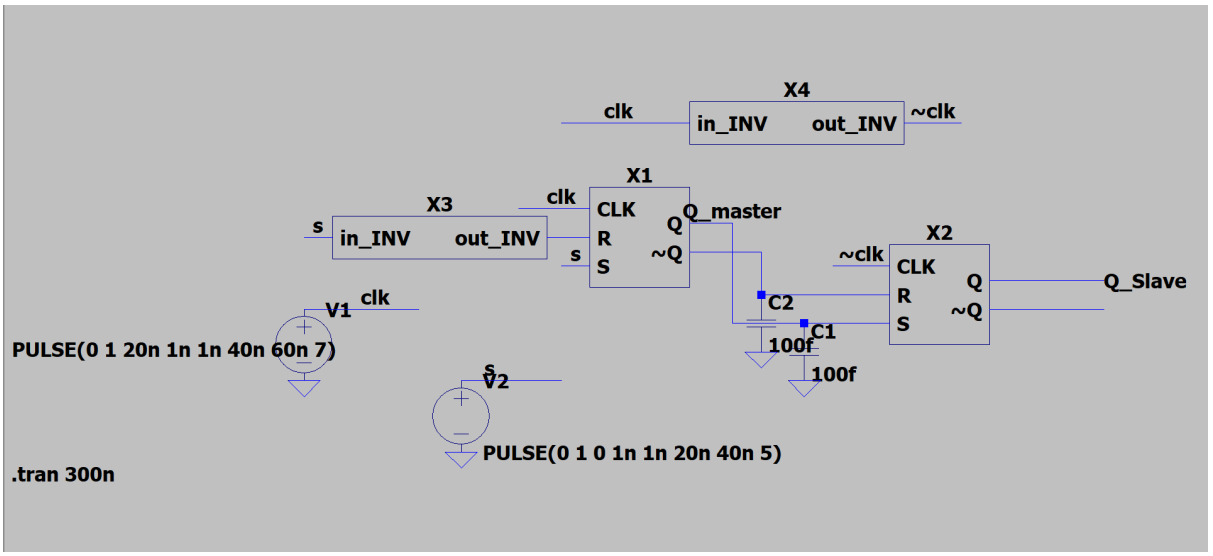

CLK
V1
PULSE(0 1 20n 1n 1n 40n 60n 5)
X1
S
CLK
IN1_AND
IN2_AND
out_And
X3
Q
IN1_NOR
IN2_NOR
OUTT_NOR
~Q
X5
S
in_INV
out_INV
R
X2
CLK
R
IN1_AND
IN2_AND
out_And
~Q
X4
IN1_NOR
IN2_NOR
OUTT_NOR
Q
V2
S
PULSE(0 1 40n 1n 1n 20n 60n 5)
.tran 100n

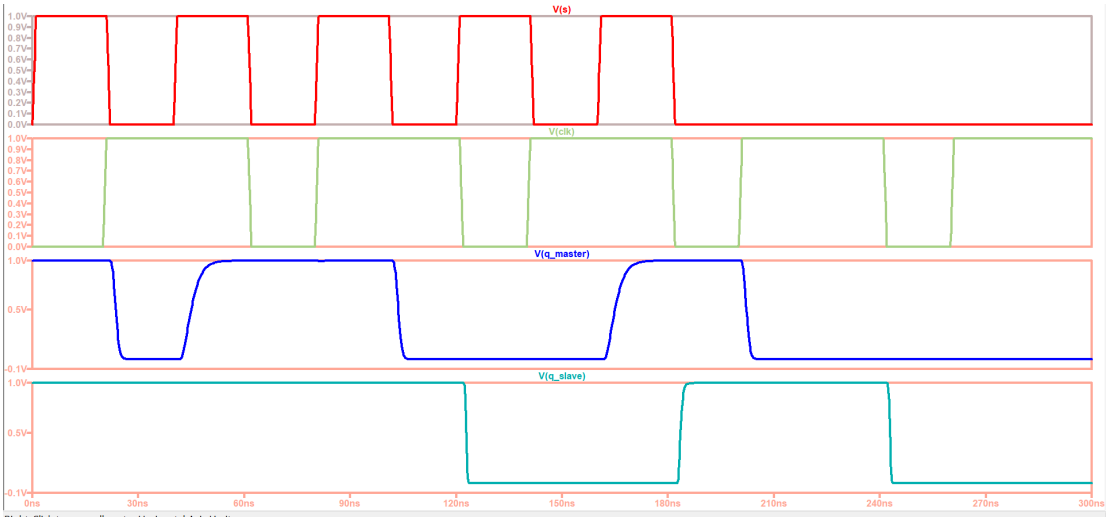

V(q)
V(clk)
V(q)
Draft11.raw
Cursor 1
V(s)
Horz: 40.509761ns
Vert: 509.76138mV
Cursor 2
V(q)
Horz: 42.136659ns
Vert: 477.94417mV
Diff (Cursor2 - Cursor1)
Horz: 1.626898ns
Vert: -31.817208mV
Freq: 614.66667MHz
Slope: -1.9557e+007
0ns
10ns
20ns
30ns
40ns
50ns
60ns
70ns
80ns
90ns
100ns


X1
S
IN1_AND
IN2_AND
out_And
X3
Q
IN1_NOR
IN2_NOR
OUTT_NOR
~Q
CLK
X2
~Q
X4
IN1_NOR
IN2_NOR
OUTT_NOR
Q
R
IN1_AND
IN2_AND
out_And

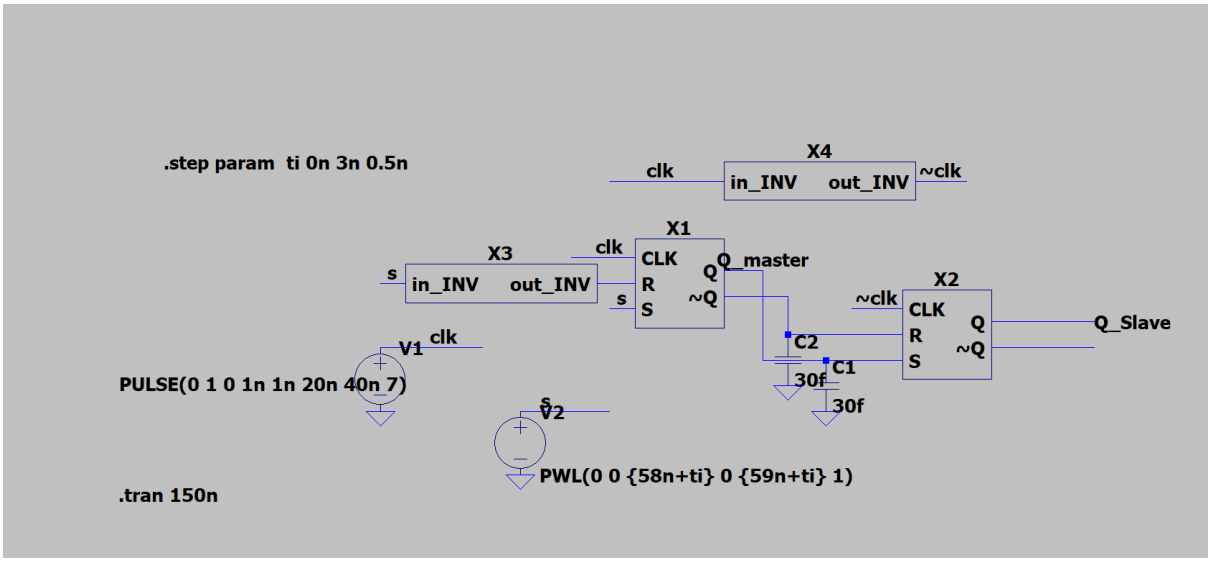

<InstName>
CLK
R
S
Q
~Q

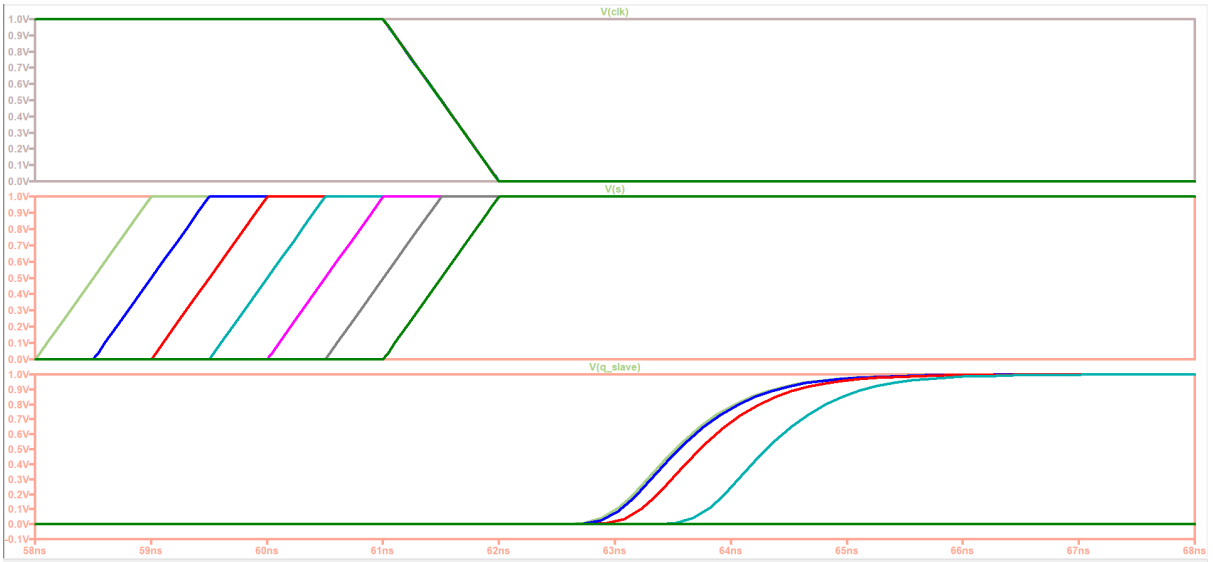
D Flip Flop:


X4
clk
in_INV
out_INV
~clk
X1
X3
clk
s
in_INV
out_INV
CLK
R
S
Q
~Q
Q_master
X2
~clk
CLK
R
S
Q
~Q
Q_Slave
C2
100f
C1
100f
V1
clk
PULSE(0 1 20n 1n 1n 40n 60n 7)
s
V2
PULSE(0 1 0 1n 1n 20n 40n 5)
.tran 300n

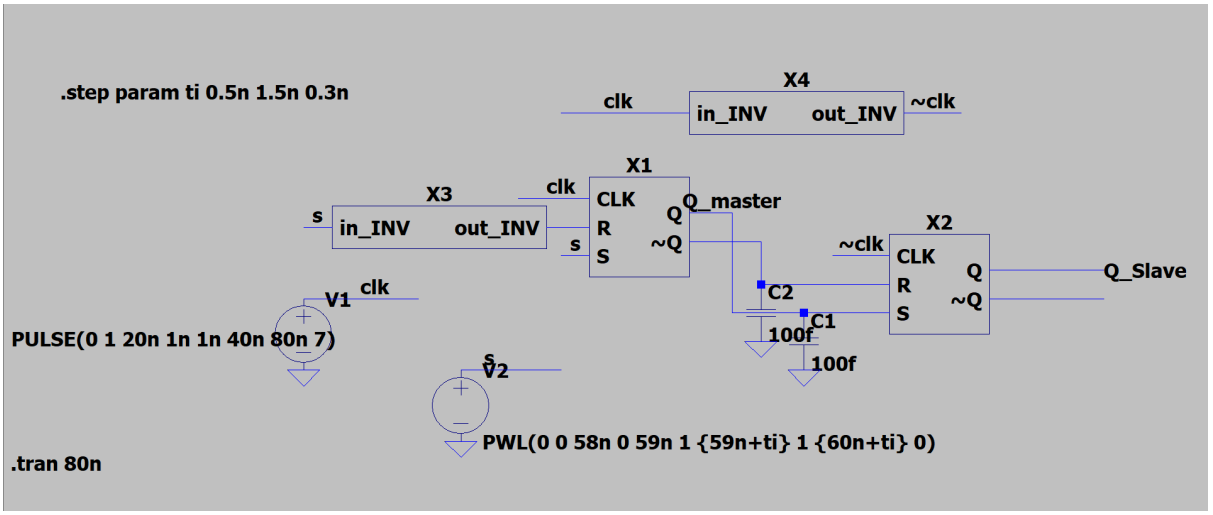


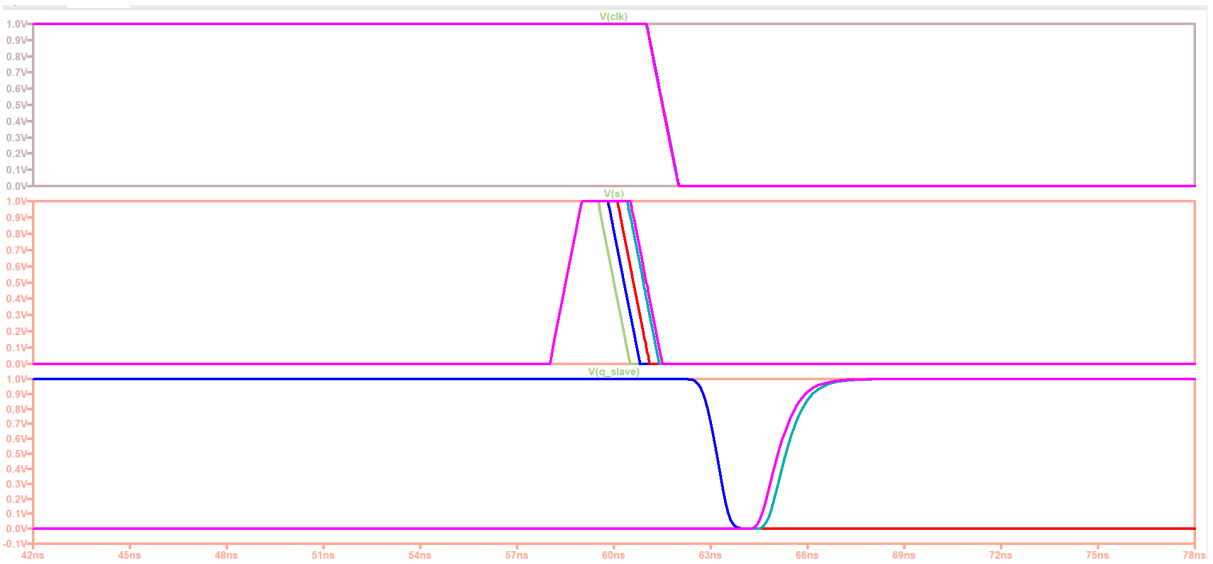
setup time :
the signal should appear befor 2ns.

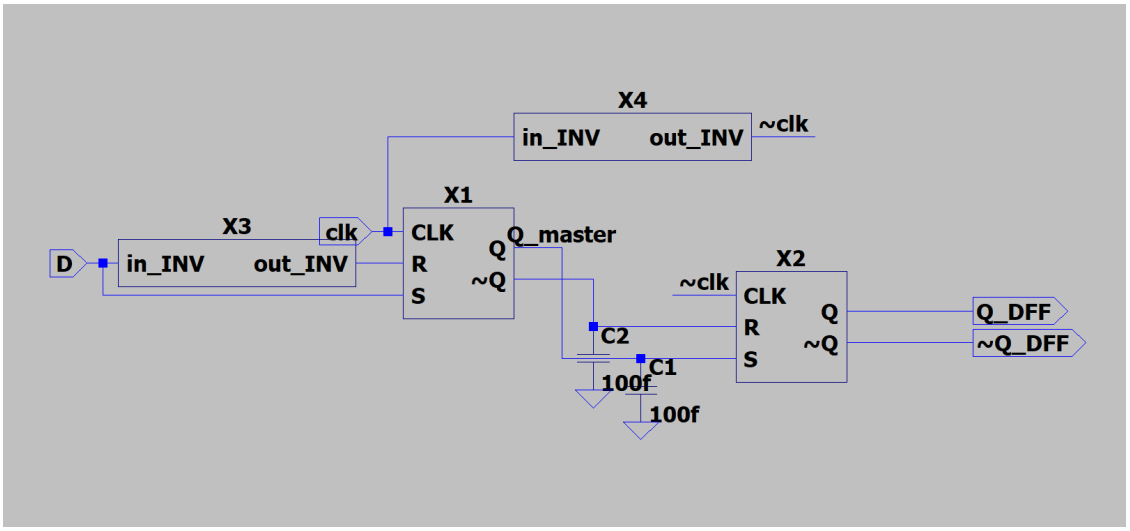


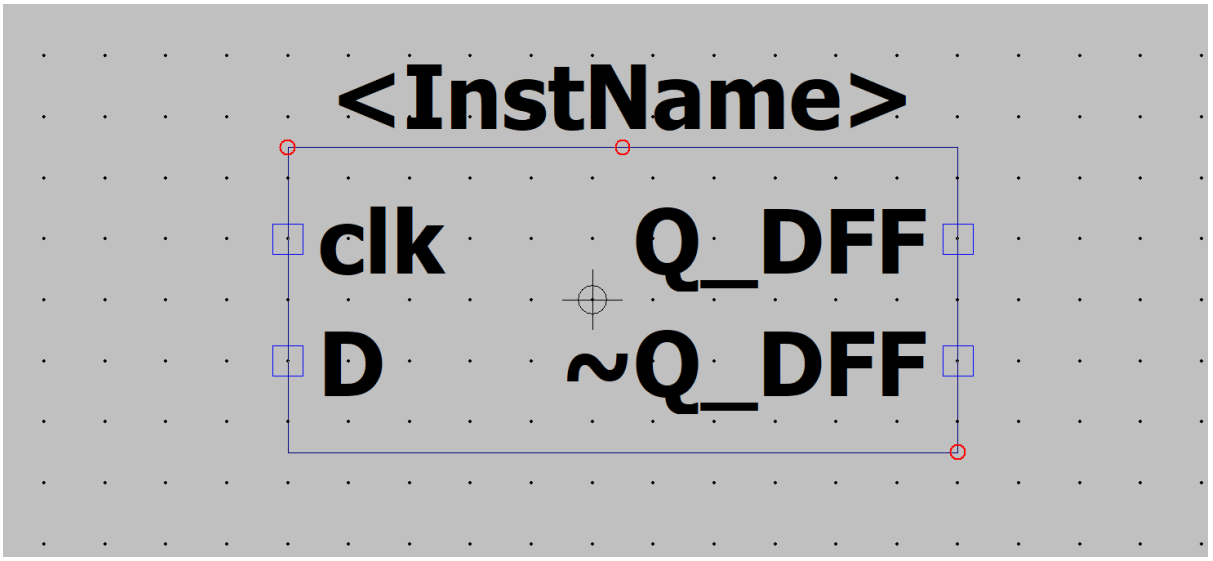


hold time :
if the signal goes to zero befor 0.7n or more this change will not appear on Q.

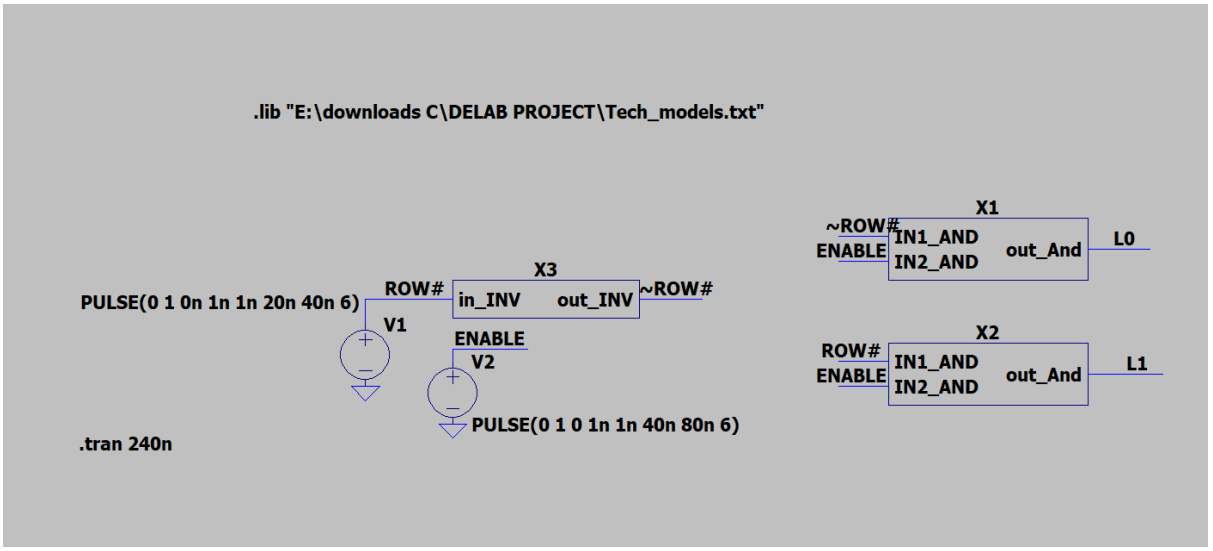


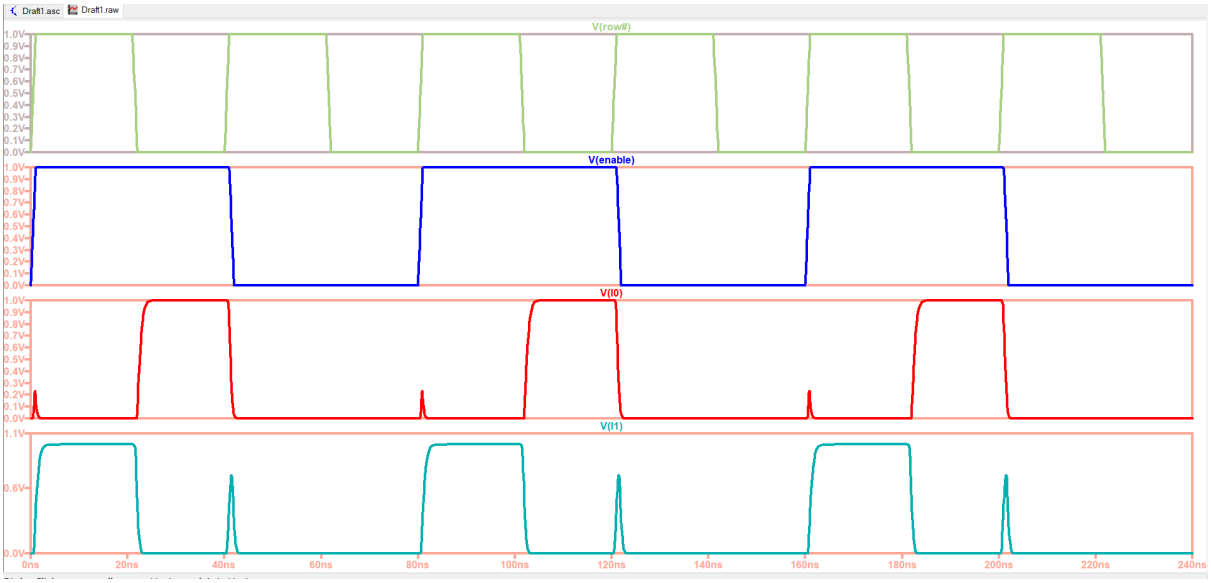


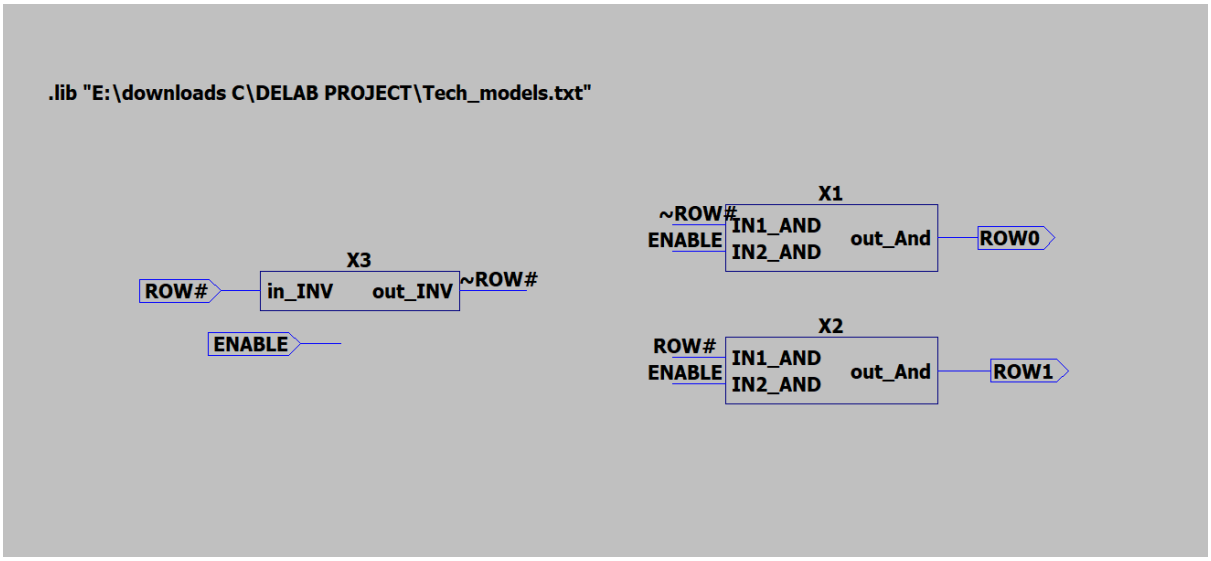

X4
in_INV
out_INV
~clk
X1
X3
clk
D
in_INV
out_INV
CLK
R
S
Q
~Q
Q_master
X2
~clk
CLK
R
S
Q
~Q
Q_DFF
~Q_DFF
C2
C1
100f
100f

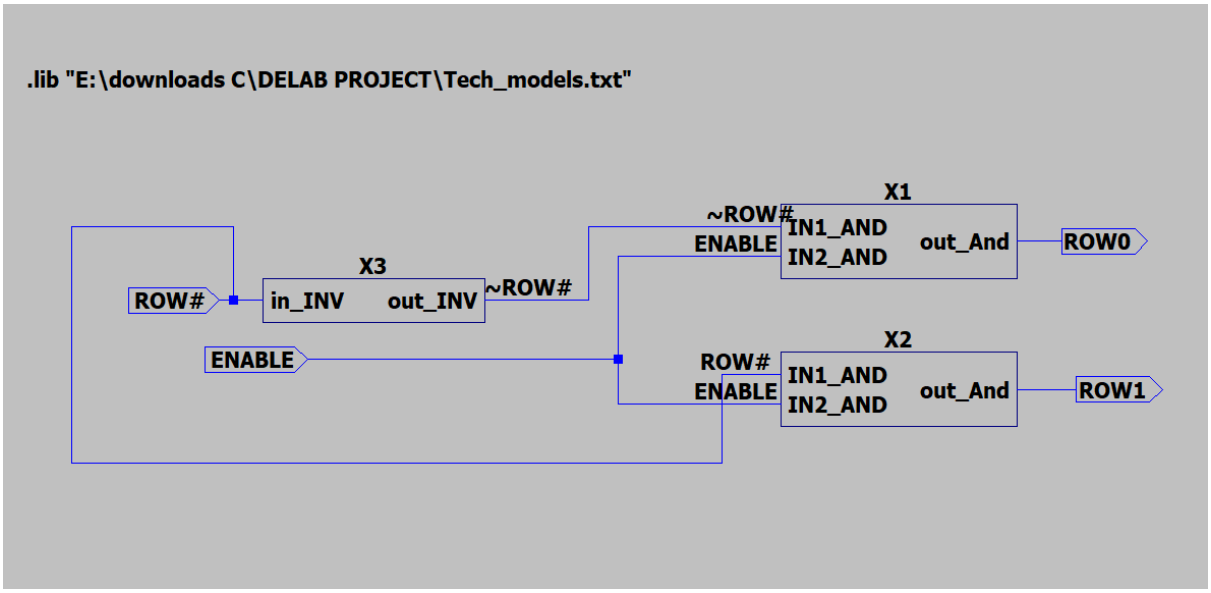

<InstName>
clk
D
Q_DFF
~Q_DFF

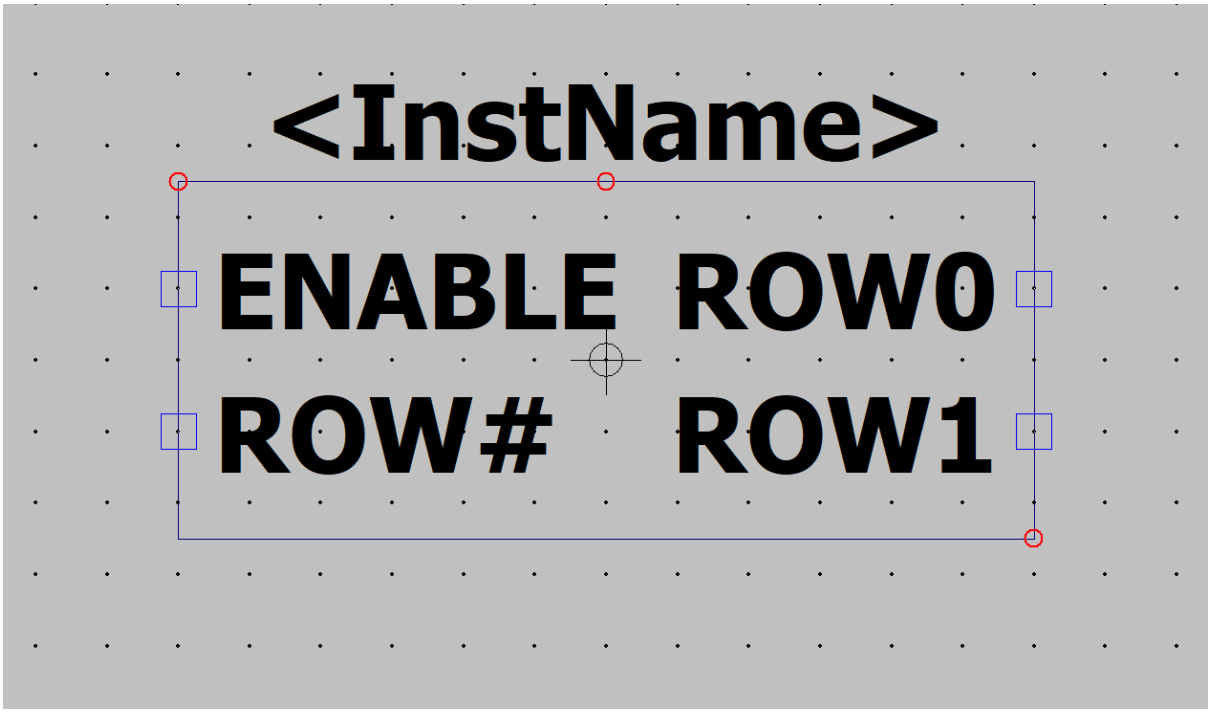
Decoder :


.lib "E:\downloads C\DELAB PROJECT\Tech_models.txt"
X1
~ROW#
ENABLE
IN1_AND
IN2_AND
out_And
L0
X3
PULSE(0 1 0n 1n 1n 20n 40n 6)
ROW#
in_INV
out_INV
~ROW#
V1
ENABLE
V2
X2
ROW#
ENABLE
IN1_AND
IN2_AND
out_And
L1
PULSE(0 1 0 1n 1n 40n 80n 6)
.tran 240n

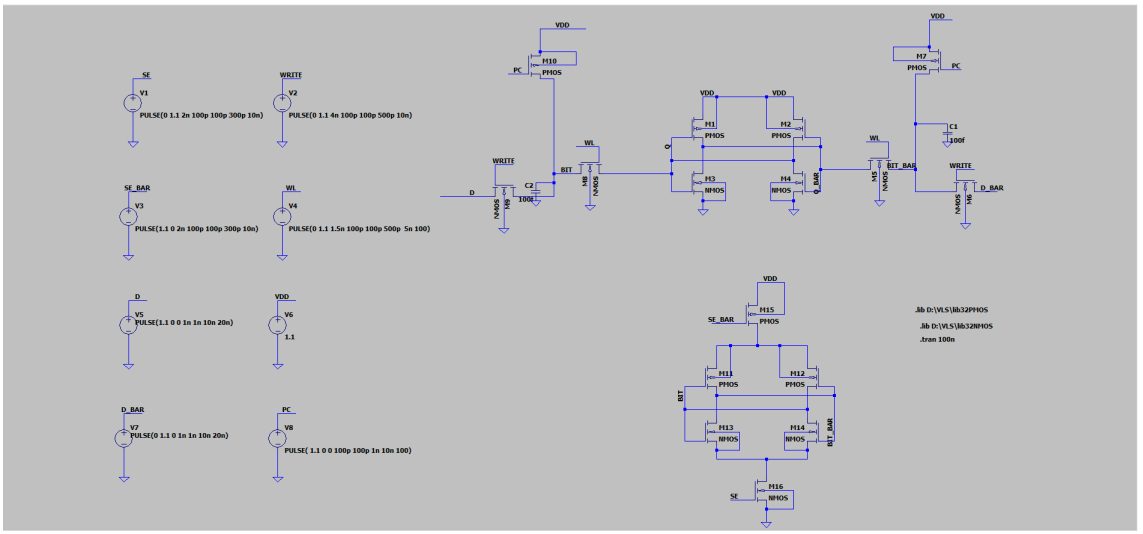

Draft1.asc
Draft1.raw
V(row#)
V(enable)
V(I0)
V(I1)
0ns
20ns
40ns
60ns
80ns
100ns
120ns
140ns
160ns
180ns
200ns
220ns
240ns

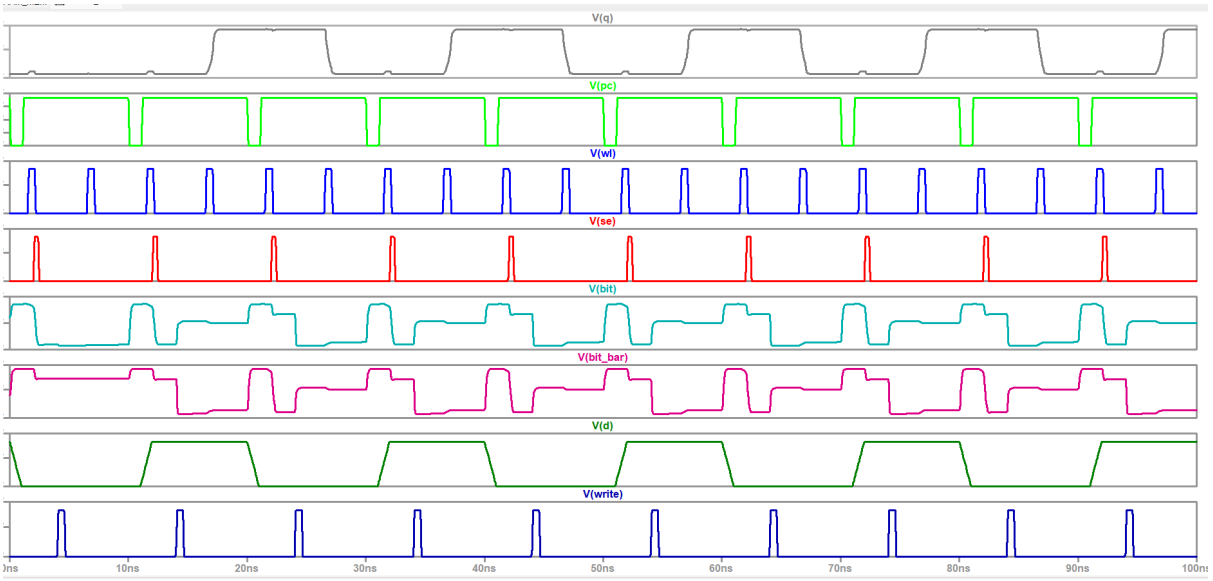

.lib "E:\downloads C\DELAB PROJECT\Tech_models.txt"
X3
ROW#
in_INV
out_INV
~ROW#
ENABLE
X1
~ROW#
ENABLE
IN1_AND
IN2_AND
out_And
ROW0
X2
ROW#
ENABLE
IN1_AND
IN2_AND
out_And
ROW1


.lib "E:\downloads C\DELAB PROJECT\Tech_models.txt"
X1
~ROW#
ENABLE
IN1_AND
IN2_AND
out_And
ROW0
X3
ROW#
in_INV
out_INV
~ROW#
ENABLE
X2
ROW#
ENABLE
IN1_AND
IN2_AND
out_And
ROW1

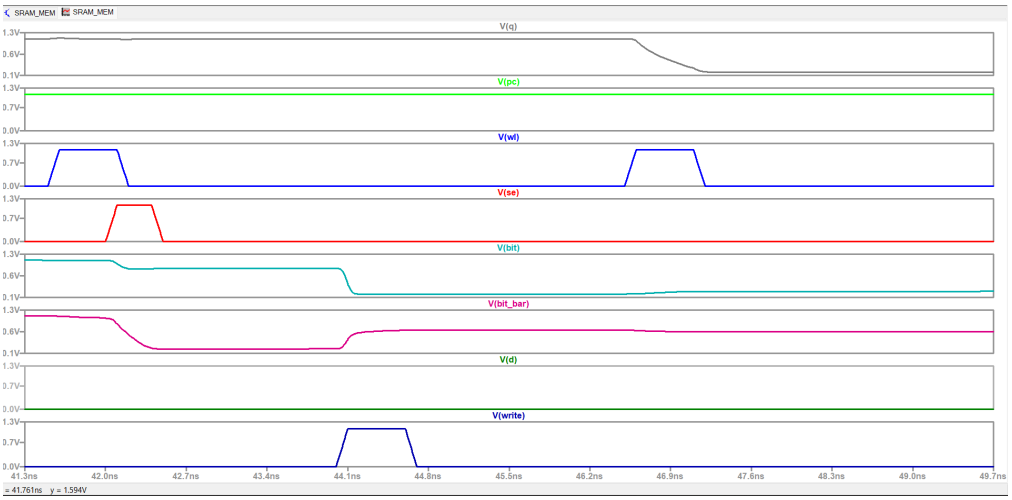

<InstName>
ENABLE
ROW#
ROW0
ROW1

SRAM :

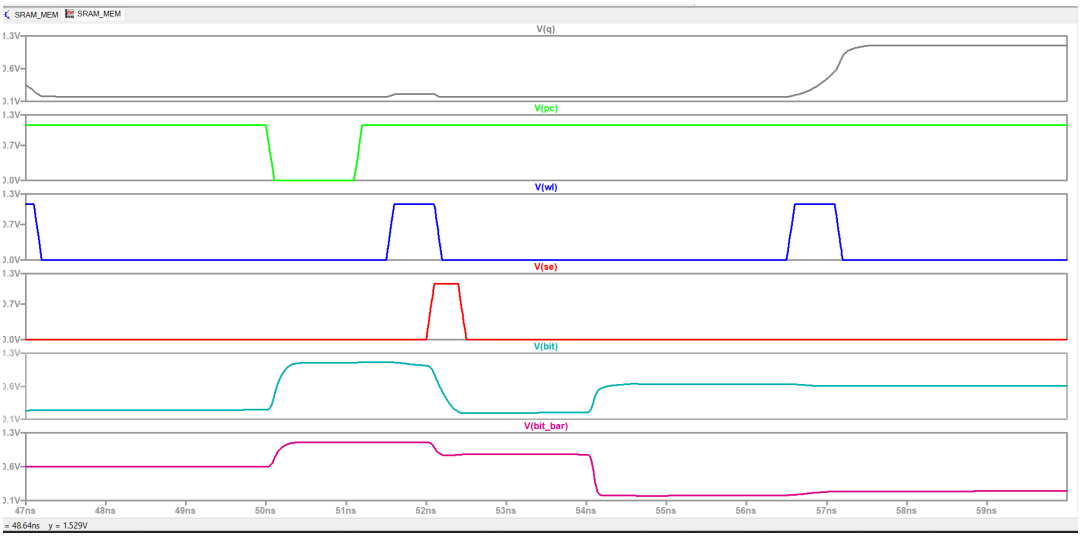

SE
V1
PULSE(0 1.1 2n 100p 100p 300p 10n)
WRITE
V2
PULSE(0 1.1 4n 100p 100p 500p 10n)
SE_BAR
V3
PULSE(1.1 0 2n 100p 100p 300p 10n)
WL
V4
PULSE(0 1.1 1.5n 100p 100p 500p 5n 100)
D
V5
PULSE(1.1 0 0 1n 1n 10n 20n)
VDD
V6
1.1
D_BAR
V7
PULSE(0 1.1 0 1n 1n 10n 20n)
PC
V8
PULSE(1.1 0 0 100p 100p 1n 10n 100)
VDD
M10
PC
PMOS
WRITE
D
M9
NMOS
C2
100f
BIT
WL
M8
NMOS
VDD
VDD
M1
PMOS
M2
PMOS
Q
M3
NMOS
M4
NMOS
Q_BAR
VDD
M7
PMOS
PC
C1
100f
WL
M5
NMOS
BIT_BAR
WRITE
D_BAR
M6
NMOS
VDD
M15
SE_BAR
PMOS
M11
PMOS
M12
PMOS
BIT
M13
NMOS
M14
NMOS
BIT_BAR
M16
SE
NMOS
.lib D:\VLS\lib32PMOS
.lib D:\VLS\lib32NMOS
.tran 100n

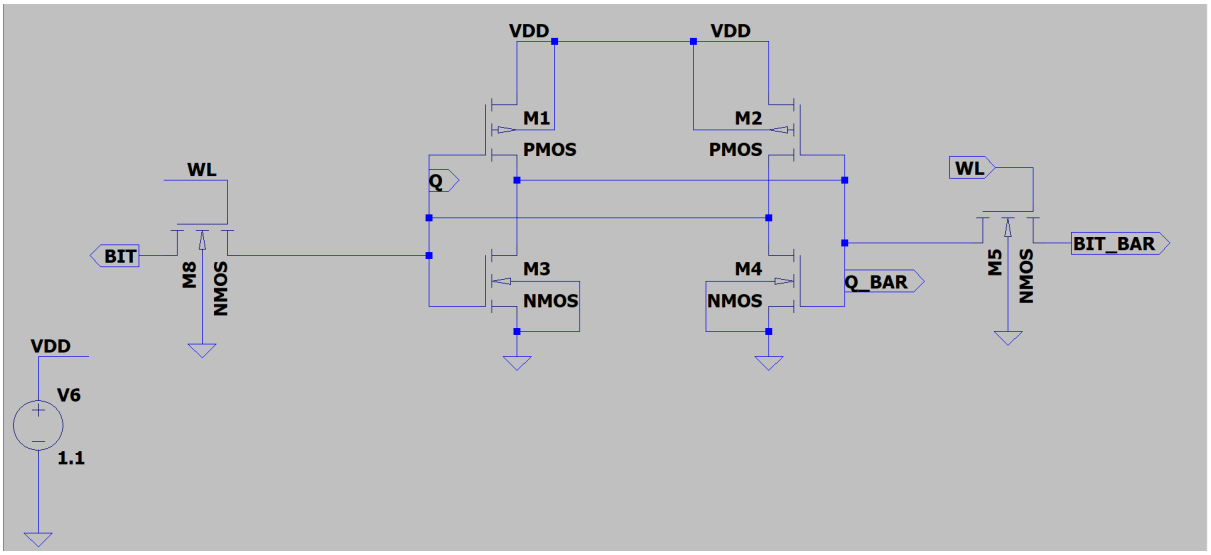

V(q)
V(pc)
V(wl)
V(se)
V(bit)
V(bit_bar)
V(d)
V(write)
0ns
10ns
20ns
30ns
40ns
50ns
60ns
70ns
80ns
90ns
100ns

Write 0

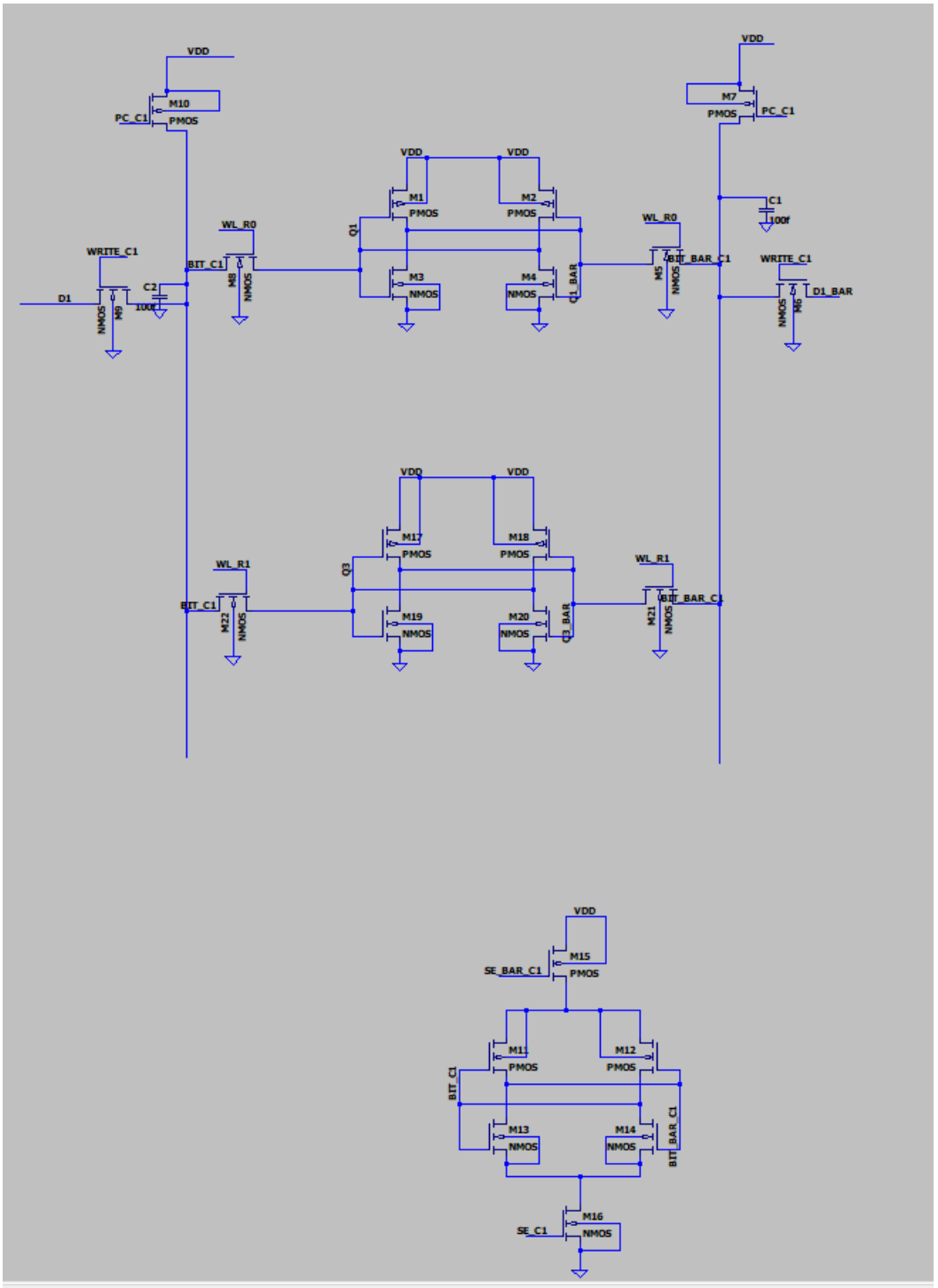

SRAM_MEM
SRAM_MEM
V(q)
V(pc)
V(wl)
V(se)
V(bit)
V(bit_bar)
V(d)
V(write)
41.3ns
42.0ns
42.7ns
43.4ns
44.1ns
44.8ns
45.5ns
46.2ns
46.9ns
47.6ns
48.3ns
49.0ns
49.7ns
= 41.76ns y = 1.594V

Read

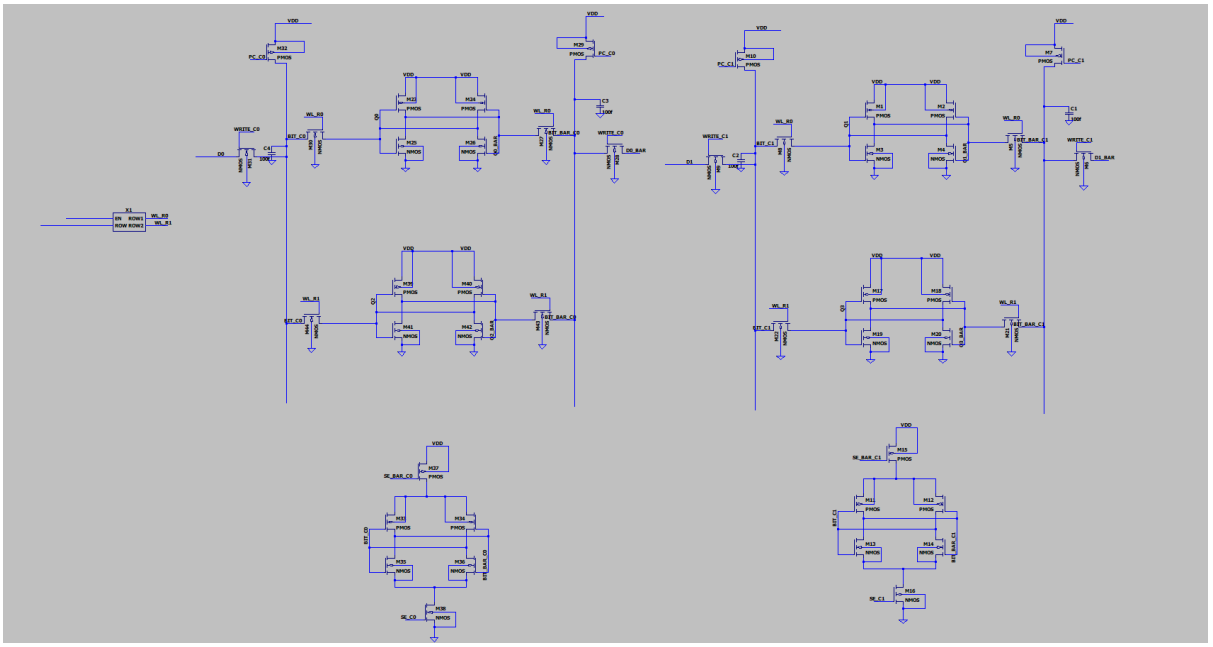

SRAM_MEM
SRAM_MEM
V(q)
V(pc)
V(wl)
V(se)
V(bit)
V(bit_bar)
47ns
48ns
49ns
50ns
51ns
52ns
53ns
54ns
55ns
56ns
57ns
58ns
59ns
= 48.64ns y = 1.529V

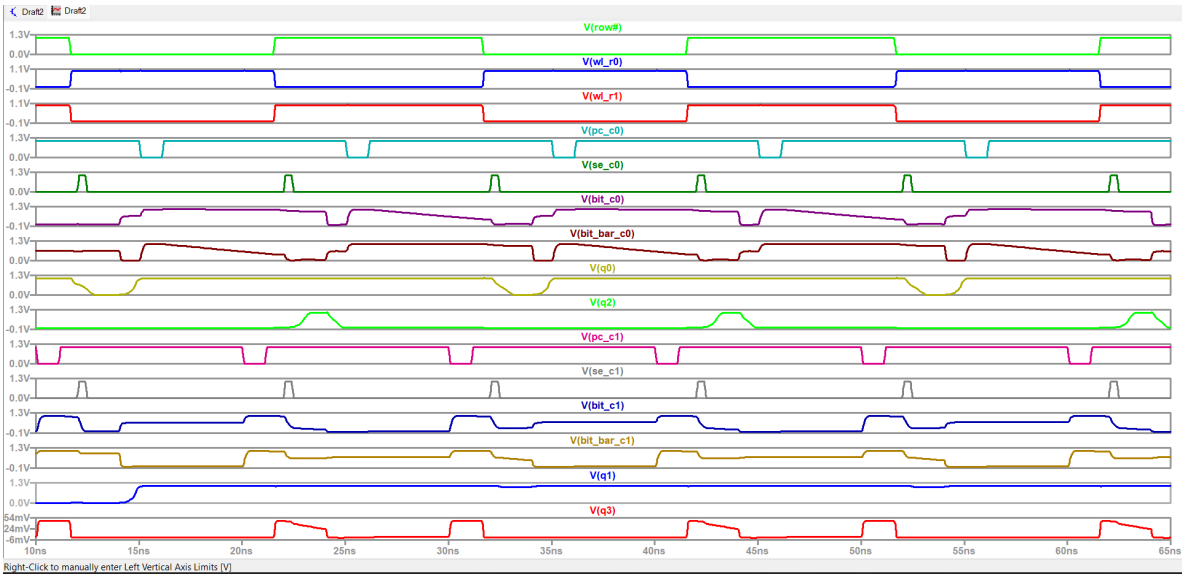


1 Column SRAM:

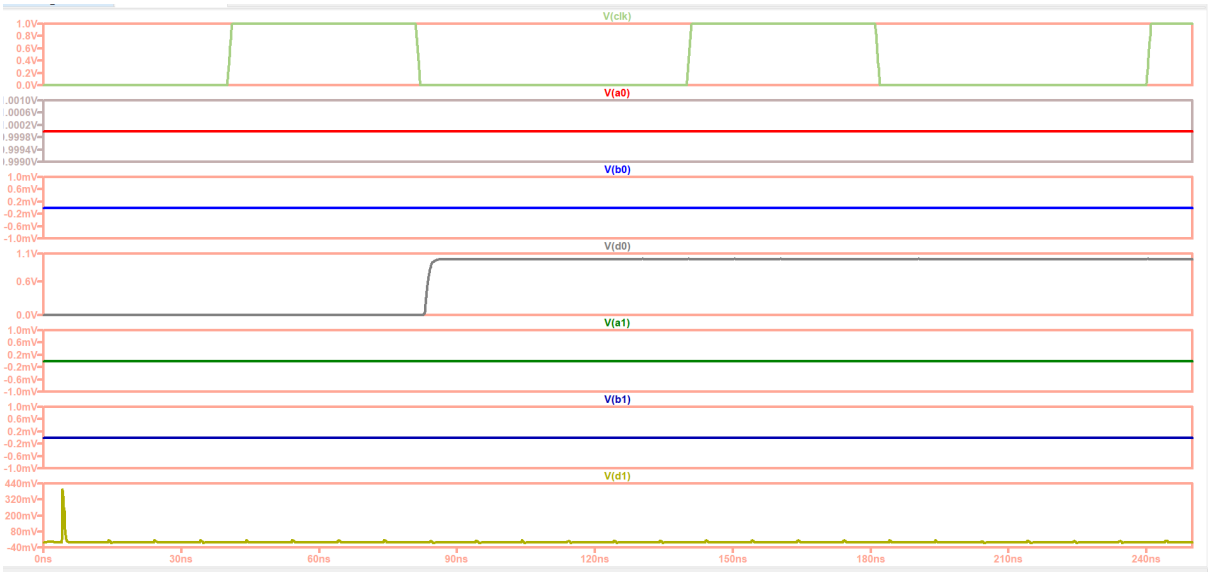

VDD
M10
PC_C1
PMOS
M7
PC_C1
M1
M2
Q1
WL_R0
WRITE_C1
BIT_C1
C2
100f
D1
M8
M9
M3
M4
C1_BAR
M5
BIT_BAR_C1
C1
M6
D1_BAR
NMOS
M17
M18
Q3
WL_R1
M19
M20
C3_BAR
M21
M22
SE_BAR_C1
M15
M11
M12
M13
M14
M16
SE_C1

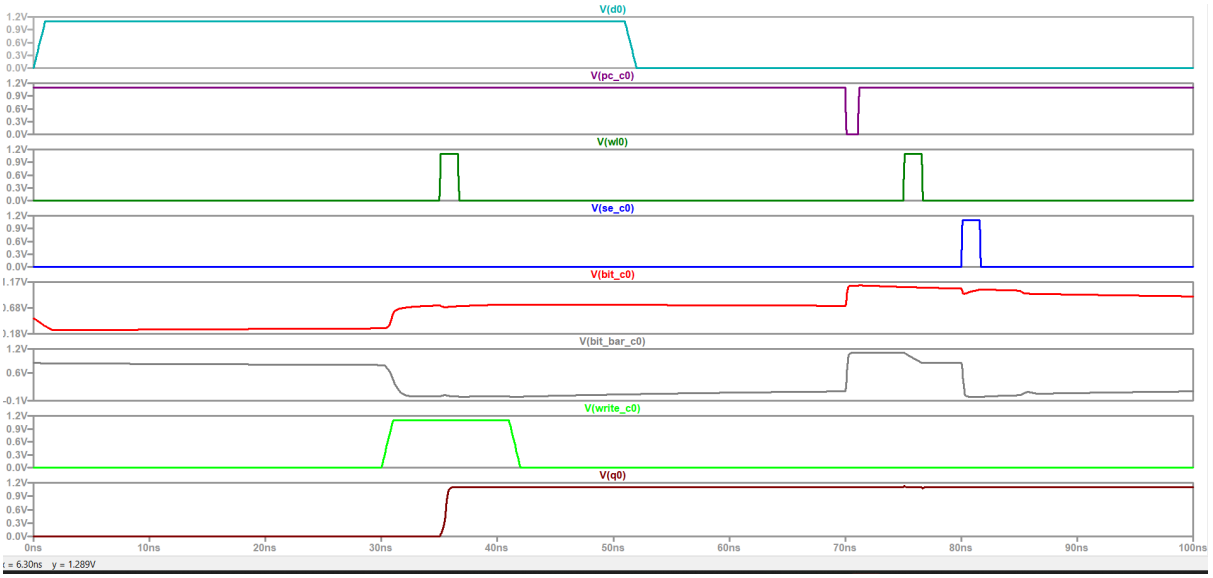
2 X 2 SRAM



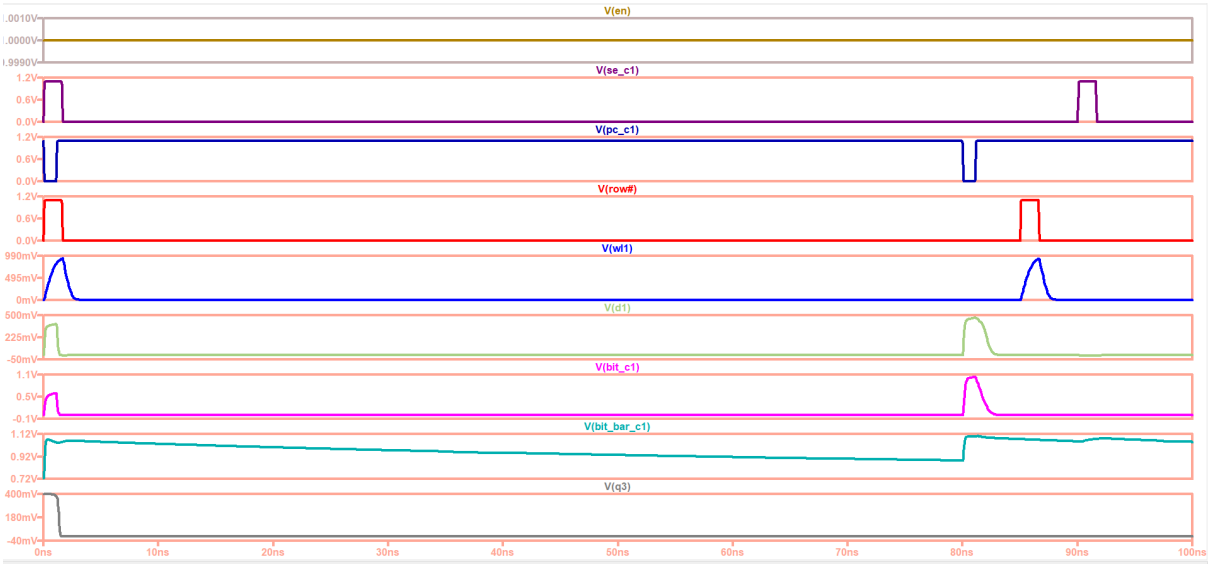

Draft2
Draft2
V(row#)
V(wl_r0)
V(wl_r1)
V(pc_c0)
V(se_c0)
V(bit_c0)
V(bit_bar_c0)
V(q0)
V(q2)
V(pc_c1)
V(se_c1)
V(bit_c1)
V(bit_bar_c1)
V(q1)
V(q3)
10ns
15ns
20ns
25ns
30ns
35ns
40ns
45ns
50ns
55ns
60ns
65ns
Right-Click to manually enter Left Vertical Axis Limits [V]

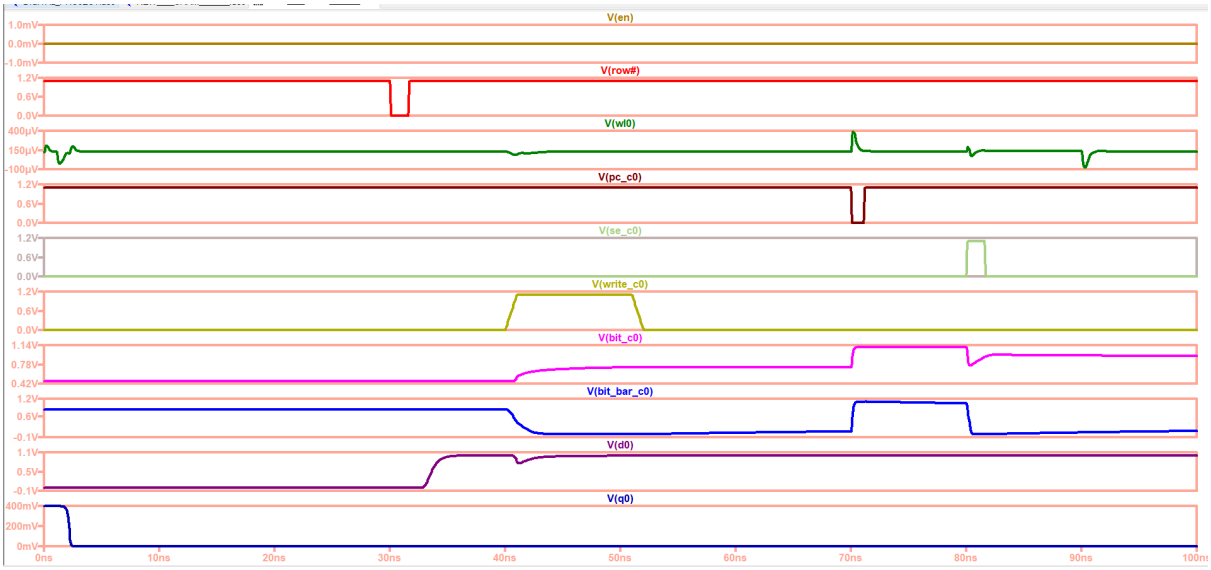
Full Design :

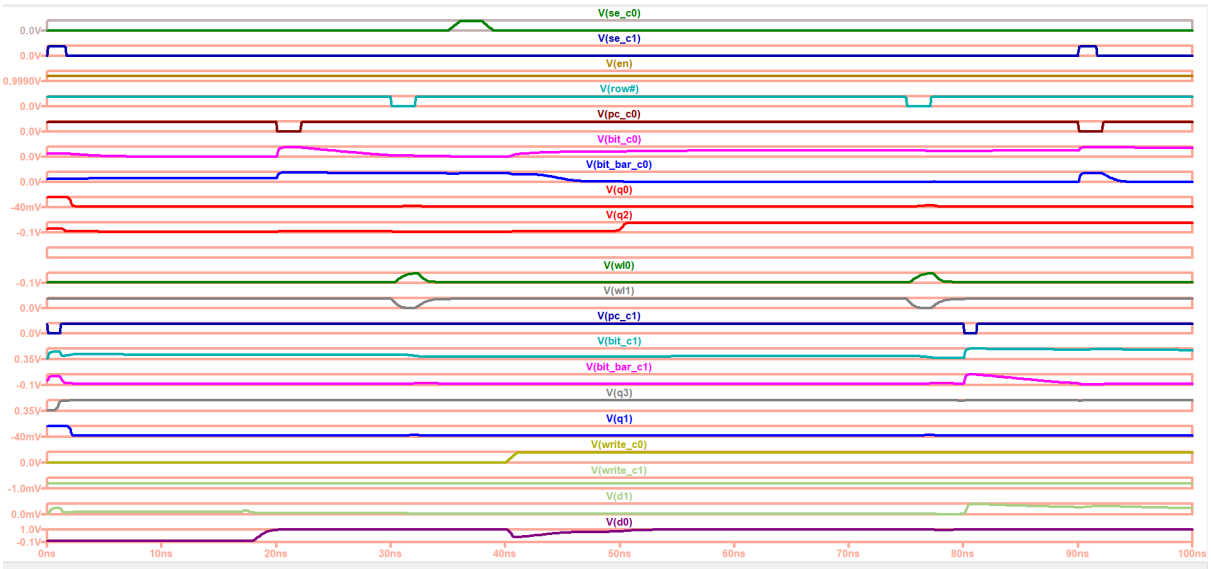




Test Cases:

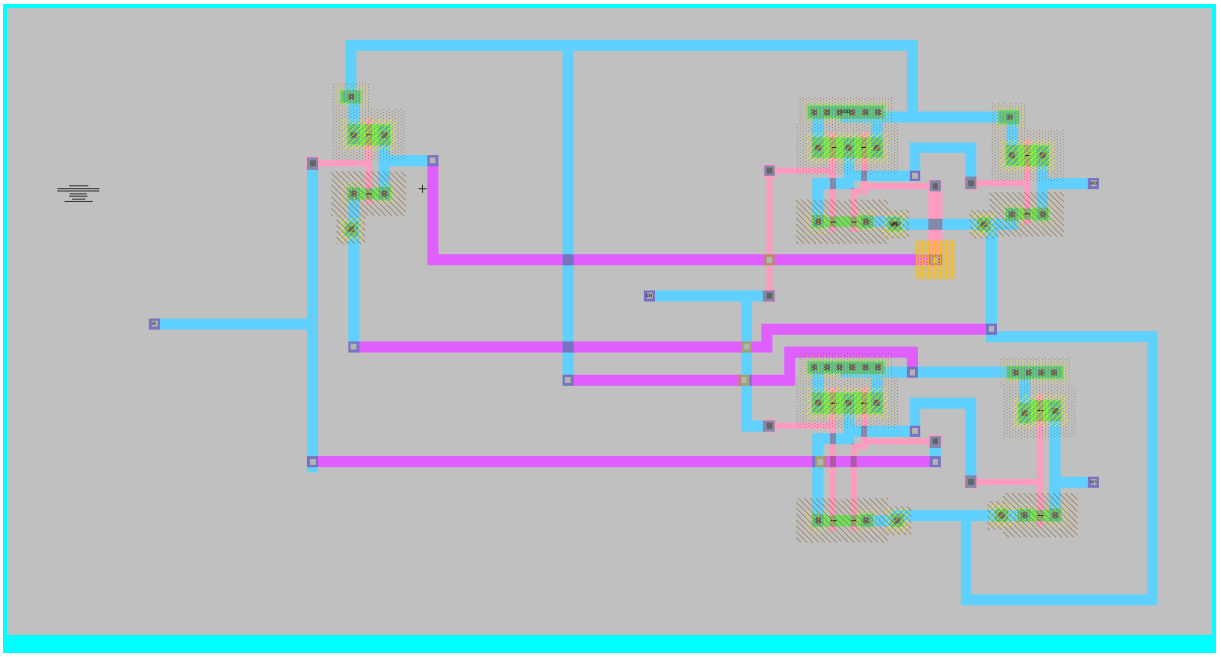

V(en)
V(se_c1)
V(pc_c1)
V(row#)
V(wl1)
V(d1)
V(bit_c1)
V(bit_bar_c1)
V(q3)
0ns
10ns
20ns
30ns
40ns
50ns
60ns
70ns
80ns
90ns
100ns

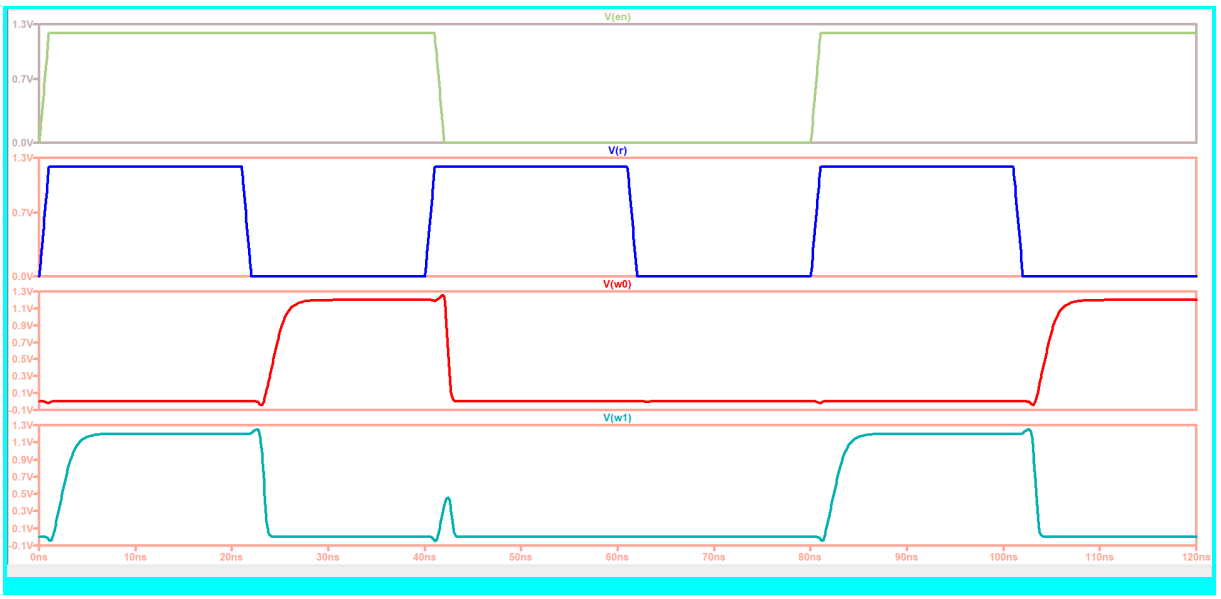

V(en)
V(row#)
V(wl0)
V(pc_c0)
V(se_c0)
V(write_c0)
V(bit_c0)
V(bit_bar_c0)
V(d0)
V(q0)
0ns
10ns
20ns
30ns
40ns
50ns
60ns
70ns
80ns
90ns
100ns


V(se_c0)
0.0V
V(se_c1)
0.0V
V(en)
0.9990V
V(row#)
0.0V
V(pc_c0)
0.0V
V(bit_c0)
0.0V
V(bit_bar_c0)
0.0V
V(q0)
-40mV
V(q2)
-0.1V
V(wl0)
-0.1V
V(wl1)
0.0V
V(pc_c1)
0.0V
V(bit_c1)
0.35V
V(bit_bar_c1)
-0.1V
V(q3)
0.35V
V(q1)
-40mV
V(write_c0)
0.0V
V(write_c1)
-1.0mV
V(d1)
0.0mV
V(d0)
1.0V
-0.1V
0ns
10ns
20ns
30ns
40ns
50ns
60ns
70ns
80ns
90ns
100ns

Layout

Decoder:

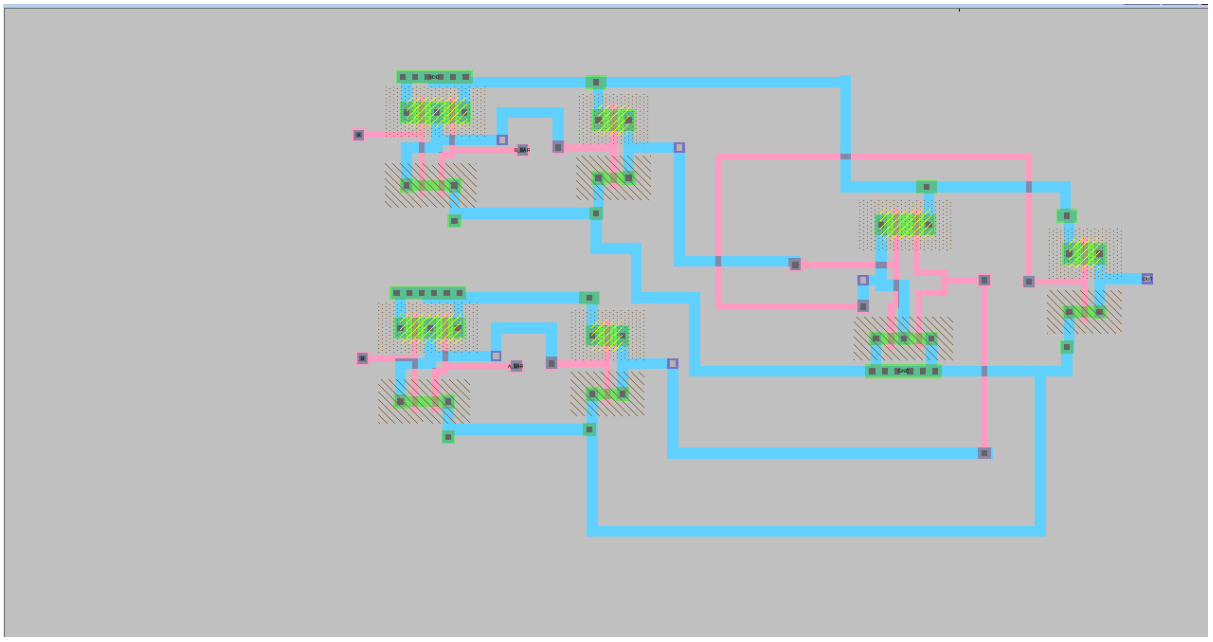


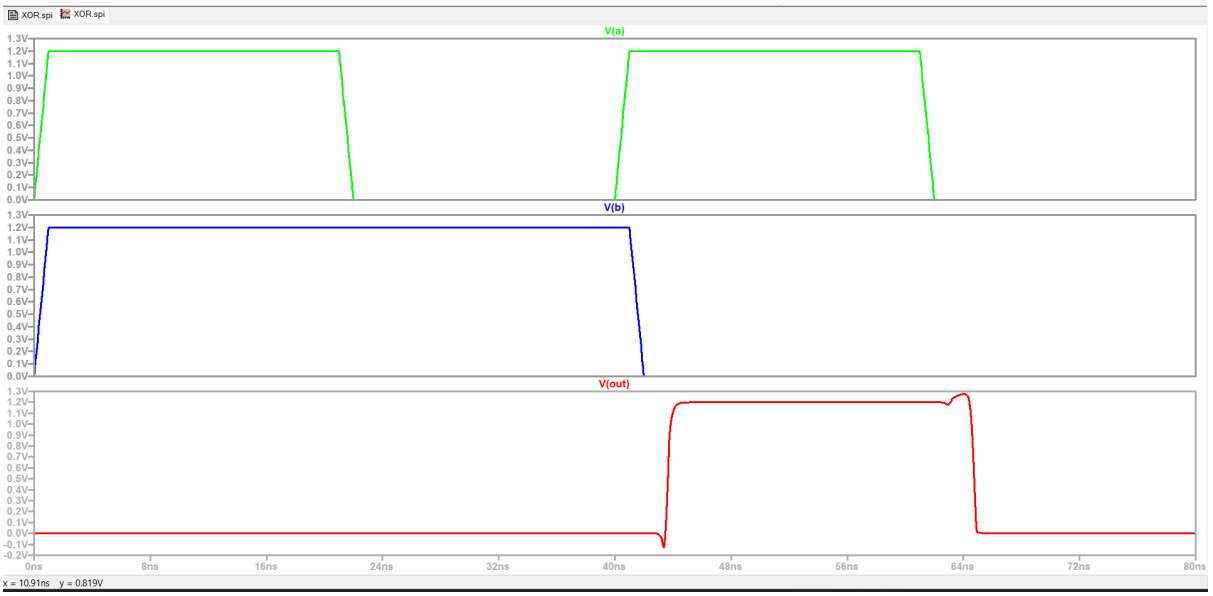


vdd VDD 0 DC 1.2

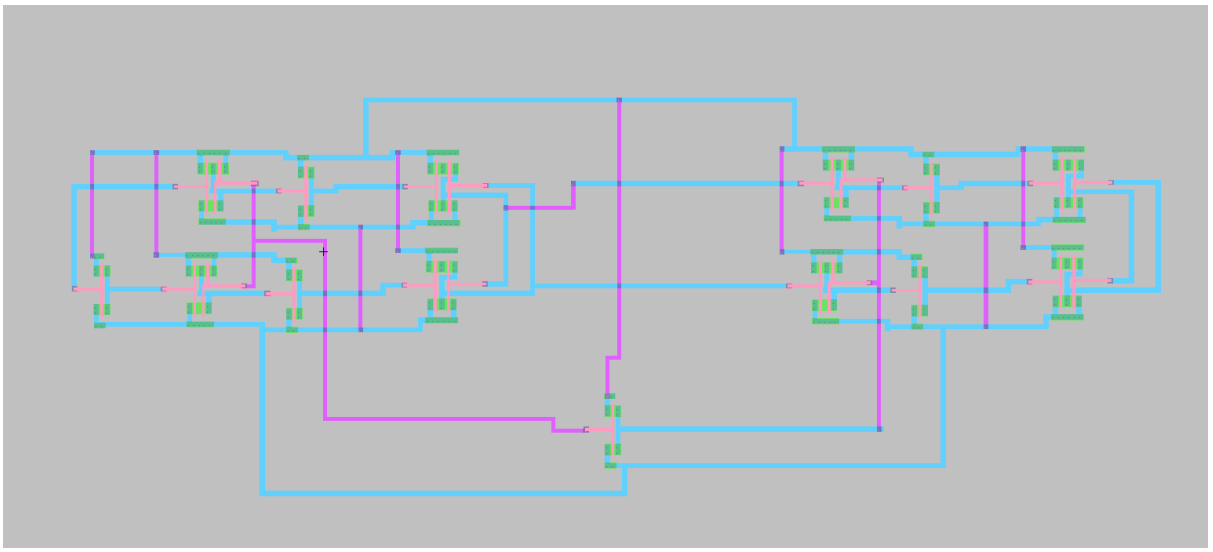
vin EN 0 PULSE(0 1.2 0 1n 1n 40n 80n 5)
vin2 R 0 PULSE(0 1.2 0 1n 1n 20n 40n 5)
cload W0 0 50fF
cload2 W1 0 50fF
.tran 0 120n
.include E:\downloads C\DELAB PROJECT - Copy\Tech_models.txt
.END

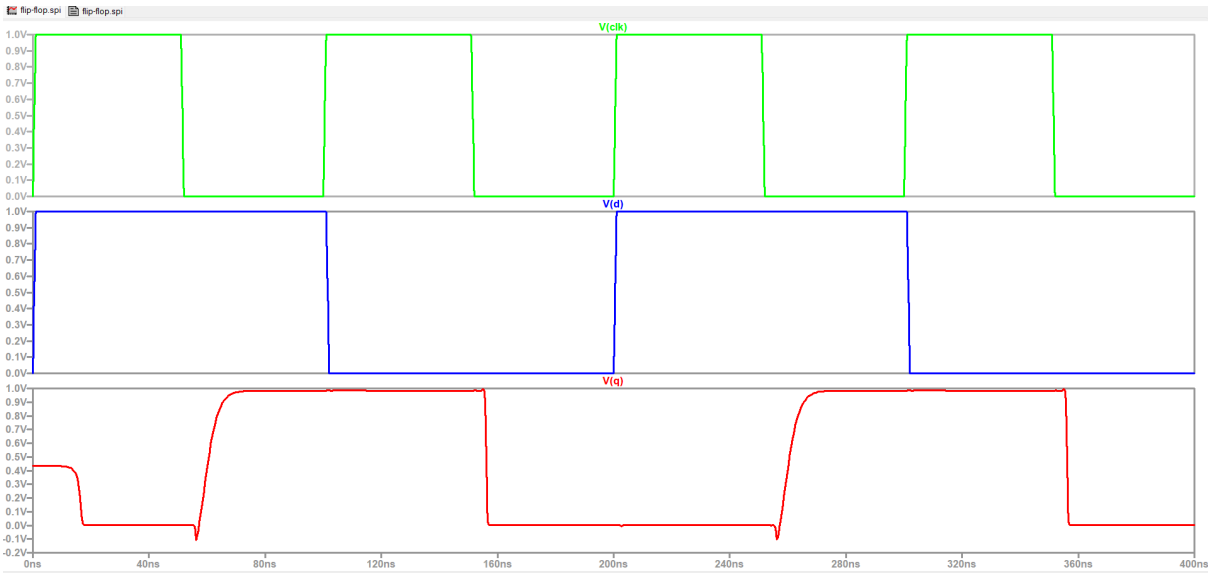
XOR



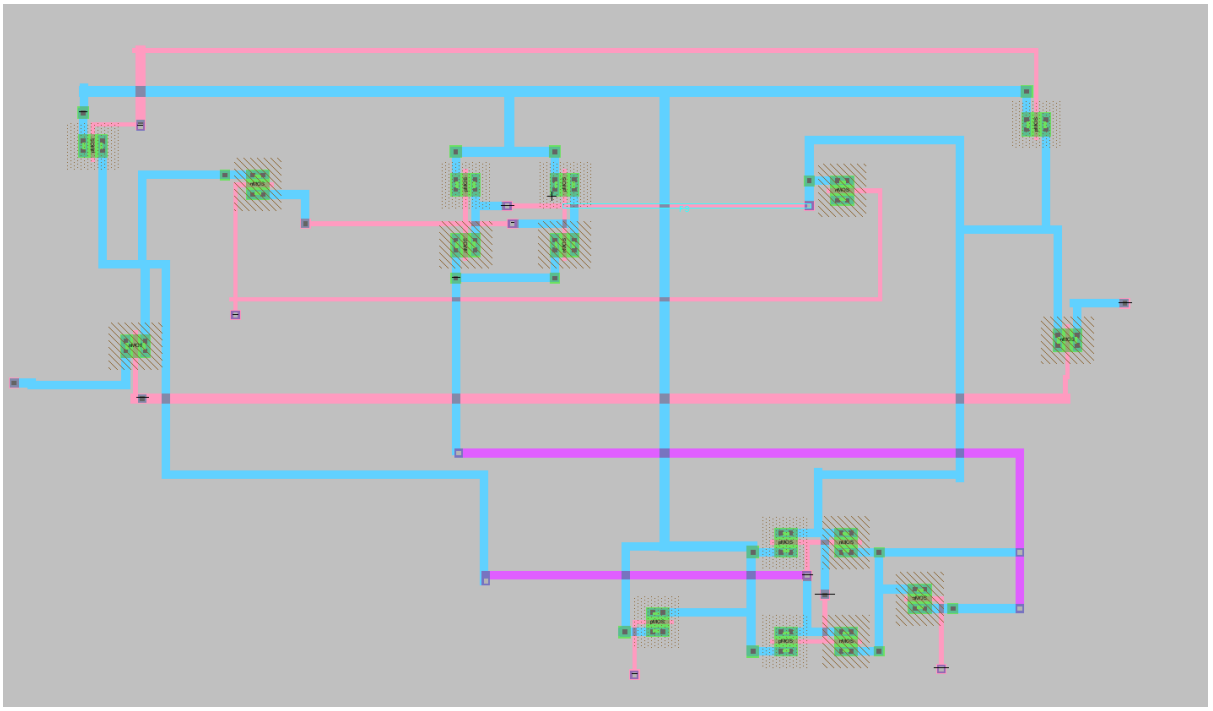


D-FF




flip-flop.spi
flip-flop.spi
V(clk)
V(d)
V(q)
1.0V
0.9V
0.8V
0.7V
0.6V
0.5V
0.4V
0.3V
0.2V
0.1V
0.0V
-0.1V
-0.2V
0ns
40ns
80ns
120ns
160ns
200ns
240ns
280ns
320ns
360ns
400ns

SRAM:

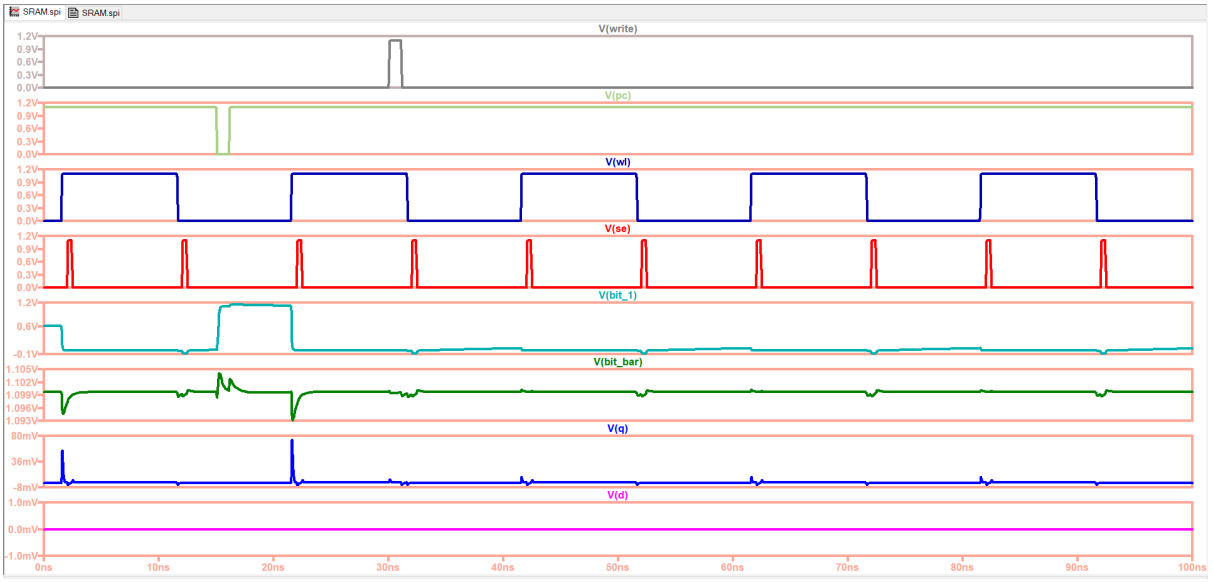


```
vdd VDD 0 DC 1.1
vin WRITE 0 PULSE(0 1.1 4n 100p 100p 500p 10n)
vin2 SE 0 PULSE(0 1.1 2n 100p 100p 300p 10n)
vin3 SE_BAR 0 PULSE(1.1 0 2n 100p 100p 300p 10n)
vin4 D 0 PULSE(1.1 0 0 1n 1n 10n 20n)
vin5 D_AR 0 PULSE(0 1.1 0 1n 1n 10n 20n)
vin6 PC 0 PULSE(1.1 0 15n 100p 100p 1n 10n 10n)
vin7 WL 0 PULSE(0 1.1 1.5n 100p 100p 10n 20n 100)
cload Q 0 50fF
cload1 Q_BAR 0 100f
cload2 BIT 0 100f
cload3 BIT_BAR 0 100f
.tran 0 100n
.include E:\downloads C\DELAB PROJECT - Copy\Tech_models.txt
.END
```

Read:


V(pc)
V(wl)
V(se)
V(bit_1)
V(bit_bar)
V(q)
0ns
10ns
20ns
30ns
40ns
50ns
60ns
70ns
80ns
90ns
100ns

Write:


SRAM.spi
SRAM.spi
V(write)
V(pc)
V(wl)
V(se)
V(bit_1)
V(bit_bar)
V(q)
V(d)
0ns
10ns
20ns
30ns
40ns
50ns
60ns
70ns
80ns
90ns
100ns

Full Design Layout: