

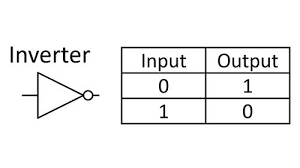
**UNIVERSITY OF JORDAN**

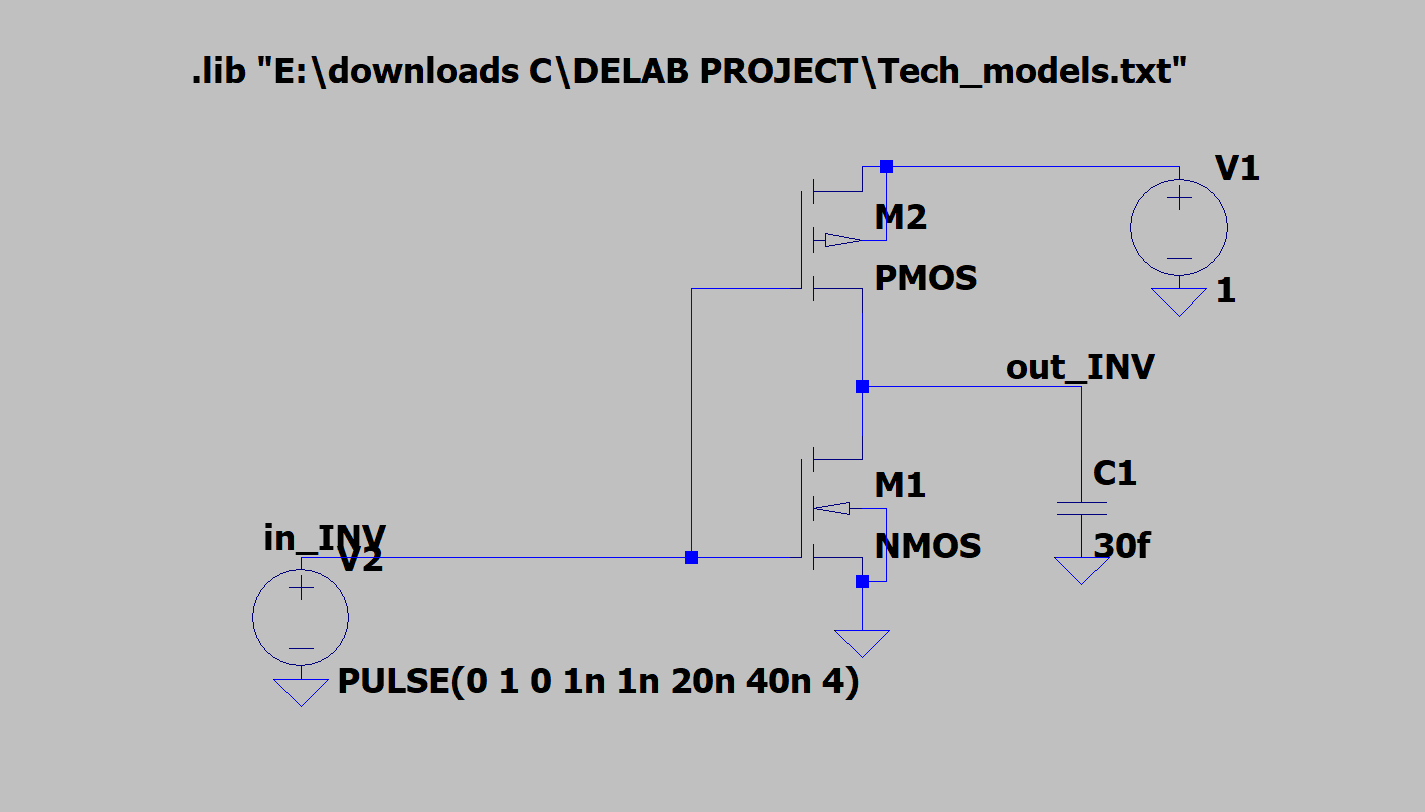
Computer Engineering Department

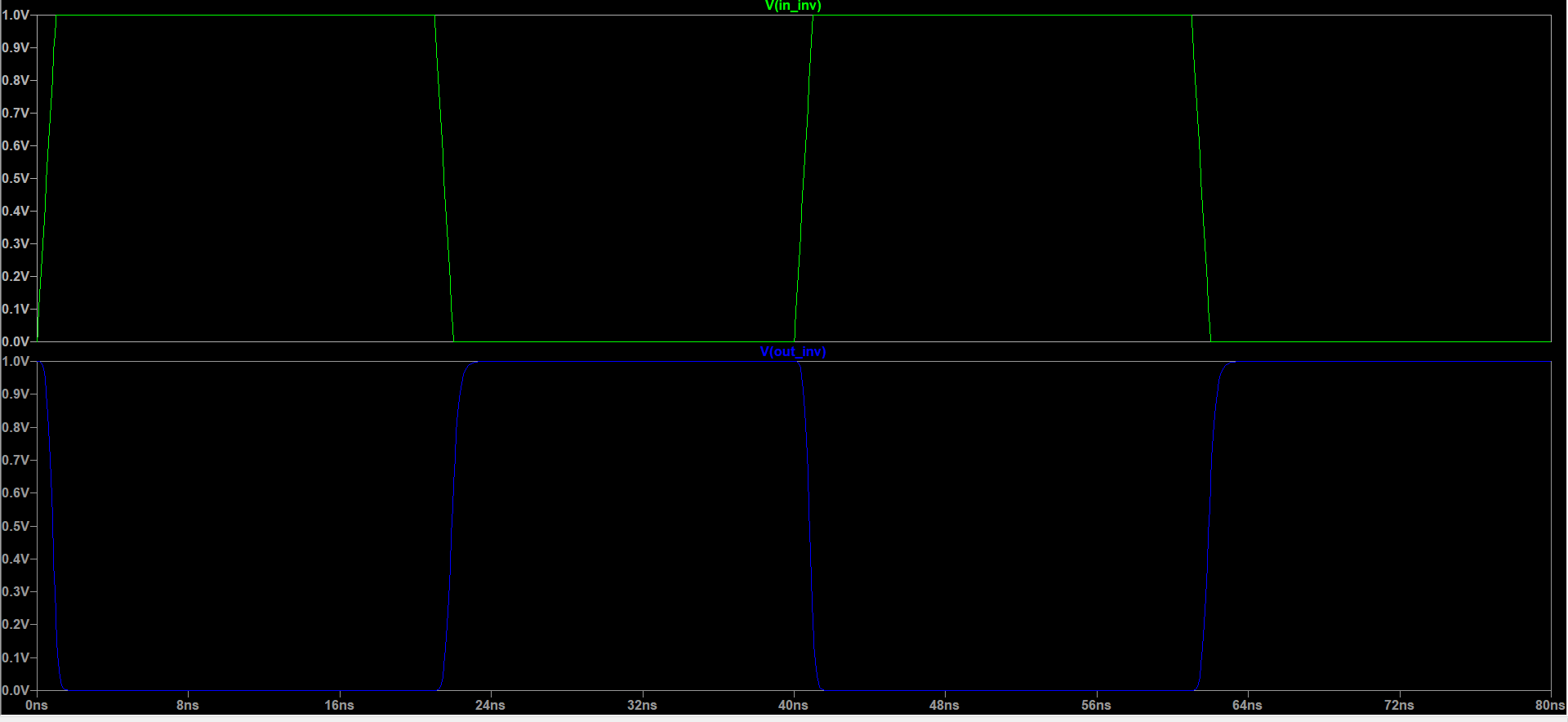
**Digital Electronics Laboratory Project**

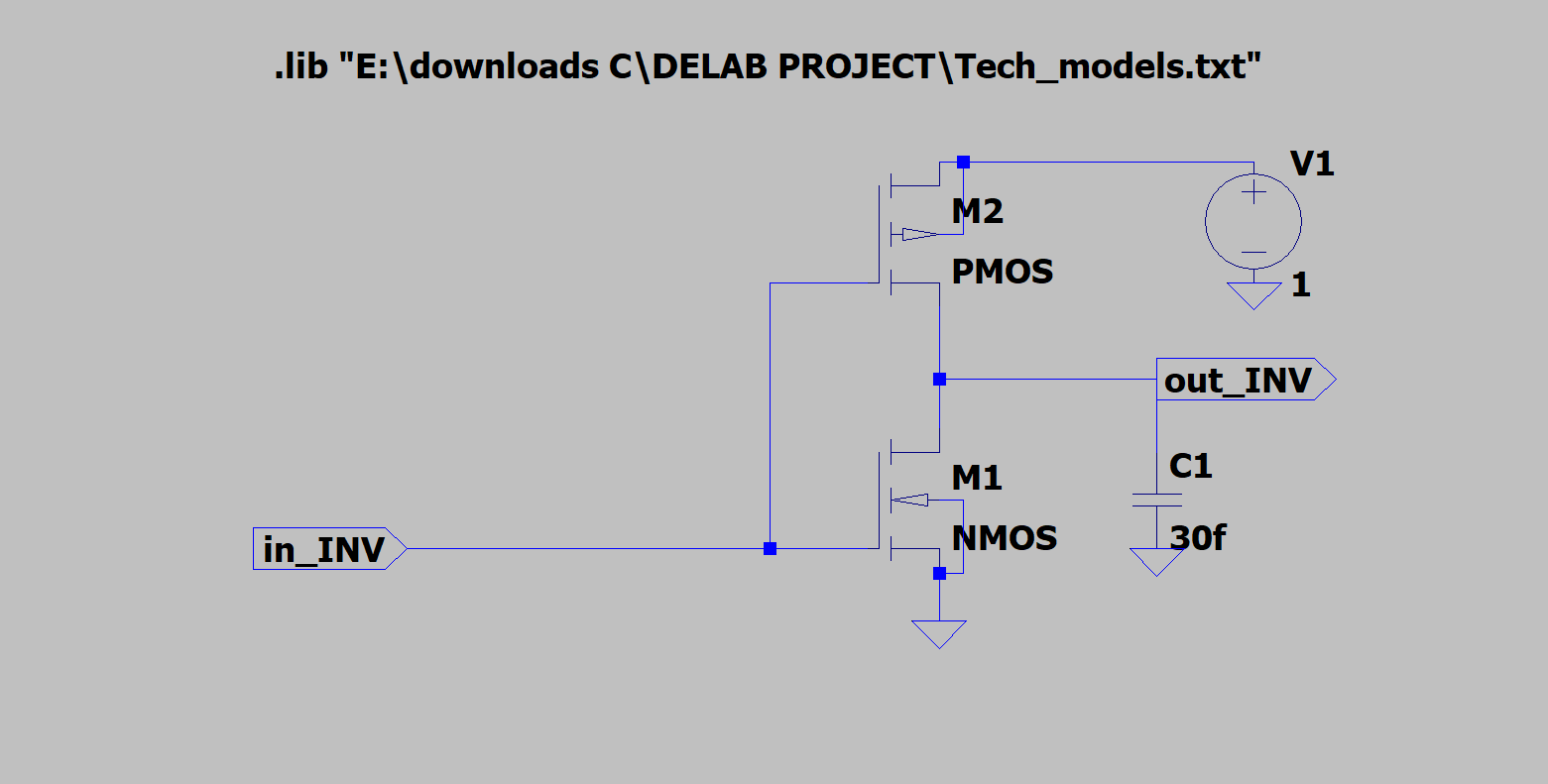
| ID | Name |
| --- | --- |
| **0194433** | **Fatima Hesham** |
| **0197035** | **Tala Kafafi** |

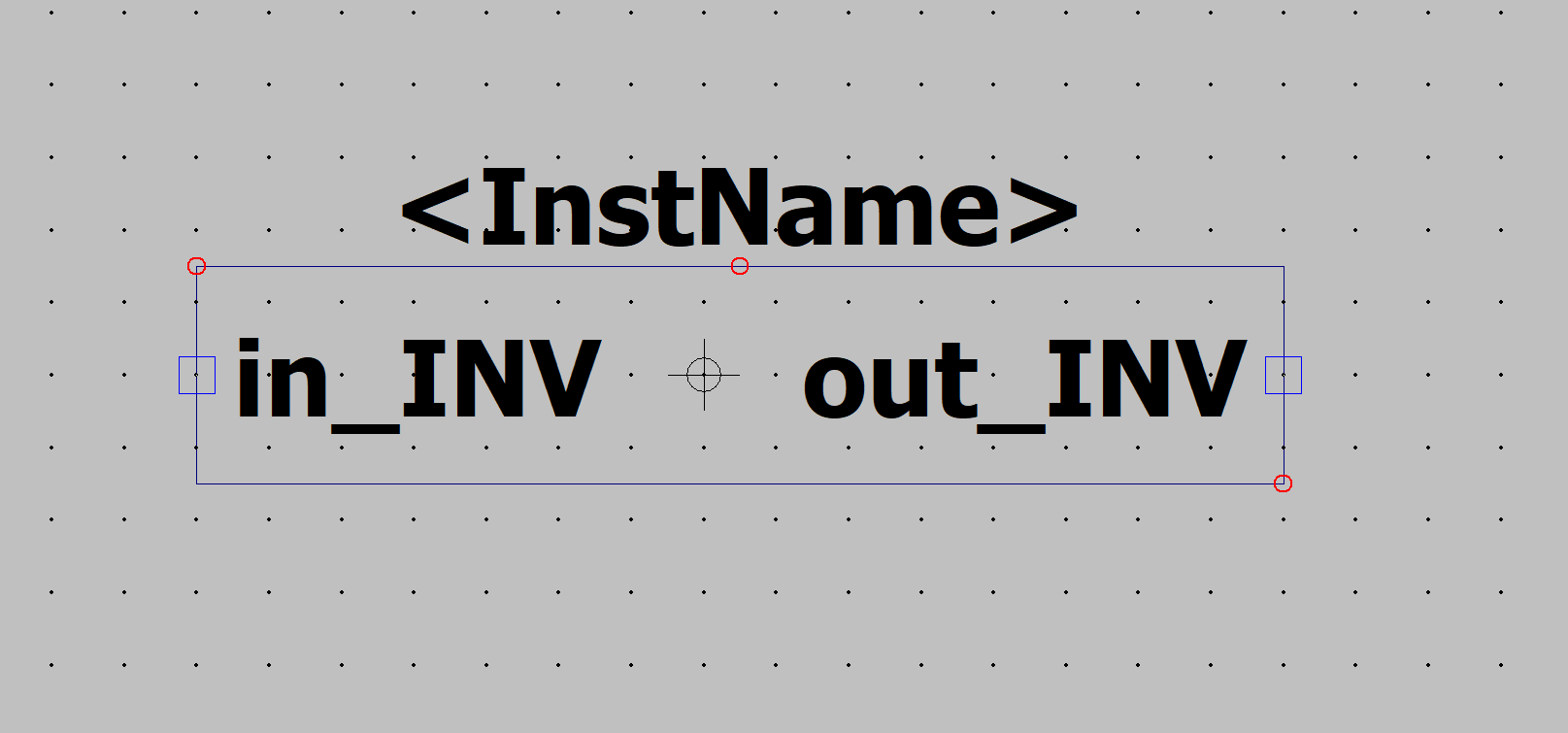
**Inverter Gate:**



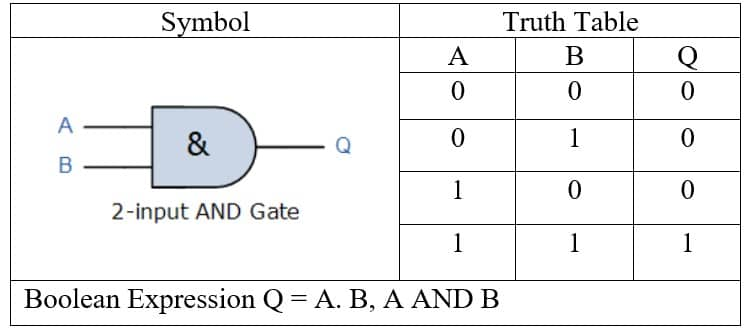


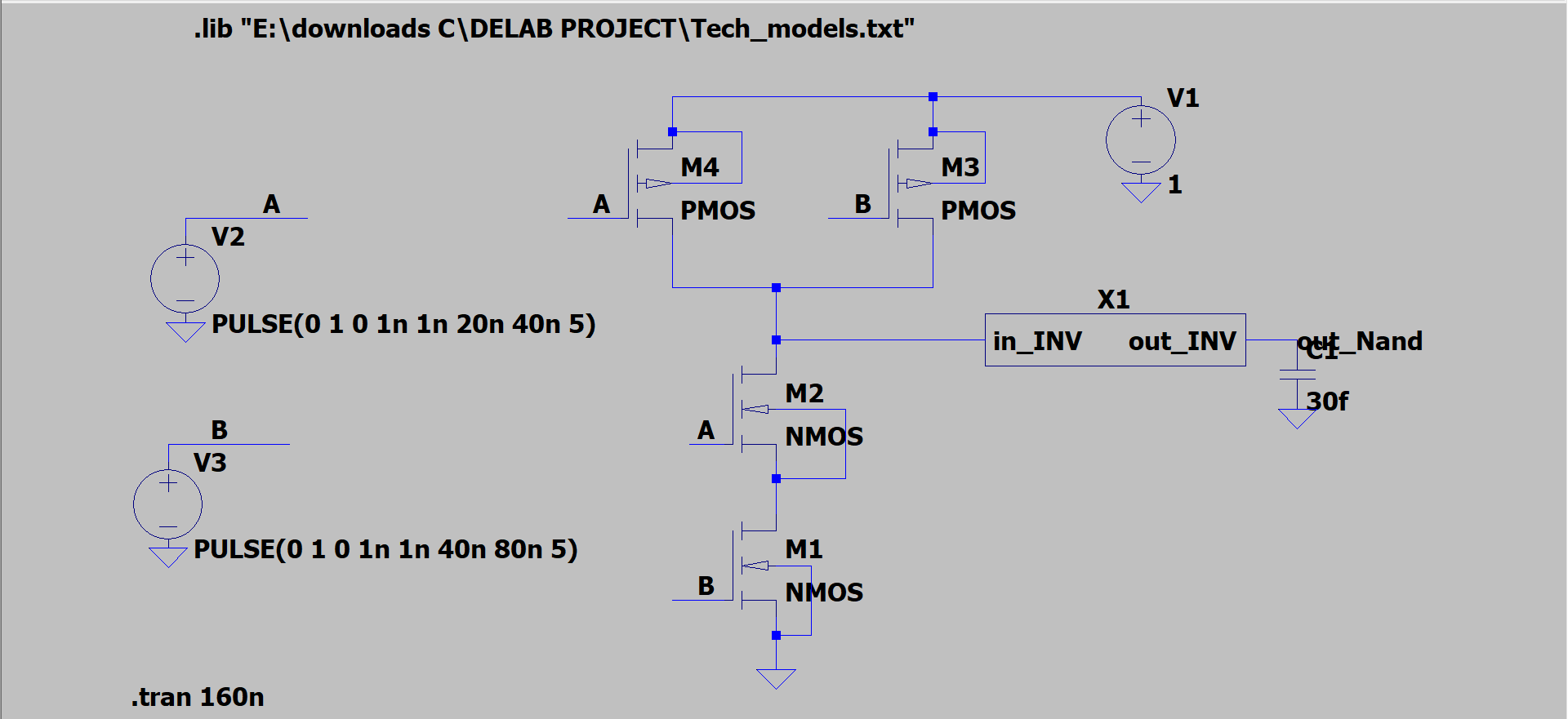


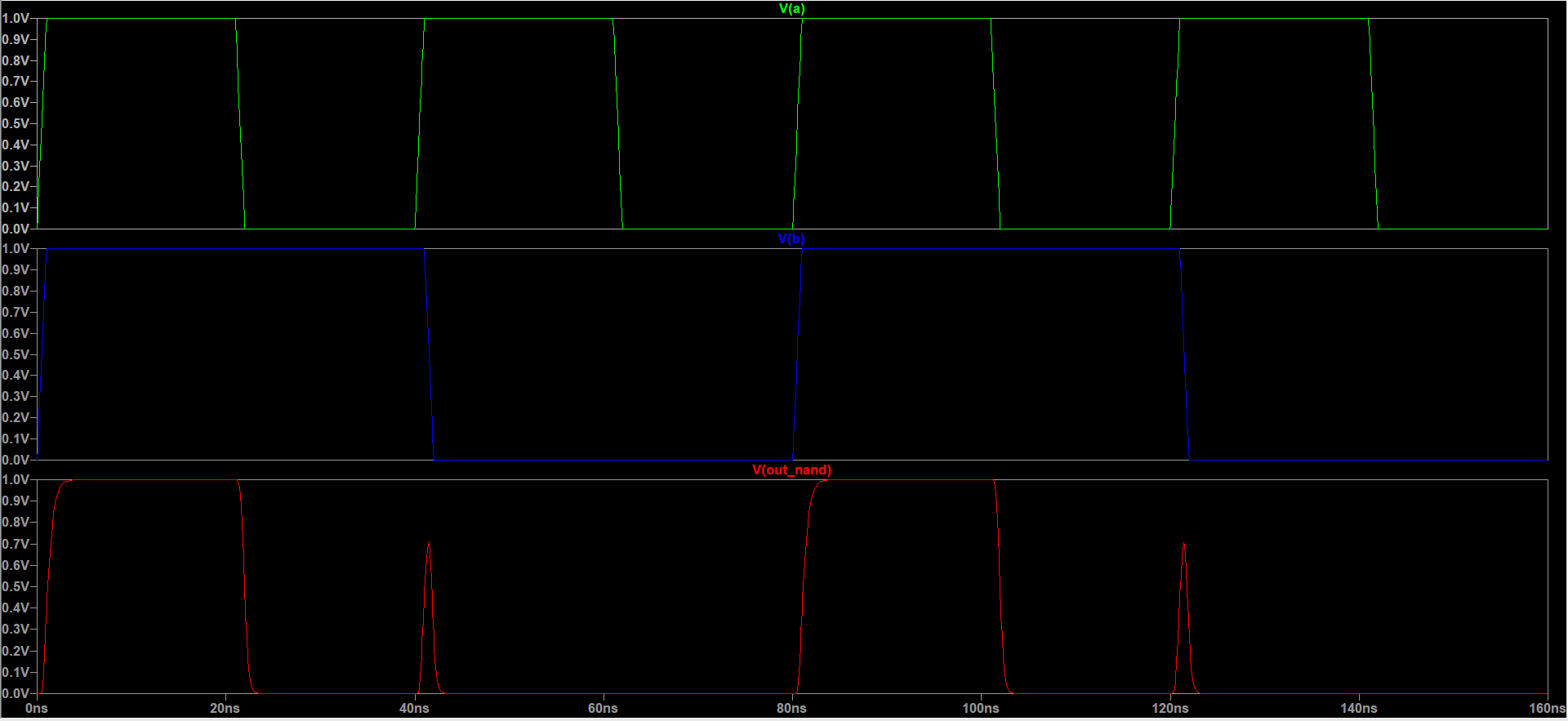


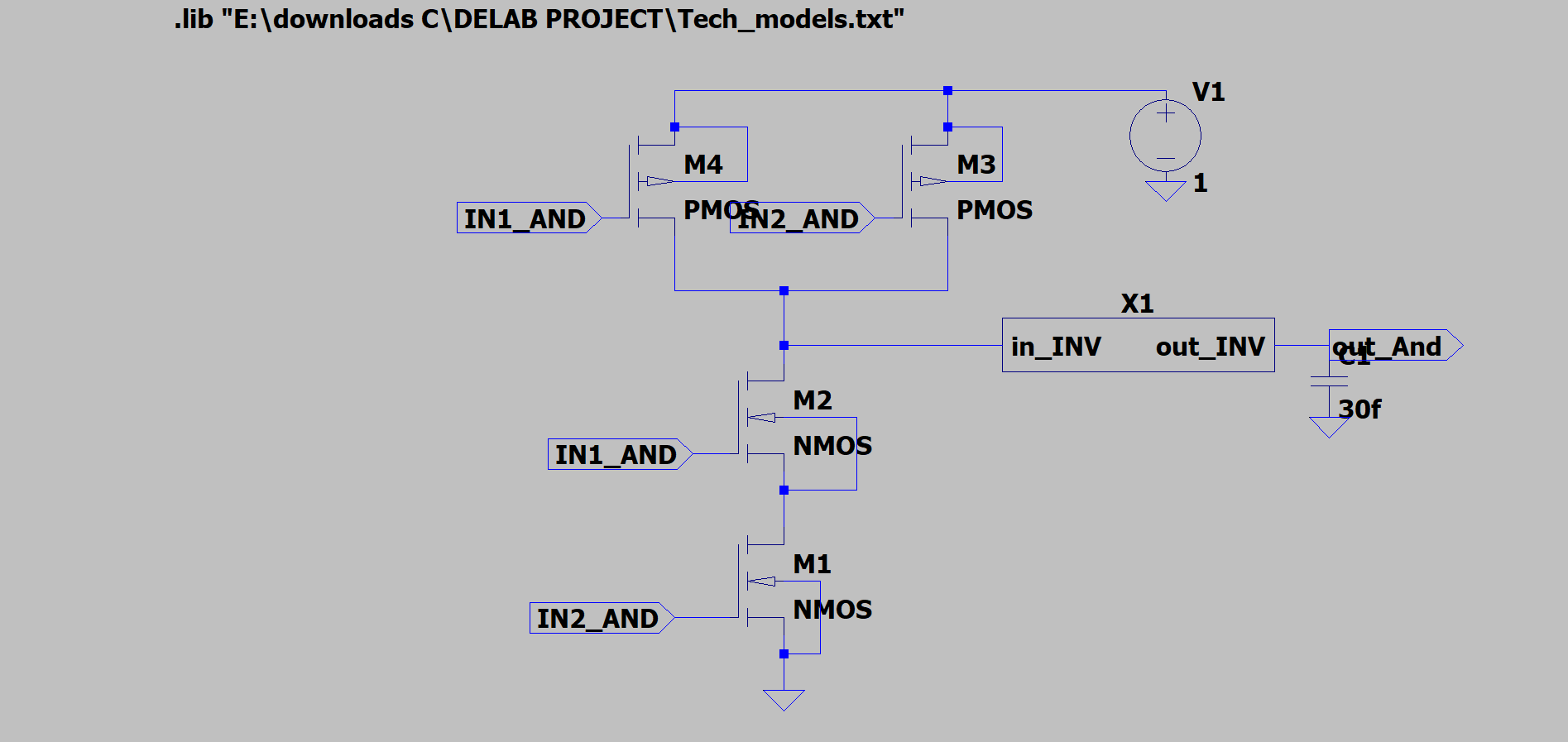


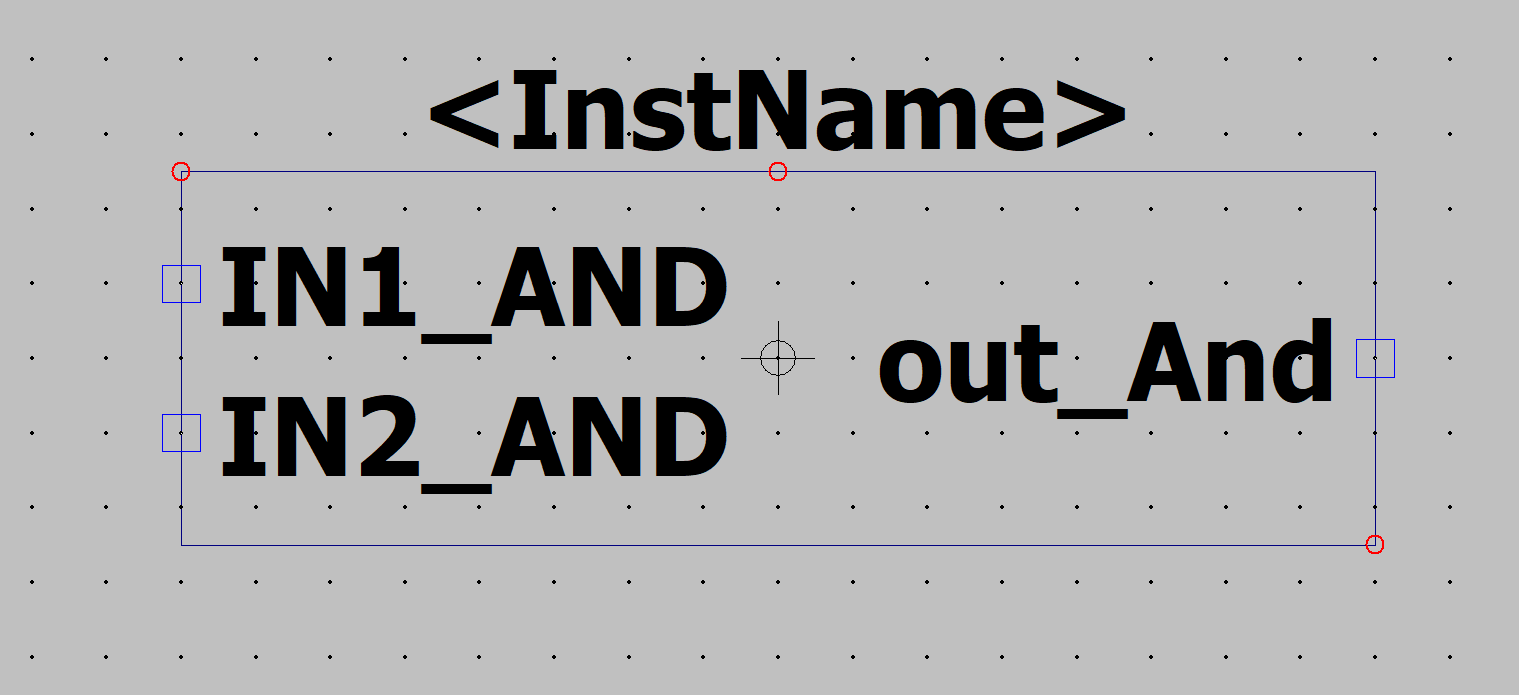
**AND Gate:**



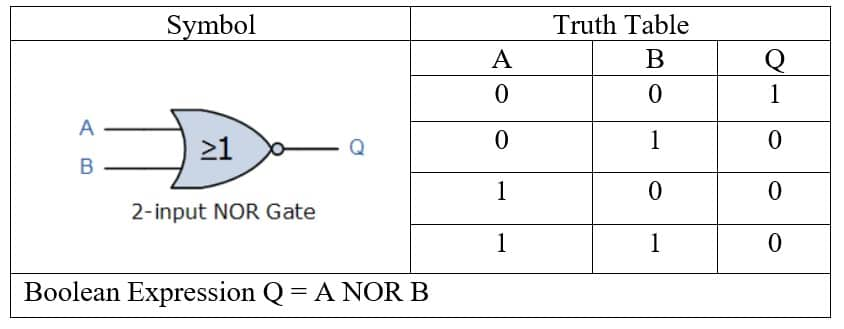


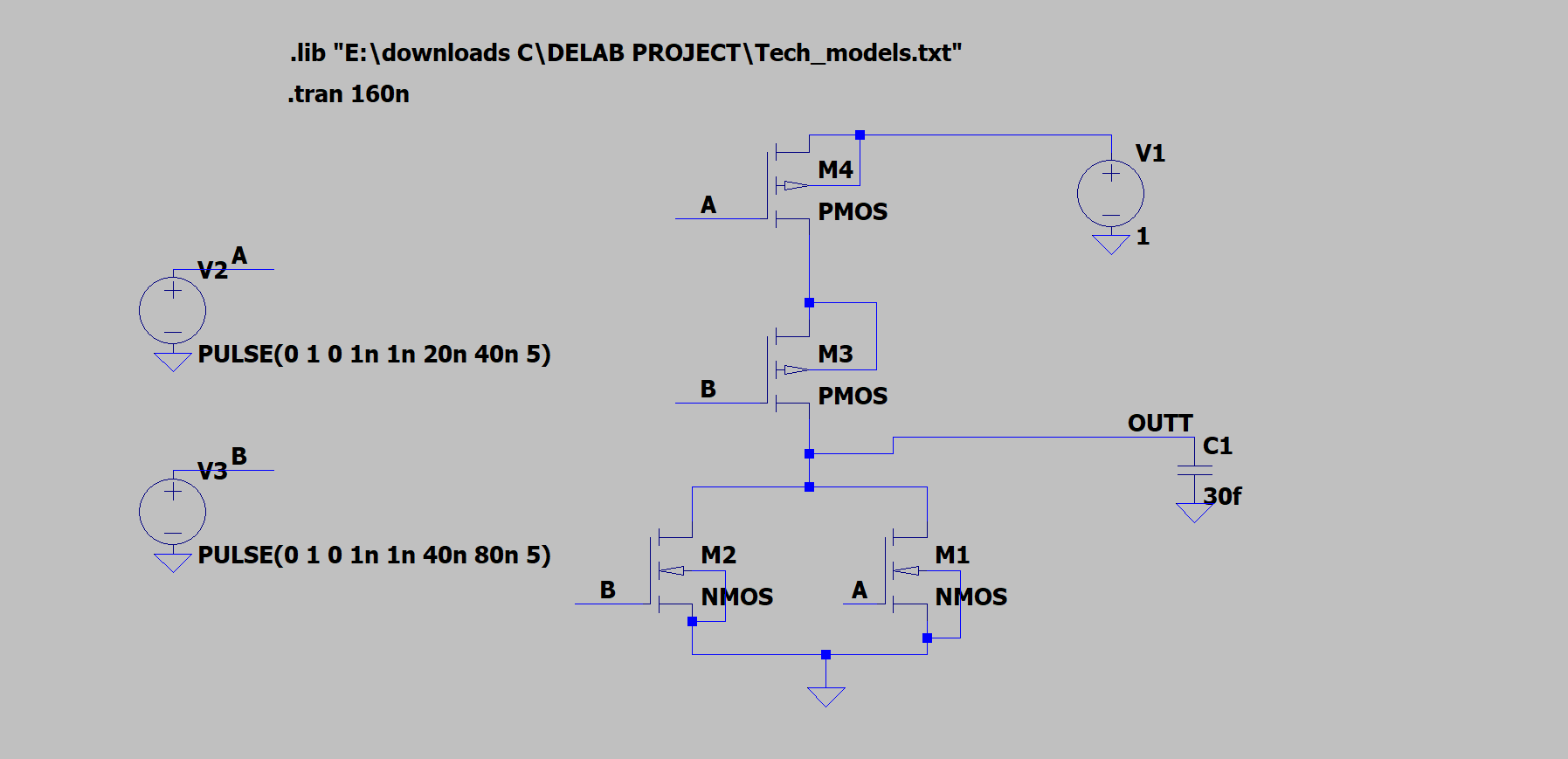


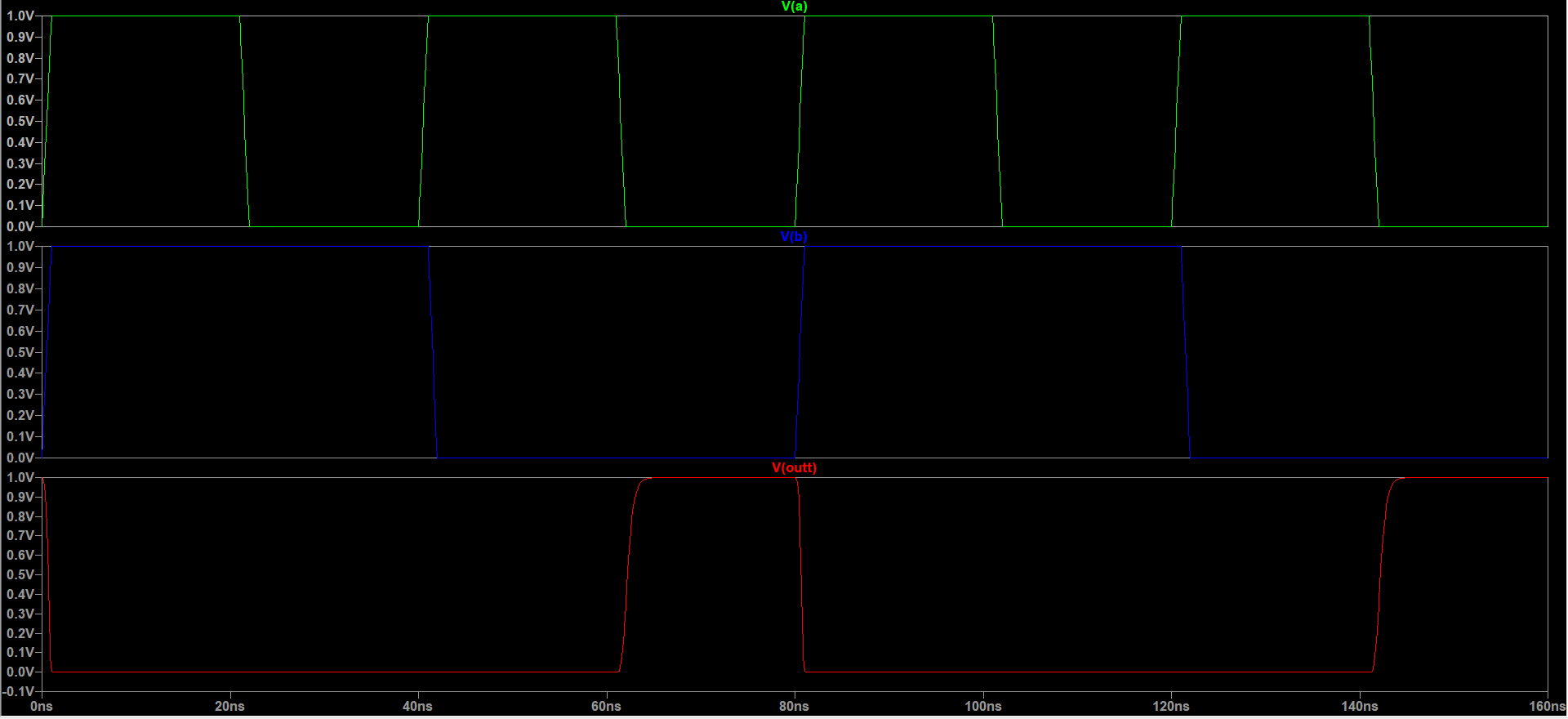


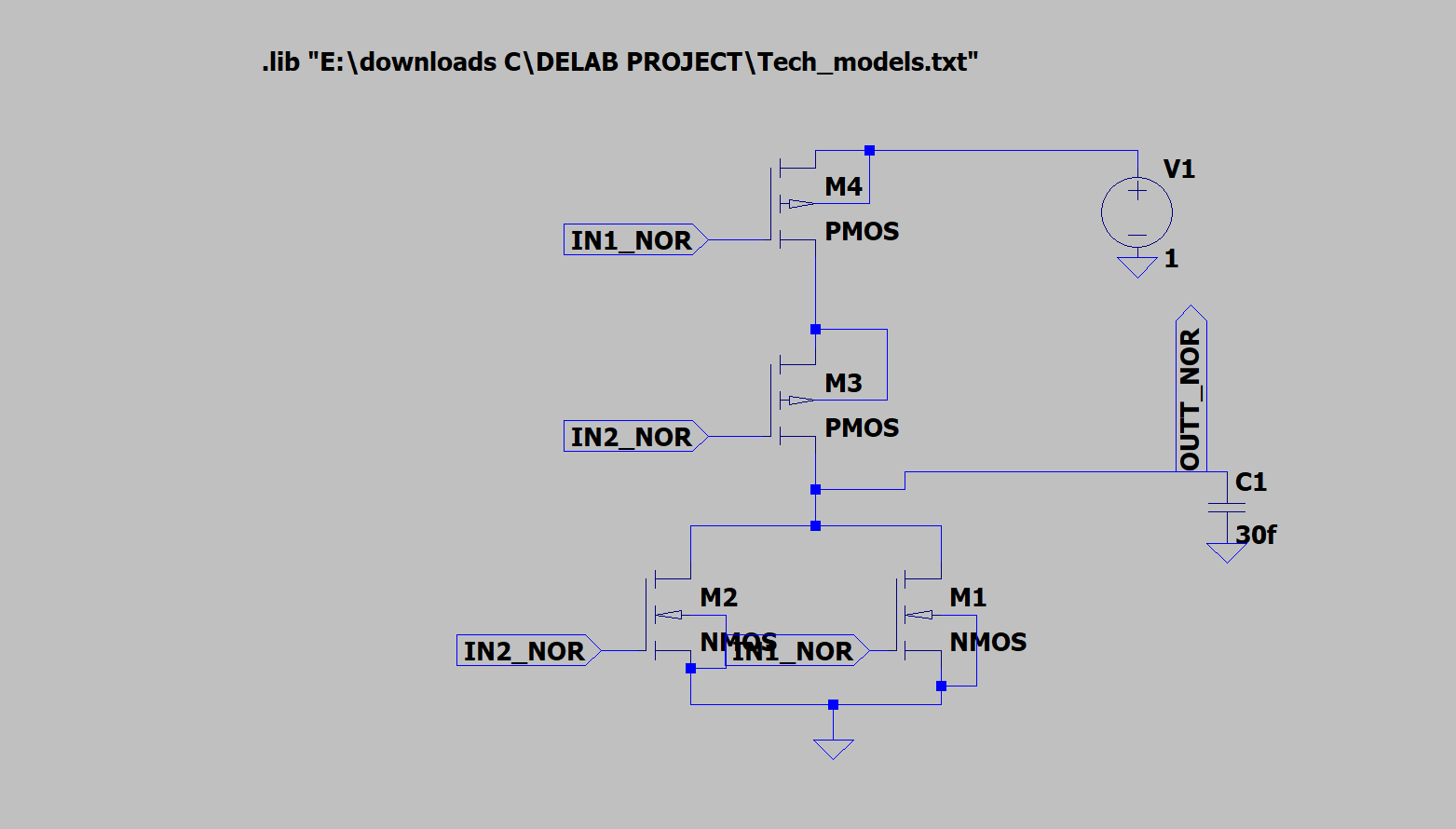


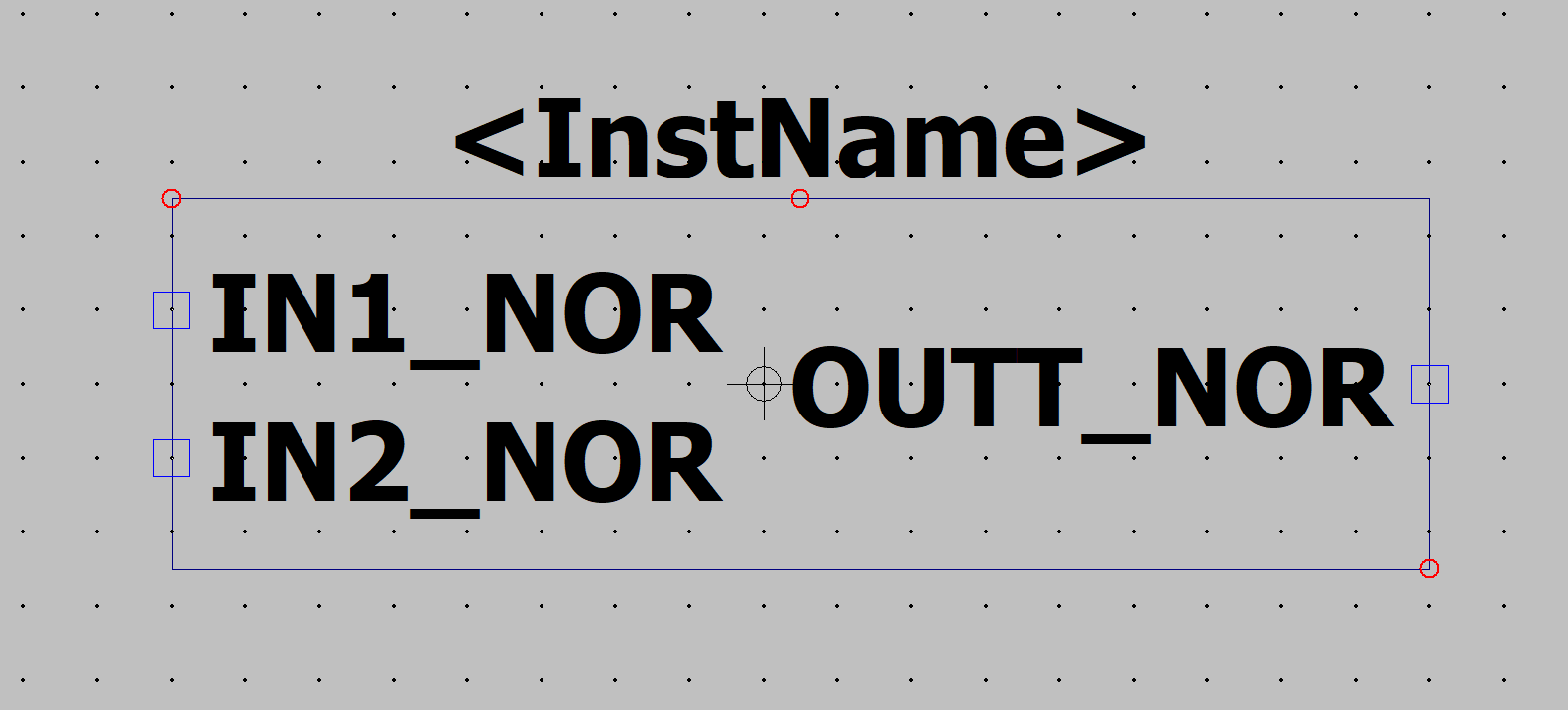
**NOR Gate:**



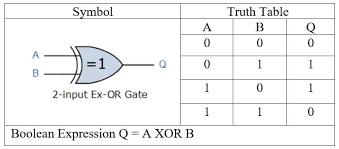


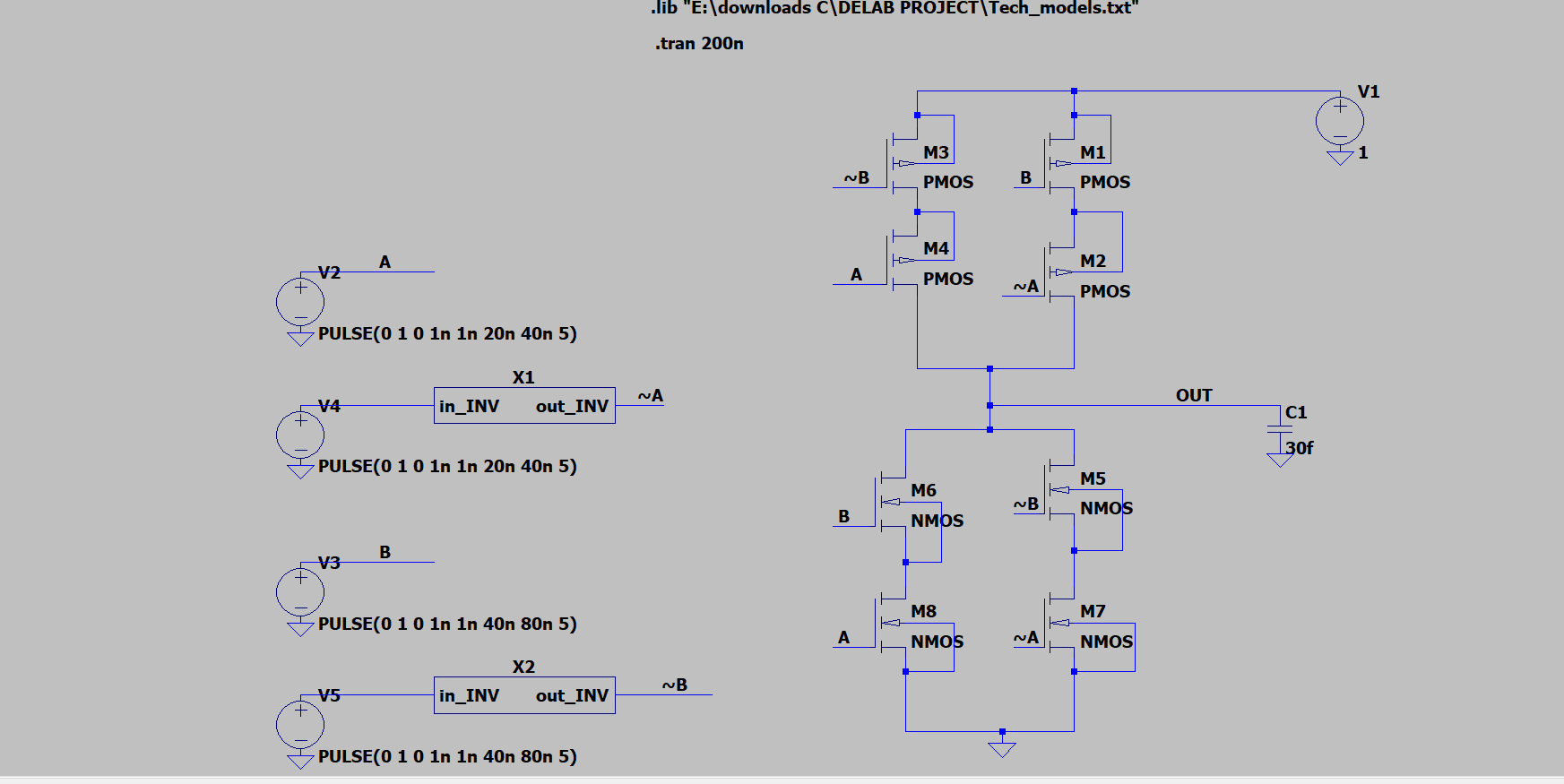


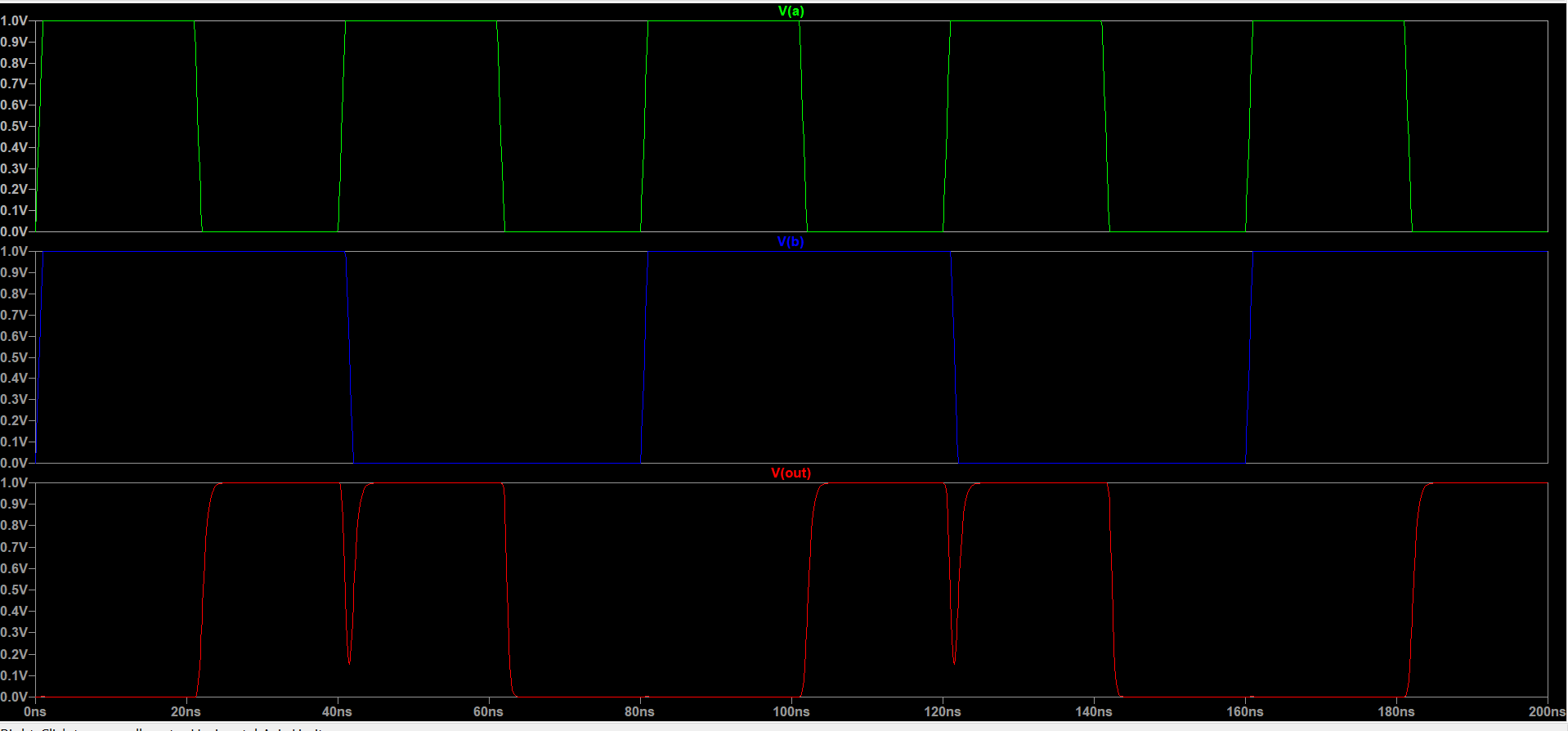


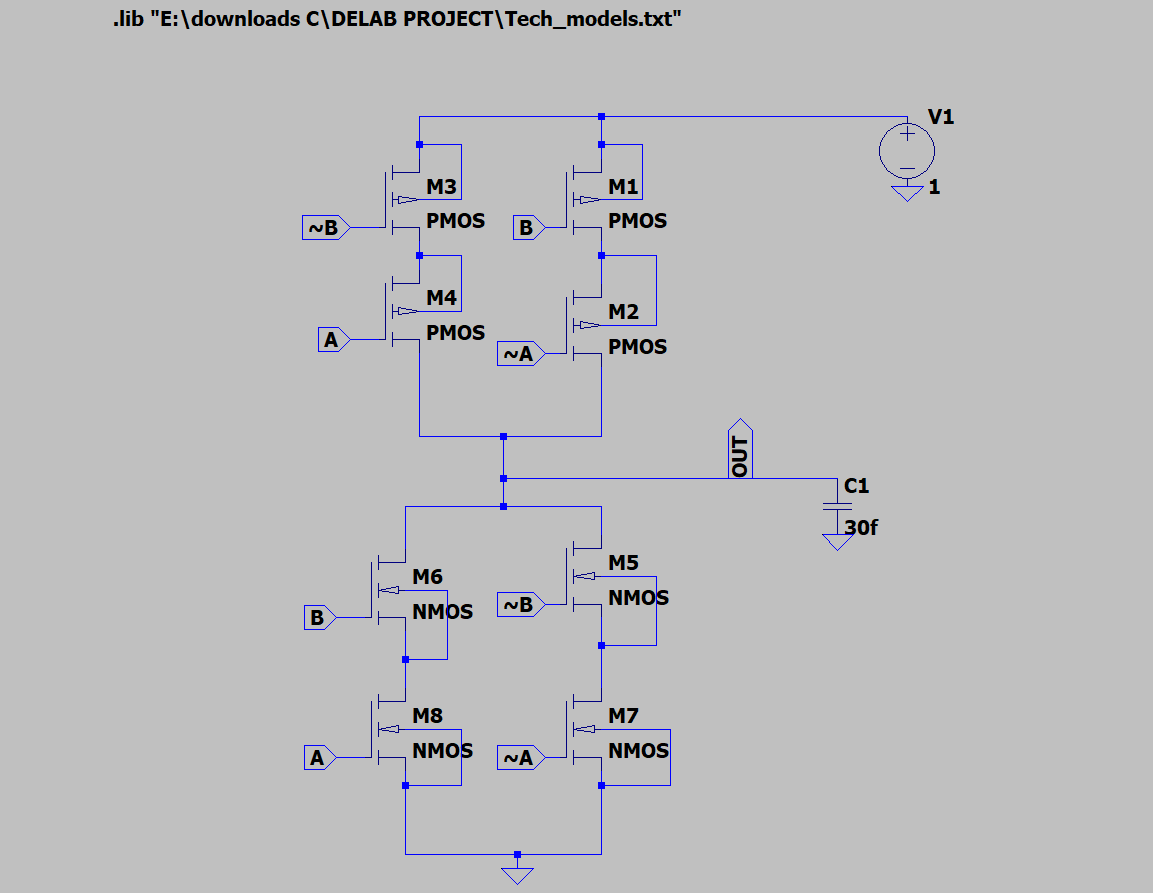


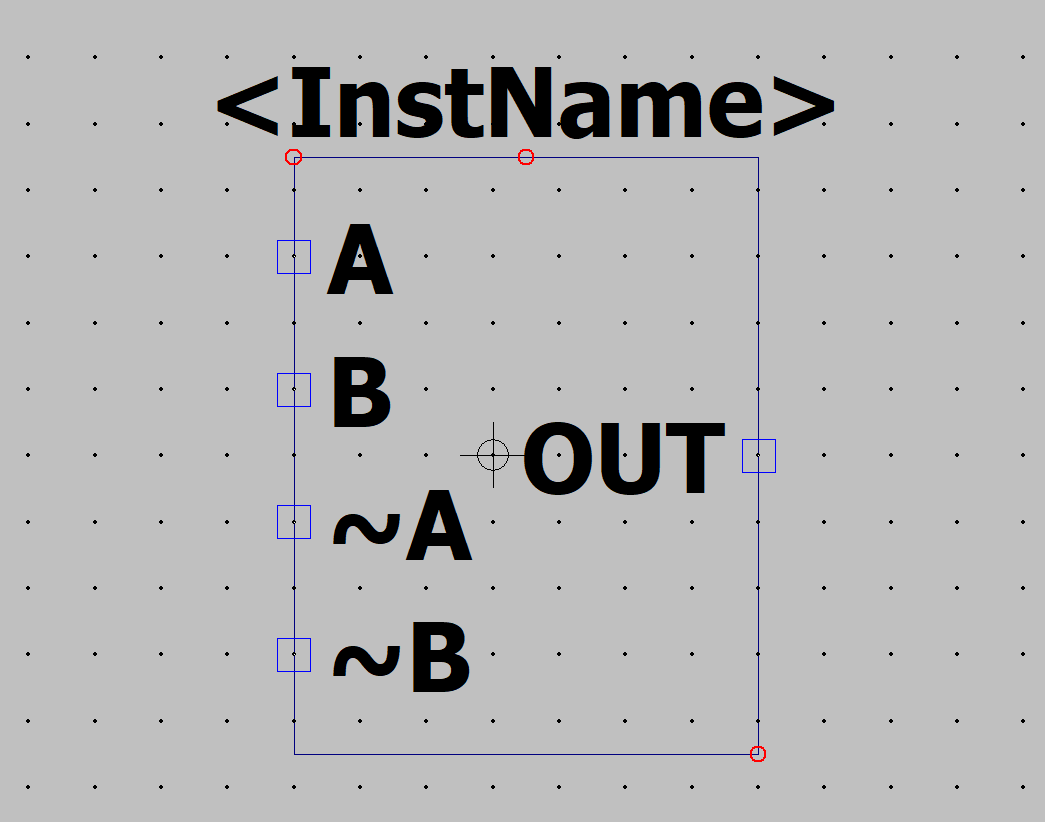
**XOR Gate:**

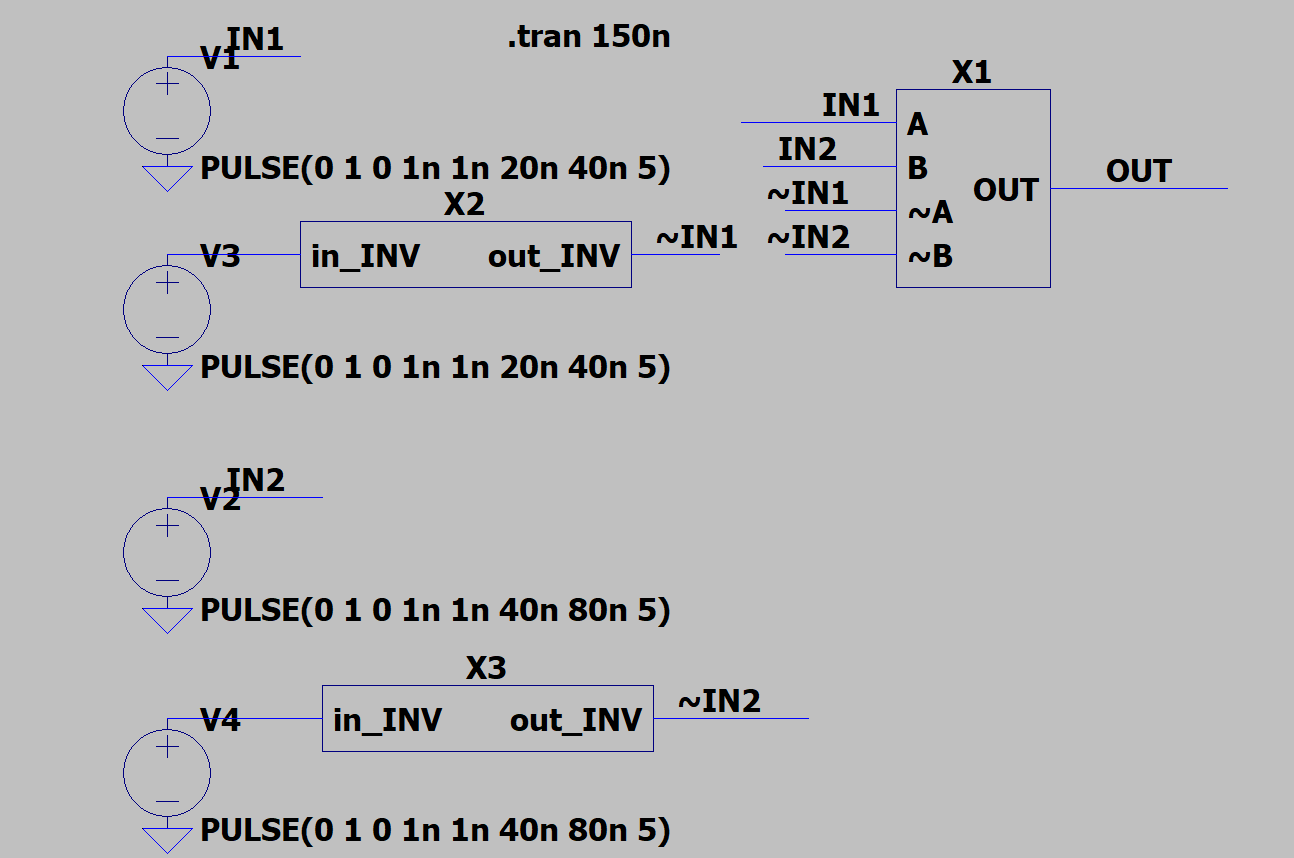


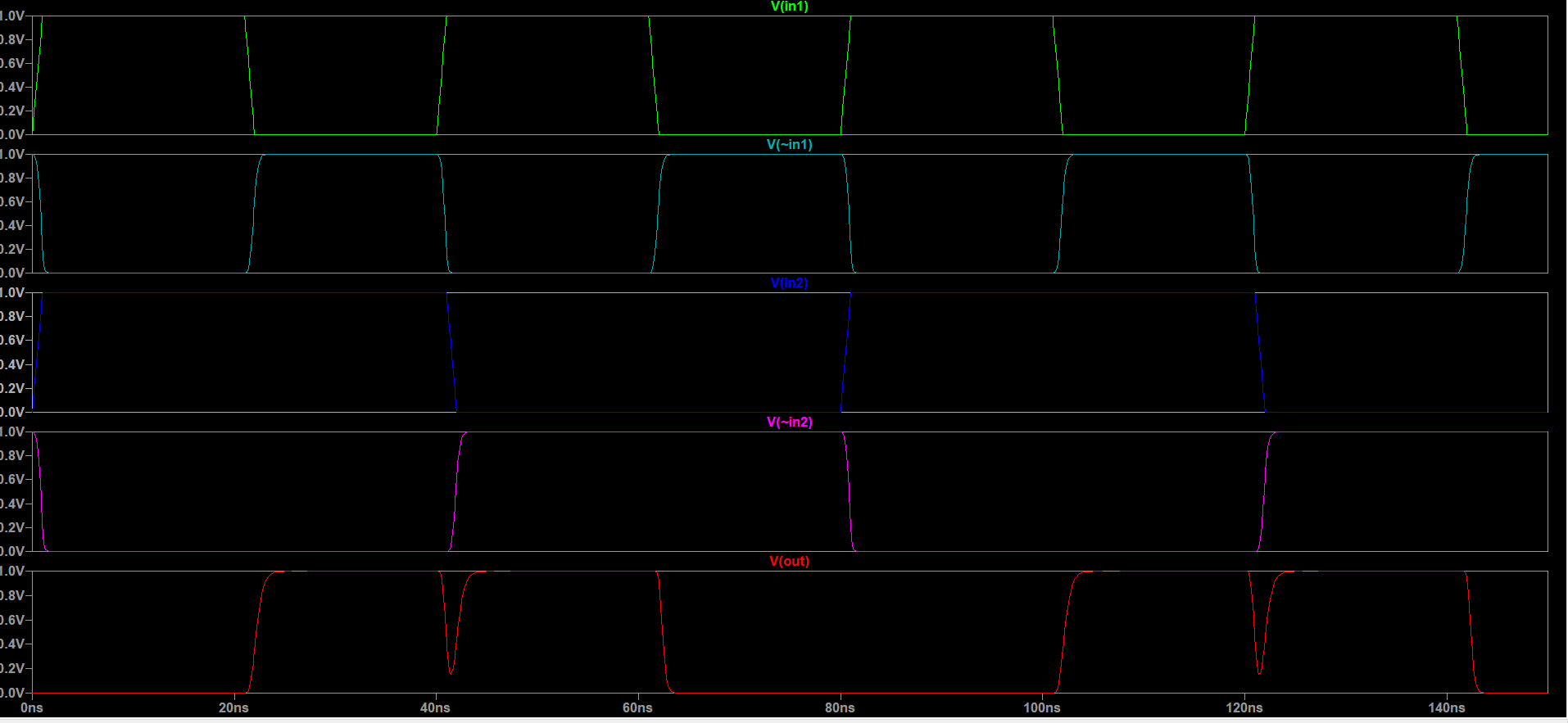




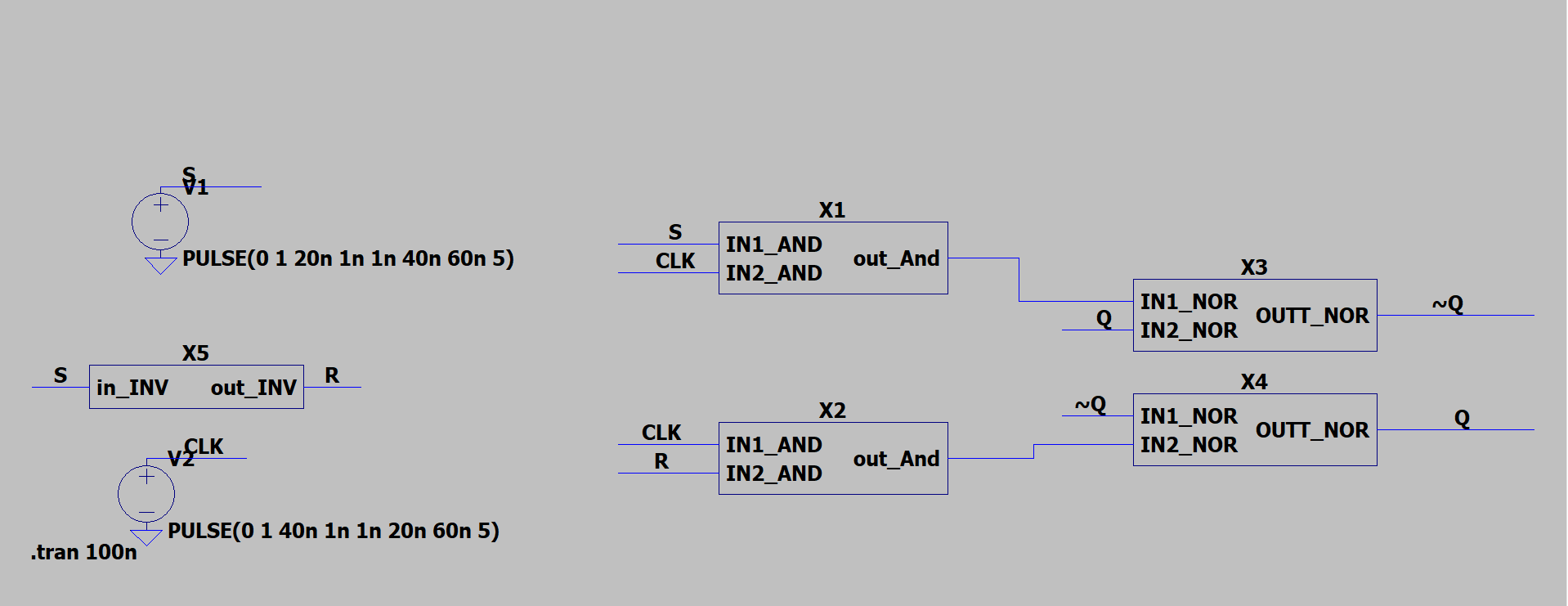


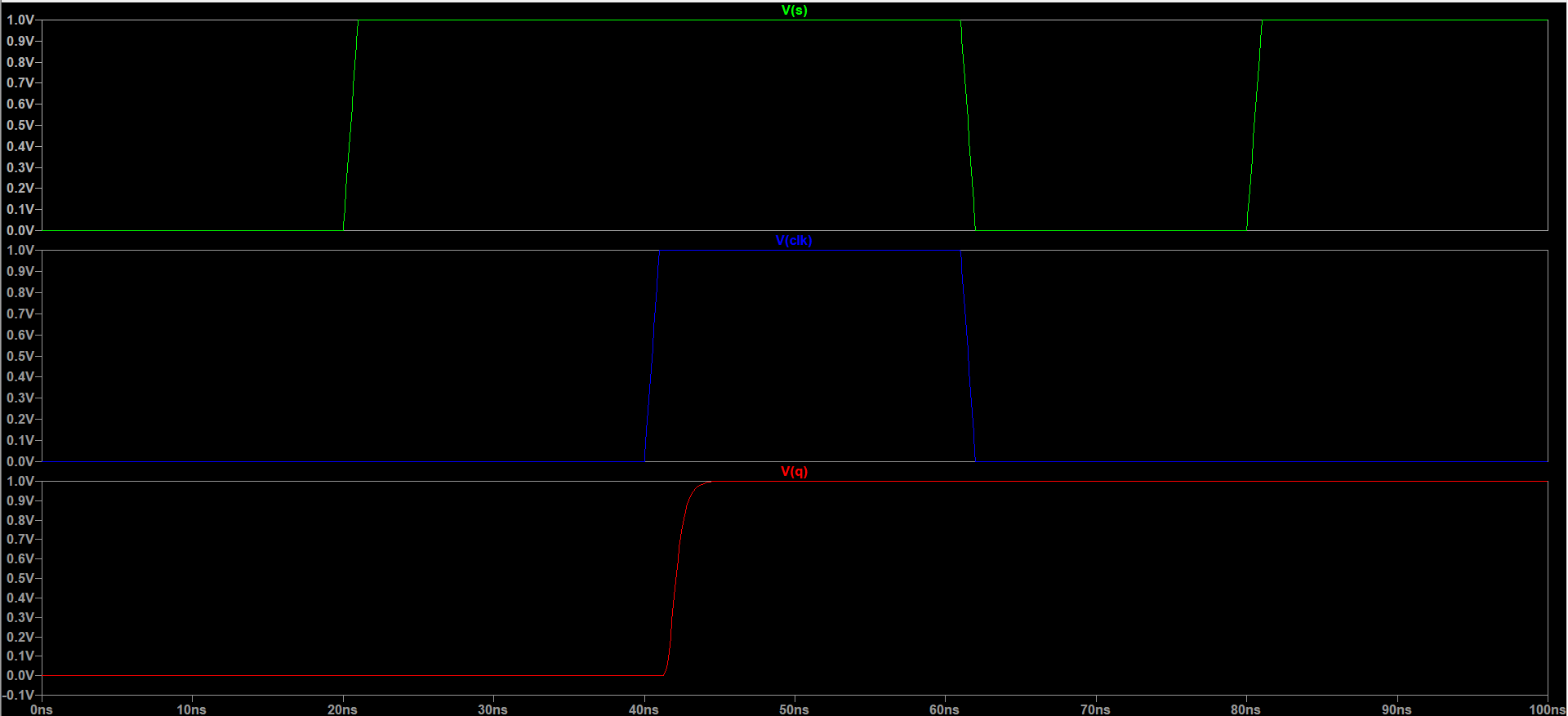




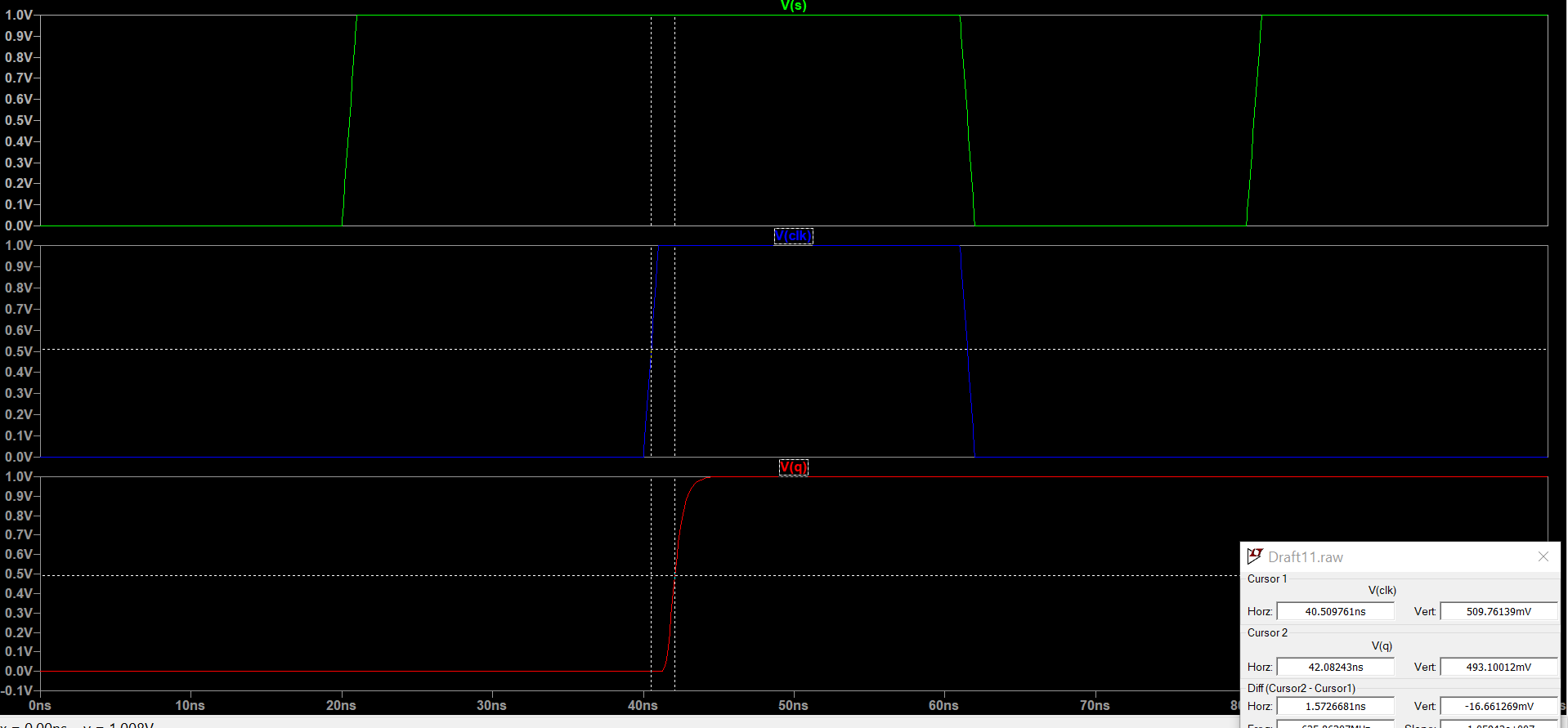


**SR LATCH:**

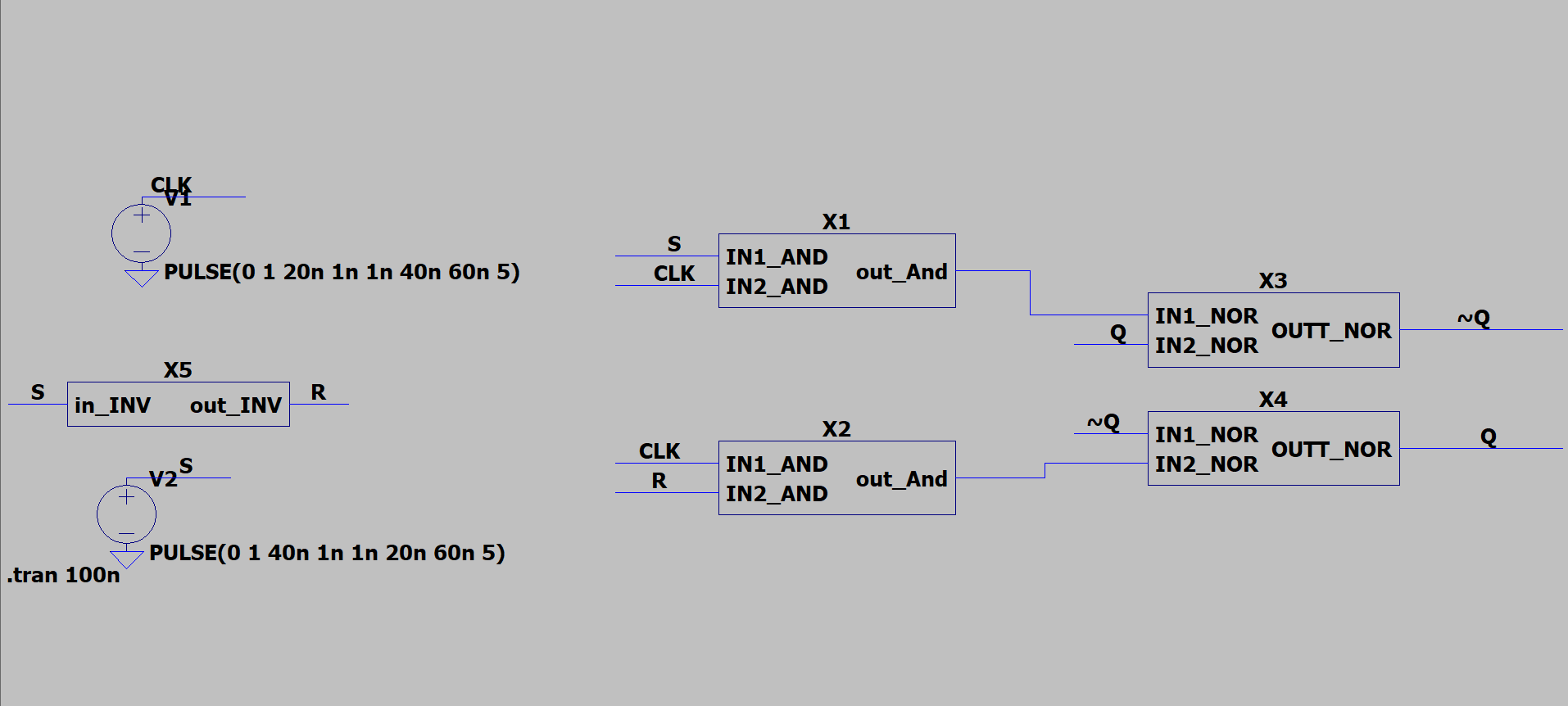


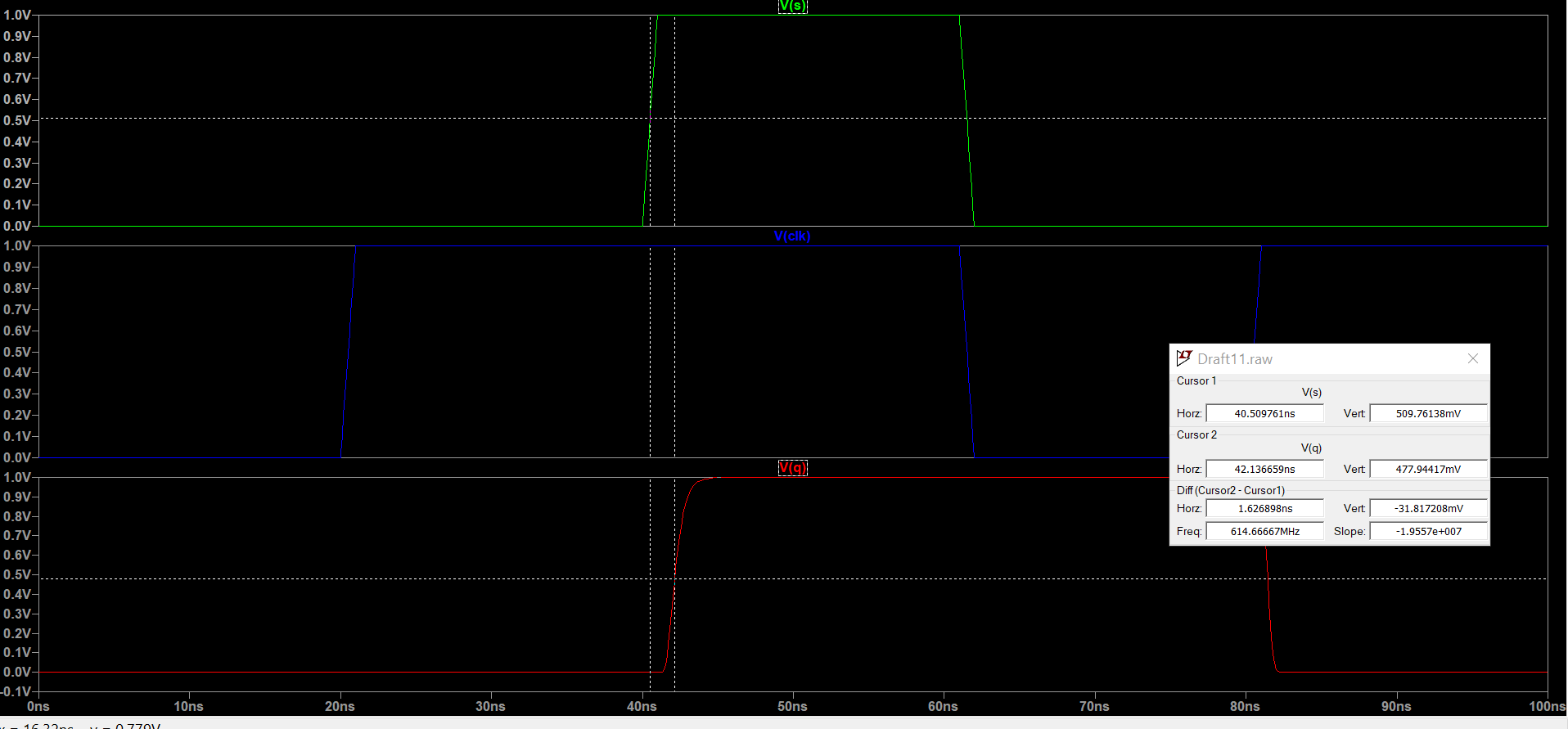


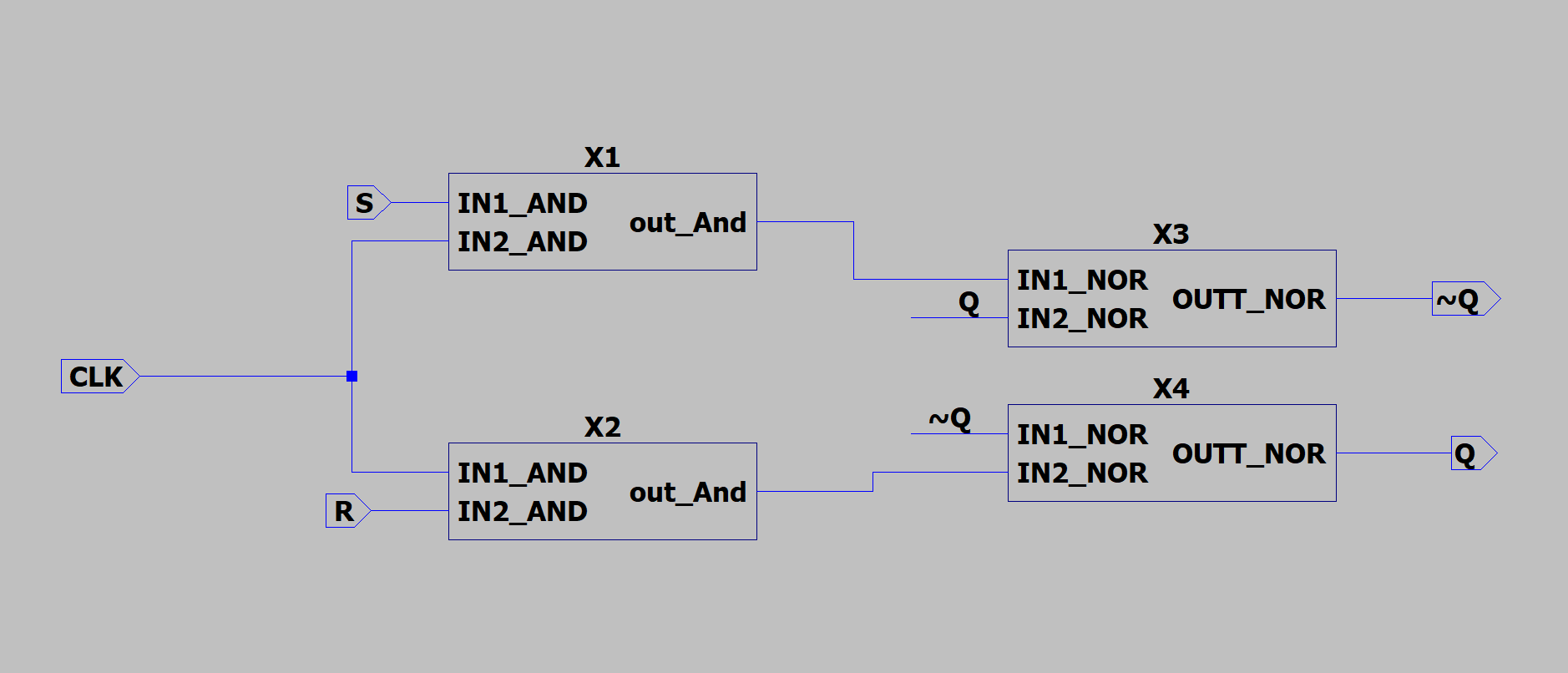
CLK To Q:

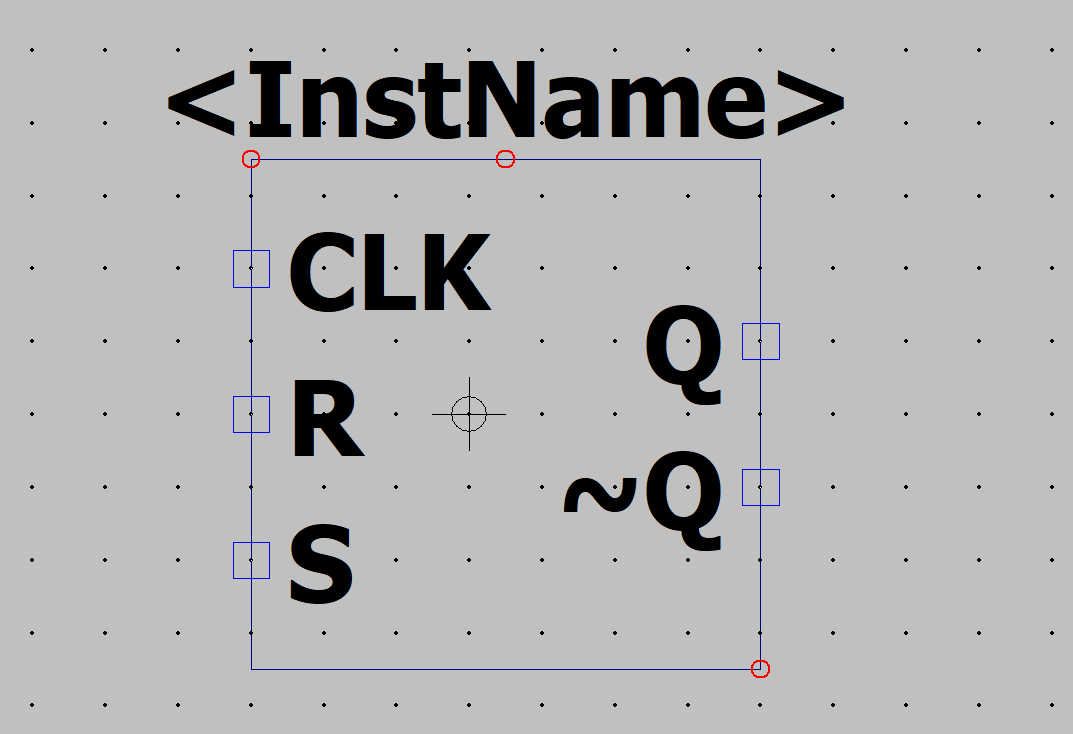


D To Q:

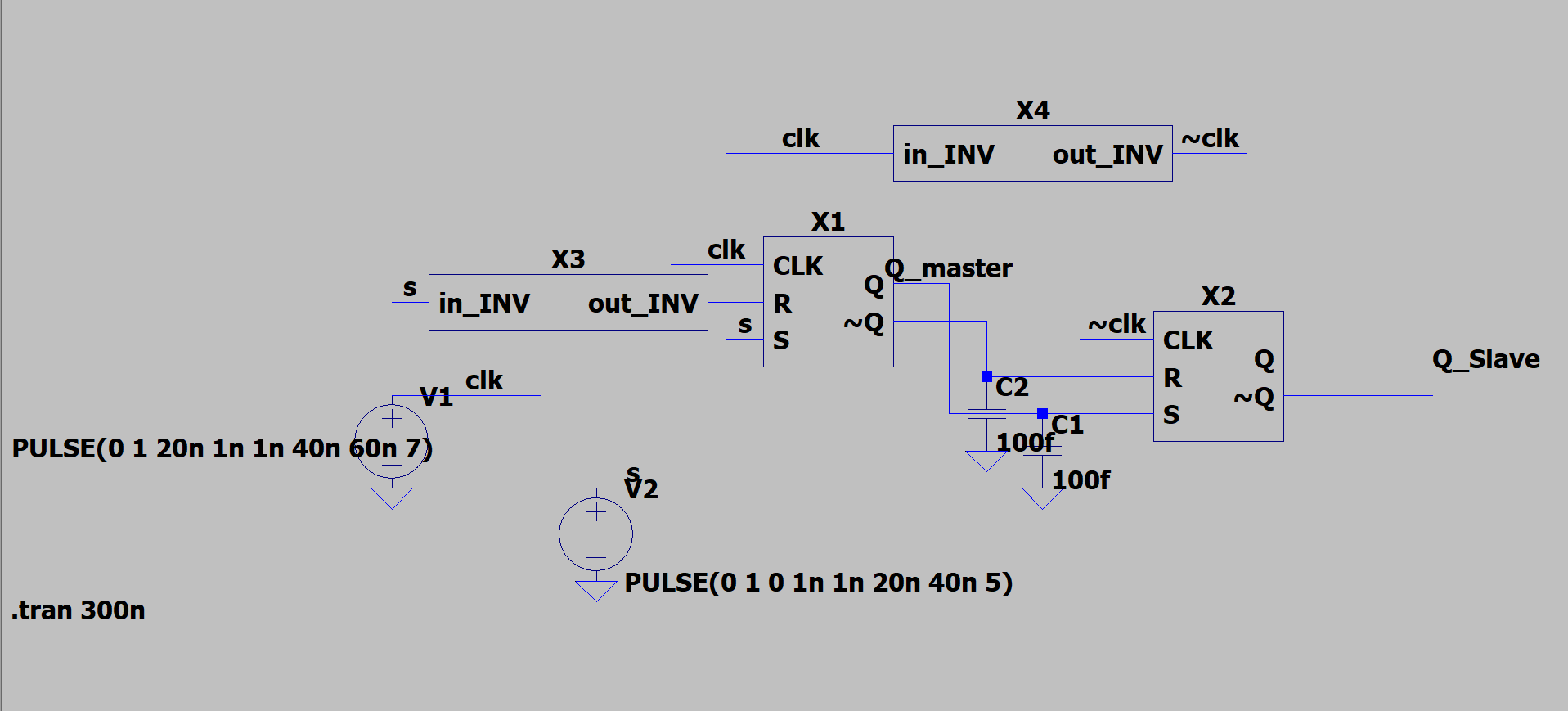


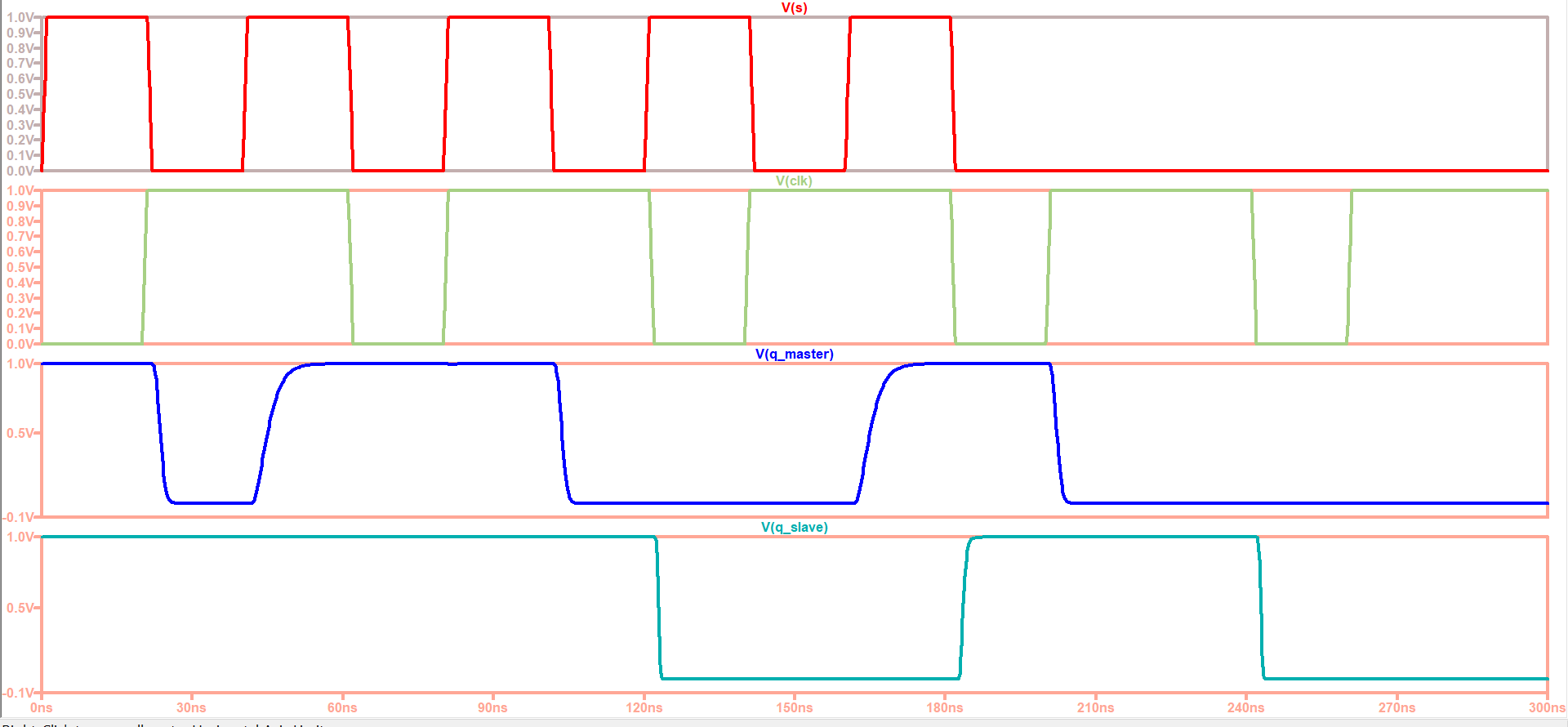






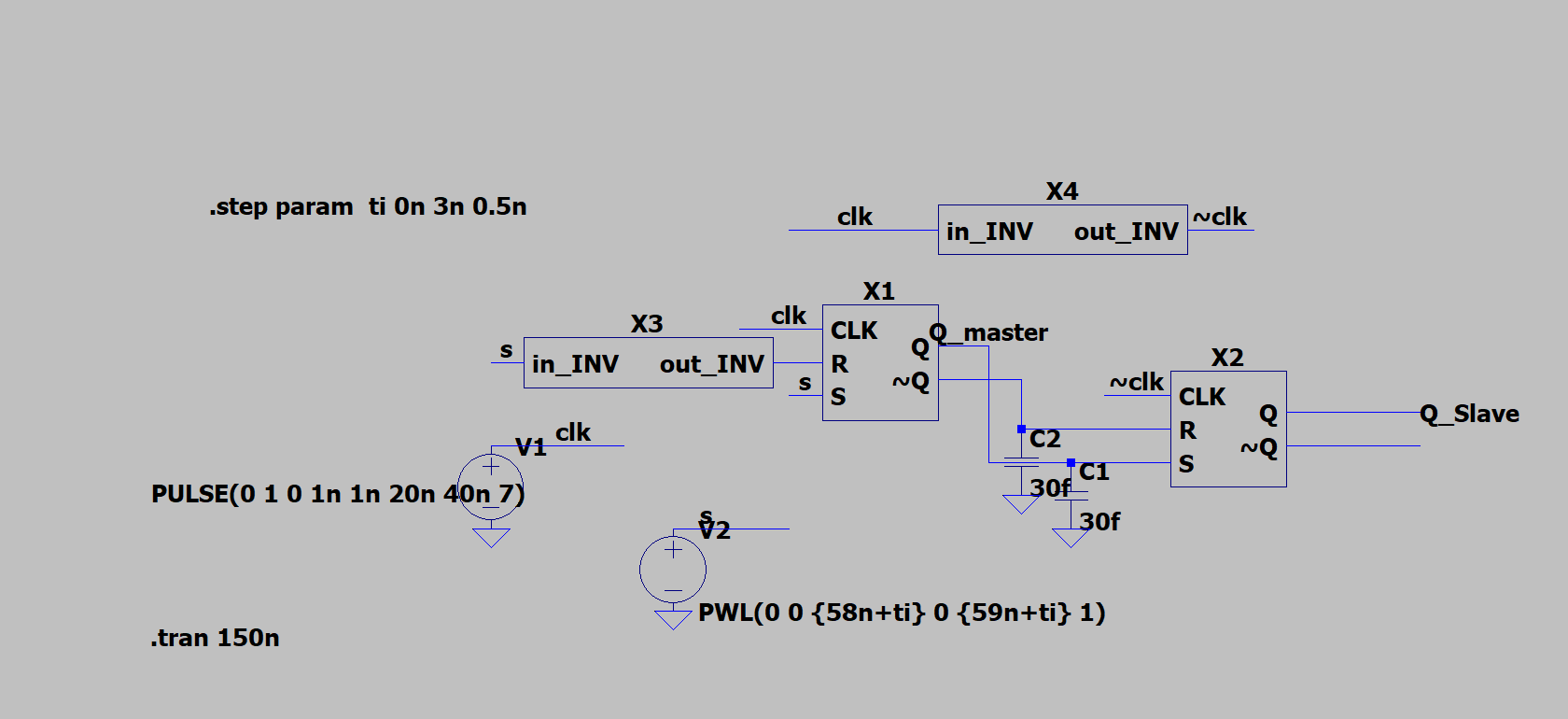
**D Flip Flop:**

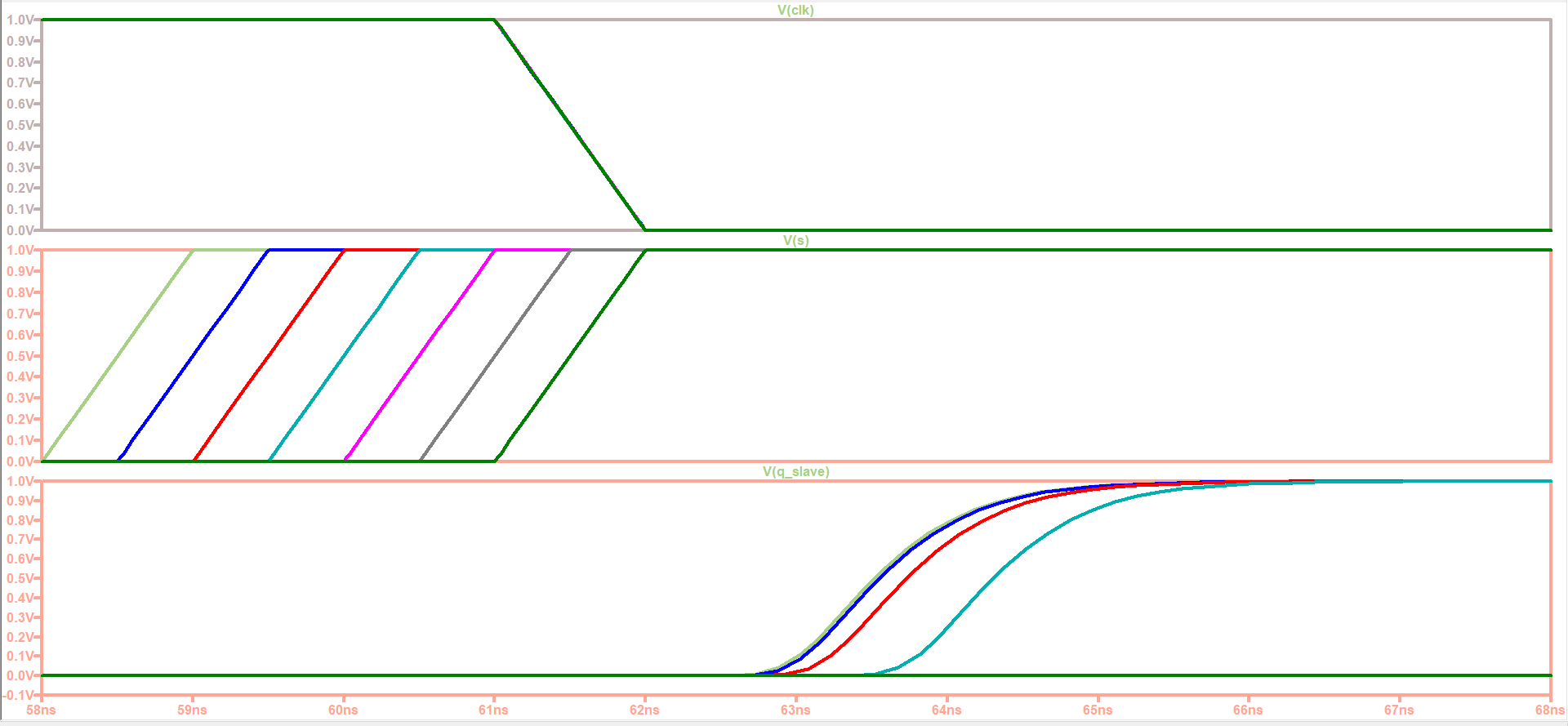




setup time :

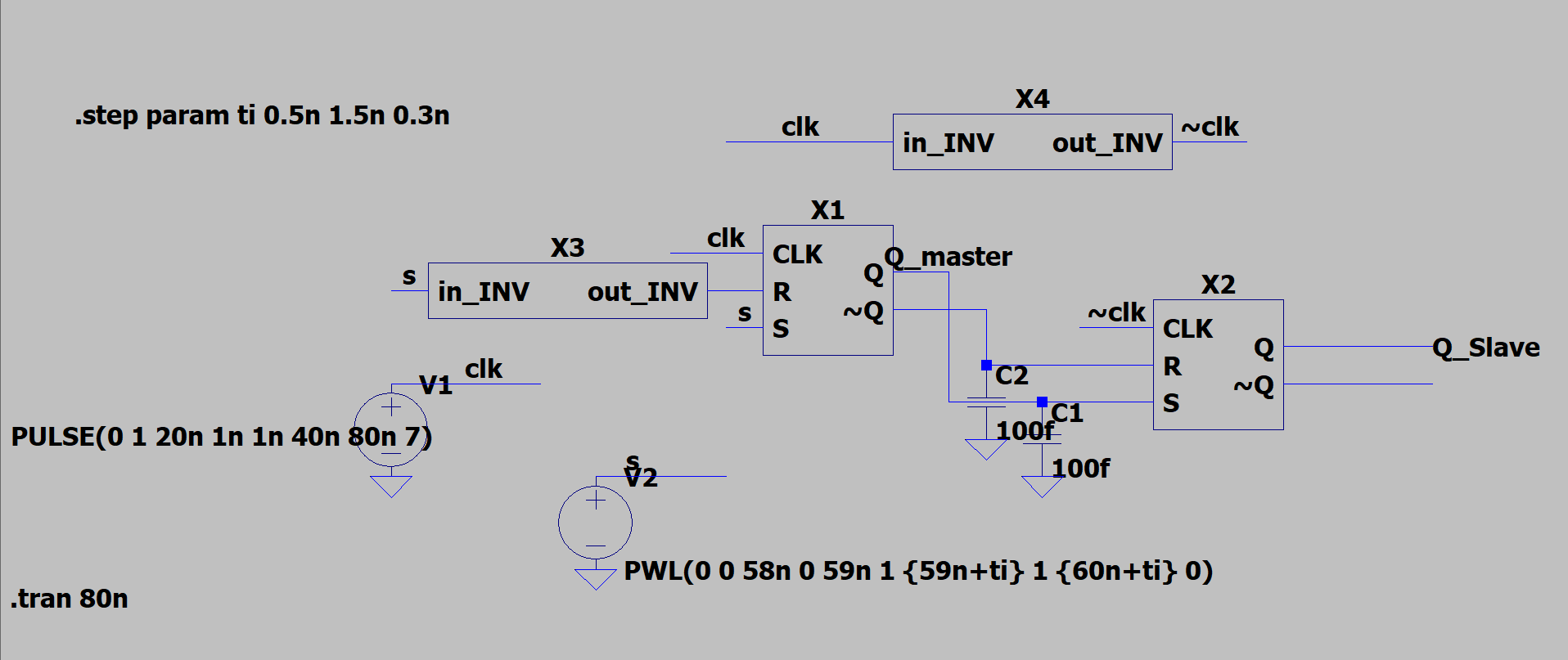
the signal should appear befor 2ns.

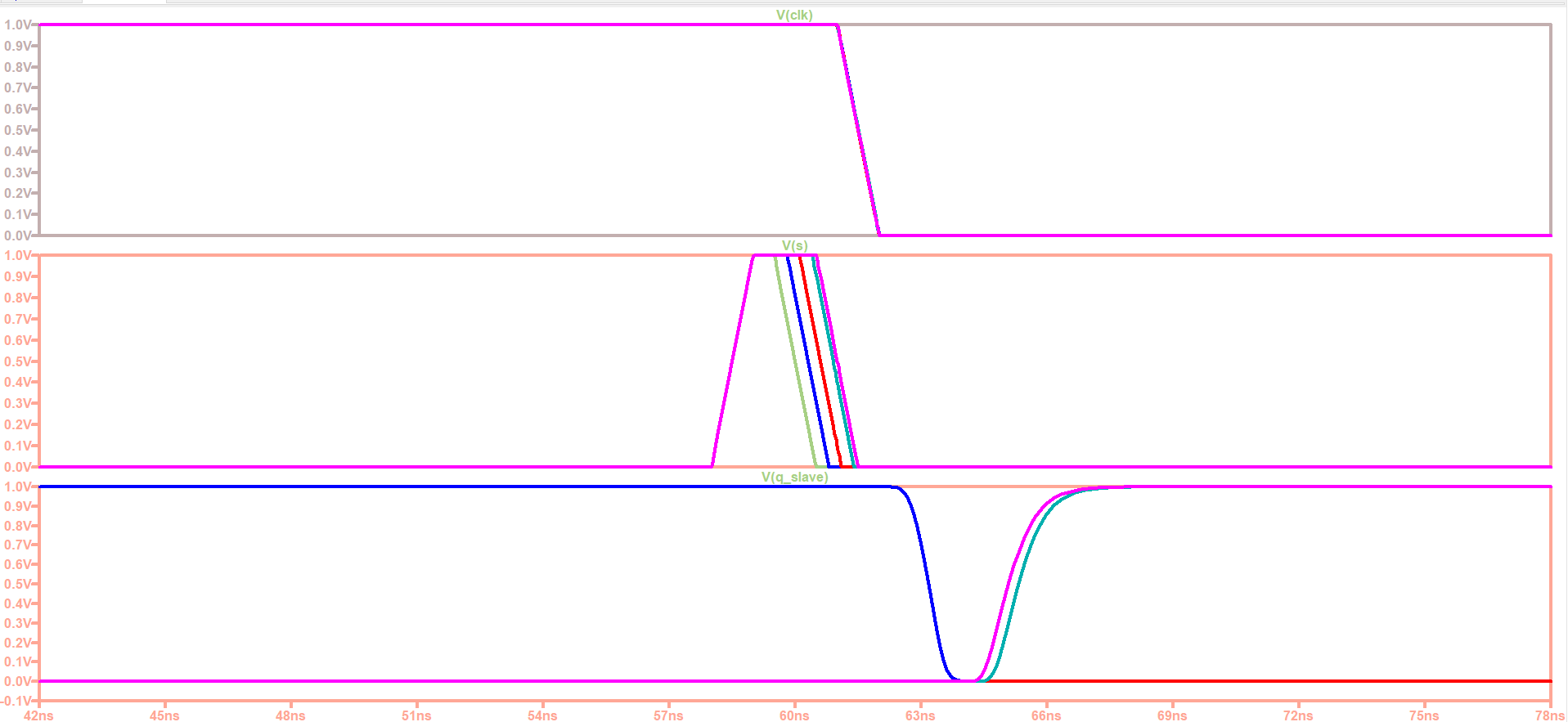


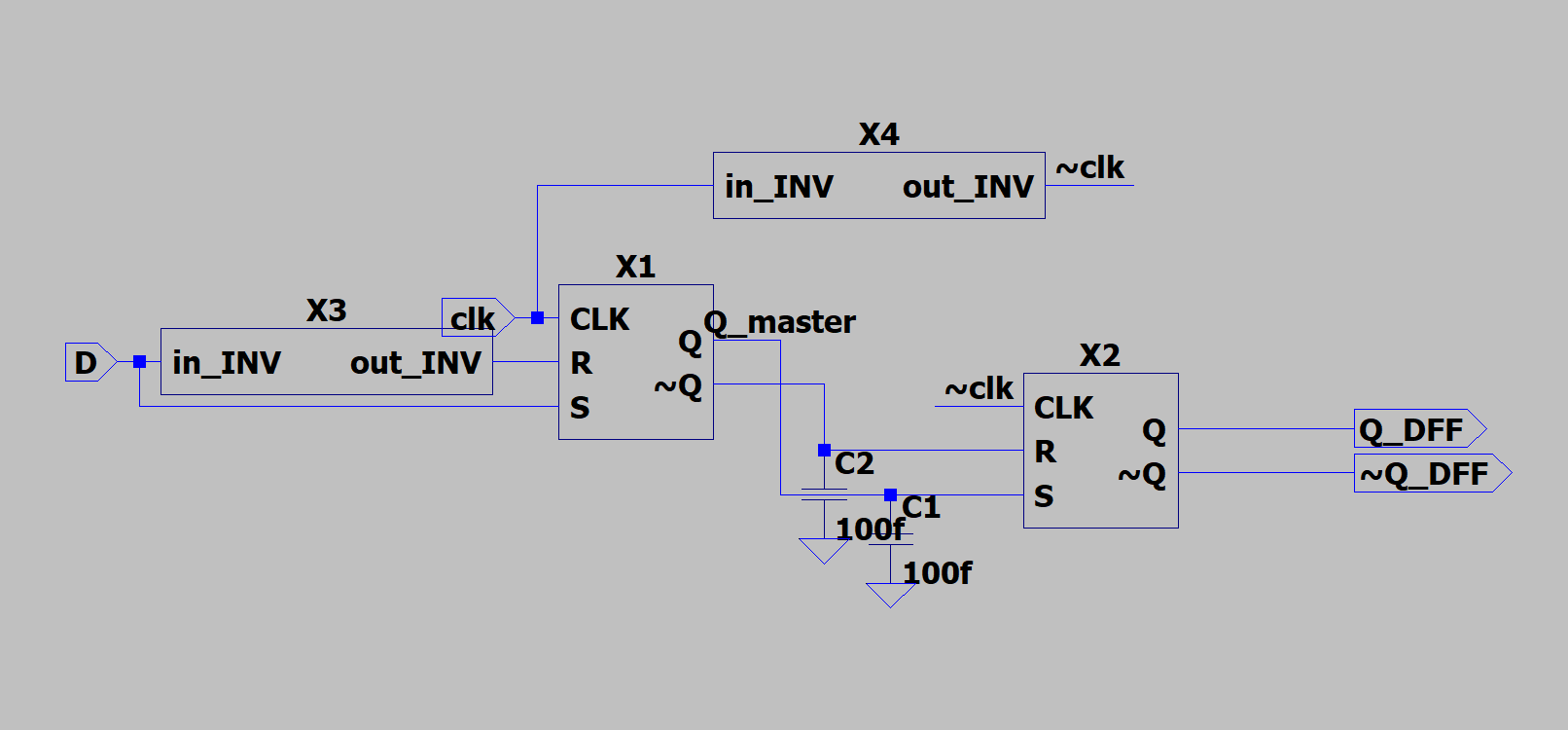


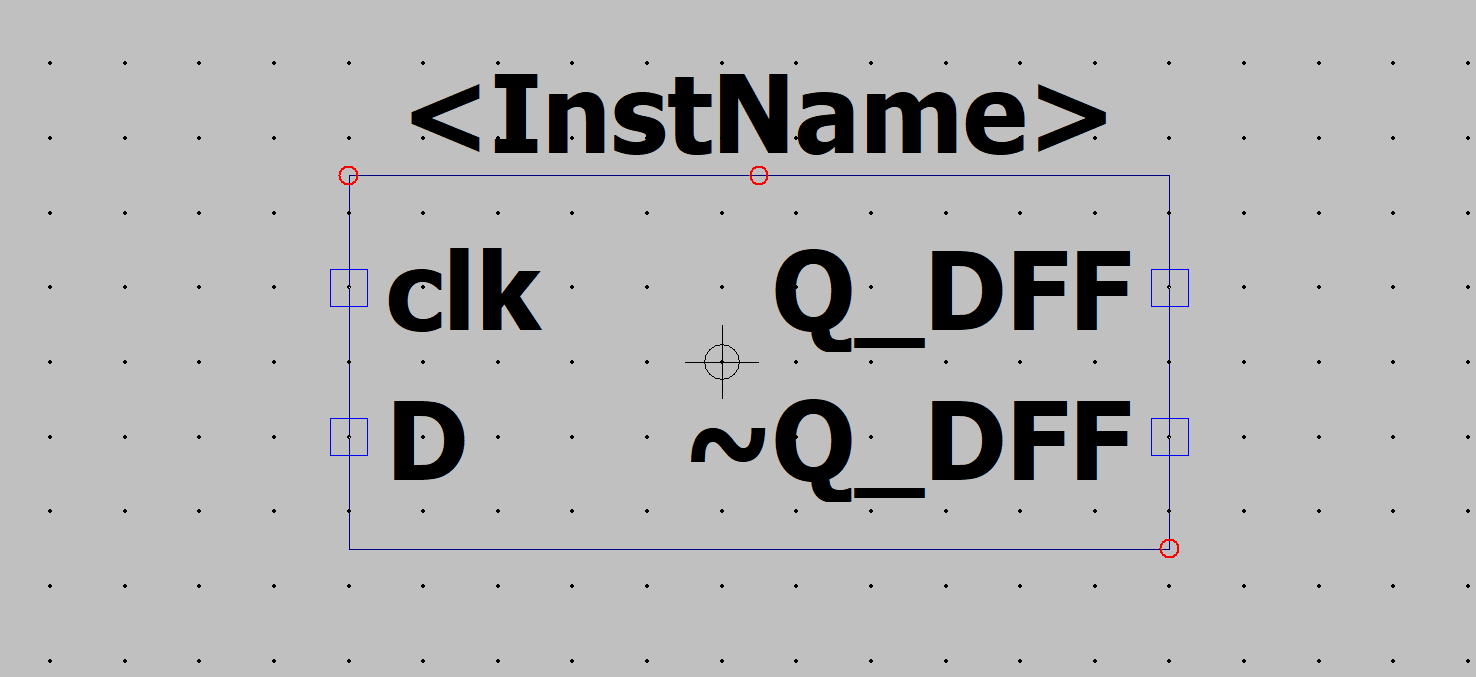
hold time :

if the signal goes to zero befor 0.7n or more this change will not appear on Q.

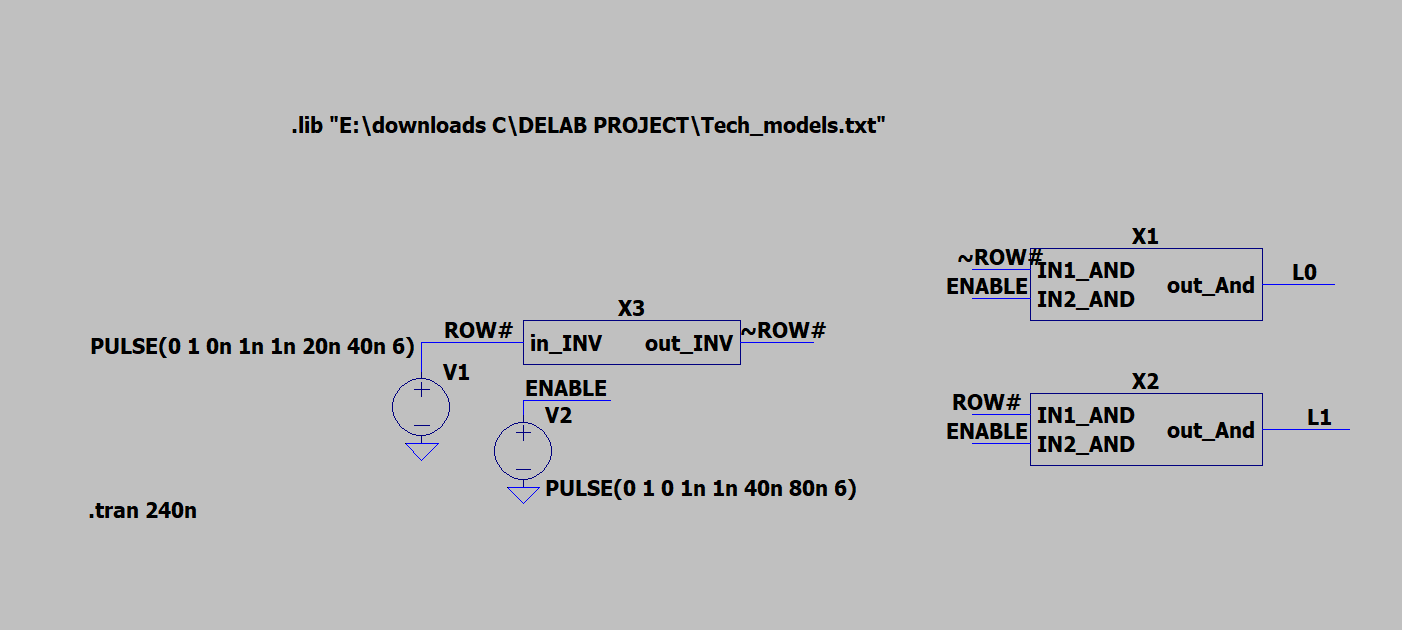


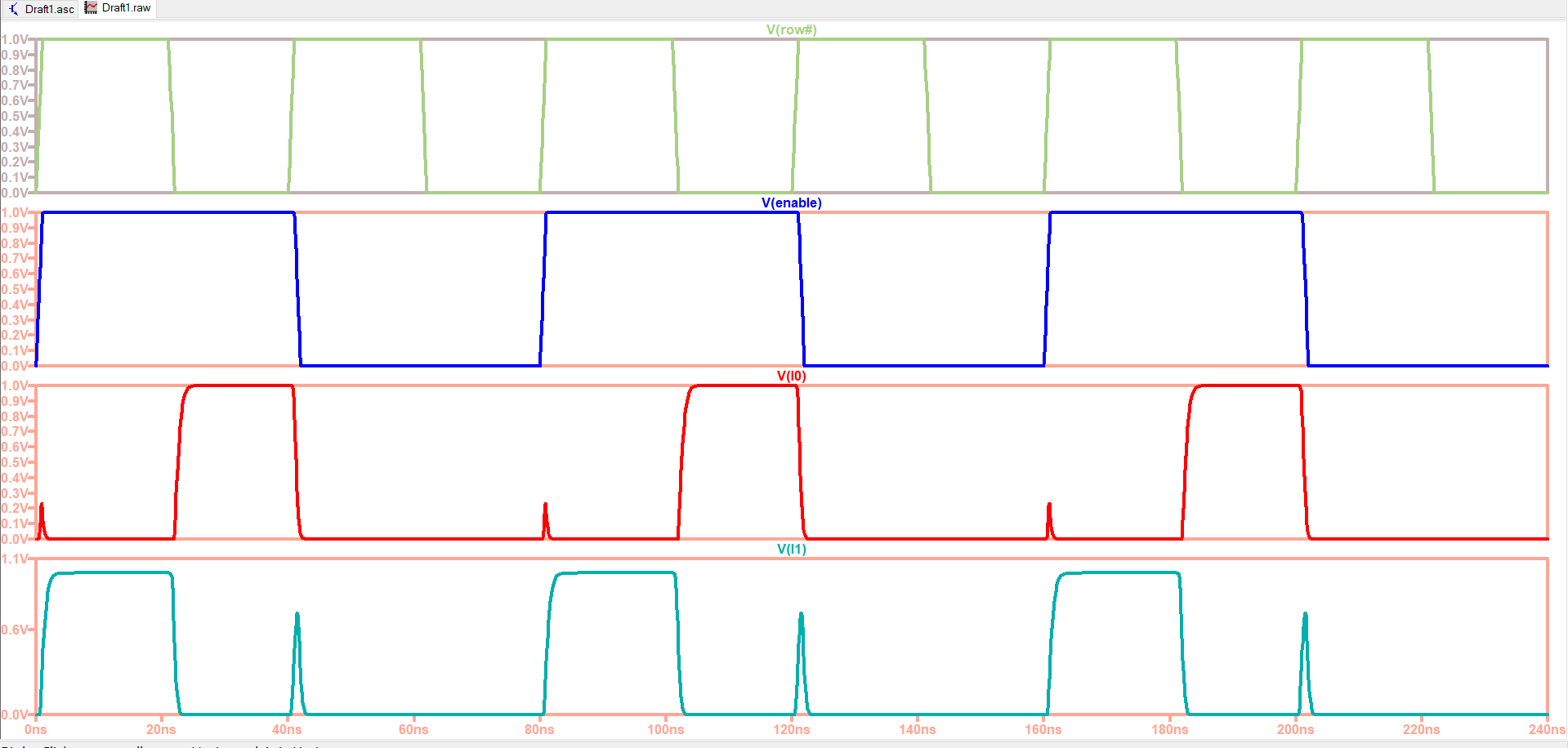


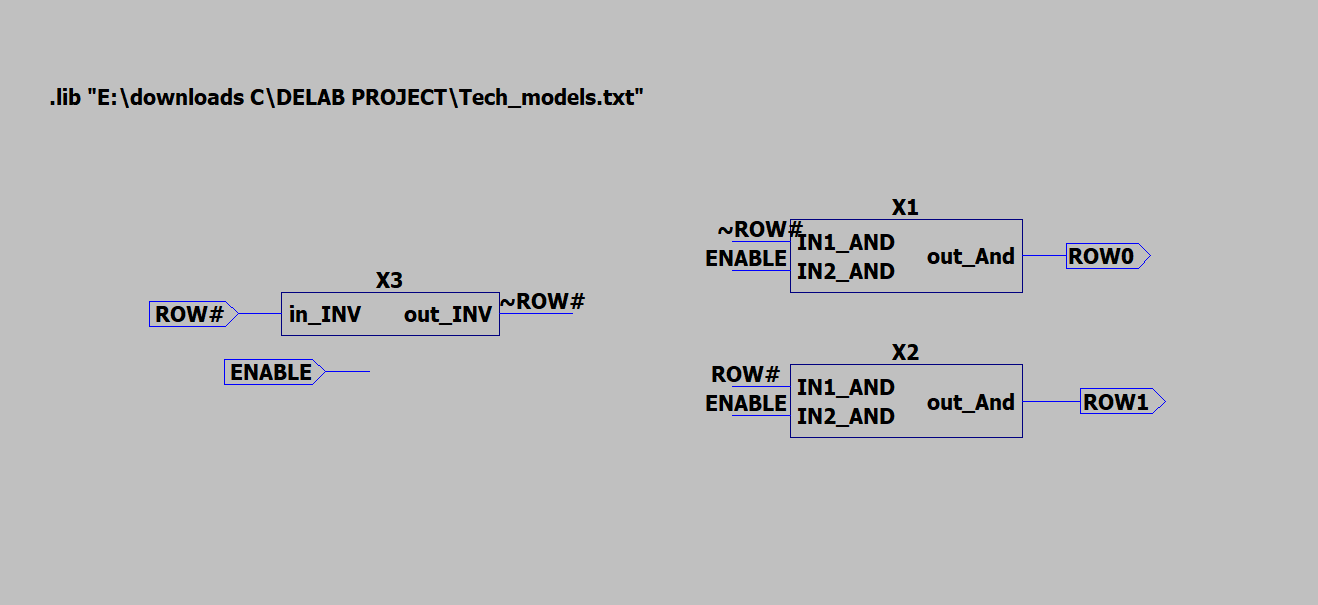


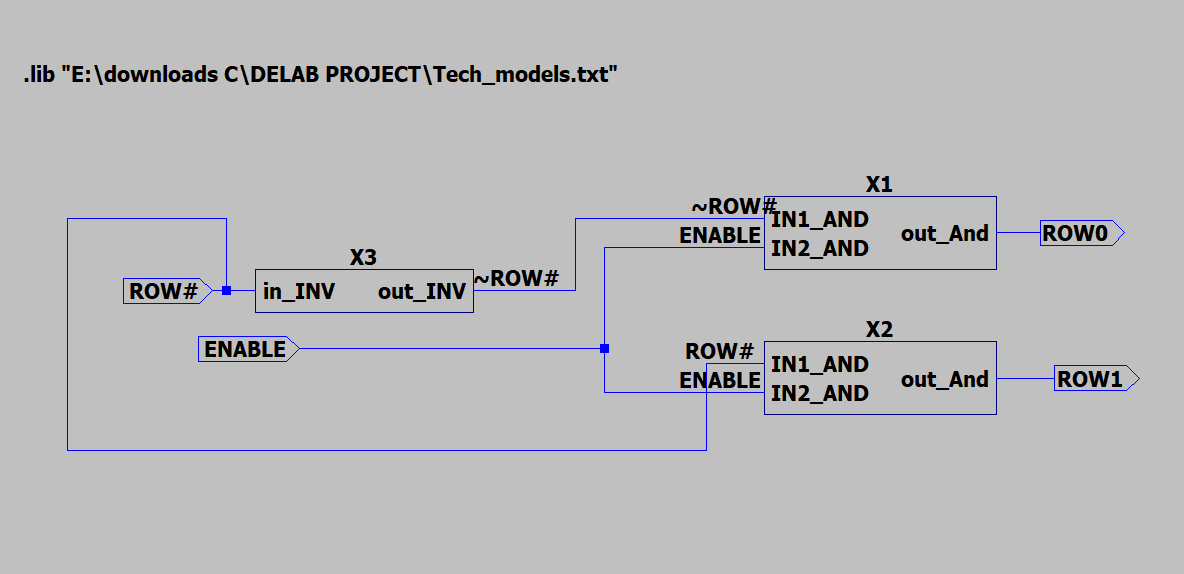


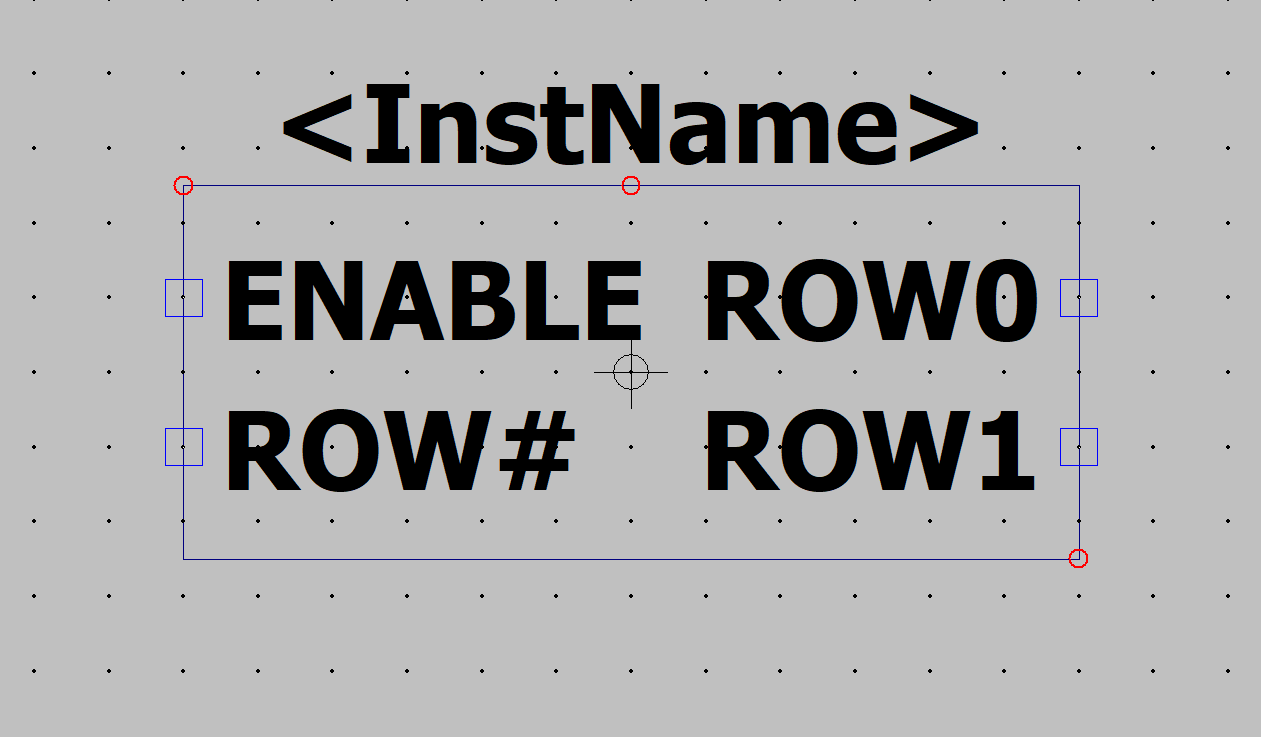
**Decoder :**



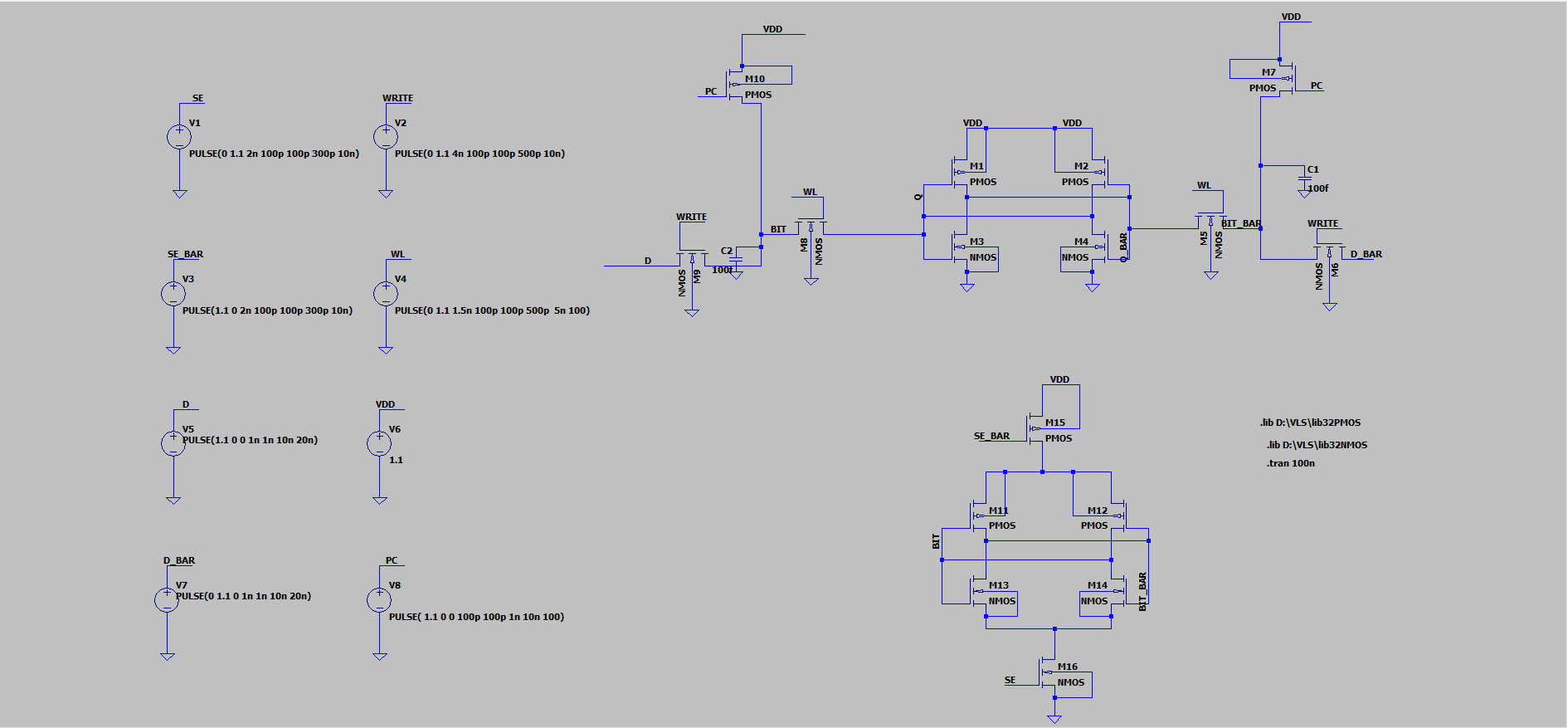








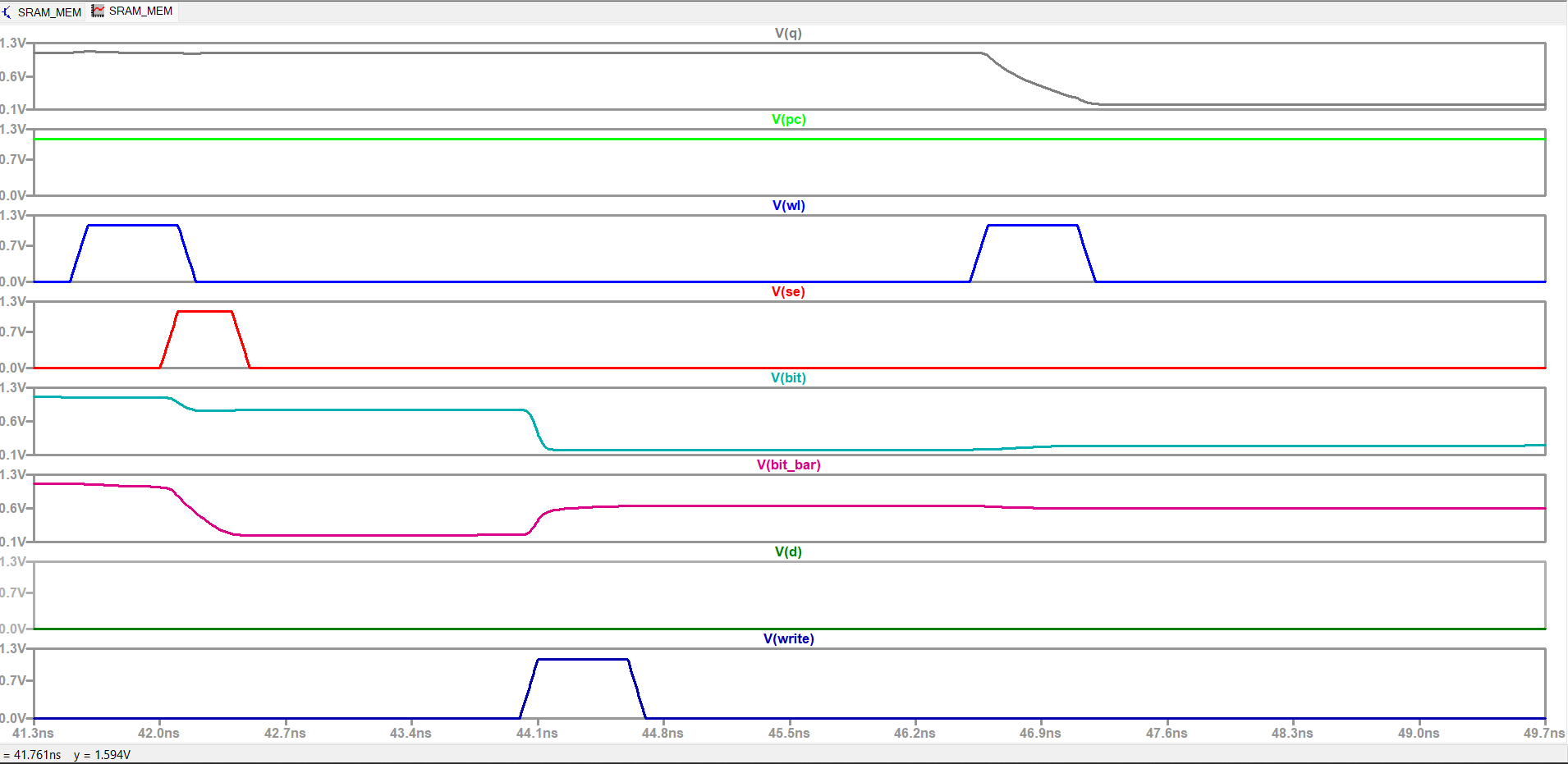
**SRAM :**



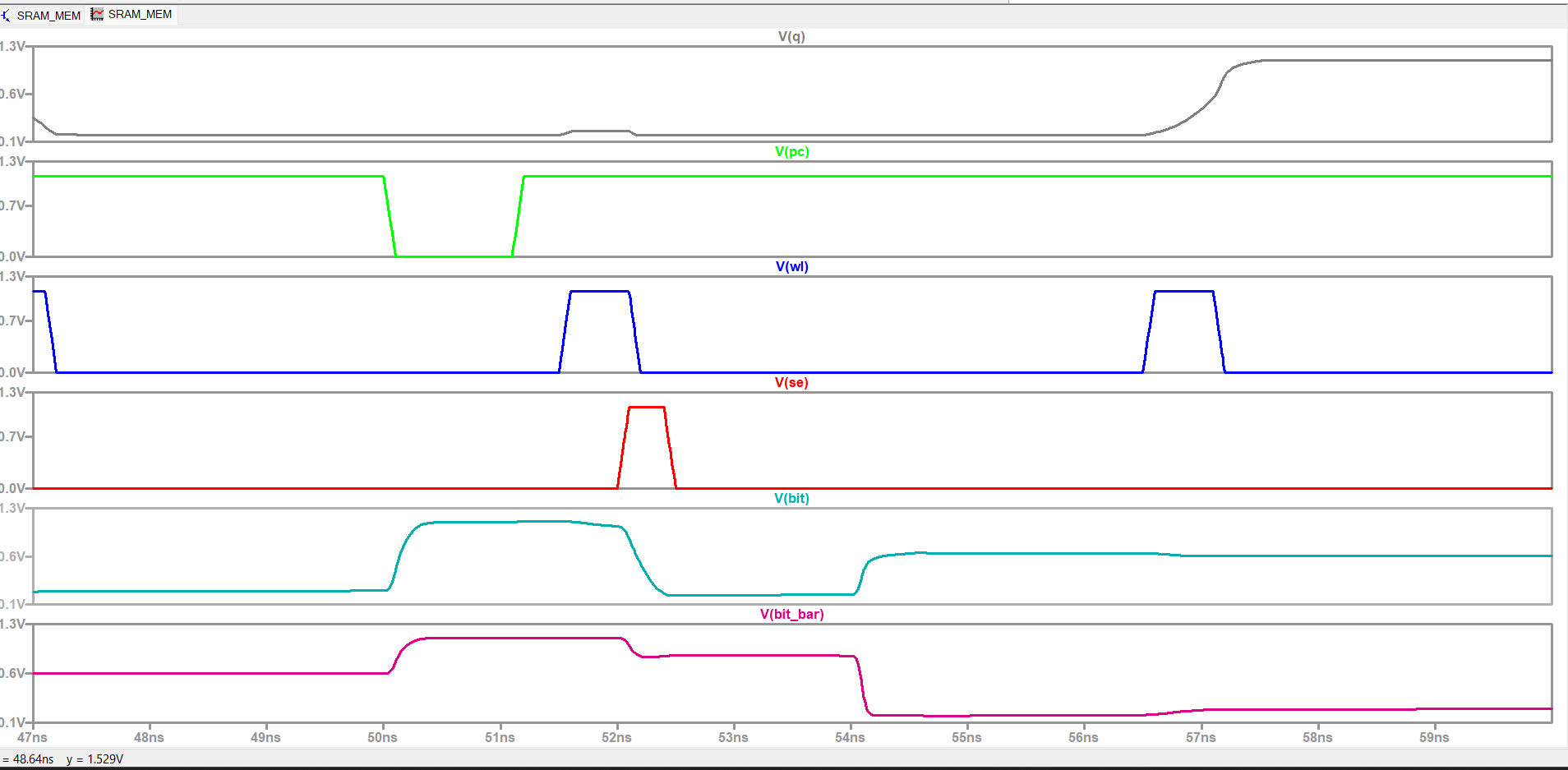
A picture containing line, diagram, colorfulness, screenshot

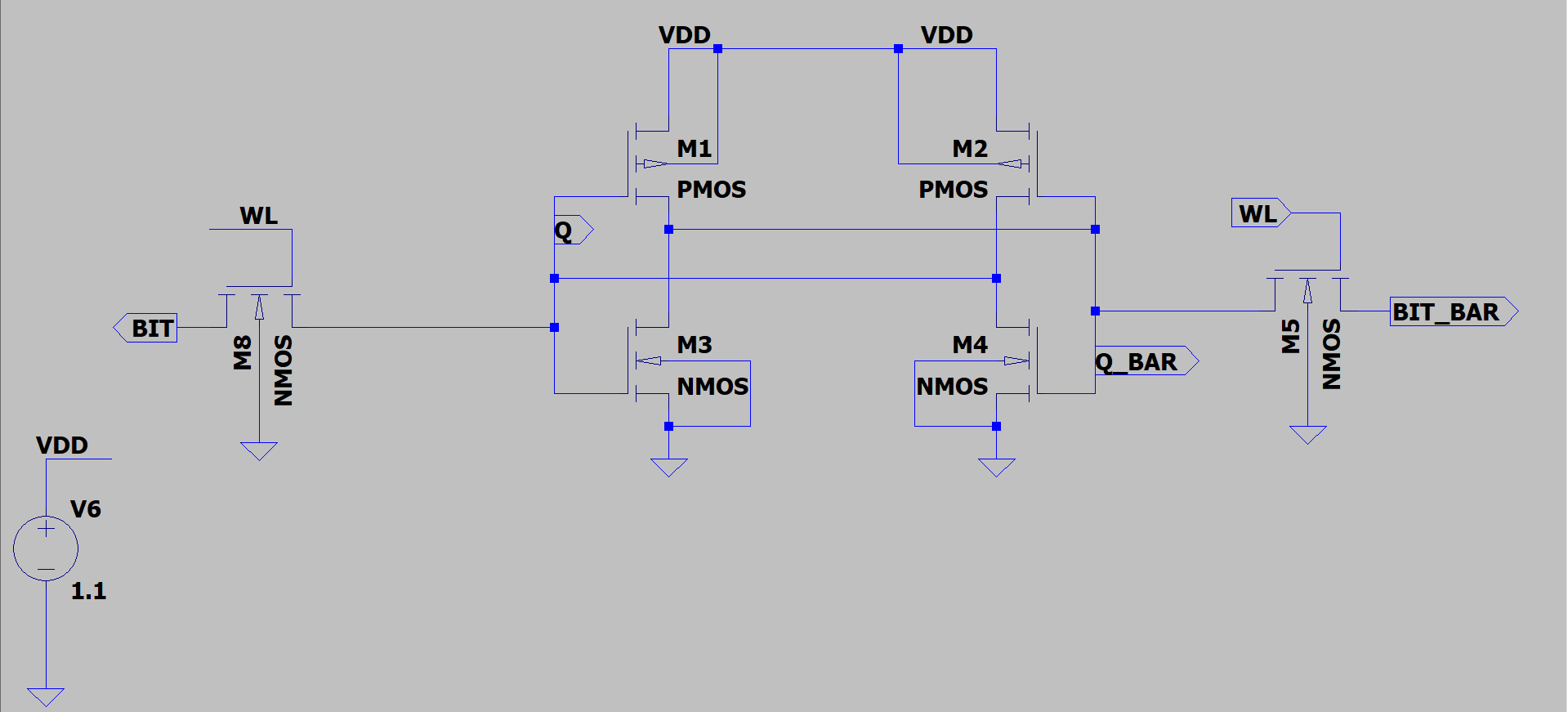
Description automatically generated

Write 0

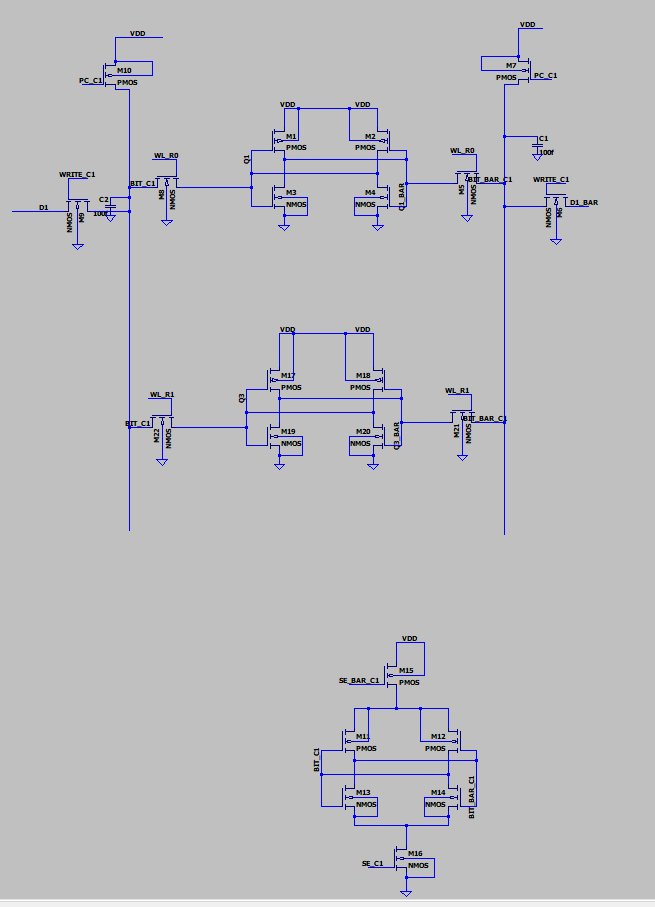


Read

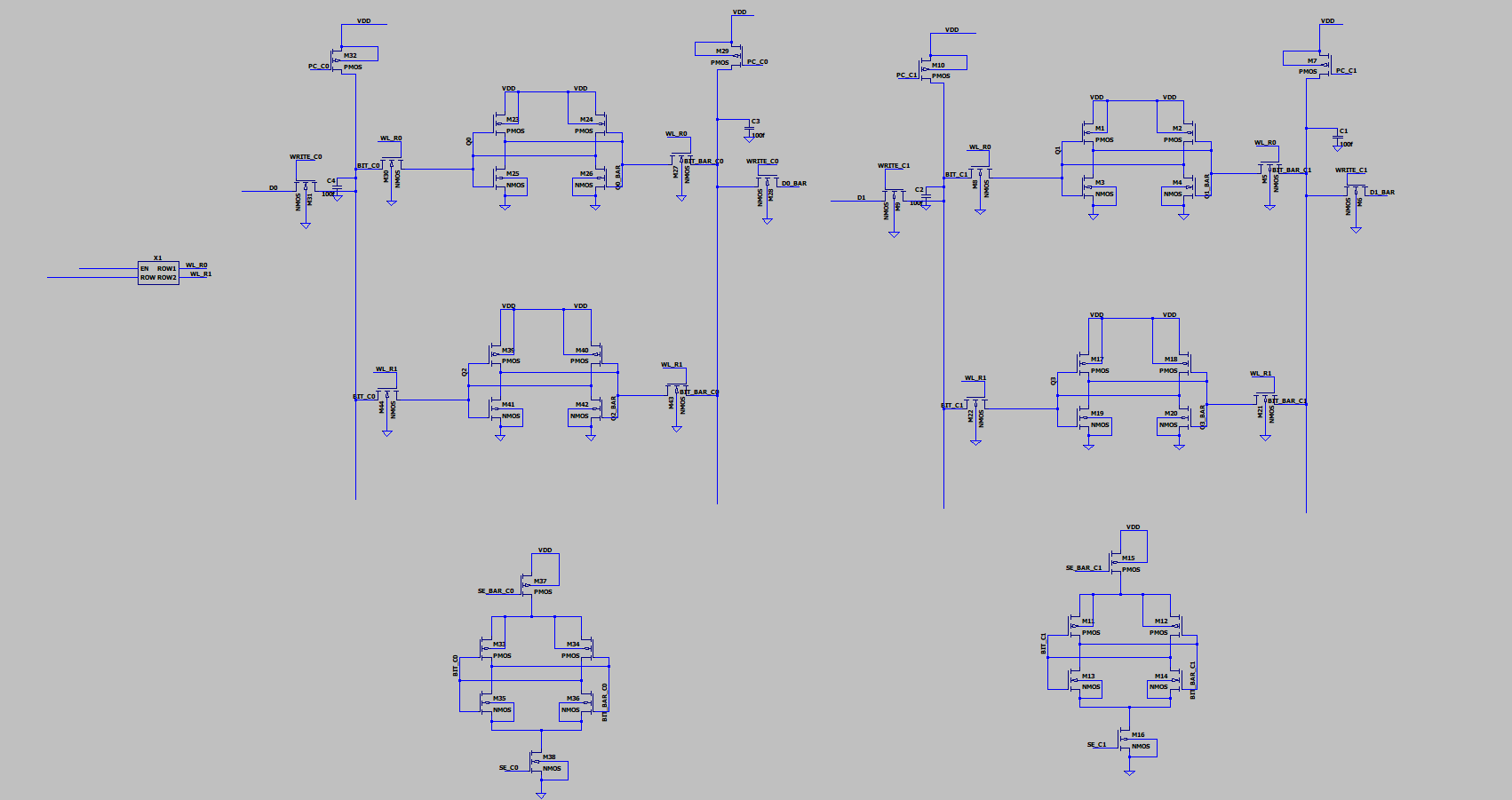




1 Column SRAM:



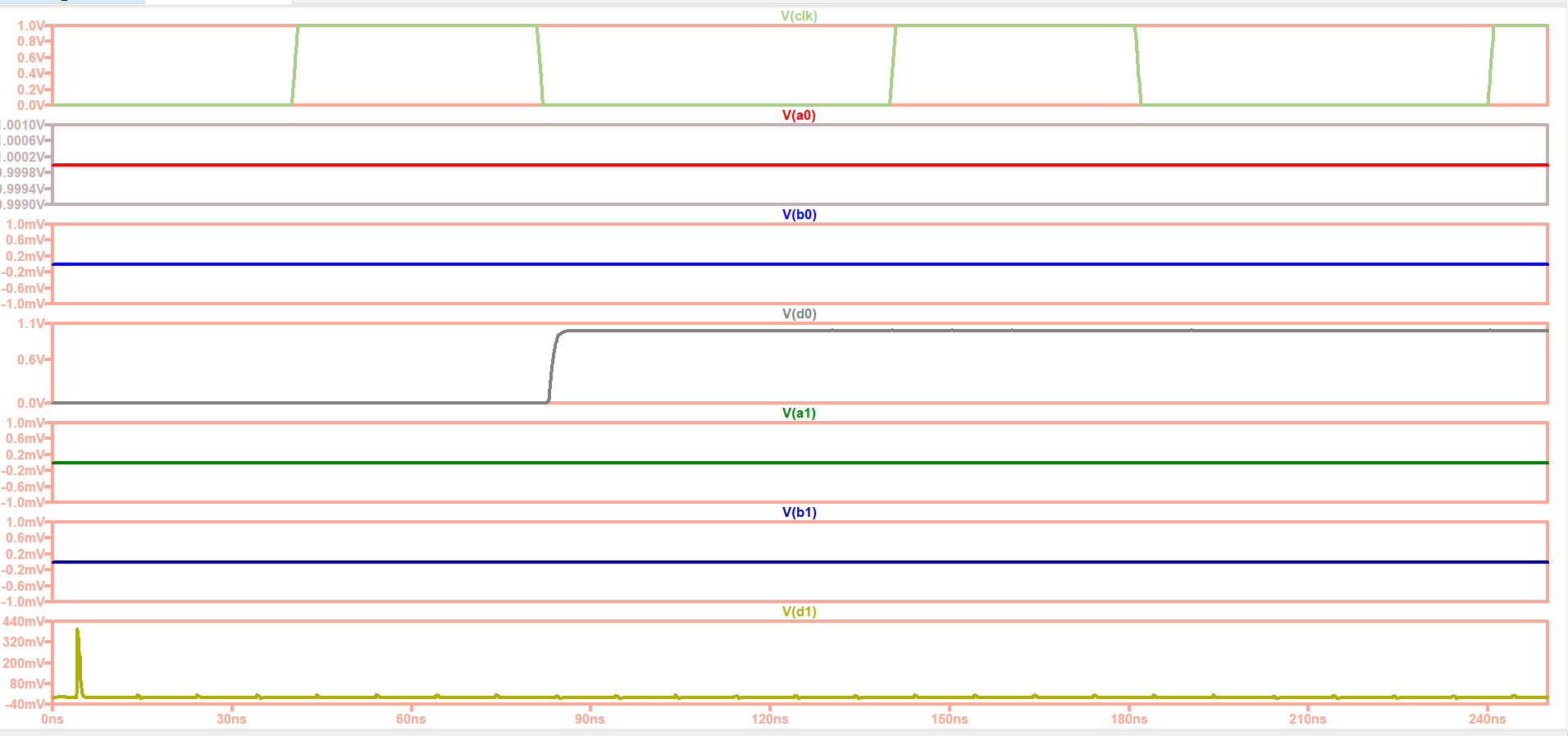
**2 X 2 SRAM**

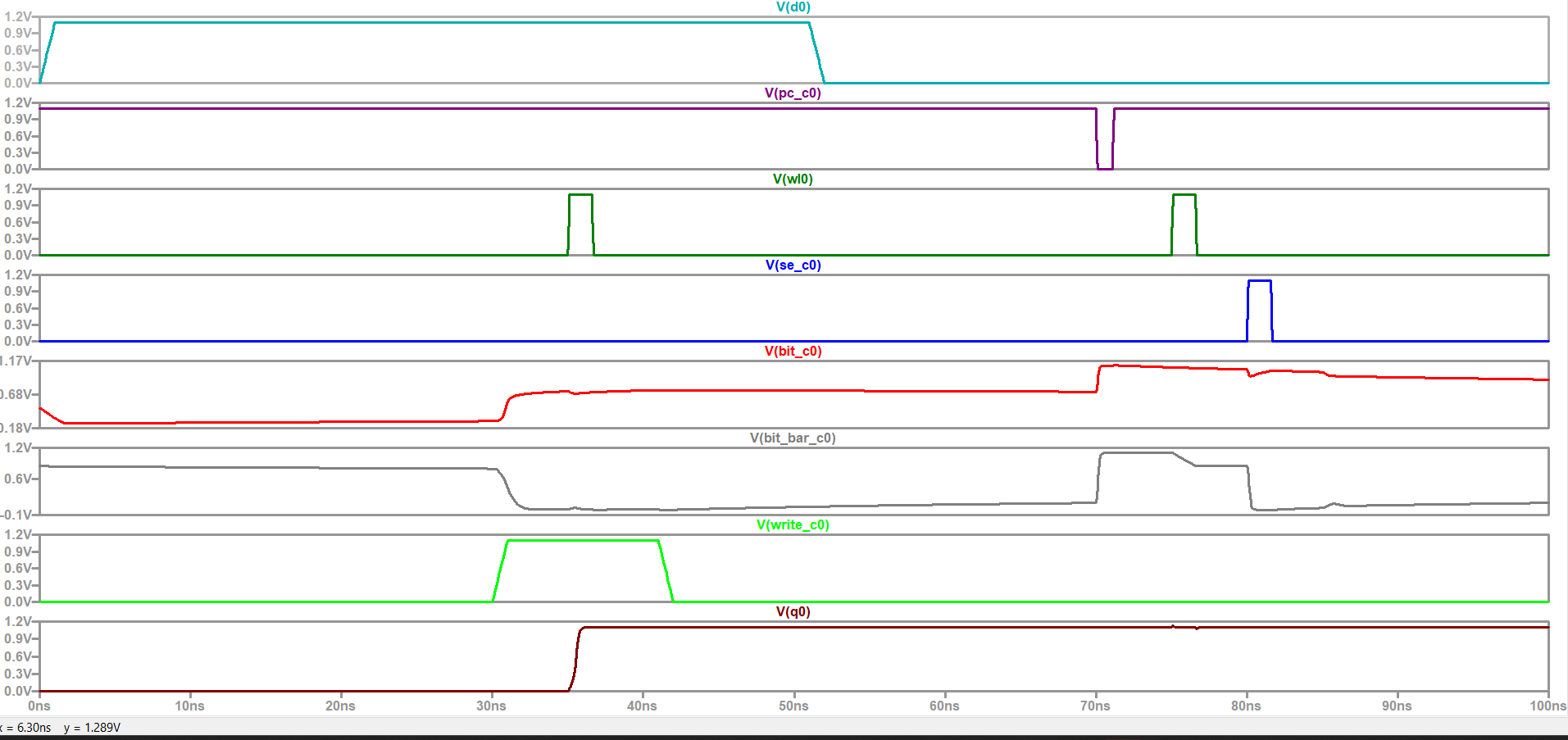


A screenshot of a computer

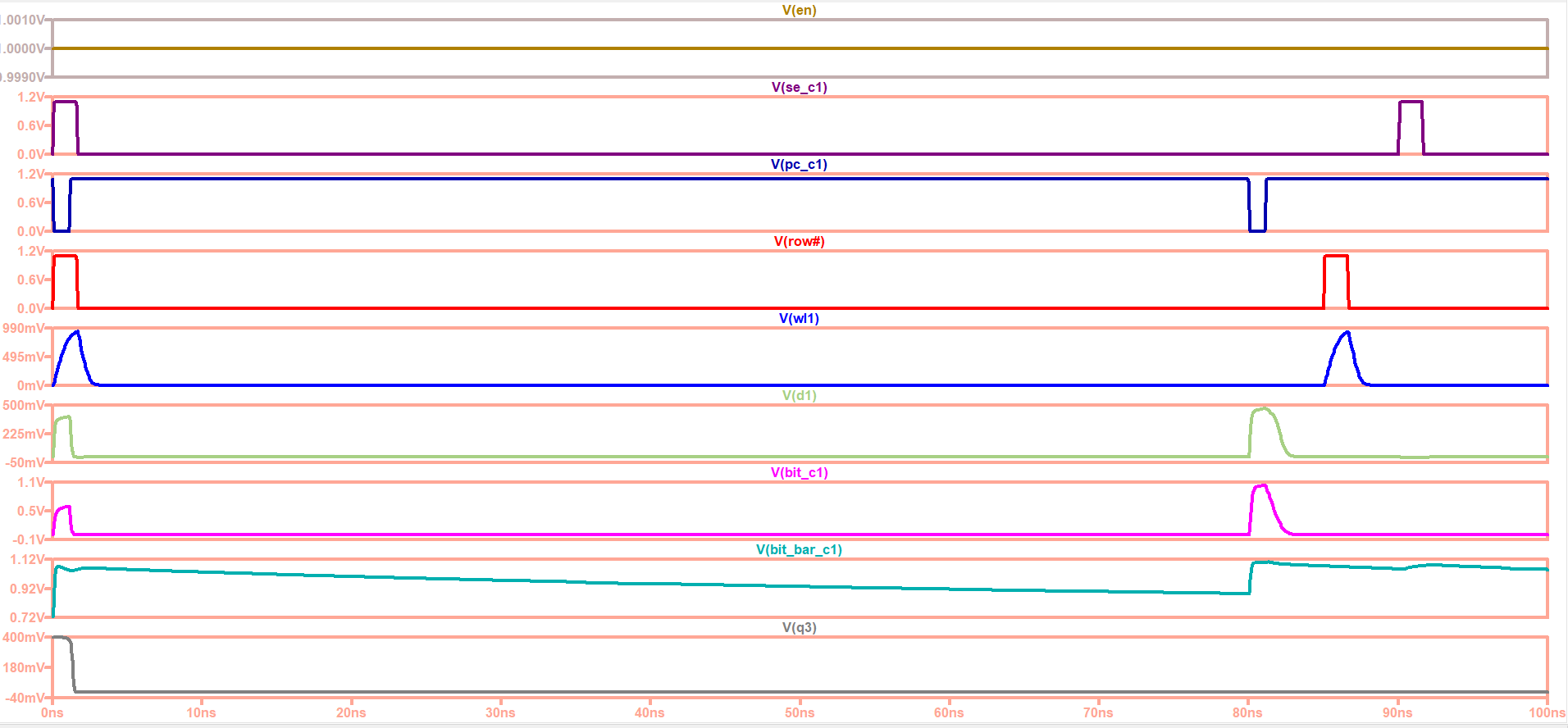
Description automatically generated with low confidence

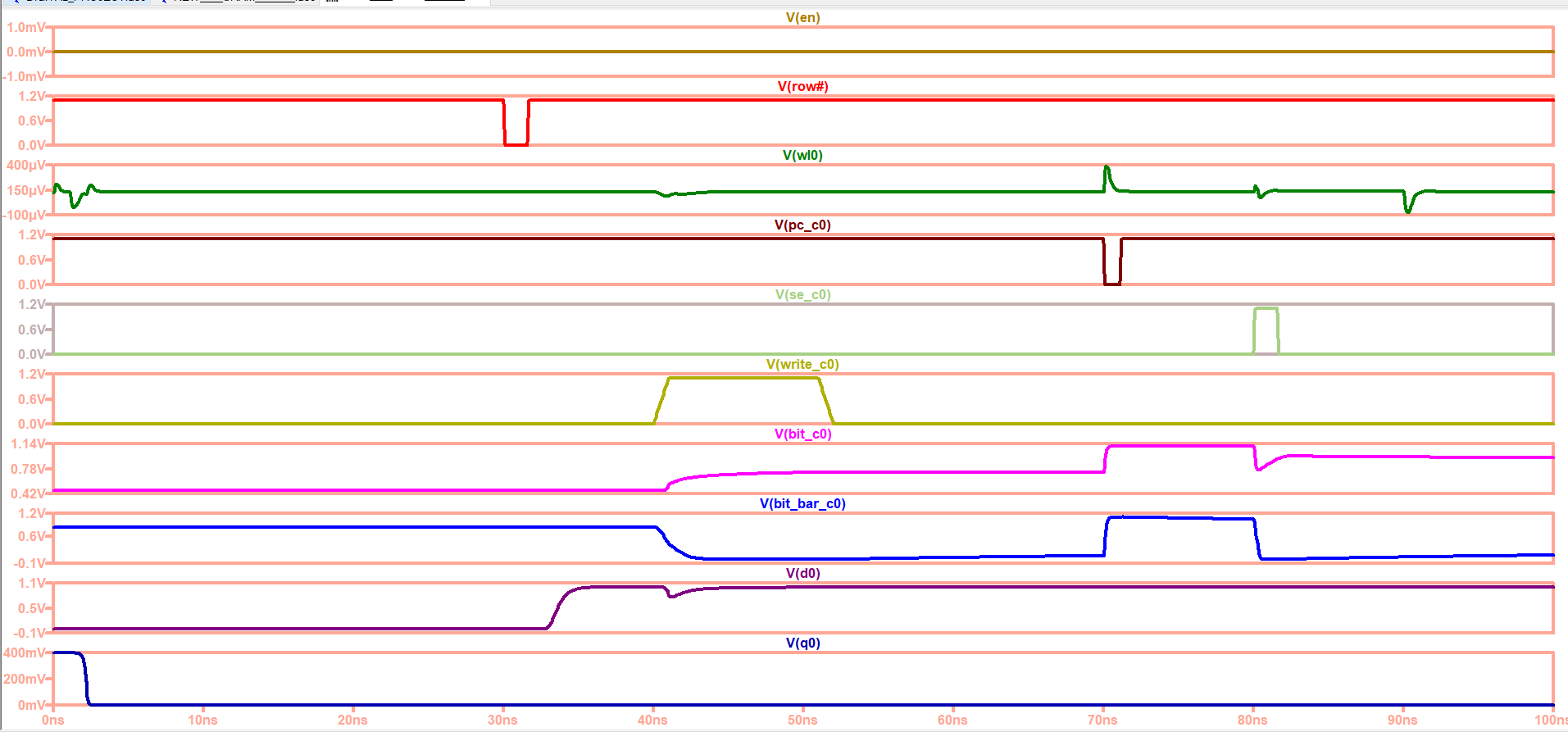
**Full Design :**

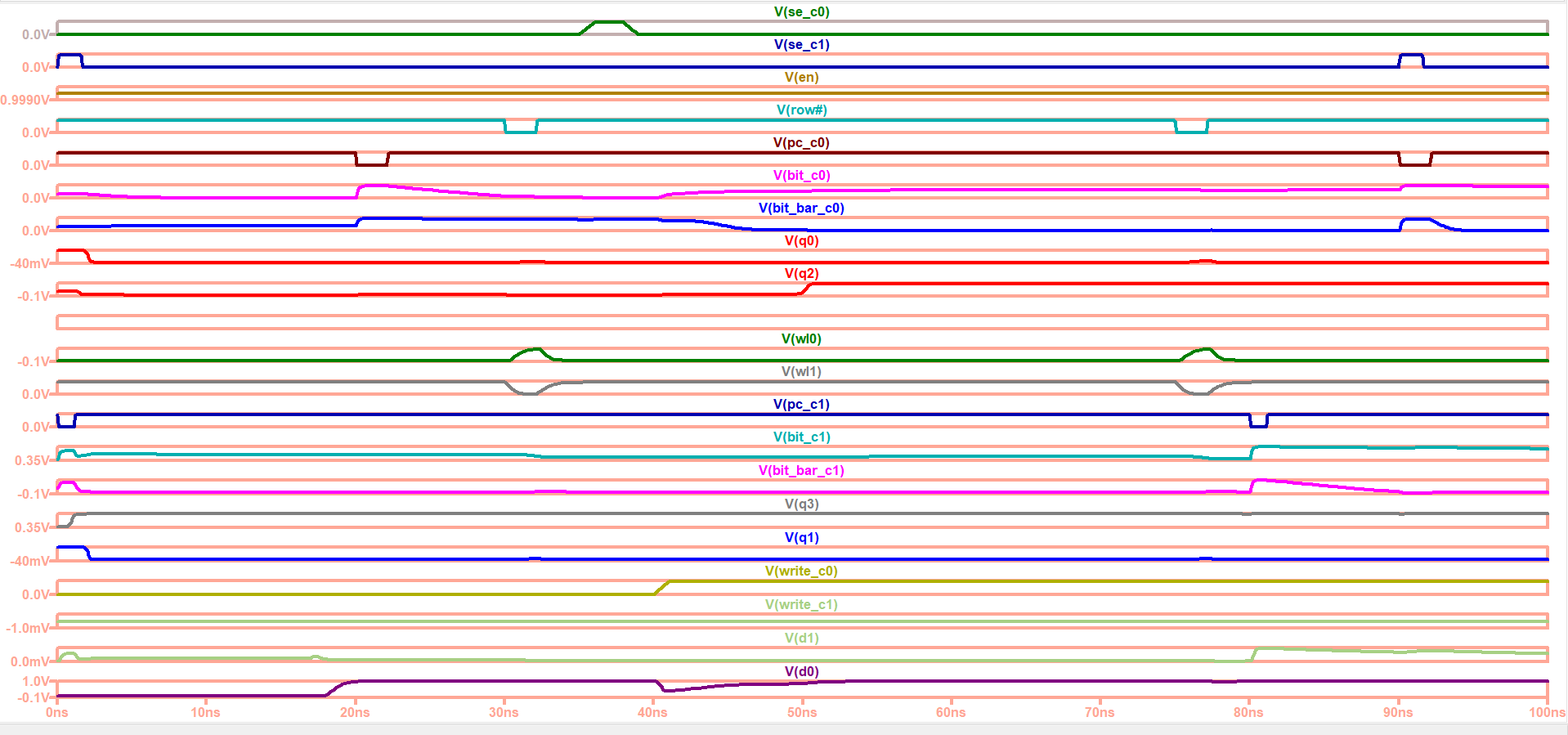




Test Cases:

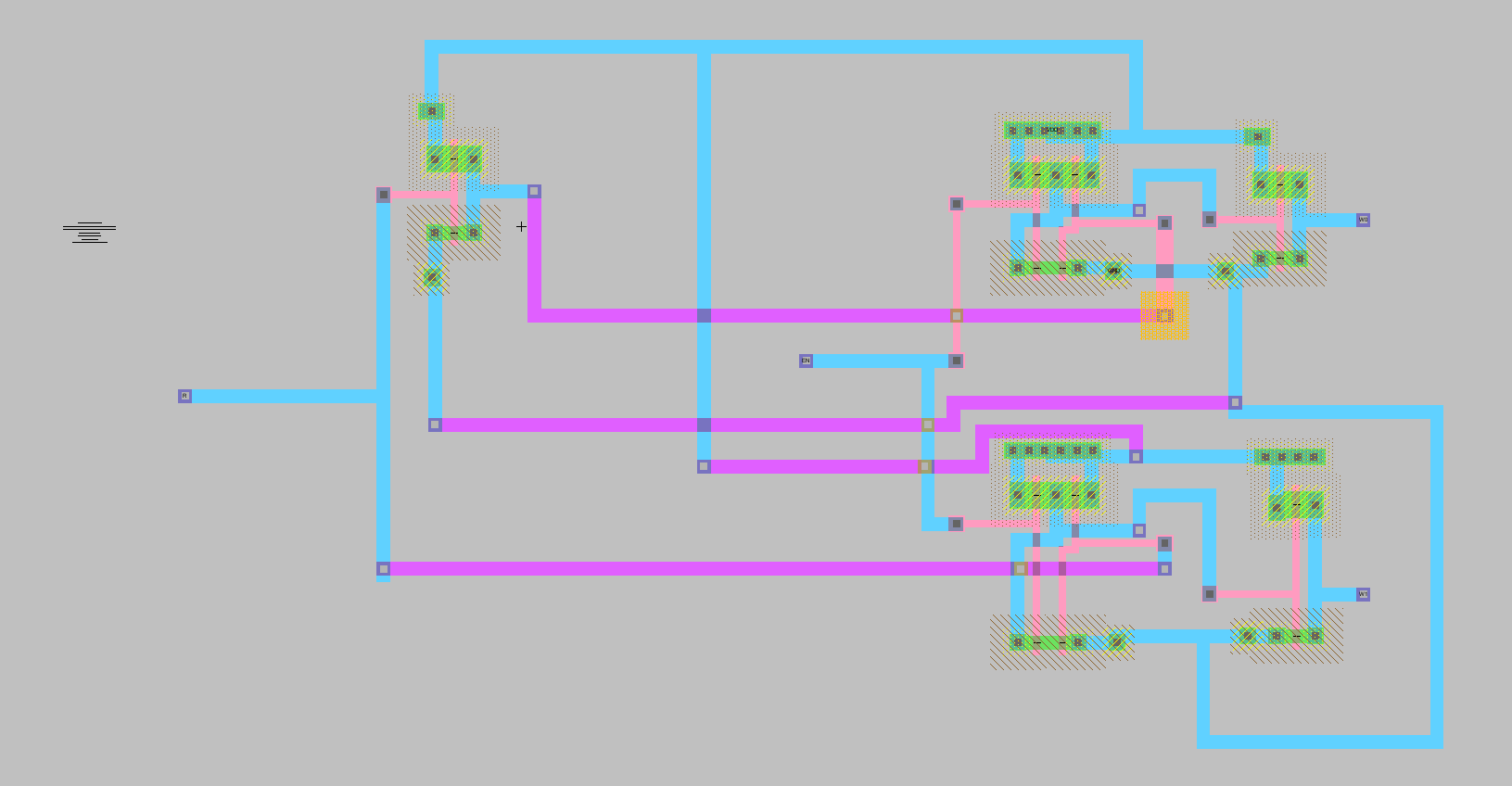


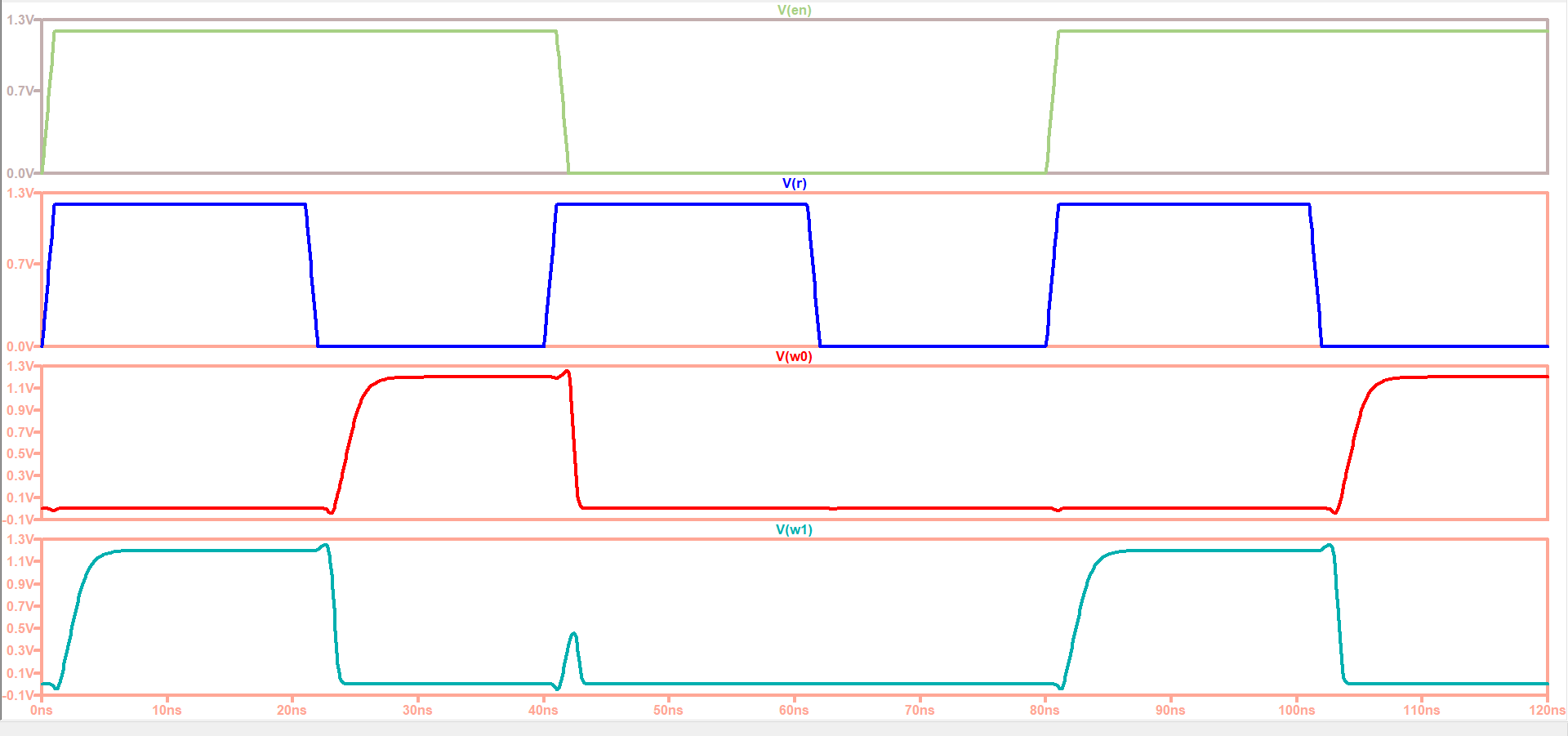




**Layout**

Decoder:

****

****

vdd VDD 0 DC 1.2

vin EN 0 PULSE(0 1.2 0 1n 1n 40n 80n 5)

vin2 R 0 PULSE(0 1.2 0 1n 1n 20n 40n 5)

cload W0 0 50fF

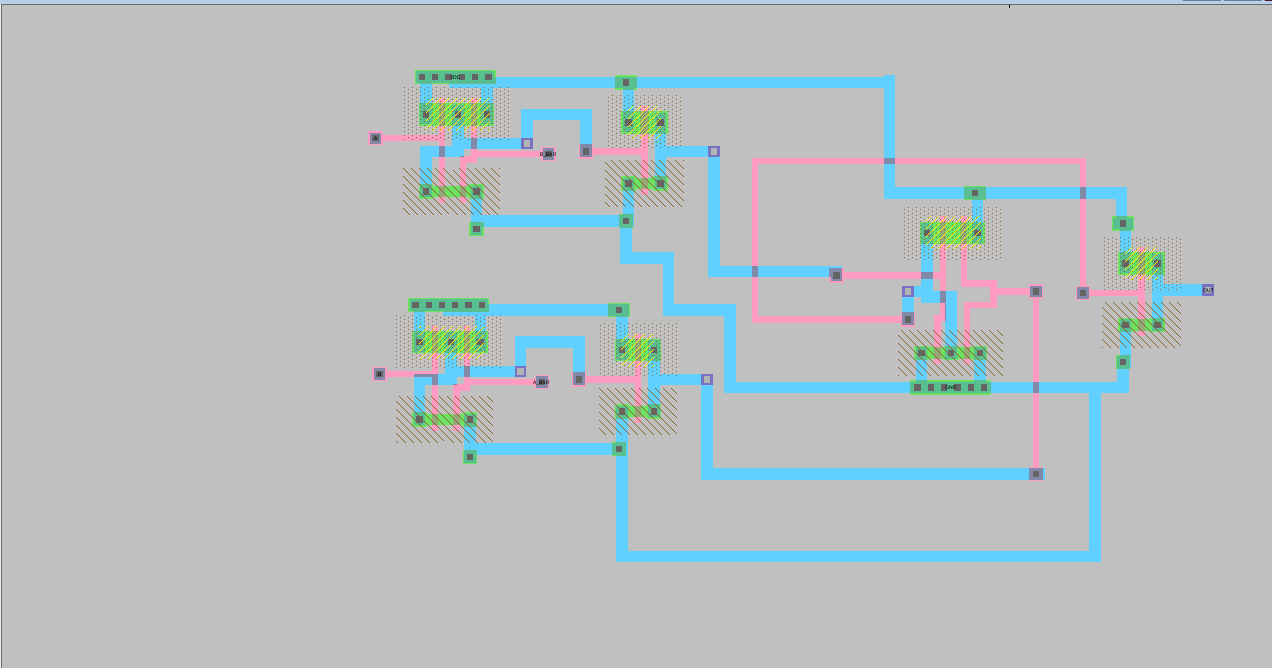
cload2 W1 0 50fF

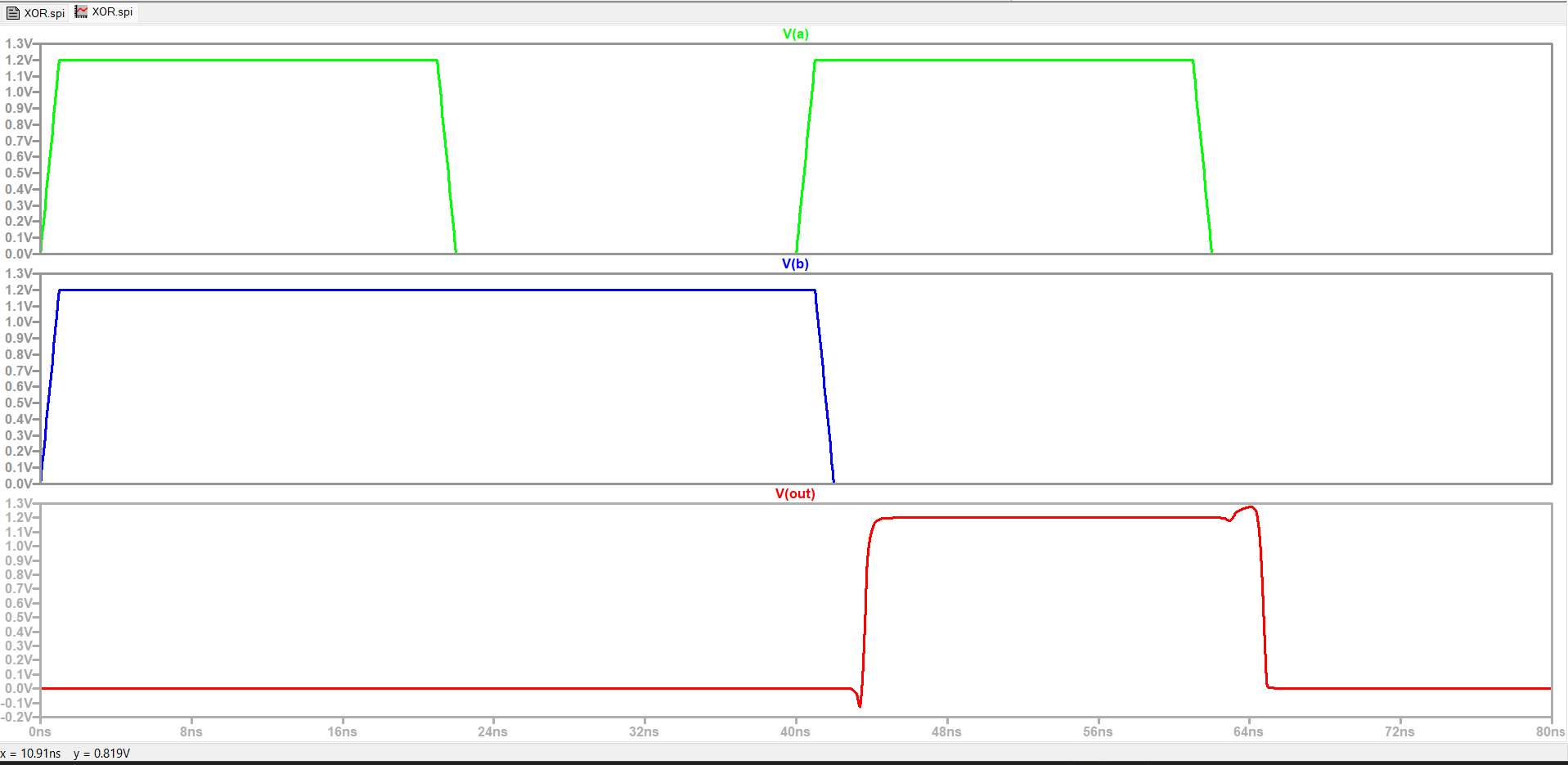
.tran 0 120n

.include E:\downloads C\DELAB PROJECT - Copy\Tech\_models.txt

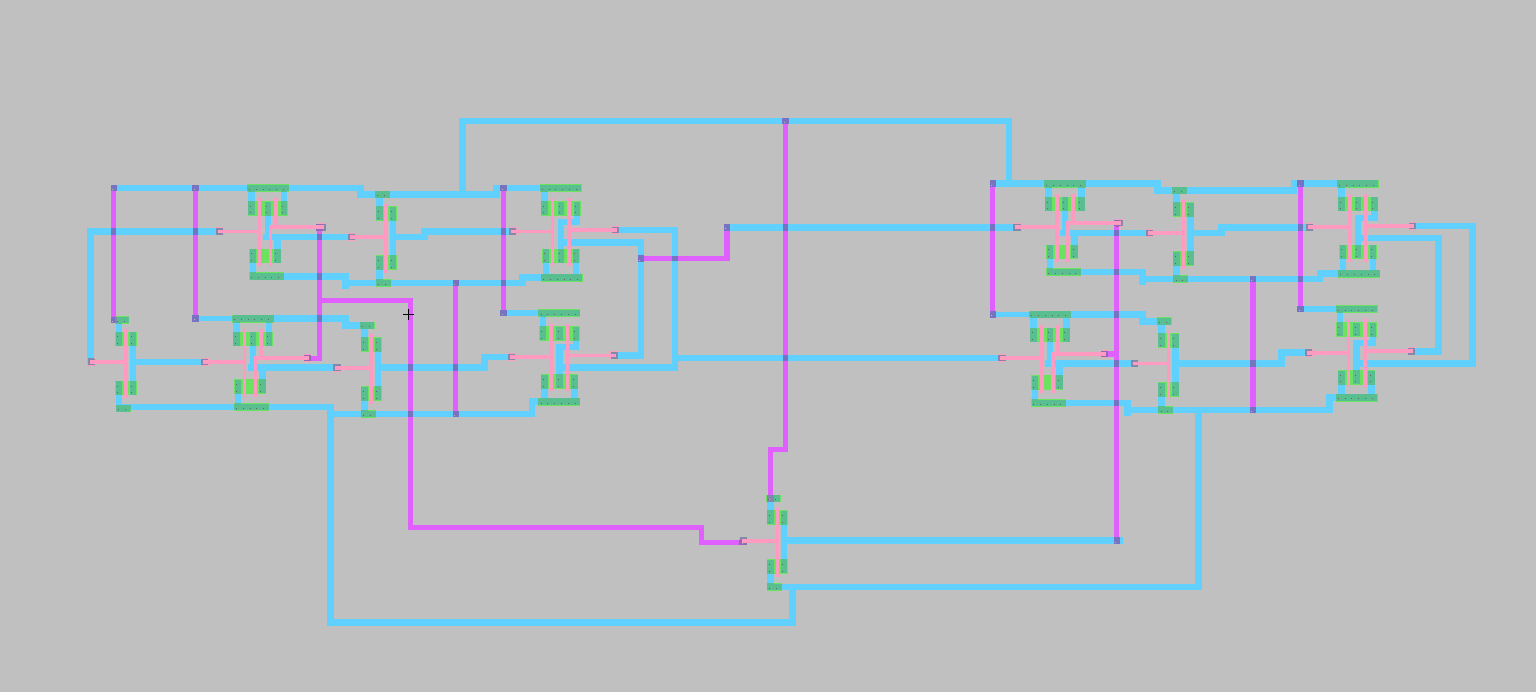
.END

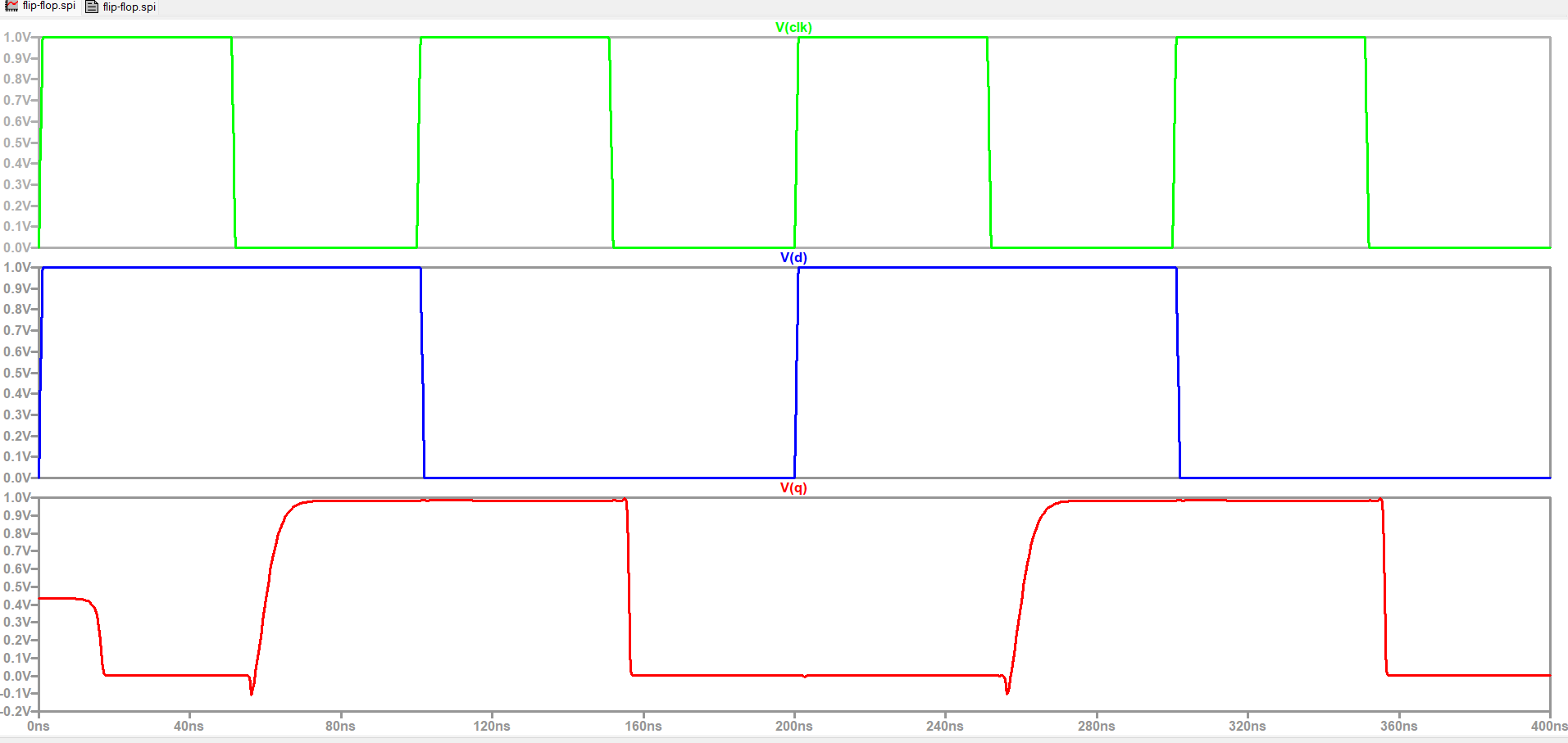
**XOR**



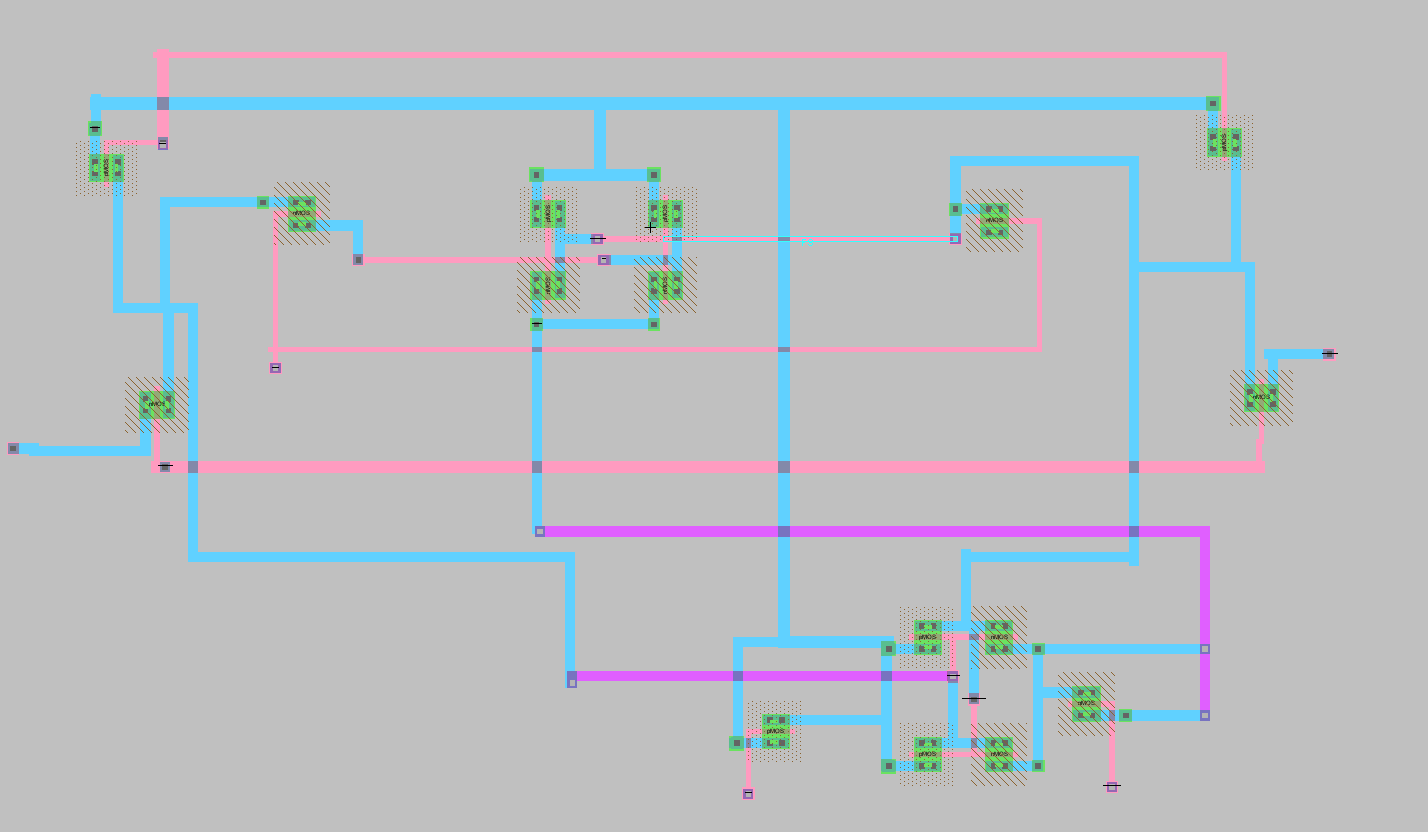


**D-FF**





**SRAM:**



vdd VDD 0 DC 1.1

vin WRITE 0 PULSE(0 1.1 4n 100p 100p 500p 10n)

vin2 SE 0 PULSE(0 1.1 2n 100p 100p 300p 10n)

vin3 SE\_BAR 0 PULSE(1.1 0 2n 100p 100p 300p 10n)

vin4 D 0 PULSE(1.1 0 0 1n 1n 10n 20n)

vin5 D\_AR 0 PULSE(0 1.1 0 1n 1n 10n 20n)

vin6 PC 0 PULSE(1.1 0 15n 100p 100p 1n 10n 10n)

vin7 WL 0 PULSE(0 1.1 1.5n 100p 100p 10n 20n 100)

cload Q 0 50fF

cload1 Q\_BAR 0 100f

cload2 BIT 0 100f

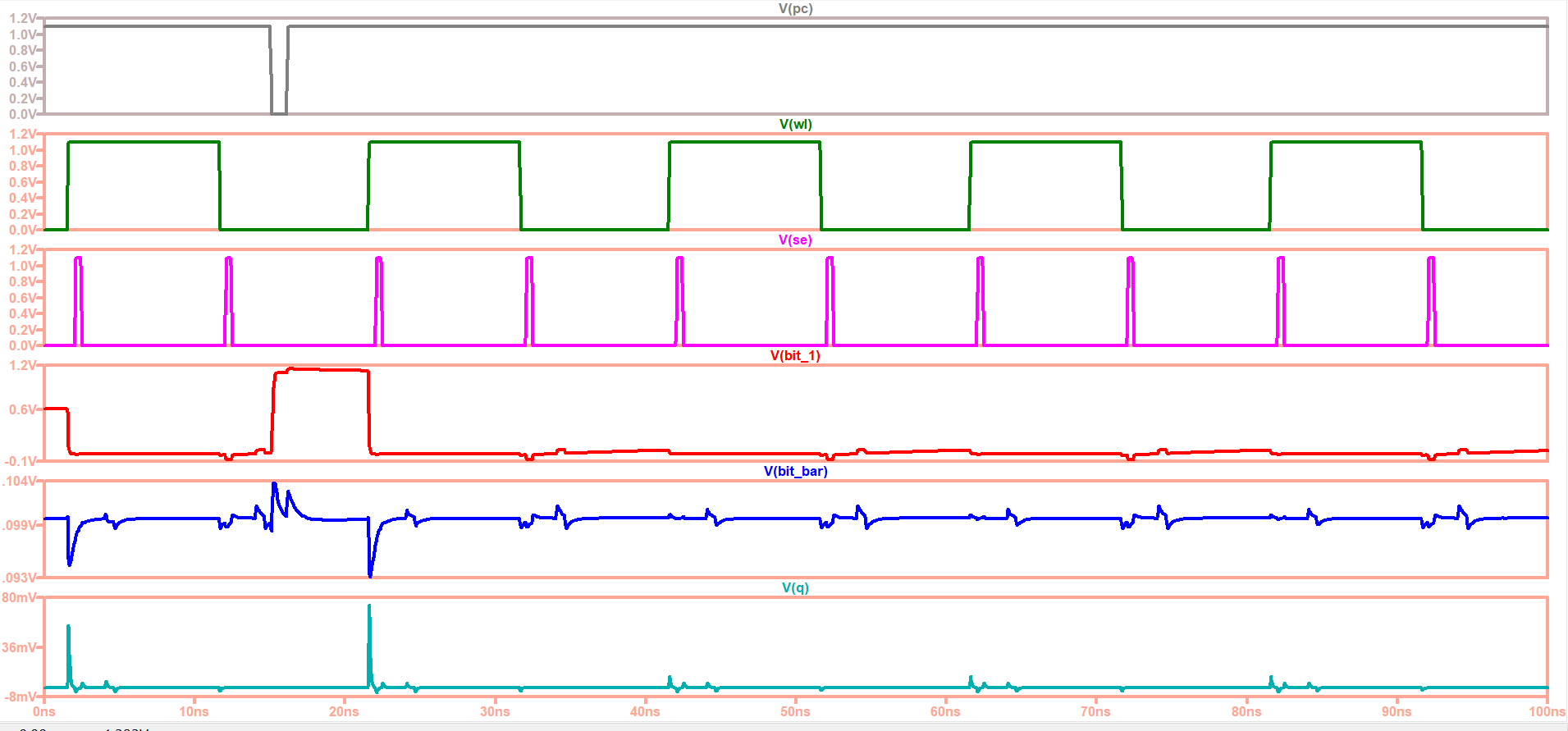
cload3 BIT\_BAR 0 100f

.tran 0 100n

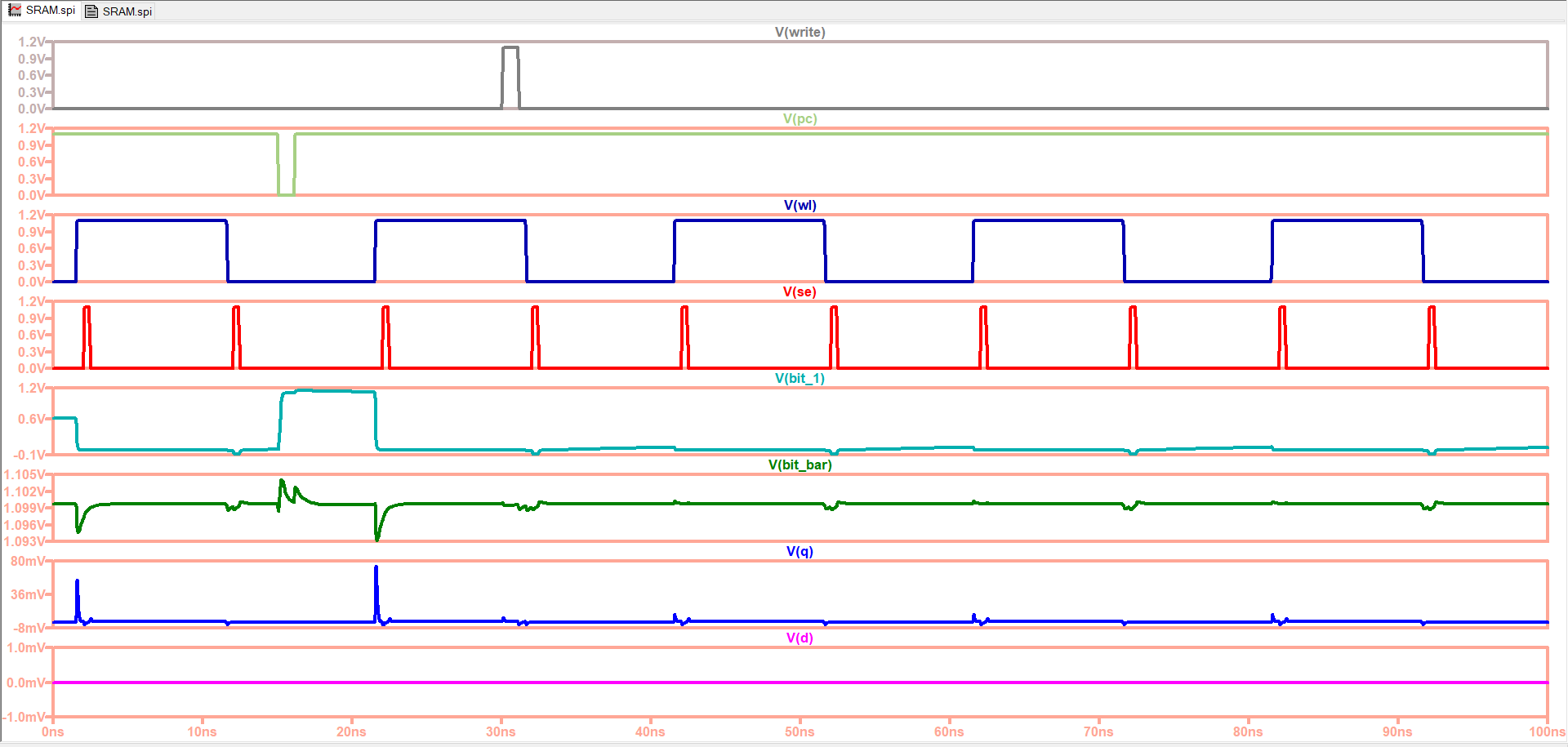
.include E:\downloads C\DELAB PROJECT - Copy\Tech\_models.txt

.END

Read:



Write:



Full Design Layout:

