

CpE 151 and EEE 234 CMOS and VLSI Design

(113.3) Great!
st dropped)

Midterm Exam

(For undergraduates: 5 lowest questions will be dropped. Graduate students: 2 lowest dropped)

1. P-type semiconductor has electrons (electrons/holes) as minority charge carriers.

2. When a voltage of 2V is applied between the G and S of a NMOS, the transistor is: (assume $V_t = 1 \text{ V}$)
(a) ON (b) OFF (c) Not enough information

3. When a voltage of -2V is applied to between the G and S of a PMOS transistor, the transistor is (Assume $|V_{tp}| = 1\text{V}$):
(a) ON (b) OFF (c) Not enough information

4. Pick the most appropriate statement from below. A 3-input NOR gate has:
(a) 3 NMOS transistors in the Pull Down Network
(b) 3 PMOS transistors in the Pull Down Network
(c) 3 NMOS transistors in parallel and 3 PMOS transistors in series
(d) 3 NMOS transistors in series and 3 PMOS transistors in parallel
(e) Both (a) and (c) are true
(f) Both (b) and (d) are true

5. If the NMOS and PMOS transistors switch places in an inverter, the resulting circuit is:
(a) Weak Inverter
(b) Strong Inverter
(c) Weak buffer
(d) Strong buffer

6. Which of the following is true about PMOS transistor?
(a) It provides a good '1'
(b) It provides a good '0'
(c) It uses p-well
(d) It has positive threshold voltage V_{tp}

7. Input dependent phase shift is brought about by which of the following transistor non-ideality?
a. Channel-charge injection
b. Clock-feed through
c. Non-zero ON-resistance
d. Negative-bias Temperature Instability (NBTI)

8. A 2:1 MUX implemented using transmission gates has uses how many PMOS transistors?
3 . 2

✓ 9. Which of the following Capacitances is fundamental to the operation of a MOS transistor?

- a. Depletion capacitance between Drain and Bulk
- b. Depletion capacitance between Source and Bulk
- c. Overlap Capacitance between Gate and Source/Drain
- d. Oxide Capacitance between Gate and Channel

✓ 10. In the Figure – 1 shown below, which capacitance shorts the input to the output at high frequencies? C_{gd}

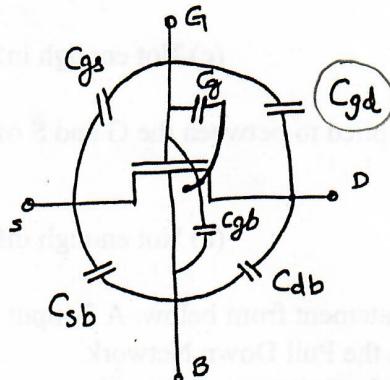


Figure – 1. MOSFET Capacitances

✓ 11. In the Figure – 2 shown below, plot the graph for the equivalent ON-resistance of a transmission gate. The On-resistance of NMOS and PMOS as a function of V_{in} .

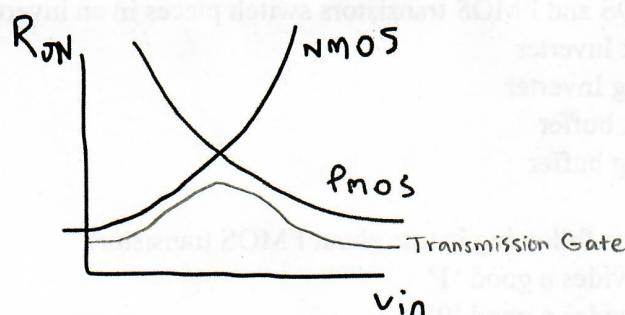


Figure – 2. On-resistance of NMOS, PMOS and transmission gate

✓ 12. Shown below are transistor higher order effects. Identify a lateral field effect from below.

- a. Subthreshold conduction
- b. Mobility degradation
- c. Body effect
- d. Velocity saturation

✓ 13. Shown below are transistor higher order effects. Identify a vertical field effect from below.

- a. Subthreshold conduction
- b. Mobility degradation
- c. Body effect
- d. Velocity saturation

14. "Pinch-off" occurs in which region of operation?

- a. Subthreshold
- b. Saturation
- c. Linear
- d. Both (b) and (c)

15. Because of short channel effect, the V_{th} of a MOSFET increases (increases/decreases) with increasing values of L.

16. For the pass transistor shown in figure - 3 below, what is the voltage at the output?

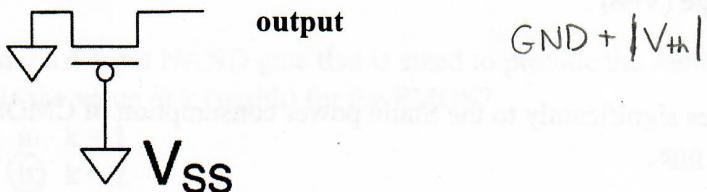


Figure – 3 PMOS Pass Transistor

17. By definition, the time from input to rising output crossing $V_{DD}/2$ is:

- a. Rise Time - (tr)
- b. Rising Propagation Delay (t_{pdr})
- c. Rising Contamination delay (t_{cdr})
- d. Setup – time

18. In RC Delay Model, which of the following substitutions is valid

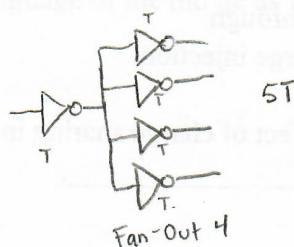
- a. PMOS transistor with a width of k times the unit transistor has a resistance of R/k
- b. NMOS transistor with a width of k times the unit transistor has a cap of $2kC$ on the gate
- c. PMOS transistor with a width of k times the unit transistor has a cap of kC on the gate
- d. NMOS transistor with a width of k times the unit transistor has a resistance of $2R/k$

19. While calculating the delay of a RC ladder using Elmore – Delay, which of the following is true?

- a. The Resistance closest to the load has the highest effect on the delay
- b. The Capacitance closest to the load has the highest effect on the delay
- c. The Resistance closest to the source has the highest effect on the delay
- d. The Capacitance closest to the source has the highest effect on the delay

20. For the figure – 4 shown below, what is the total delay in terms of T. T is defined as the delay of a parasitic-free fanout-of-1 inverter?

- a. 2 T
- b. 3 T
- c. 4 T
- d. 5 T



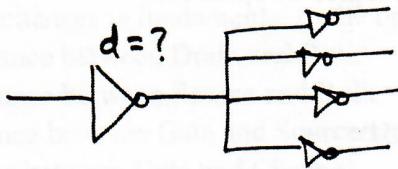


Figure – 4 Fanout-of-4 inverter

✓ 21. The biggest saving in Dynamic power consumption is brought about by reducing which of the following?

- a. Activity factor (α)
- b. Capacitance (C)
- c. Supply voltage (V_{DD})
- d. Frequency (f)

✓ 22. Which of these contributes significantly to the Static power consumption of CMOS circuits?
Pick the most significant one.

- a. $P_{\text{switching}}$
- b. $P_{\text{shortcircuit}}$
- c. Subthreshold – leakage
- d. Contention current

✓ 23. The activity factor of memory components is relatively low (low/high) compared to that for logic components.

✓ 24. When transistors switch, both nMOS and pMOS networks may be momentarily ON at the same time, leading to a blip of current called short-circuit current.

✓ 25. The output of a Dynamic Logic Circuits is valid only during which phase?

- a. Pre-charge
- b. Discharge
- c. Evaluate
- d. Charge-sharing

✓ 26. The charge leakage mechanism of capacitance imposes a lower (lower/upper) limit on the clock frequency of Dynamic Circuits.

✓ 27. In Dynamic Circuits, the output at a node can go higher than the supply voltage because of which effect?

- a. Charge sharing
- b. Charge leakage
- c. Clock feed through
- d. Channel charge injection

✓ 28. In order to reduce the effect of charge sharing in Dynamic circuits, the critical nodes should be pre-charged.

✓ 29. Consider a 4 input NOR gate that is sized to provide the same current as a unit inverter. What is the value of k (width of the PMOS) for the PMOS?

- a. $k = 1$
- b. $k = 2$
- c. $k = 4$
- d. $\textcircled{d} k = 8$

✓ 30. For the NOR gate in problem # ²⁹ 30, what is the value of K for the NMOS transistor?

- a. $k = 1$
- b. $k = 2$
- c. $k = 4$
- d. $k = 8$

✓ 31. Consider a 4 input NAND gate that is sized to provide the same current as a unit inverter. What is the value of k (width) for the PMOS?

- a. $k = 1$
- b. $\textcircled{b} k = 2$
- c. $k = 4$
- d. $k = 8$

✓ 32. For the NAND gate in problem # ³¹ 32, what is the value of k (width of the PMOS) for the PMOS?

- a. $k = 1$
- b. $k = 2$
- c. $\textcircled{c} k = 4$
- d. $k = 8$

✓ 33. For the NOR gate in problem # 30, what is the value of g (logical effort)?

- a. $g = 5/3$
- b. $g = 6/3$
- c. $g = 7/3$
- d. $g = 8/3$

$$\frac{(2(4)+1)}{3} = \frac{8+1}{3} = \frac{9}{3}$$

$\textcircled{e} g = \frac{9}{3}$

✓ 34. For the NAND gate in problem # 30, what is the value of g (logical effort)?

- a. $g = 5/3$
- b. $\textcircled{b} g = 6/3$
- c. $g = 7/3$
- d. $g = 8/3$

$$\frac{n+2}{3} = \frac{4+2}{3} = \frac{6}{3}$$

✓ 35. What is your favorite movie, specify language of the movie as well.

The Avengers in English.