1. More on Karnaugh maps
    a. Further example with don't cares and wrapping
        i. f_3 = m0 + D2 + D5 + D7 + m8 + m10

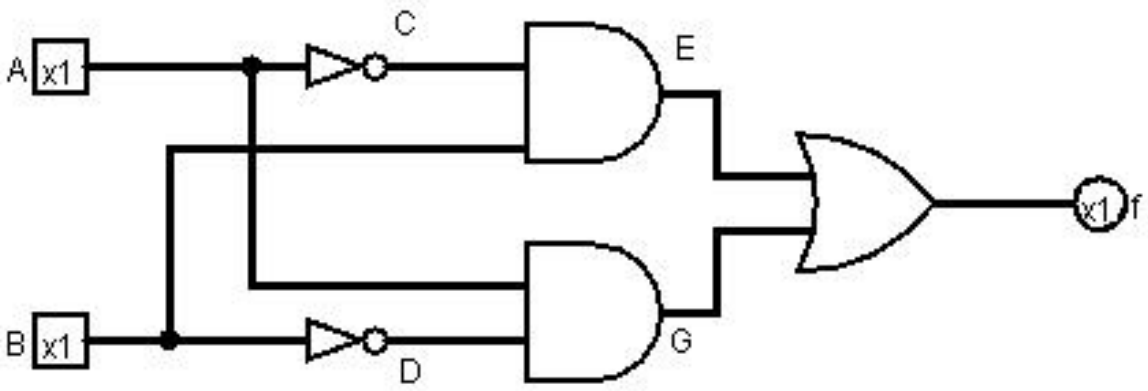
CD \ *AB*	**00**	**01**	**11**	**10**
00				
01				
11				
10				

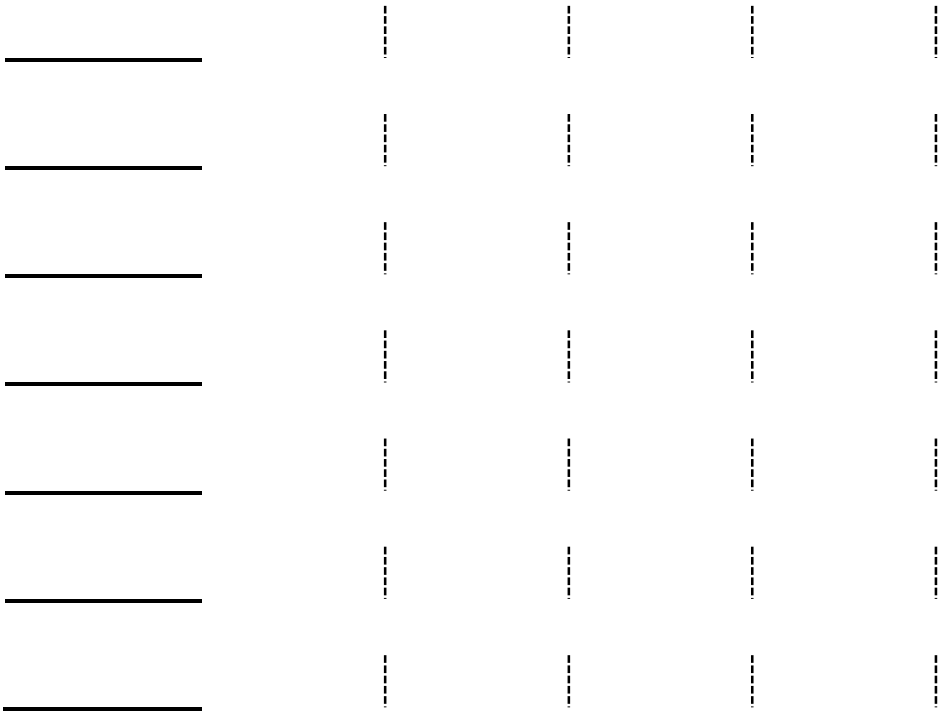
    b. Whether or not don't cares are included depends on your desired use case

2. Timing
    a. Worst case path

    b. Timing diagram

    c. Example
        i. Implementation of XOR using only AND, OR, NOT on next page
            1. A ⊕ B = A * ~B + ~A * B
        ii. Assume that we have the following gate delays
            1. NOT = 3 ns
            2. AND = 5 ns
            3. OR = 4 ns
        iii. What is the clock time of the circuit, if inputs become valid at time 0 ns?





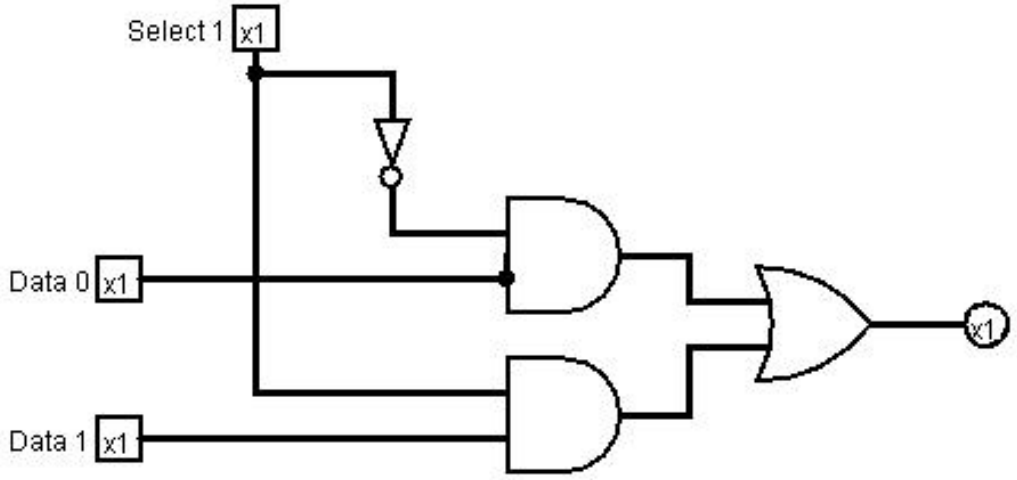
3. Combinational circuit building blocks

4. Multiplexors

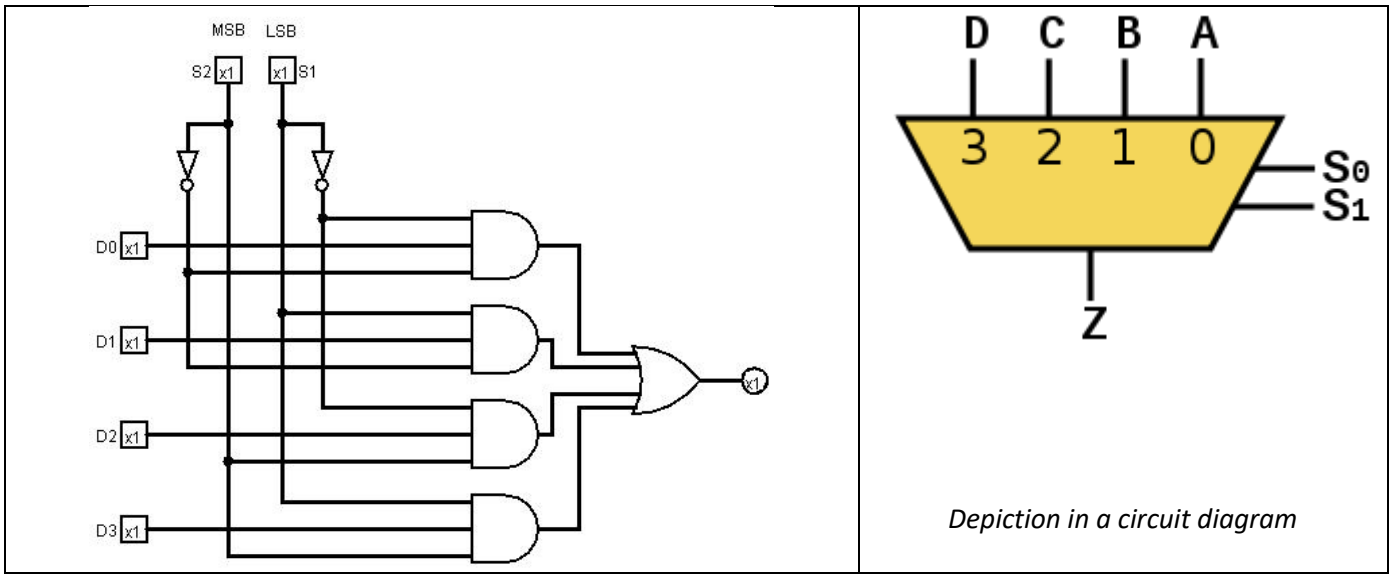
a. Implementation

b. Example

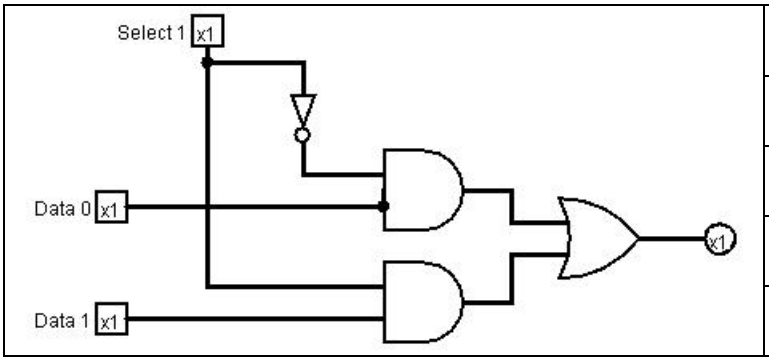
i. 2 to 1 MUX



ii. 4 to 1 MUX



c. Truth table for simple 2-bit 2 to 1 MUX
   i. Idealized picture below



Data 0	Data 1	Select	Output
10	11	0	
01	00	1	
11	01	0	
10	01	1	

d. Can use MUXes to implement functions