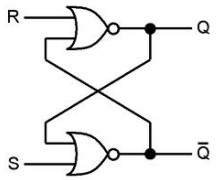
1. More on latches
    a. S-R NOR latch below



Circuit Diagram

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	Undefined

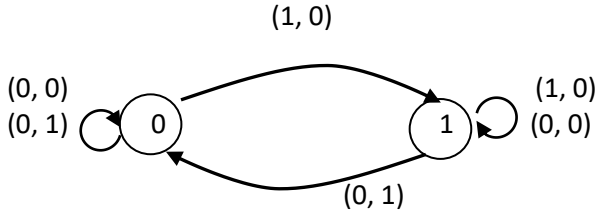
Characteristic Table

    b. State transition table for S-R NOR latch

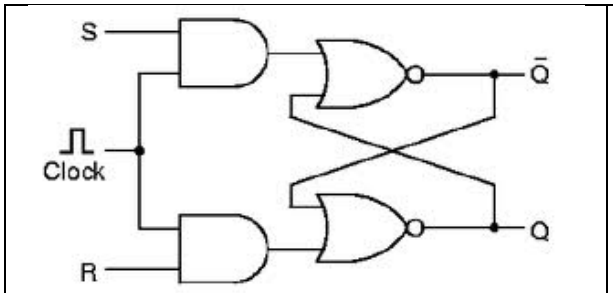
State Transition Table for S-R NOR Latch				
Present Inputs		**Present State**	**Next State**	**Type of Circuit**
S	**R**	**Q**	**Q'**	
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

    c. State transition diagram
        i. Visual representation of circuit's output

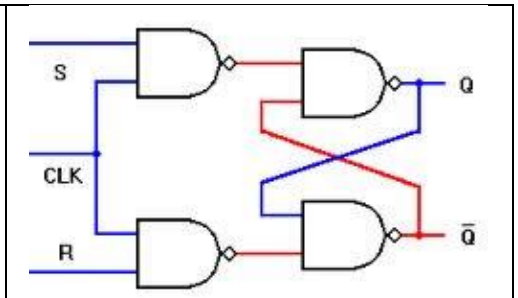
        ii. For every state, all possible output combinations need to be listed



2. Other latches
    a. Clocking the latches

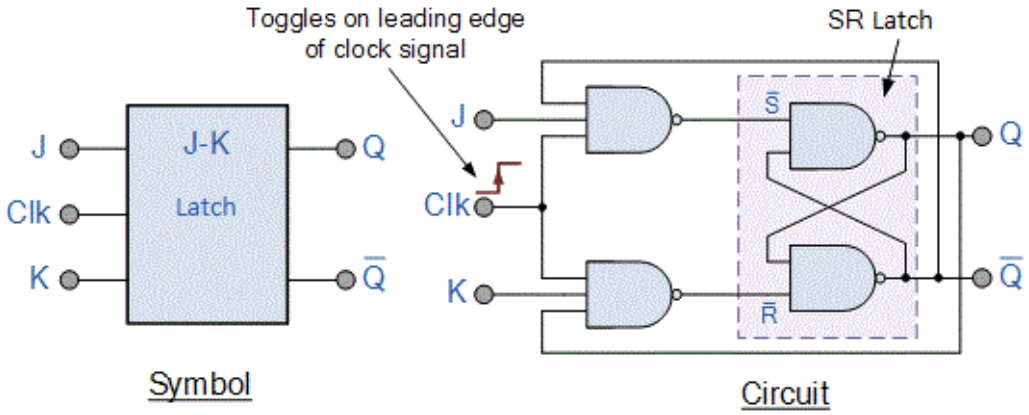


Clocked S-R NOR Latch

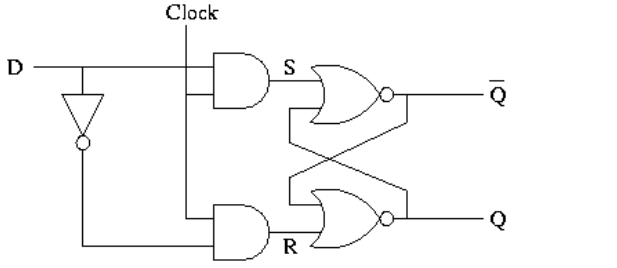


Clocked S-R NAND Latch

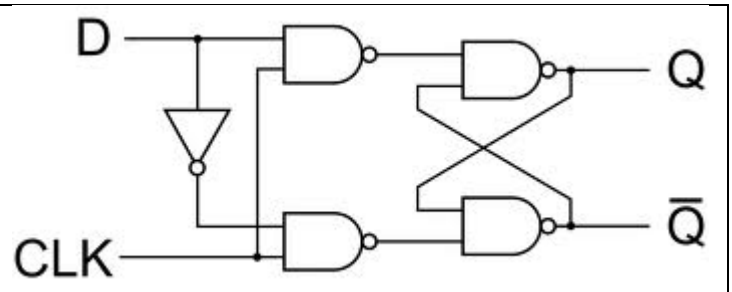
b. Clocked J-K latch
    i. Like a S-R latch



b. Clocked D latch



Clocked NOR D Latch



Clocked NAND D Latch

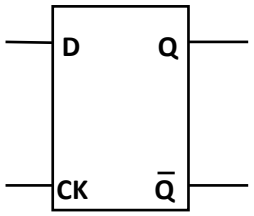
2. Flip-flops
    a. Circuit terminology

    b. Back to flip-flops

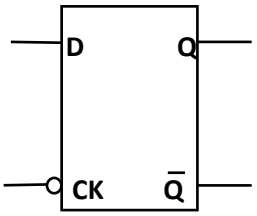
    c. Advantages

    d. Disadvantage

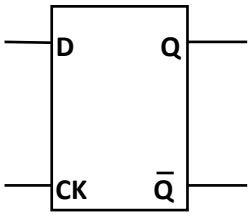
    e. Types of flip flops



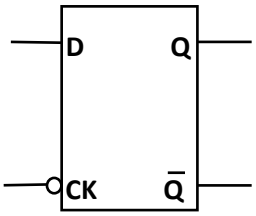
Positive D Latch



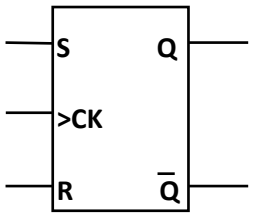
Negative D Latch



Rising Edge D Flip-Flop

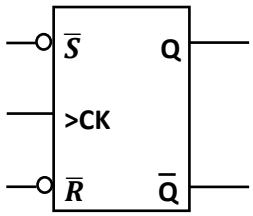


Falling Edge D Flip-Flop



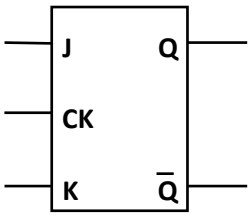
S-R Flip-Flop (NOR)

S	R	*Q(t + 1)*
0	0	
0	1	
1	0	
1	1	



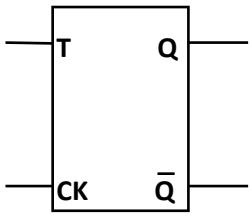
S-R Flip-Flop (NAND)

S	R	*Q(t + 1)*
0	0	
0	1	
1	0	
1	1	



J-K Flip-Flop

J	K	*Q(t + 1)*
0	0	
0	1	
1	0	
1	1	



T Flip-Flop

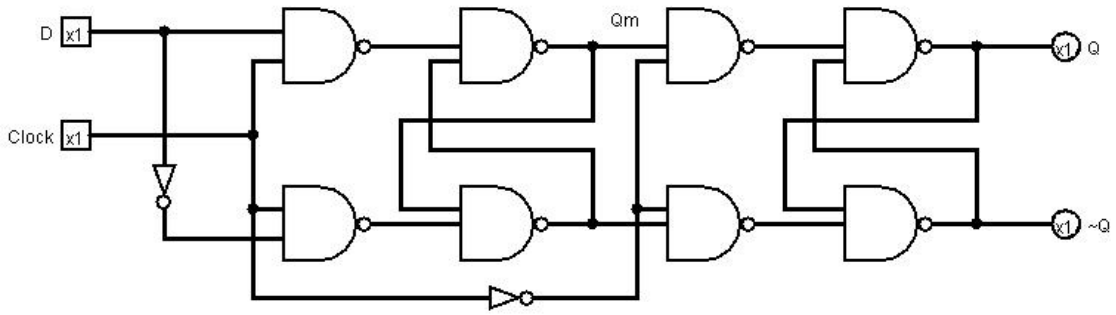
T	*Q(t + 1)*
0	
1	

    f. Named flip flops work similarly to their latch counterparts
        i. One new addition

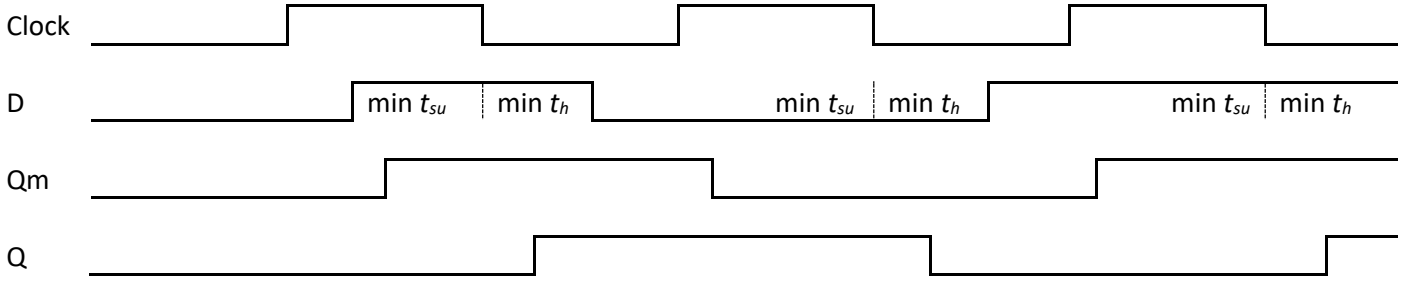
3. Flip flop timing terminology
   a. t_{su}

   b. t_h

4. Falling edge-triggered master-slave D flip-flop



   a. Timing diagram



5. Rising-edge triggered D flip-flop