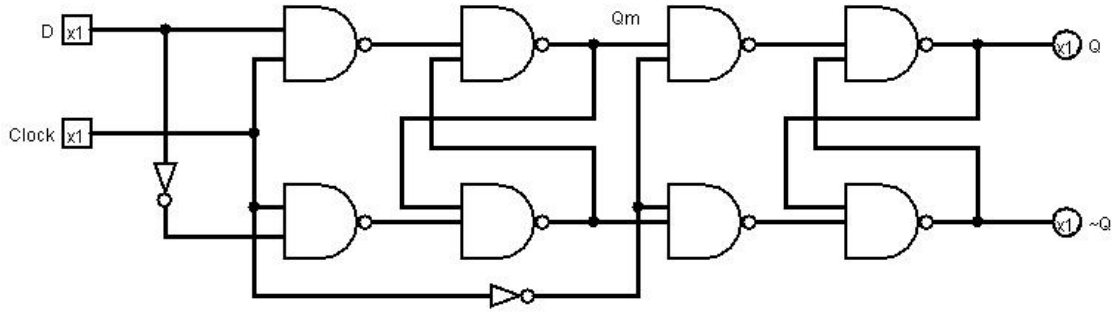
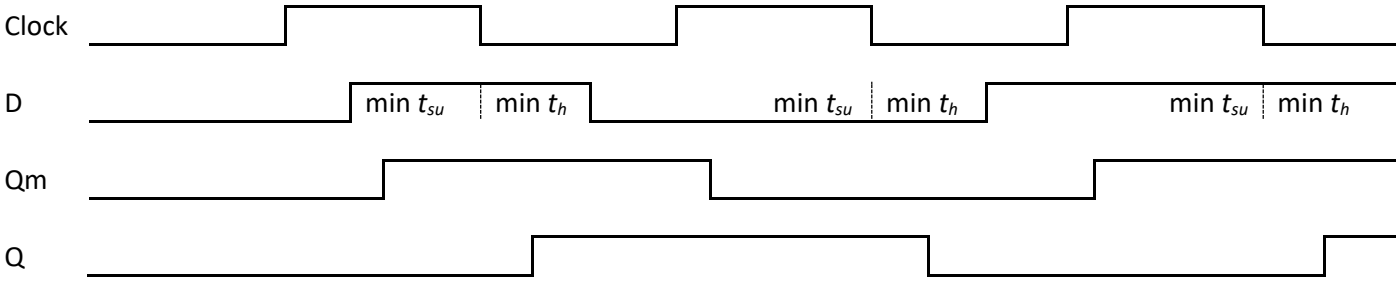
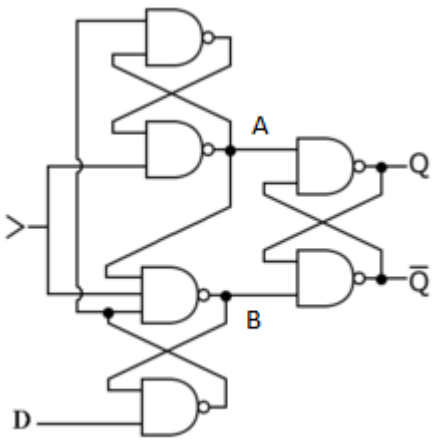
1. Falling edge-triggered master-slave D flip-flop

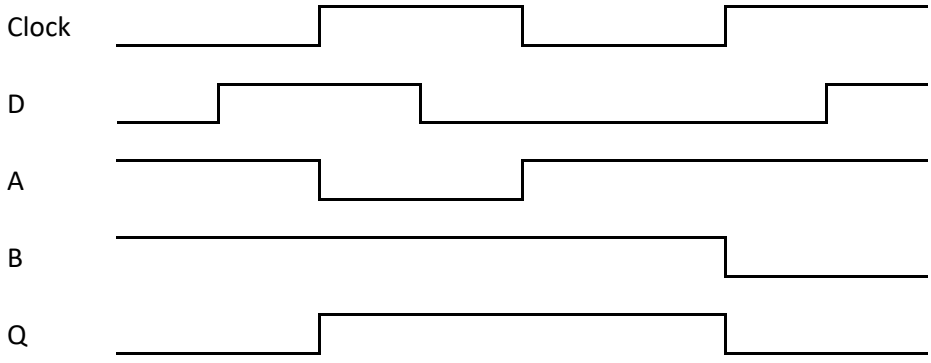



a. Timing diagram




2. Rising-edge triggered D flip-flop



3. Flip flop timing

   a. Two main times to consider for flip flops
      i. Setup time

      ii. Flip flop propagation delay

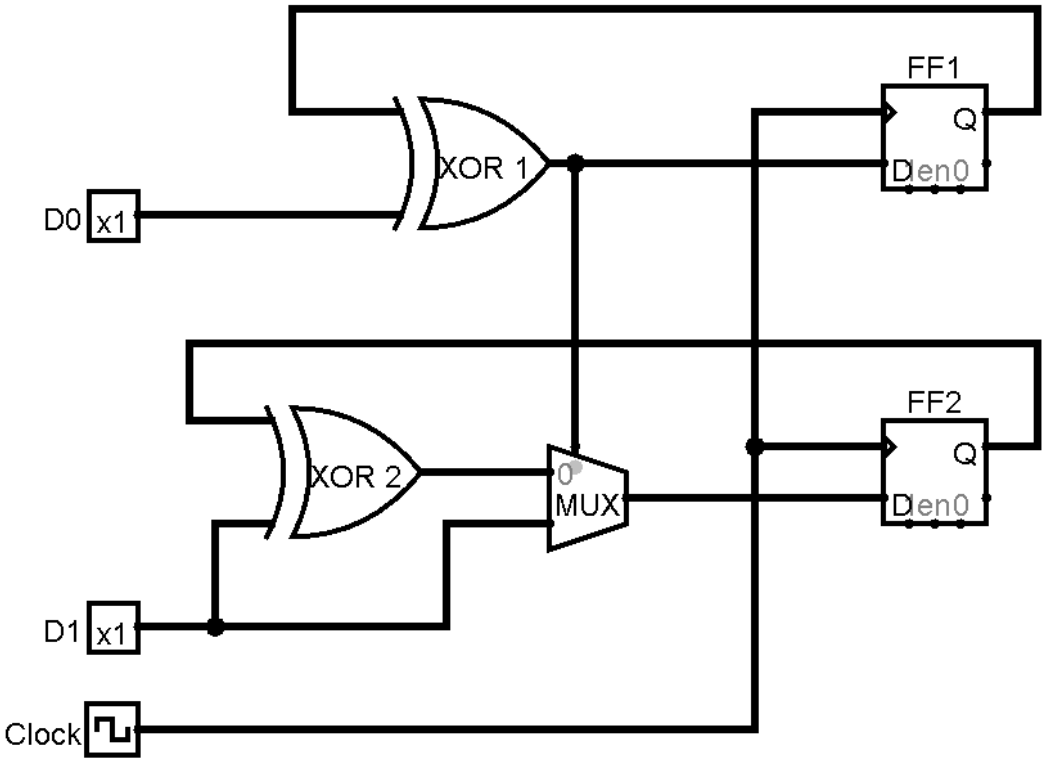
      iii. Hold time – not important

   b. Keeping track of times in larger circuit diagrams
      i. Inputs start at time 0

      ii. Flip flops start at their propagation delay

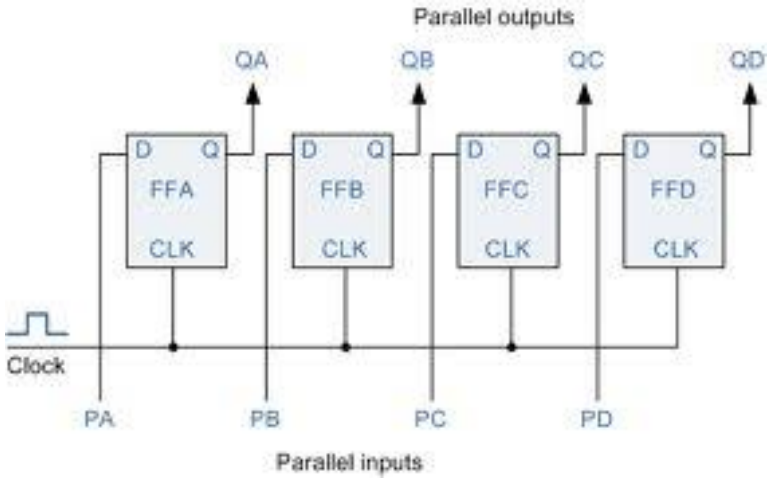
      iii. Calculating delays for each gate

c. Example
   i. DFF setup delay = 4 ns
   ii. DFF propagation delay = 2 ns
   iii. XOR gate delay = 2 ns
   iv. MUX gate delay = 3 ns

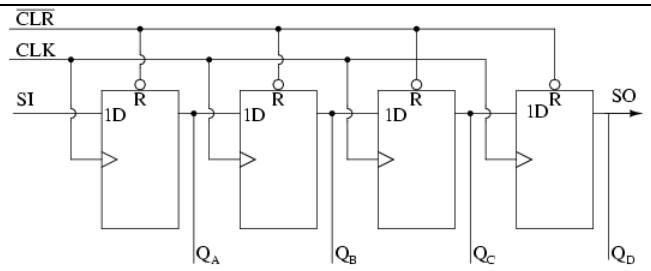



4. Registers

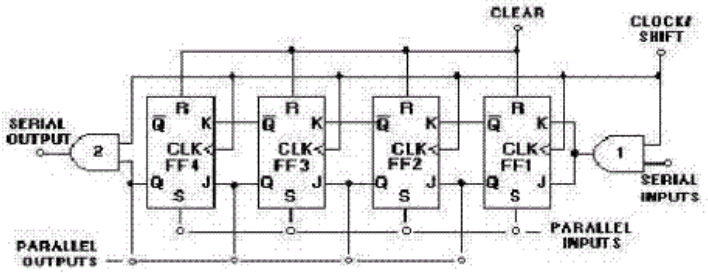
a. Parallel register



b. Shift register



Serial-in/ Parallel out shift register details



Shift register with variety of function modes

5. Counter

a. Eventually “saturates”

b. Ripple (asynchronous) counters

c. Synchronous counter

i. How example below counts

ii. Below: synchronous implementation using T flip flops