Parameter	Value	Type
DATA_WIDTH	8	Signed Integer
ADDR_WIDTH	8	Signed Integer
SIZE_WIDTH	8	Signed Integer

dma_controller_module

clk
rstn
start
uart_data[DATA_WIDTH-1..0]
uart_data_valid
start_address[ADDR_WIDTH-1..0]
transfer_size[SIZE_WIDTH-1..0]

uart_read_enable
memory_write_address[ADDR_WIDTH-1..0]
memory_write_data[DATA_WIDTH-1..0]
memory_write_enable
done

inst2

uart_module

clk
rstn
re

data_out[DATA_WIDTH-1..0]
data_valid

inst1

Parameter	Value	Type
DATA_WIDTH	8	Signed Integer
ADDR_WIDTH	8	Signed Integer
MEMORY_DEPTH	256	Signed Integer

memory_module

clk
rstn
write_address[ADDR_WIDTH-1..0]
data_in[DATA_WIDTH-1..0]
we
read_address[ADDR_WIDTH-1..0]
re

data_out[DATA_WIDTH-1..0]

inst

OUTPUT data out

CLK INPUT
VCC

RSTN INPUT
VCC

dma_system_top

clk
rstn
start
start_address[ADDR_WIDTH-1..0]
transfer_size[SIZE_WIDTH-1..0]
mem_read_address[ADDR_WIDTH-1..0]
mem_read_enable
uart_reset_ptr

done
mem_read_data[DATA_WIDTH-1..0]

inst3

OUTPUT done

Parameter	Value	Type
BUFFER_SIZE	16	Signed Integer
DATA_WIDTH	8	Signed Integer

Parameter	Value	Type
DATA_WIDTH	8	Signed Integer
ADDR_WIDTH	8	Signed Integer
SIZE_WIDTH	8	Signed Integer
MEMORY_DEPTH	256	Signed Integer
UART_BUFFER_SIZE	16	Signed Integer

Revision: