Talha Ahmed

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Education

Sungkyunkwan University *Sept 2023 – June 2025 (expected)*
MS in Electrical and Computer Engineering

- GPA: 3.5/4.5
- **Coursework:** SoC Architecture, Digital IC, Memory System, Advance Algorithms
- **Research Area:** Secure Computer Architecture, Matmul Algorithms

UIT University *Aug 2018 – Aug 2022*
BS in Software Engineering

- GPA: 3.1/4.0
- **Research Area:** Computer Architecture

Technologies

Languages: Scala, CHISEL, C, Python, CUDA, Verilog, Assembly

Technologies: Chipyard, Git, Vivado, Linux, RISC-V ISA

Experience

Research Assistant *Sept 2023 – Present*
Computer Architecture and Systems Lab - COMPASS LAB SKKU *Suwon, South Korea*

- Server setup for Firesim with Alveo-U280 FPGA for cloud based FPGA acceleration.
- Evaluate multiple matmul algorithms on GPU using CUDA.
- Improving the security and performance by minimizing the overhead for NVMe based storage.

RISC-V CPU Designer *Oct 2022 – Sept 2023*
Internee *July 2022 – Sept 2022*
Intensivate *Berkeley, California (Remote)*

- Integrate memory system IP with the Rocket Chip based server class CPU in CHISEL.
- Design an integrate GPIO in SoC with appropriate cells.
- Verify the integration of SRAM based memory IPs in RTL.
- Added new MMIO modules in Rocket Chip for better understanding the RTL generation flow.

Research Assistant *Sept 2022 – Aug 2023*
Research Intern *Sept 2019 – Sept 2022*
Micro Electronics Research Lab - MERL *Karachi, Pakistan*

- Designed a System on Chip (SoC) Generator in CHISEL HDL.
- Taped out a generated SoC in Google MPW6 Shuttle using Skywater 130nm PDK.
- Designed Timer and SPI device and integrated M and C extension in NucleusRV core.
- Involved in reverse engineering of Rocket Chip.

Projects

SoC-Now: Open Source Web based RISC-V SoC Generator. *Github: SoC-Now*
Bachelor's Final Year Project

- Developed plug-and-play SoC components (e.g., bus interconnects, devices and RV32imfc core), made configurations parametrized with CHISEL, integrated a web interface for automated SoC generation and emulation.
- Tools Used: Scala, CHISEL, Python

OpenRegFile: Open Source Register File Generator *GSoC'22*

- Extended the OpenRAM memory compiler to automate latch-based register file generation using Skywater 130nm standard cells. OpenRegFile produces spice netlists, layouts, and Verilog models, utilizing hierarchical decoders and muxes from SRAM designs.
- Tools Used: Python, OpenRAM

MDU_RV32: Multiplication and Division Unit for RV32 Core. *Github: mdu_rv32*

- Implemented M extension in NucleusRV (a RISC-V based core in CHISEL) along with compliance verification.
- Tools Used: Scala, CHISEL

Mentorship

Linux Foundation Mentorship Program 2023 - Mentor F Extension

Mentored a RISC-V sponsored project in Linux Foundation.

Google Summer of Code 2022 - Mentee OpenRegFile

Project "Register File Generator" under supervision of CROSS - UC Santa Cruz.

Poster Presentation

RISC-V Summit Europe 2023 Extended Abstract

ChipShop: A Cloud-Based GUI for Accelerating SoC Design

First Firesim and Chipyard User and Developer Workshop at ASPLOS'23 Workshop

ChipShop: A Cloud-Based GUI for Accelerating SoC Design

Workshop on Open Source EDA Technology - WOSET'22 Workshop

SoC-Now: An Open-Source Web based RISC-V SoC Generator
Bitstream Chef
OpenRegFile: Open-Source Register File Generation

RISC-V International Summit 2020 Presentation

Reverse Engineering of Rocket Chip

Achievement

Multi Project Wafer 6 Github: soc-now-mpw6

SoCNow generated SoC is taped out in Google sponsered MPW-6.

Extras

Technical Report Writing for Engineers: *Future Learn, University of Sheffield.* Certificate

XOR Linked List Data Structure: Article