

## Education

### Sungkyunkwan University

MS in Electrical and Computer Engineering

Sept 2023 – June 2025 (expected)

- GPA: 3.67/4.5
- **Coursework:** SoC Architecture, Digital IC, Memory System, Advance Algorithms
- **Research Area:** Secure Computer Architecture, Matmul Algorithms

### UIT University

BS in Software Engineering

Aug 2018 – Aug 2022

- GPA: 3.1/4.0
- **Research Area:** Computer Architecture, Digital Design Automation

## Technologies

**Languages:** Scala, CHISEL, C, Python, CUDA, Verilog, Assembly

**Technologies:** Chipyard, Git, Vivado, Linux, RISC-V ISA

## Experience

### Research Fellow

Computer Architecture and Systems Lab - COMPASS LAB SKKU

Sept 2023 – Present

Suwon, South Korea

- Server setup for Firesim with Alveo-U280 FPGA for cloud-based FPGA acceleration.
- Evaluate multiple matmul algorithms on GPU using CUDA.
- Improving the security and performance by minimizing the overhead for NVMe based storage.

### RISC-V CPU Designer

Oct 2022 – Sept 2023

### Internee

Intensivate

July 2022 – Sept 2022

Berkeley, California (Remote)

- Integrate memory system IP with the Rocket Chip based server class CPU in CHISEL.
- Design and integrate GPIO in SoC with appropriate cells.
- Verify the integration of SRAM based memory IPs in RTL.
- Added new MMIO modules to Rocket Chip for better understanding the RTL generation flow.

### Google Summer of Code 2022

Center for Research in Open Source Software - CROSS

June 2022 – Sept 2022

Santa Cruz, California (Remote)

- Implement the digital design of the latch-based register file.
- Extend OpenRAM memory compiler for register file generation.
- Use open source Skywater PDKs for compilation and fix DRC and LVS issues.

### Research Assistant

Sept 2022 – Aug 2023

### Research Intern

Micro Electronics Research Lab - MERL

Sept 2019 – Sept 2022

Karachi, Pakistan

- Designed a System on Chip (SoC) Generator in CHISEL HDL.
- Taped out a generated SoC in Google MPW6 Shuttle using Skywater 130nm PDK.
- Designed Timer and SPI device and integrated M and C extension in NucleusRV core.
- Involved in reverse engineering of Rocket Chip.

## Publications

### An Experimental Study of Merkle Tree-Based Security Mechanism for Secure SSD Storages

Osaka, Japan

Talha Ahmed and Seokin Hong

2025 International Conference on Electronics, Information, and Communication (ICEIC)

[10.1109/ICEIC64972.2025.10879627](https://doi.org/10.1109/ICEIC64972.2025.10879627) [🔗](#)

## Achievement

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### Tape-out: Multi Project Wafer 6

[Github: soc-now-mpw6](#) 

SoCNow generated SoC is taped out in Google sponsored MPW-6.

## Mentorship

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### Linux Foundation Mentorship Program 2023 - Mentor

[Blog](#) 

Mentored a RISC-V sponsored project in Linux Foundation.

### Google Summer of Code 2022 - Mentee

[Blog](#) 

Project “Register File Generator” under supervision of CROSS - UC Santa Cruz.

## Projects

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### SoC-Now: Open Source Web based RISC-V SoC Generator.

[Github: SoC-Now](#) 

#### Undergrad Final Year Project

- Developed plug-and-play SoC components (e.g., bus interconnects, devices and RV32imfc core), made configurations parametrized with CHISEL, integrated a web interface for automated SoC generation and emulation.
- Tools Used: Scala, CHISEL, Python

### OpenRegFile: Open Source Register File Generator

[GSoC'22](#) 

- Extended the OpenRAM memory compiler to automate latch-based register file generation using Skywater 130nm standard cells.
- OpenRegFile produces spice netlists, layouts, and Verilog models, utilizing hierarchical decoders and muxes from SRAM designs.
- Tools Used: Python, OpenRAM, Magic, Netgen

### MDU\_RV32: Multiplication and Division Unit for RV32 Core.

[Github: mdu\\_rv32](#) 

- Implemented M extension in NucleusRV (a RISC-V based core in CHISEL) along with compliance verification.
- Tools Used: Scala, CHISEL

## Poster Presentation

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### RISC-V Summit Europe 2023

[Extended Abstract](#) 

ChipShop: A Cloud-Based GUI for Accelerating SoC Design

### First Firesim and Chipyard User and Developer Workshop at ASPLOS'23

[Workshop](#) 

ChipShop: A Cloud-Based GUI for Accelerating SoC Design

### Workshop on Open Source EDA Technology - WOSET'22

[Workshop](#) 

SoC-Now: An Open-Source Web based RISC-V SoC Generator

Bitstream Chef

OpenRegFile: Open-Source Register File Generation

### RISC-V International Summit 2020

[Presentation](#) 

Reverse Engineering of Rocket Chip

## Extras

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**Technical Report Writing for Engineers:***Future Learn, University of Sheffield.*

[Certificate](#) 

**XOR Linked List Data Structure:**

[Article](#) 