LAB # 02

Develop, implement & simulate Full Adder & Half Adder through Schematic & Gate Level Modeling

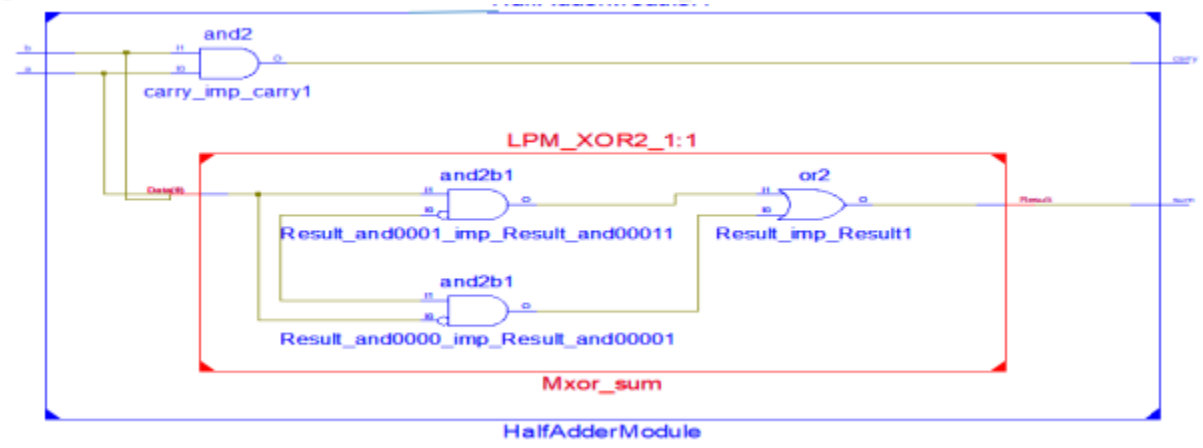
Objective: Develop, implement & simulate Half Adder & Full Adder through Schematic & Gate Level Modeling.

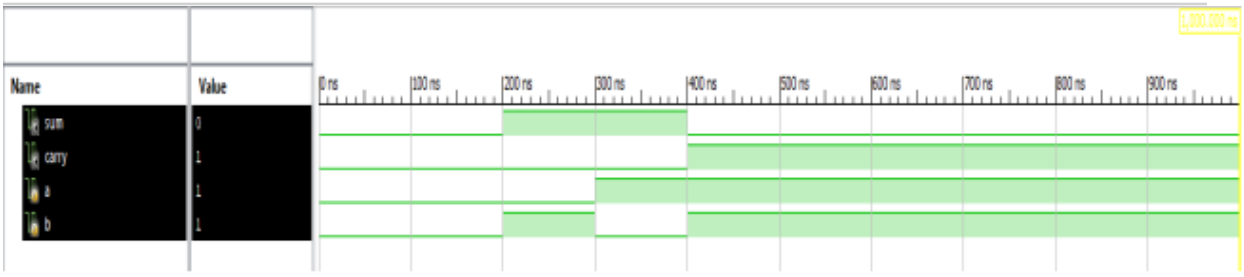
Task 1: Develop, implement & simulate Half Adder through Schematic & Gate Level Modeling

```
`timescale 1ns / 1ps
module HalfAdderTf;
   // Inputs
   reg a;
   reg b;
   // Outputs
   wire sum;
   wire carry;
   // Instantiate the Unit Under Test (UUT)
   HalfAdderModule uut (
      .a(a),
      .b(b),
      .sum(sum),
      .carry(carry)
   );
   initial begin
      // Initialize Inputs
      a = 0; b = 0;
      #100;
      a = 0; b = 0;
      #100;
      a = 0; b = 1;
      #100;
      a = 1; b = 0;
      #100;
      a = 1; b = 1;
      #100;
      // Wait 100 ns for global reset to finish
      // Add stimulus here
   end
endmodule
```

```
`timescale 1ns / 1ps
module HalfAdderModule(
    input a,
    input b,
    output sum,
    output carry
    );

xor(sum,a,b);
and(carry,a,b);
endmodule
```





Task 2: Develop, implement & simulate Full Adder using schematic & Gate Level Modeling

```
`timescale 1ns / 1ps
module FullAdderModule(
    input a,
    input b,
    input cin,
    inout s1,
    inout c1,
    inout c2,
    output sum,
    output cout
    );
xor(s1,a,b);
xor(sum,s1,cin);
and(c1,cin,s1);
and(c2,a,b);
or(cout,c1,c2);

endmodule
```

```
`timescale 1ns / 1ps
module FullAdderTf;
    // Inputs
    reg a;
    reg b;
    reg cin;
    // Outputs
    wire sum;
    wire cout;
    // Bidirs
    wire s1;
    wire c1;
    wire c2;
    // Instantiate the Unit Under Test (UUT)
    FullAdderModule uut (
        .a(a),
        .b(b),
        .cin(cin),
        .s1(s1),
        .c1(c1),
        .c2(c2),
        .sum(sum),
        .cout(cout)
    );
    initial begin
        // Initialize Inputs
        a = 0;
        b = 0;
        cin = 0;
        // Wait 100 ns for global reset to finish
        #100;
        a=0; b=0; #100;
```