LAB 11

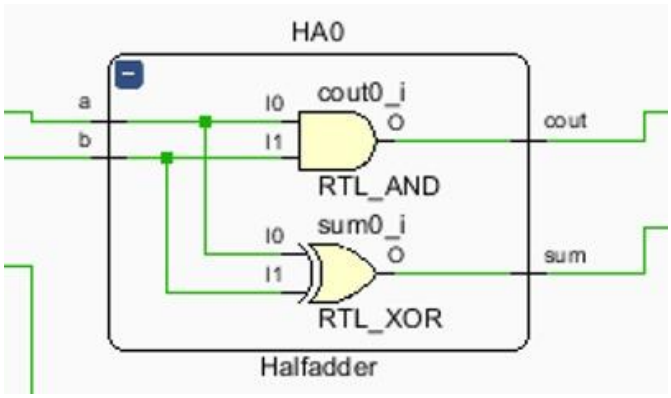
OBJECTIVE

Reproduce and implement Half Adder by using FPGA Kit.

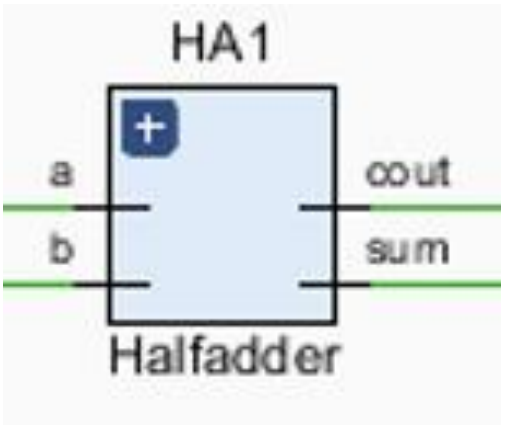
Verilog Module Code:

```
module Halfadder(
    input a,
    input b,
    output sum,
    output cout
    );


    reg sout,c;

    always@(*)
    begin
            sout<=a^b;
            c=a&b;
    end

    assign sum=sout;
    assign cout=c;
endmodule
```

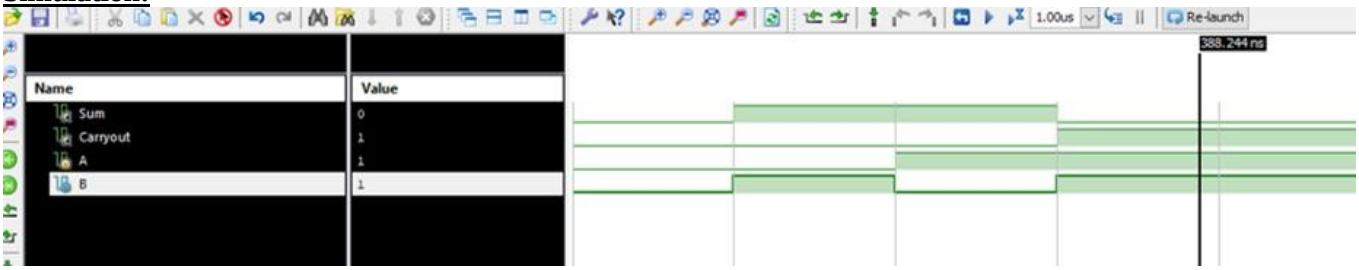
Design Schematic 01:



Design Schematic 02:



Simulation:



Conclusion:

In this lab we learn how to Reproduce and implement Half Adder by using FPGA Kit.