LAB 12

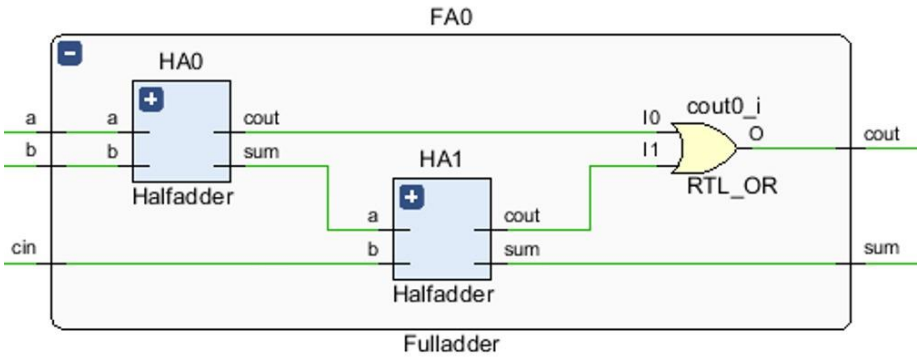
OBJECTIVE

Reproduce and implement Full Adder by using FPGA Kit.

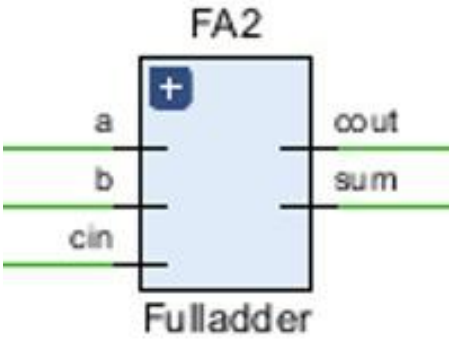
Verilog Module Code:

```
module Fulladder(
    input a,
    input b,
    input cin,
    output sum,
    output cout
    );


wire c1,c2,s;
reg c;

    Halfadder HA0(a,b,s,c1);
    Halfadder HA1(s,cin,sum,c2);


    always@(*)
    begin

            c <= c1||c2;
    end


    assign cout = c;


endmodule
```

Design Schematic 01:



Design Schematic 02:



Simulation:

Conclusion:

In this lab we learn how to Reproduce and implement Full Adder by using FPGA Kit.