



The Next-Generation of Intelligent, Embedded-Edge Programmable Devices



2021

Rapid Silicon was founded in 2021



Headquarters Silicon Valley

Other locations: Penang, Lahore



130

Our team consists of 130 employees

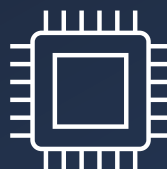


150+

Our exec team has 150+ years of industry experience

FPGA

Low to mid-range FPGA



Applications

Variety of domain-specific FPGAs suited to diverse target applications



Open-Source

Industry's first open-source EDA tool



Financing Funded by top semiconductor VCs



Production:
TSMC
#1 Fab in the world



Quality & Operations:
World Class
manufacturing



Experienced Team Built by Industry Veterans

15+ FPGAs Delivered



Total Units Shipped

10B+



Executive Team
PLD Experience

150 years



Complex SoC
Tapeouts

300+

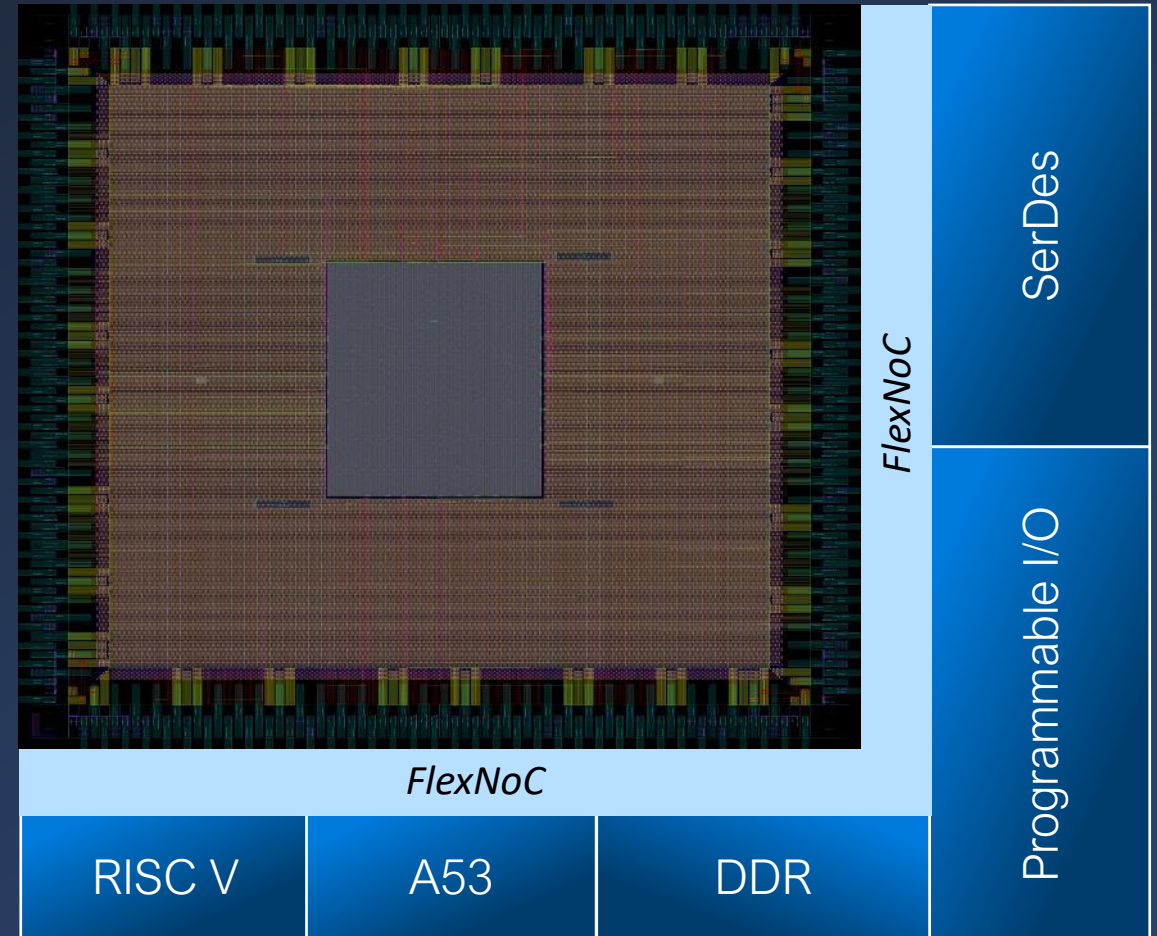


Advanced
Nodes

10+

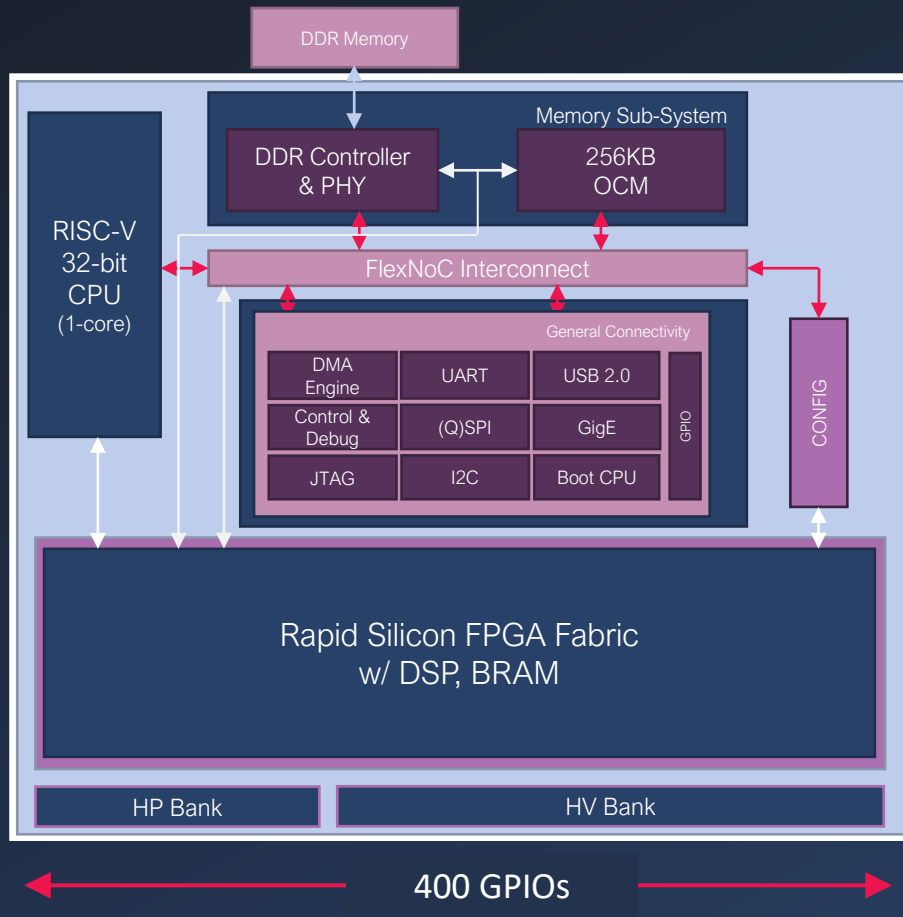
Rapid Silicon Product Differentiation

- 1 | Use OpenFPGA to design core fabric for fast time to market
- 2 | Utilizing industry standard, silicon-proven 3rd party IP libraries for time to market and reliability
- 3 | FlexNoC enables easy IP integration to a wide range of IP to develop variants quickly
- 4 | Singular Focus on Edge Products!
No datacenter distraction



Introducing Gemini

The new standard for cost-effective Embedded FPGAs



Built on proven TSMC 16nm FinFET process

30-100K Logic Density built on Open Standard
6-input LUT Logic Blocks

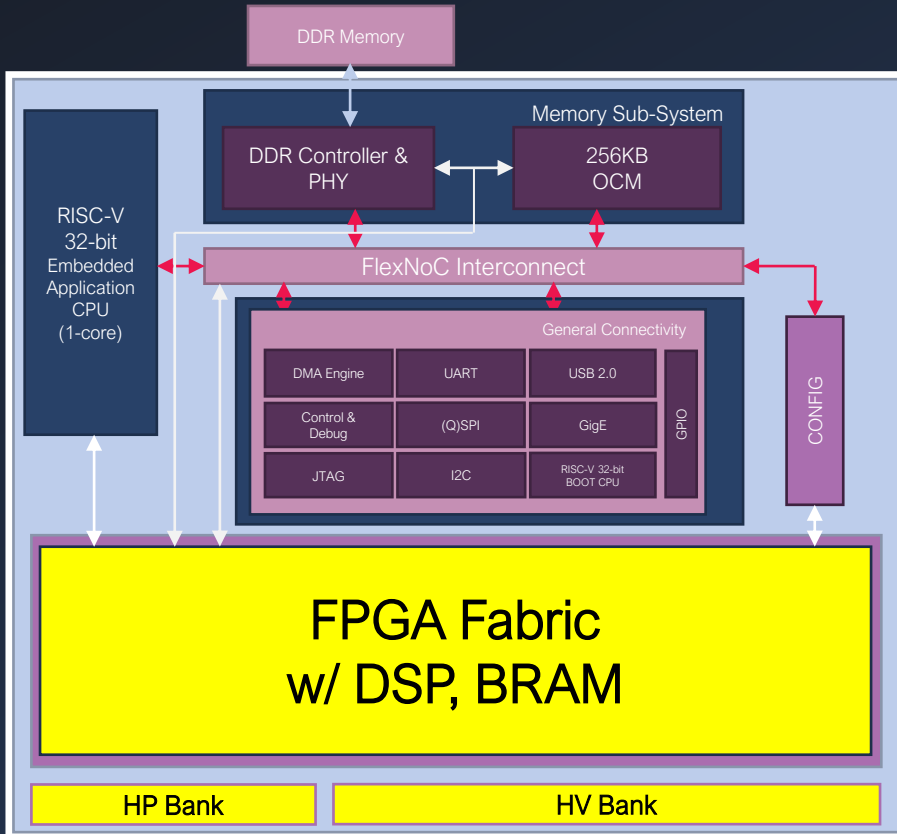
Hardened 32-bit RISC-V processor running @
533MHz

Hardened FlexNoC and Connectivity Block

Hard 32-bit Memory Controller

500+ I/O – Industry leading I/O-to-LC ratio

Gemini (Rapid Si) Fabric Domain



Fracturable 6-input LUT with carry chain

64-bit/128-bit AXI interface to Processing Domain running up to 400 MHz

36Kb True Dual Port RAM

18x20 Multipliers w/ 64-bit accumulator and carry

General Purpose (HV) and High Performance (HP) I/O Banks

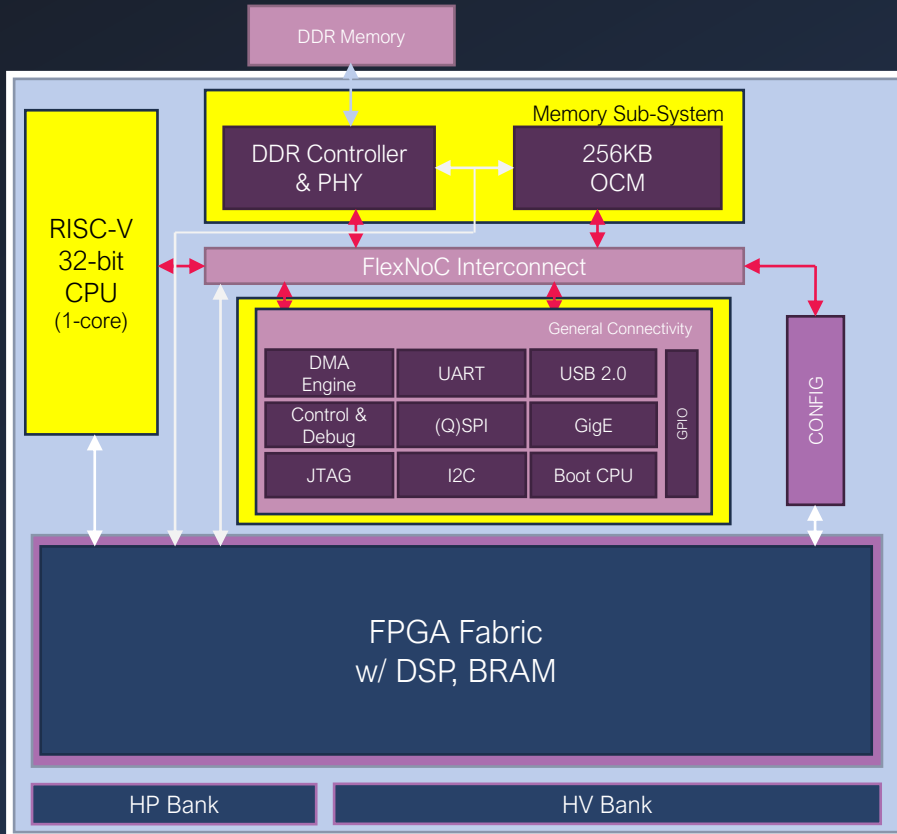
LVC MOS, LVTTTL, SSTL (I/II), PCI66/X, LVDS, LVPECL, BLVDS, RSDS

40-bit bank size

Selectable drive strength, slew rate, ODT

Native support for LVDS @ 1.2Gbps and MIPI @ 1.5Gbps

Gemini Processing Domain



RISC-V A45 Processor CPU Subsystem

16KB I/D Cache + 64K tightly integrated I/D Memory

Memory Management Unit (MMU), Physical Memory Protection(PMP), and programmable Physical Memory Attribute (PMA)

DDR3 / DDR4 Controller and PHY

Data-rates up to 2133 Mbps

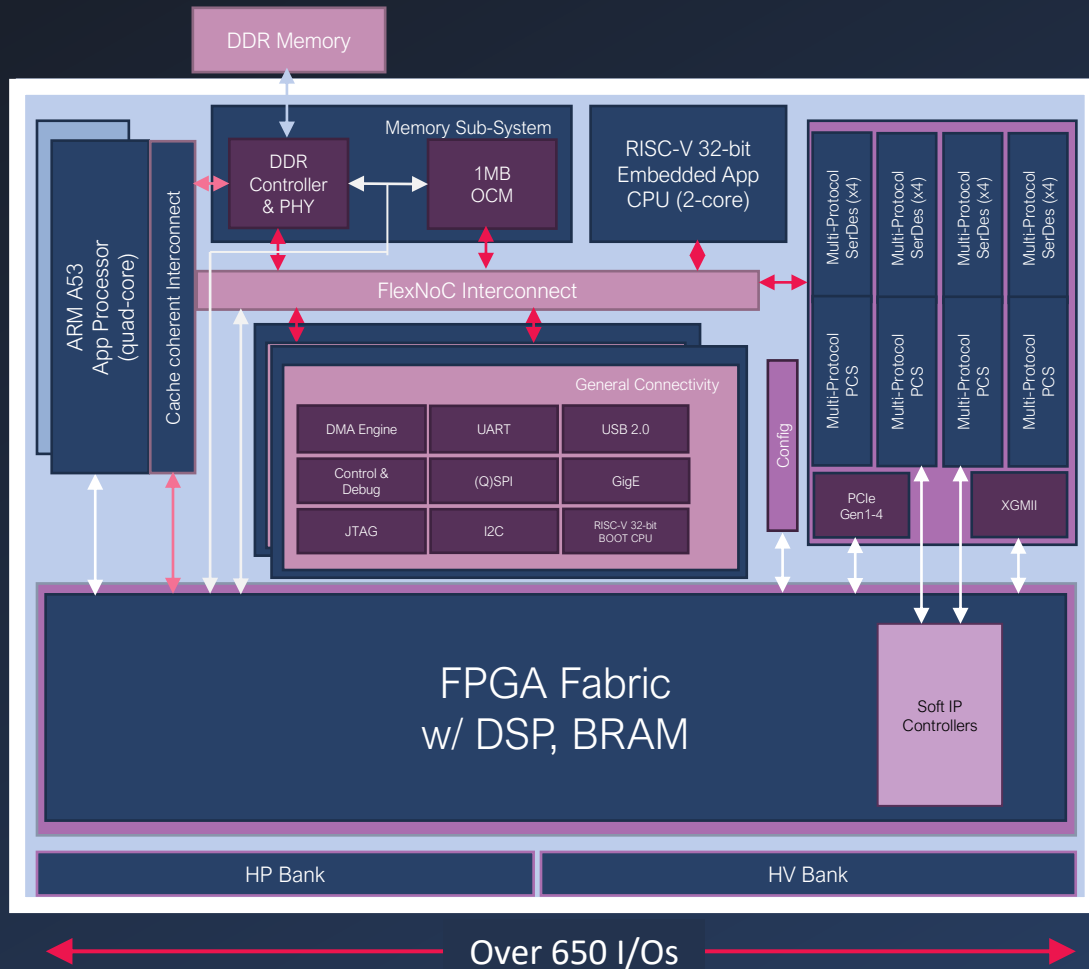
16-bit or 32-bit DDR memory interface

256KB On-chip Memory and Controller



Orion for Signal Compute & Throughput

Application-Level Processing and High-Speed Transceivers - Built for Low Power



Built on proven TSMC 16nm FinFET process

120-350K Logic Density

Dual/Quad-core Arm Cortex-A53 Processors

Hardened dual 32-bit RISC-V Processors

Hardened FlexNoC and Connectivity Block

Up to 24 Multi-Protocol 16Gb Transceivers
with hardened PCIe Gen 4 & Ethernet

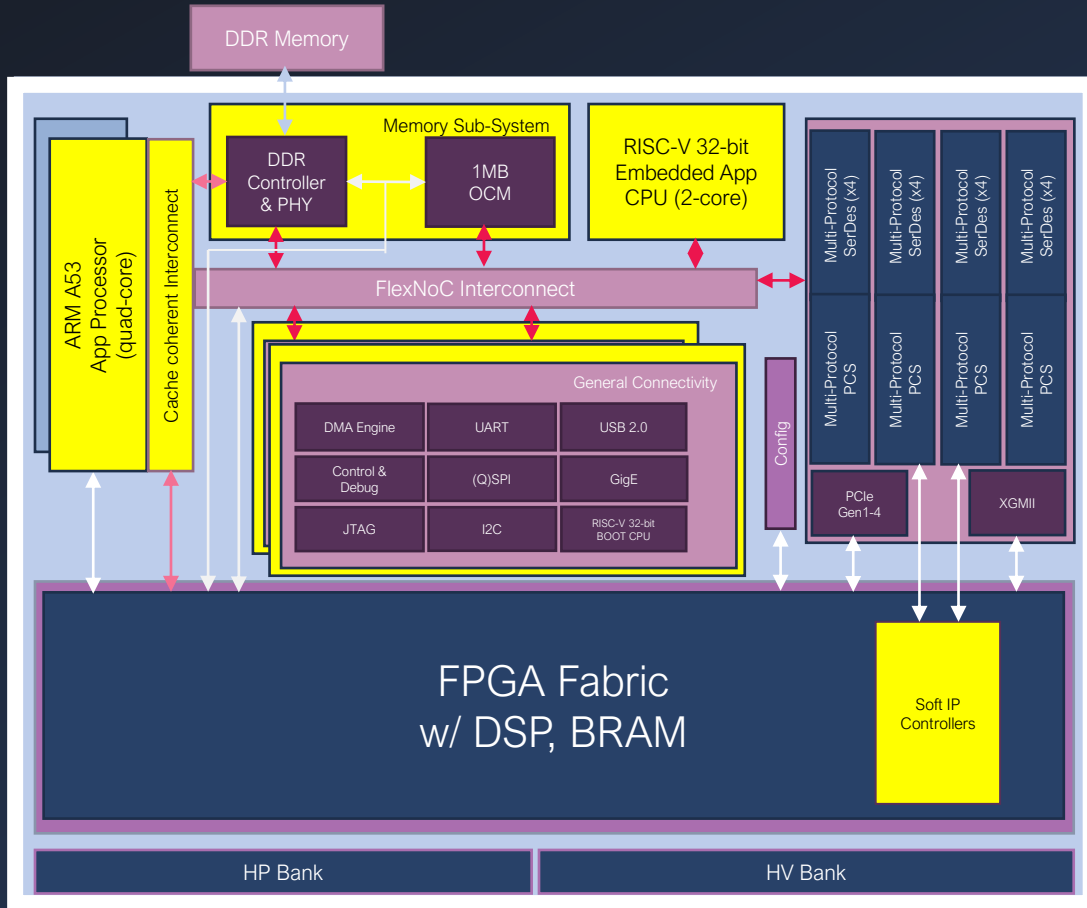
Hard 32-bit DDR Memory Controller

Multiple Power Domains for Low Power

Up to 650 I/O available



Orion Processing Domain



Dual/Quad-Core Arm Cortex-A53 Processors running up to 1.6GHz

Hardened dual 32-bit RISC-V processor running up to 533MHz

Lock Step Capable

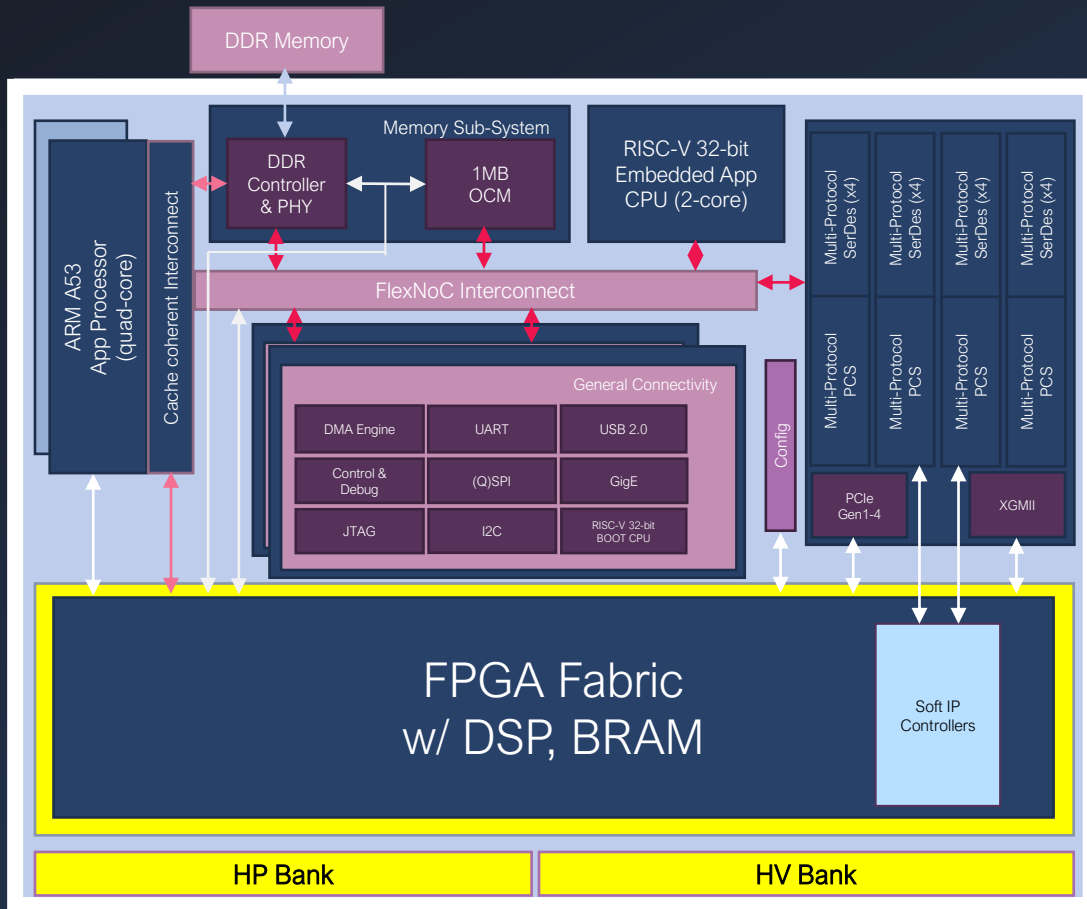
Support for UEFI, Zephyr RTOS, Linux OS

Hard DDR Memory Controller

DDR4, LPDDR4/5 up to 2666 Mbps

On-Chip Memory up to 1 MB

Orion Programmable Fabric Domain



Fracturable 6-input LUT w/ carry chain

64-bit/128-bit AXI interface to Processing Domain running up to 400MHz

36Kb BRAM with FIFO support

18x20 DSP with 64-bit accumulator and carry

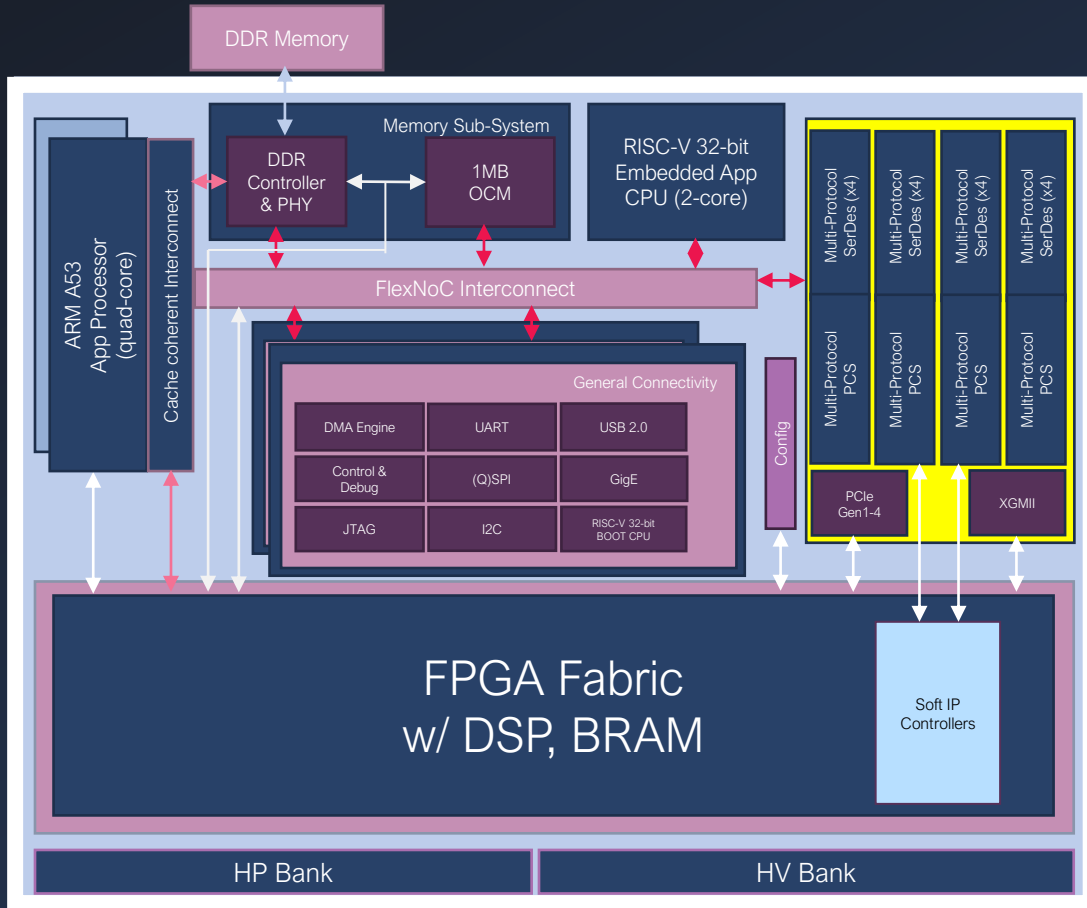
32-bit FPU w/ BFLOAT16 + INT8 + FP16/32 support

General Purpose (HV) and High Performance (HP) I/O Banks

LVDS @ 1.6Gbps and MIPI Support @ 2.5Gbps

40-bit banks with selectable drive strength, slew rate, ODT

Orion High Speed Interfaces



Up to 24, 16Gbps Transceivers

- Power and Area Optimized

Multi-Protocol PCS

- Hardened PCIe Gen 4 x8 support
- Hardened XGMII Ethernet Support

Large set of protocol support

- V-by-One HS, (Q)SGMII, IEEE 802.3 XAUI and 10G-KR, JESD204B/C, CPRI, HiGig, DP, (e)DP, SRIO

Integrated Fractional PLL

Adaptable PMA for data eye integrity



Introducing Vega embedded FPGA (eFPGA)

Unlock the Potential of Your SoC with Vega eFPGA: Flexible, Powerful, and Efficient!



- Customizable & Scalable architecture
- Logic – 6-input look-up-tables (LUTs) with integrated fast adders for efficient implementation of complex logic functions
- DSP – 18x20 multiplier, 64-bit accumulator to efficiently execute math functions such as FIR filters
- Block RAM – 36 Kb or 18 Kb True Dual Port RAM for improved system performance
- Designed for TSMC's 16nm FinFET process node
- High-Performance, Flexible I/O supporting up to 3.3V with support for LVDS and MIPI

Maximizing Benefits with Vega IP

Harnessing the Power of Vega eFPGA IP for Your Business

Customize Vega to Suit Your Needs

Leverage the power of our modular architecture to suit your needs. Specify the number of logic blocks, DSPs, BRAMs, interconnect, and PPA budget to help you architect the exact FPGA you need

Enhance Flexibility with On-Chip FPGA functionality

Eliminate the need for an on-board FPGA and reduce manufacturing costs, board space, time to market, and the need for multiple SoC variants with on-chip FPGA functionality. Empower your SoC with Vega eFPGA.

Accelerate Your Processor with Vega eFPGA

Eliminate the need for sacrifices in board-space, I/O latency, and bandwidth while using standard FPGA for processor acceleration. Vega eFPGA brings those accelerators on-chip, without the limitations or overhead of I/O pad-count or chip-to-chip communication interfaces.

Seamlessly Integrate and verify Vega IP into your SoC Design

Vega eFPGA is designed to provide seamless integration into your SoC, and can be verified at multiple levels for maximum reliability

Program Vega with Raptor Design Suite

Experience industry's first most capable open-source tool to implement your design using Vega eFPGA IP

Custom Process Portability

Vega IP designed for TSMC's 16nm FinFET process node. For other process technologies, we can easily port Vega IP to meet your needs





The only open-source commercial EDA tool



Raptor Design Suite: Industry's First Open-Source EDA Tool

OPEN &
PROPRIETARY

OPEN-SOURCE

OPEN-SOURCE

OPEN-SOURCE

OPEN-SOURCE
W/ CLA

OPEN-SOURCE
OPTION

OPEN-SOURCE

Design
Entry

IP
Management

Synthesis

Place
&
Route

Timing
Analysis

Simulation

AI/ML

FOEDAG / Verific

- Tcl backend, full design automation support
- Qt-based GUI frontend GTKWave integration

LiteX

- Python-based design builder
- Support for Python-to-RTL
- Library of 50+ qualified and verified open-source Soft IPs (AXI bridges, RiscV soft processors...)

Yoysys

- Verific design parsing for mixed language support, IEEE 1735 encryption
- Yosys optimized for RS architecture
- ABC-DE for device architecture mapping

OpenFPGA/VPR

- OpenFPGA started by Rapid Silicon CTO
- VPR is the most robust open-source place & route engine
- Verific Verilog parser added with IEEE 1735 encryption support

OpenSTA

- Industry standard – also used by AMD-Xilinx & MicroSemi

Verilator/GHDL/Icarus

- Verilator 2 states simulation can boot Linux in simulation < 1 minute
- QEMU for SW development
- GHDL support for VHDL designs
- Icarus support for 4 state and timed simulation

CFU IP

- Based on Google CFU playground
- Implements a custom CPU architecture for AI & ML Workloads
- Up to 10x faster than other implementations
- Innovating new, compact AI/ML models



Open-Source Advantages

Community Engagement

Proven Historical Growth
(Linux and RISC-V)

Easy Access via GitHub

Increased Engagement → Support
via Forums, Slack Channels...



Non-Proprietary

User Control

Enables Custom Modification

Google, Apple and many more
moving to Open Source

Innovation

Endless & Continuous Improvement

No End-of-Life or Archived Tools

Focus on Differentiation

First Commercial-Grade Open-Source EDA Tool

Open-Source Gravitas

Industries are moving rapidly to open source – the FPGA industry is in the early days





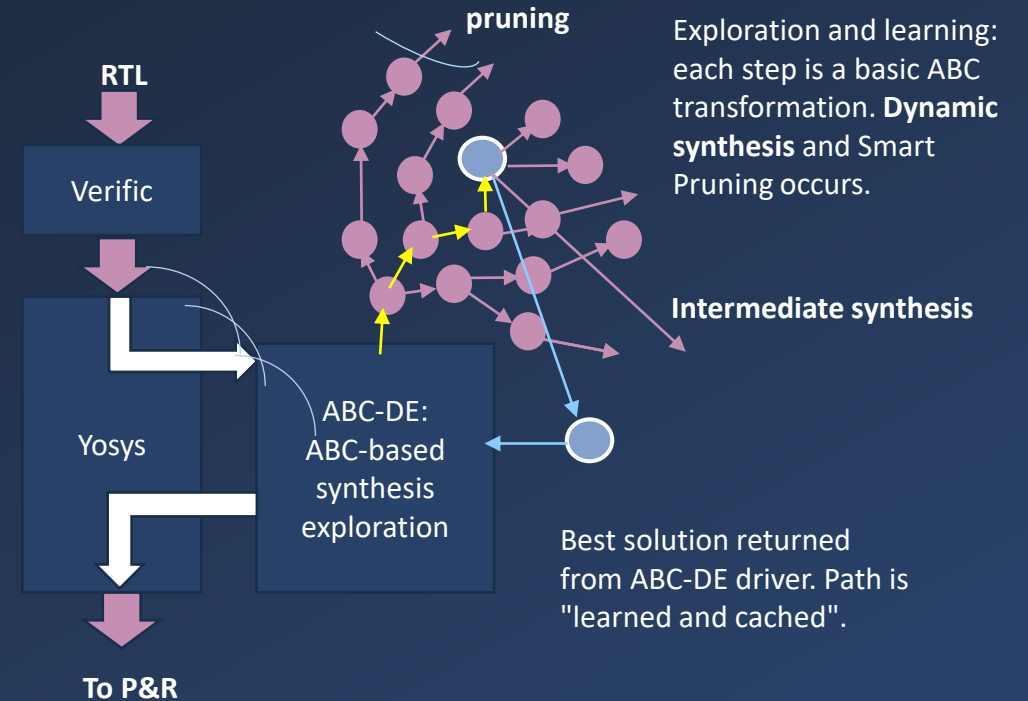
AI Based Enhancement to Yosys ABC

1 Yosys is an open-source implementation of ABC, a logic synthesis engine developed over decades

2 DE is AI-based design exploration addition to ABC, adaptive to the nature of the design, dynamically optimizing

3 Performs dynamic incremental transformations and mapping of boolean logic
Up to 3x reduction in area

4 Benchmarked and proven in public EPFL competition
31 unique Winners out of 46 benchmarks.



Rapid Silicon Flow
(Yosys + ABC-DE)

Intuitive Raptor User Interface

File Project Simulation View Processing Help

Source

- and2_gemini
 - Design Sources(1)
 - and2.v
 - Constraints(2)
 - pin_mapping.pin

Hierarchy

Status	Task	Stats
	IP Generate	
✓	> Analysis	
	> Simulate RTL	
✓	> Synthesis	
	> Simulate Gate	
✓	> Placement	
✓	> Routing	
	> P&R View	
	> Simulate PNR	
✓	> Timing Analysis	
✓	> Power	
✓	> Bitstream Generation	

and2.v synthesis.rpt packing.rpt placement.rpt timing_analysis.rpt

Search Save Undo Redo Cut Copy Paste Delete Select

24 VPR FPGA Placement and Routing.
25 Version: 8.1.0-dev+36371250e-dirty
26 Revision: v8.0.0-6860-g36371250e-dirty
27 Compiled: 2023-01-09T13:01:45
28 Compiler: GNU 9.4.0 on Linux-5.15.0-57-generic x86_64
29 Build Info: Release IPO VTR_ASSERT_LEVEL=2
30
31 University of Toronto
32 verilogtorouting.org
33 vtr-users@googlegroups.com
34 This is free open source code under MIT license.
35
36 VPR was run with the following command-line:
37 /home/ichollangi/ravi/Raptor/build/bin/vpr /home/ichollangi/ravi/Raptor/build/share/raptor/etc/devices/gemini/gemini_vpr.xml and2_gemini_post_synth.v --sdc_file and2_gemini_openfpga.sdc --route_chan_width 192 --suppress_warnings check_rr_node_warnings.log.check_rr_node --clock_modeling ideal --timing_report_npaths 100 --abs
38
39 Architecture file: /home/ichollangi/ravi/Raptor/build/share/raptor/etc/devices/gemini/gemini_vpr.xml
40 Circuit name: and2_gemini_post_synth
41
42
43 # Loading Architecture Description
44 Warning 1: Model 'io' input port 'outpad' has no timing specification (no clock specified to create a sequential input port, not combinational connected to any outputs, not a clock input)
45 Warning 2: Model 'io' output port 'inpad' has no timing specification (no clock specified to create a sequential output port, not combinational connected to any inputs, not a clock input)
46 Warning 3: Model 'mmio' input port 'SI' has no timing specification (no clock specified to create a sequential input port, not combinational connected to any outputs, not a clock input)
47 Warning 4: Model 'mmio' output port 'SO' has no timing specification (no clock specified to create a sequential output port, not combinational connected to any inputs, not a clock output)
48 Warning 5: Model 'z_pad_twof' output port 'logic0' has no timing specification (no clock specified to create a sequential output port, not combinational connected to any inputs, not a clock output)
49 Warning 6: Model 'logic0' output port 'logic0' has no timing specification (no clock specified to create a sequential output port, not combinational connected to any inputs, not a clock output)
50 Warning 7: Model 'logic1' output port 'logic1' has no timing specification (no clock specified to create a sequential output port, not combinational connected to any inputs, not a clock output)
51 Warning 8: Model 'dsp_phy' input port 'sc_in' has no timing specification (no clock specified to create a sequential input port, not combinational connected to any outputs, not a clock input)
52 Warning 9: Model 'dsp_phy' output port 'sc_out' has no timing specification (no clock specified to create a sequential output port, not combinational connected to any inputs, not a clock output)
53 Warning 10: Model 'bram_phy' input port 'sc_in' has no timing specification (no clock specified to create a sequential input port, not combinational connected to any outputs, not a clock input)
54 Warning 11: Model 'bram_phy' input port 'PL_DATA_i' has no timing specification (no clock specified to create a sequential input port, not combinational connected to any outputs, not a clock input)
55 Warning 12: Model 'bram_phy' input port 'PL_ADDR_i' has no timing specification (no clock specified to create a sequential input port, not combinational connected to any outputs, not a clock input)
56 Warning 13: Model 'bram_phy' input port 'PL_WEN_i' has no timing specification (no clock specified to create a sequential input port, not combinational connected to any outputs, not a clock input)
57 Warning 14: Model 'bram_phy' input port 'PL_REN_i' has no timing specification (no clock specified to create a sequential input port, not combinational connected to any outputs, not a clock input)
58 Warning 15: Model 'bram_phy' input port 'PL_ENA_i' has no timing specification (no clock specified to create a sequential input port, not combinational connected to any outputs, not a clock input)
59 Warning 16: Model 'bram_phy' input port 'PL_INIT_i' has no timing specification (no clock specified to create a sequential input port, not combinational connected to any outputs, not a clock input)
60 Warning 17: Model 'bram_phy' input port 'RAM_ID_i' has no timing specification (no clock specified to create a sequential input port, not combinational connected to any outputs, not a clock input)
61 Warning 18: Model 'bram_phy' output port 'sc_out' has no timing specification (no clock specified to create a sequential output port, not combinational connected to any inputs, not a clock output)
62 Warning 19: Model 'bram_phy' output port 'PL_DATA_o' has no timing specification (no clock specified to create a sequential output port, not combinational connected to any inputs, not a clock output)
63 Warning 20: Model 'bram_phy' output port 'PL_ADDR_o' has no timing specification (no clock specified to create a sequential output port, not combinational connected to any inputs, not a clock output)
64 Warning 21: Model 'bram_phy' output port 'PL_WEN_o' has no timing specification (no clock specified to create a sequential output port, not combinational connected to any inputs, not a clock output)
65 Warning 22: Model 'bram_phy' output port 'PL_CLK_o' has no timing specification (no clock specified to create a sequential output port, not combinational connected to any inputs, not a clock output)

IPs

Available IPs

- axi2axilite_bridge_v1_0
- axi_cdma_v1_0
- axi_crossbar_v1_0
- axi_crossbar_v2_0
- axi_dma_v1_0
- axi_ram_v1_0
- axi_register_v1_0
- axil_crossbar_v1_0
- axil_crossbar_v2_0
- axil_eio_v1_0
- axil_ethernet_v1_0
- axil_gpio_v1_0
- axil_interconnect_v1_0
- axil_ocla_v1_0
- axil_quadspi_v1_0
- axil_uart16550_v1_0
- axis_adapter_v1_0
- axis_async_fifo_v1_0
- axis_broadcast_v1_0
- axis_fifo_v1_0
- axis_interconnect_v1_0
- axis_pipeline_register_v1_0
- axis_ram_switch_v1_0
- axis_switch_v1_0
- axis_uart_v1_0
- axis_width_converter_v1_0
- dsp_v1_0
- i2c_master_v1_0
- i2c_slave_v1_0
- jtag_to_axi_v1_0
- priority_encoder_v1_0
- reset_release_v1_0
- vexriscv_cpu_v1_0
- axi_async_fifo_v1_0

Console Messages Reports

Console

Write I/O mapping into xml file 'PinMapping.xml'

Write I/O mapping into xml file 'PinMapping.xml' took 0.00 seconds (max_rss 2052.0)

exit':

Finish execution with 0 errors

The entire OpenFPGA flow took 151.371 seconds

Thank you for using OpenFPGA!

Incr Slack updates 1 in 8.068e-06 sec

Full Max Req/Worst Slack updates 1 in 3.061e-06 sec

Incr Max Req/Worst Slack updates 0 in 0 sec

Incr Criticality updates 0 in 0 sec

Full Criticality updates 1 in 4.625e-06 sec

INFO: BIT: Design and2_gemini bitstream is generated

INFO:

#

GTKWave - /home/alain/RapidSilicon/Raptor/counter

Marker: -- | Cursor: 0 sec

From: 0sec To: 1 us

Signals

Time	clock0	counter[3:0]	counter_up[3:0]	reset
0	0	0	0	0
100 ns	0	0	0	0
200 ns	0	0	0	0
300 ns	0	0	0	0
400 ns	0	0	0	0
500 ns	0	0	0	0
600 ns	0	0	0	0
700 ns	0	0	0	0
800 ns	0	0	0	0
900 ns	0	0	0	0
1000 ns	0	0	0	0

Waves

100 ns 200 ns 300 ns 400 ns 500 ns 600 ns 700 ns 800 ns 900 ns

u0 1 2 3 4 5 6 7 8 9 A B C D E F 0 1 2 3 4 5 6 7 8 9 A B C D E F 0 1 2 3 4 5 6 7 8 9 A B C D E F 0 1

u0 1 2 3 4 5 6 7 8 9 A B C D E F 0 1 2 3 4 5 6 7 8 9 A B C D E F 0 1 2 3 4 5 6 7 8 9 A B C D E F 0 1

Dir Type Signals

Dir	Type	Signals
I	std_logic	clock0
O	std_logic_vector	counter[3:0]
O	std_logic_vector	counter_up[3:0]
I	std_logic	reset

Append Insert Replace

VPR - Versatile Place and Route

Open-source Place & Route Tool, developed by University of Toronto, led by Vaughn Betz

Used by several non-FPGA companies

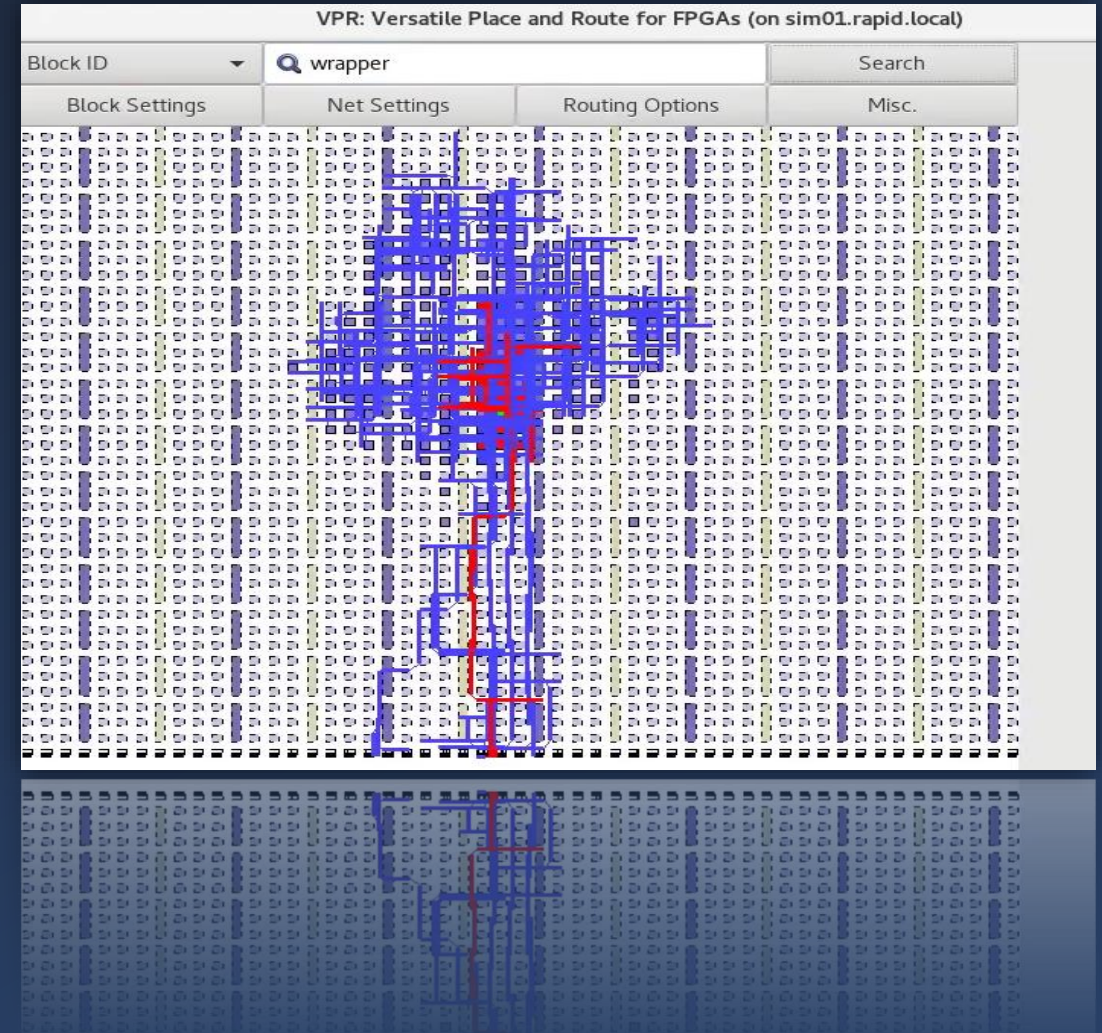
Supports parallel threads

Annealing schedule driven

User-configurable options for packing and routing

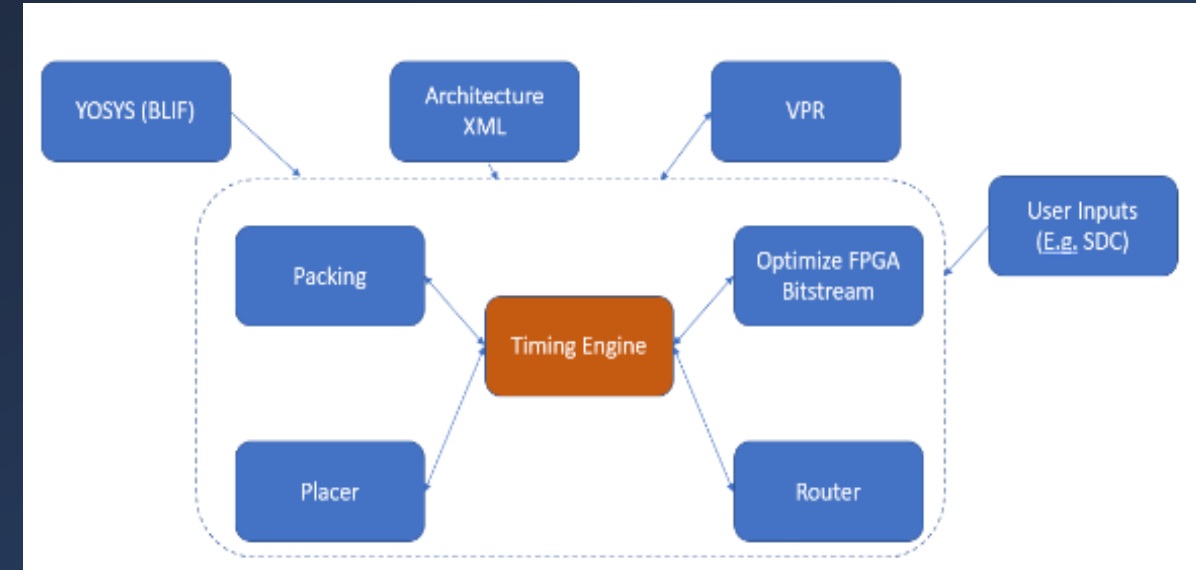
Timing, Area and Balanced prioritization with re-route capability

Fanout, Effort level and Initial seeding control



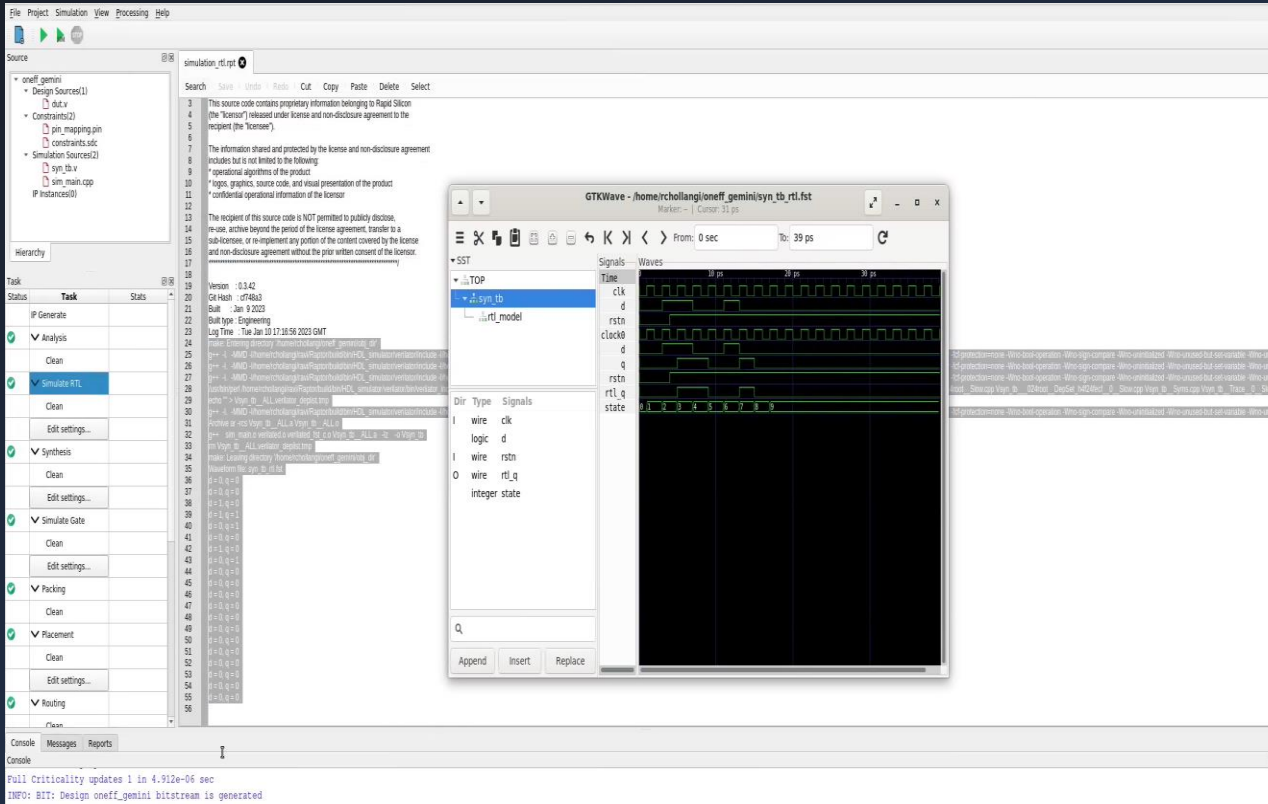
OpenSTA - Industry Standard Timing

- Supports standard file formats for timing analysis
- Used by many significant companies
- Rich TCL interface to read design, specify timing constraints and create timing reports
- Supports external delay calculator API
- Integrated RC effective capacitance algorithm for delay calculation
- Allows query based incremental updates of delays, arrival and required times



OpenSTA, best-in-class timing engine, used for timing analysis & optimization

Comprehensive simulation support



- Fully integrated simulator engine for Verilog and VHDL designs
- Verilator (fastest Verilog/SystemVerilog 2 states simulator)
- GHDL for VHDL simulation
- Icarus for 4 states and Timed simulation
- In-built GTKWave waveform viewer
- Supports RTL and Gate level simulations
- Multi-threaded simulations are supported
- 100% Open source



EPFL: Best in Class LUT6 Implementation

École polytechnique fédérale de Lausanne (EPFL) Combinatorial Benchmark Suite Competition

- 37 best solutions over 46 benchmarks
- Up to 3x reduction in size
- Optimal results for at least 2 designs

"...23 natively combinational circuits designed to challenge modern logic optimization tools."



- 30 unique wins, 2 category ties
- 2x more than next closest entrant
 - Better than all other entrants in EDA industry
 - Won in area hands-down! (**23 Best area over 23 benchmarks**)

Full results here: [benchmarks/best_results at master · lsils/benchmarks \(github.com\)](#)

Best LUT-6 Implementations - 2022

The best LUT-6 implementations keep track of the best results of LUT-6 mapped benchmarks, both for size (# of LUTs) and depth (# of levels).

Best results for LUT-6 count

Arithmetic Benchmarks

Benchmark name	Inputs	Outputs	LUT-6 count	Levels	Authors	Method
Adder	256	129	129	127	T. Besson	ABC-DE: ABC Design Explorer
Barrel shifter	135	128	512	4	R. K. Brayton & A. Mishchenko	ABC Extreme Mapper
Divisor	128	128	3101	1110	T. Besson	ABC-DE: ABC Design Explorer
Hypotenuse	256	128	39516	4560	A. Grosnit, C. Feng, X. Li, et al.	NAILS
Log2	32	32	6326	151	T. Besson	ABC-DE: ABC Design Explorer
Max	512	130	511	183	T. Besson	ABC-DE: ABC Design Explorer
Multiplier	128	128	4424	168	T. Besson	ABC-DE: ABC Design Explorer
Sine	24	25	1114	62	T. Besson	ABC-DE: ABC Design Explorer
Square-root	128	64	2994	1069	T. Besson	ABC-DE: ABC Design Explorer
Square	64	128	3071	108	T. Besson	ABC-DE: ABC Design Explorer

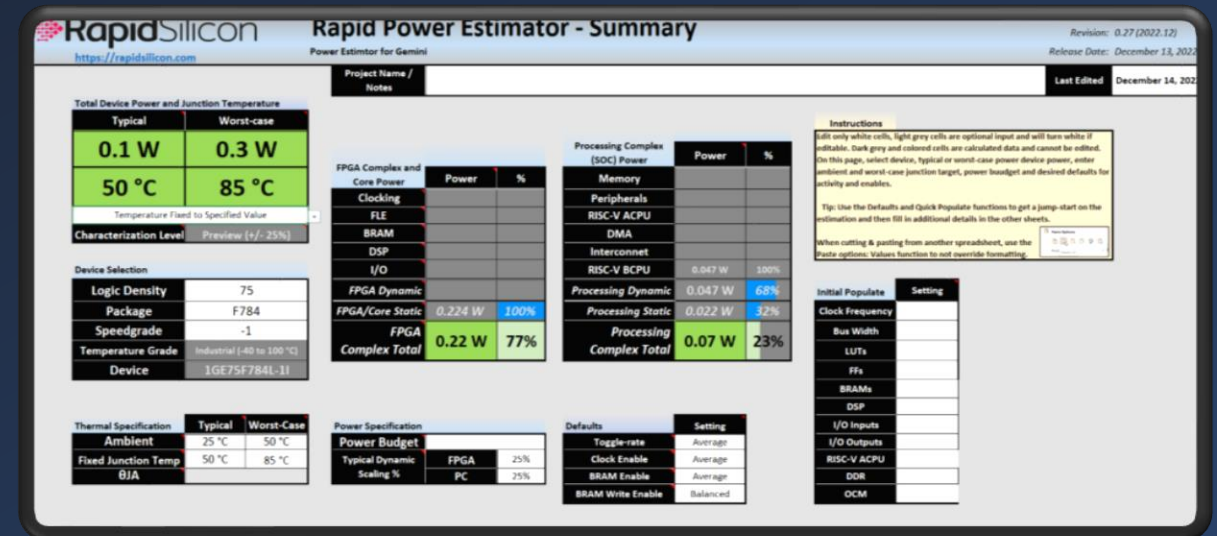
Random-Control Benchmarks

Benchmark name	Inputs	Outputs	LUT-6 count	Levels	Authors	Method
Round-robin arbiter	256	129	276	30	T. Besson	ABC-DE: ABC Design Explorer
Alu control unit	7	26	26	2	A. Grosnit, C. Feng, X. Li, et al.	NAILS
Coding-cavlc	10	11	54	6	T. Besson	ABC-DE: ABC Design Explorer
Decoder	8	256	264	2	L. Machado and J. Cortadella	Support-Reducing Decomp
I2c controller	147	142	182	7	T. Besson	ABC-DE: ABC Design Explorer
Int to float converter	11	7	20	3	T. Besson	ABC-DE: ABC Design Explorer
Memory controller	1204	1231	1735	14	T. Besson	ABC-DE: ABC Design Explorer
Priority encoder	128	8	94	20	T. Besson	ABC-DE: ABC Design Explorer
Lookahead XY router	60	30	19	5	T. Besson	ABC-DE: ABC Design Explorer



Rapid Power Estimator and Board Tool

- Early estimation based on Excel
 - Evaluating open-source spreadsheet tools
- Generally, first look at device architecture
 - Used prior to installation/use of Raptor
- Provide board-level power and pinout guidance / support
- Back-end power estimation under investigation



RPE is the view into RapidSilicon's Power Efficiency

Rapid Silicon is Alive and Thriving

Rapidly Progressing Test Chip and EDA Tools

MPW1 Test Chip
Demo



1:30

[Video](#)

Open-Source EDA
Tool Strategy



1:12

[Video](#)

Raptor EDA Demo



1:25

[Video](#)

CEO Message



2:23

[Video](#)

Summary

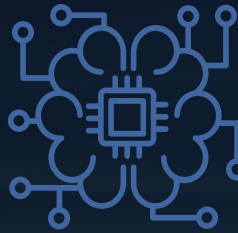
Accepting the Challenge to Build Next-Gen FPGAs and SoCs for Cost-Sensitive Markets



Experienced Team

150+ Years of Executive Team
PLD Experience

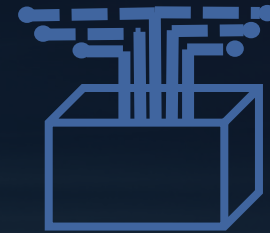
Incredible PLD Company
Diversity



The Right Architecture

Leverage Open-Source and 3rd-
Party IP for fast TTM

Utilize FlexNoC to quickly and
easily add IP



Embracing Open-Source

First to Integrate OS Tool Chain
for PLD Design

Rapid Tool Evolution and
Improvement

Add FPGAs to an existing portfolio of stand-alone FPGAs (Production Silicon) or Embedded FPGAs.

Off-the-shelf Core FPGA IP (eFPGA, Silicon proven IP)

Tailored FPGA Core IP (DSP, BRAM, LUT, Routing, IOs, Secure configuration...)

Design Services (Full SOC integration)

Complete end-to-end Software stack

Customizable Software stack mix-and-match with existing stacks



Interested in Learning More?

Join our Early Access Champions Program*

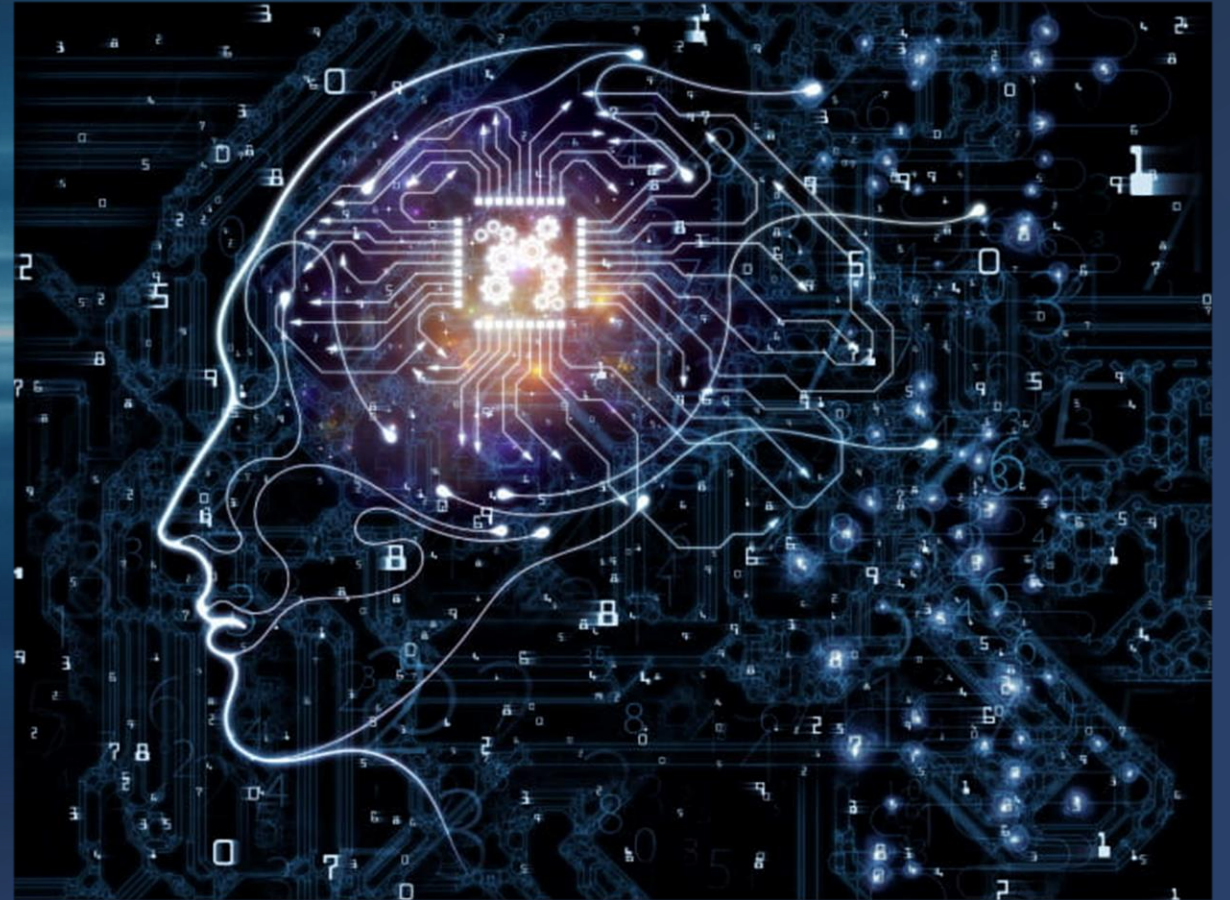
Updates on:

Product Development
Tool Flow
Solutions

Early Access to Silicon & Dev Kits

Direct Technical Support

* Requires NDA and non-binding MOU





Thank you