5G/O-RAN Evolution and its Deployment with FPGA Devices

Overview – The Move Towards Open Radio Access Network (O-RAN) Architectures

The evolution towards 5G networks heralds a compelling shift towards open radio access network (ORAN) architectures, breaking away from the closed systems of traditional RAN setups that have long dominated cellular and mobile networks. This paradigm shift allows for the separation of numerous traditional RAN functions between hardware and software components, fostering an environment where operators have the freedom to select and integrate components from a diverse range of vendors. By dismantling the rigid structures of traditional RAN setups, 5G ORAN introduces a dynamic, adaptable, and cost-efficient approach to network deployment. However, alongside the myriad benefits of this newfound flexibility, challenges arise in synchronization, security, and power management. The departure from single-vendor solutions to the disaggregation of the RAN architecture heightens the potential attack surface, posing security risks to critical infrastructure and necessitating precise timing and synchronization sources.

The Role of FPGAs in O-RAN Architecture

To address these challenges and safeguard against potential risks, network equipment vendors and service providers must carefully assess crucial network components required to maintain the integrity and security of their networks and data. Among these critical components are Field Programmable Gate Arrays (FPGAs), renowned for their adaptability and multifaceted functionality within Open Radio Access Network (ORAN) environments. FPGAs play diverse roles ranging from serving as a hardware root-of-trust to accelerating network functions and facilitating secure communications.

In the realm of 5G cellular network infrastructure, hardware design engineers are compelled to select components that not only meet essential functionalities but also offer the flexibility to achieve desired objectives. FPGAs emerge as indispensable assets in these complex endeavors, owing to their inherent capability for dynamic design and reconfiguration. This innate flexibility renders FPGAs exceptionally well-suited for addressing the intricate and demanding requirements inherent in advanced technologies.

For decades, FPGAs have been integral to telecom networks, adeptly facilitating tasks ranging from enhancing network functions to streamlining data transmission processes. Amidst the industry's transition towards Open Radio Access Network (ORAN) architectures, FPGAs, particularly those boasting low power consumption, reaffirm their pivotal role. They excel in critical functions such as establishing hardware root-of-trust, ensuring synchronization across diverse components, and executing real-time network packet encryption and decryption. As telecommunications continue to evolve, FPGAs persist as invaluable allies, adeptly navigating the complexities of modern network infrastructures with unparalleled finesse and reliability.

NeuLink FPGAs for O-RAN Deployments

With the transition to 5G, characterized by the integration of new frequencies and heightened expectations regarding the diversity and volume of connected devices, significant shifts have emerged. Notably, there's a considerable emphasis on reducing latency for data traversing the network. Concurrently, within traditional telecommunications environments, a noticeable trend toward software-defined architectures has emerged, accompanied by the disaggregation of critical network hardware components. For instance, the conventional baseband unit, responsible for powering cell phone towers in

previous generations, has undergone fragmentation into distinct units: the Distributed Unit (DU), Control Unit (CU), and Radio Unit (RU). This restructured framework offers enhanced capabilities and flexibility, aligning with the escalating demands of network data traffic and diverse applications.

In the O-RAN architecture, comprising Distributed Unit, Control Unit, and Radio Unit, seamless communication and collaborative functionality are imperative. Achieving this necessitates precise timing and synchronization, alongside robust hardware security measures. The IEEE 1588 Precision Timing Protocol serves as the cornerstone for synchronizing the distributed clocks within this architecture's distributed system. To fulfill these requirements, the NeuLink ***Orion*** offers indispensable capabilities for implement timing synchronization protocol along with various functionalities across the RU, DU, and CU units.

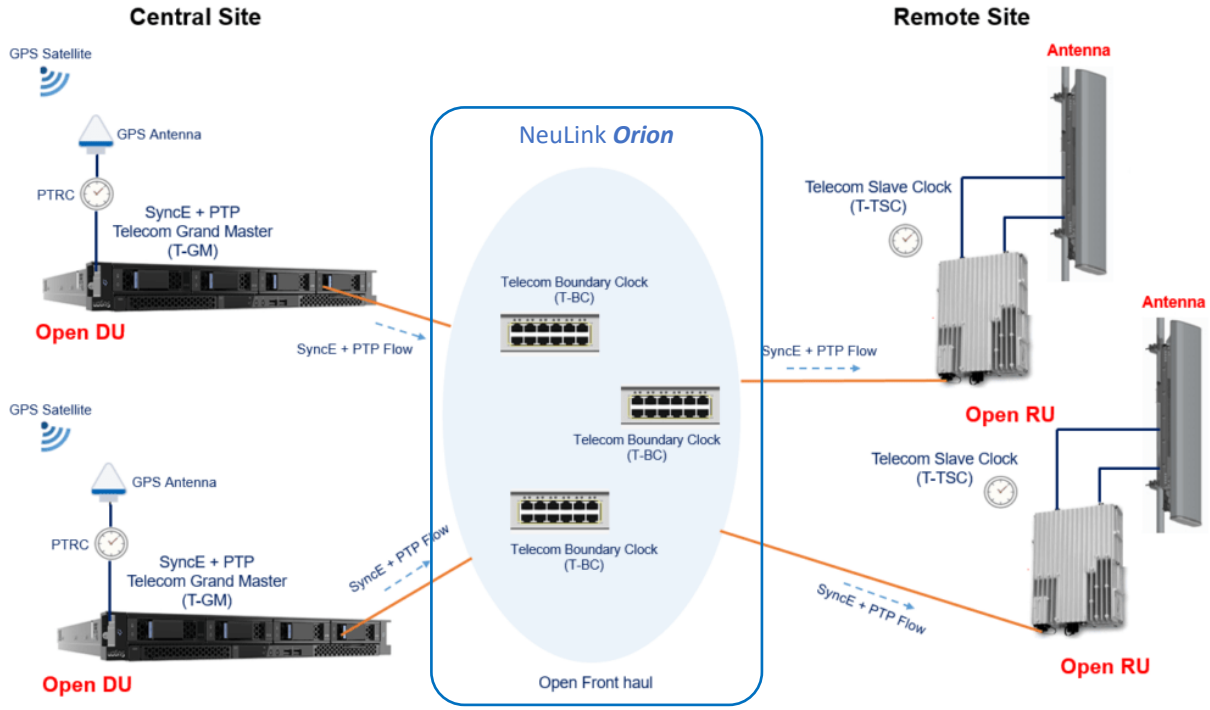

Figure 1: IEEE 1588 timing synchronization using NeuLink *Orion* FPGA

Leveraging the ***Orion*** FPGAs, the IEEE 1588 protocol and ITU profiles can be implemented in Verilog codes, incorporating relevant soft IP cores. By harnessing the built-in cryptographic capability in these FPGA devices, they're utilized to encrypt and decrypt data transmitted to and from firmware. This ensures the integrity of the firmware by guaranteeing that it remains unaltered and that any updates are executed securely.

Addressing security concerns extends beyond ensuring the secure transmission and reception of data between firmware. It encompasses establishing secure communication channels with all hardware elements linked to the host CPU. The ***Gemini*** and ***Virgo*** device families feature hardened RISC-V CPU cores, programmable to execute a myriad of cryptographic algorithms and secure messaging protocols, fortifying the overall security posture of the system.

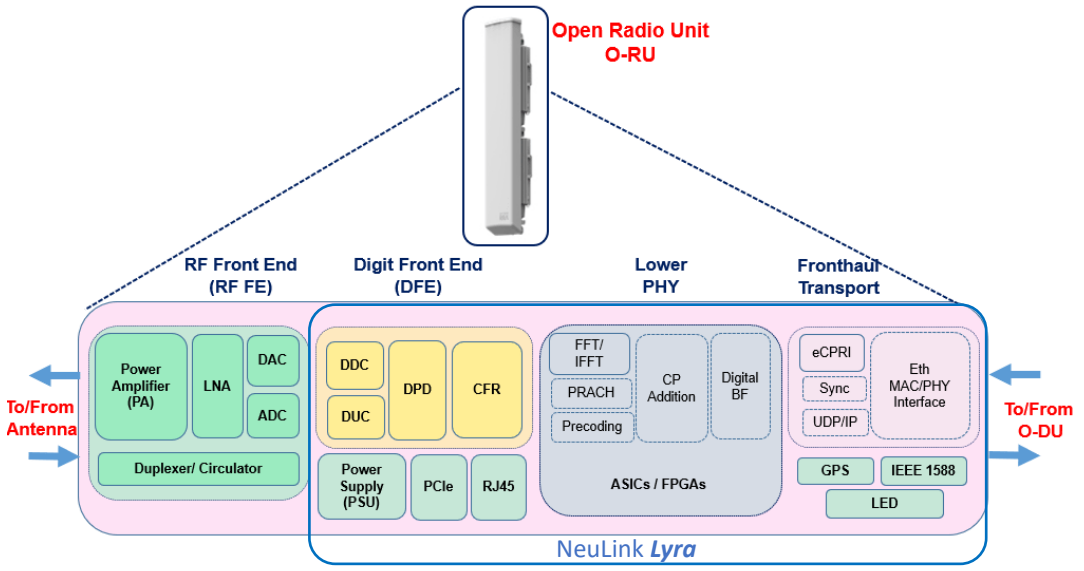

Figure 2: O-RU Implementation with NeuLink *Lyra* FPGA

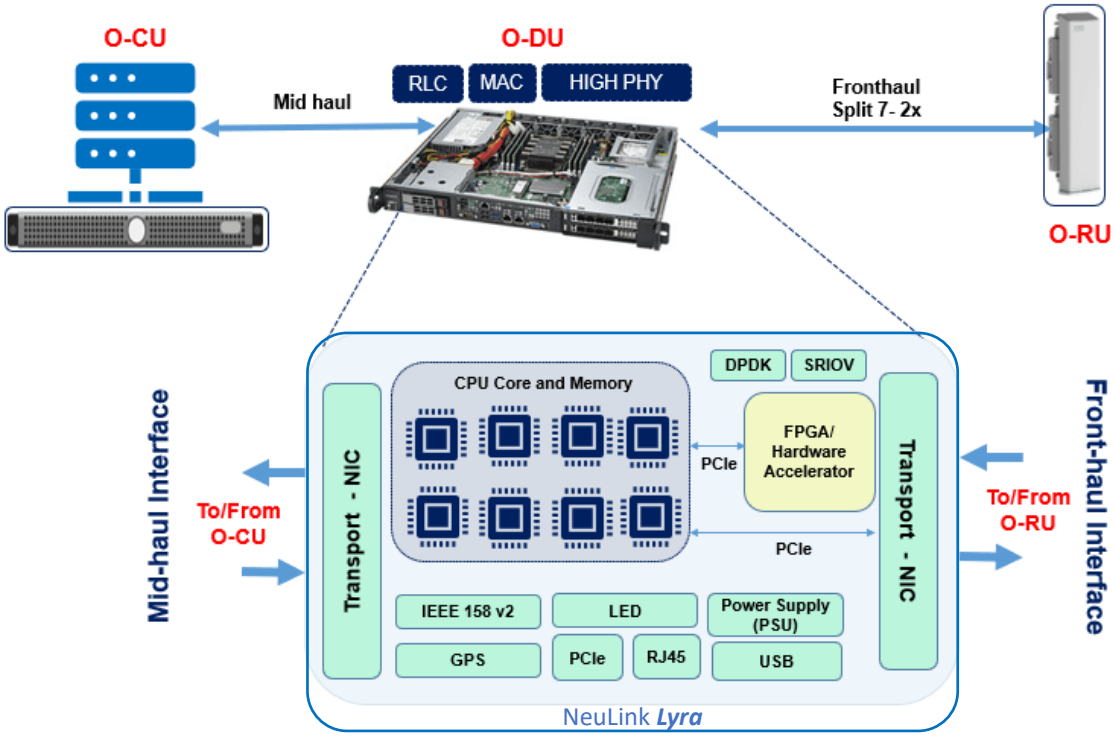

Figure 3: O-DU Implementation with NeuLink *Lyra* FPGA

NeuLink's ***Lyra*** devices has large FPGA fabric along with harden multi-core ARM and RISC-V CPUs as well as multiple transceivers to handle high bandwidth of data transfer makes them ideal candidates to implement complete Radio Unit (RU) and Distributed Unit (DU) implementation as shown in above Figure. For Radio Unit (RU) RF frontend can be implemented with partner such as Arctic Semiconductor's RF frontend solution with digital processing on ***Lyra*** device. Lower PHY functionality in O-RU and FPGA Accelerator functionality in O-DU can also be implemented using NeuLink's ***Gemini*** or ***Orion*** devices depending on logic complexity.

NeuLink – Your 5G and O-RAN Deployment Solution Hub

The FPGA product portfolio from NeuLink encompasses a range of families including Virgo, Gemini, Orion, and Lyra, which are integral to diverse applications within O-RAN architecture deployments. These FPGA devices play a pivotal role in implementing secure messaging protocols such as Management Component Transport Protocol (MCTP) and Security Protocol & Data Model (SPDM), facilitating Advanced Crypto services like Authentication and Encryption, enabling Small Cell Digital Front End implementation for Radio Unit, ensuring precise 1588 Synchronization and full functionality of Distributed Unit. Across these functions, the FPGAs handle myriad of critical tasks including Power Management, Bus Extension, Level shifting, and Control Logic Implementation.

The Raptor Design suite accompanies these devices, empowering designers to program the FPGAs. NeuLink provides a comprehensive portfolio of soft IPs tailored for 5G O-RAN applications, encompassing crucial functionalities such as CRC Encoder/Decoder, Beamformer, Interleaver/De-Interleaver, Channel Coding, and more. This rich ecosystem equips designers with all the necessary tools to seamlessly implement applications in both 5G and O-RAN deployments.