Unlocking Embedded Vision Capabilities with Neulink FPGAs

Overview – Emergence of FPGAs in Embedded Vision

The integration of embedded vision, artificial intelligence (AI), and deep learning into various systems has ushered in a transformative wave across multiple sectors. This integration primarily occurs at the edge to circumvent the latency, cost, and complexity associated with transmitting data to centralized data centers for processing.

The landscape of image and video processing applications is evolving rapidly, prompting designers to reassess their choices of processing solutions. Whether it's Applications Processors (AP), Application-Specific Integrated Circuits (ASIC), or Application-Specific Standard Products (ASSP), the need for efficient and adaptable solutions has never been greater. Despite the considerable investments tied to existing software and the complexities of transitioning to new platforms, designers are exploring co-processing solutions. These solutions aim to strengthen computational capabilities for emerging, data-intensive applications while upholding cost and power efficiency benchmarks. This paradigm shift is fundamentally reshaping how videos and images are analyzed across various sectors, including healthcare diagnostics, public safety, retail, and online media.

In navigating this evolving landscape, it becomes imperative to address several key challenges. These include the need for adaptability, power efficiency, compactness, and affordability. A solution that can deliver robust computational capabilities, akin to a high-performance co-processor, becomes essential. Furthermore, seamless integration of comprehensive connectivity options and support for a wide range of input/output standards and protocols are crucial for success in this dynamic environment.

FPGAs have emerged as compelling solutions to surmount the challenges encountered in embedded vision, spanning areas such as co-processing, bridging, and machine learning domains. Their adoption extends across a spectrum of industries, including industrial, consumer electronics, and automotive sectors. Neulink has responded to the demands of this market by introducing its Gemini and Virgo series of FPGA devices, tailored to meet the diverse requirements of contemporary applications.

FPGA Driven Co-processing for Embedded Vision

Addressing the need for an unparalleled co-processor boasting extensive connectivity while optimized for low-power consumption and cost efficiency, Neulink had developed the Gemini family of FPGA devices. These FPGAs are engineered to meet the escalating demand for various applications including efficient co-processing capabilities. Leveraging its parallel processing architecture, the Gemini facilitates optimized distribution of computational tasks offloading application core and ensuring unparalleled performance.

The processing workflow begins with the application core capturing image data from sensor, which it delegates to the FPGA for processing. Within the FPGA, tasks including filtering, color space conversion, and binary morphology are managed.

This approach significantly reduces the CPU's computational load, thereby enhancing overall system performance. By leveraging the complementary strengths of both CPU and FPGA, Gemini effectively boosts processing capabilities while maintaining efficiency.

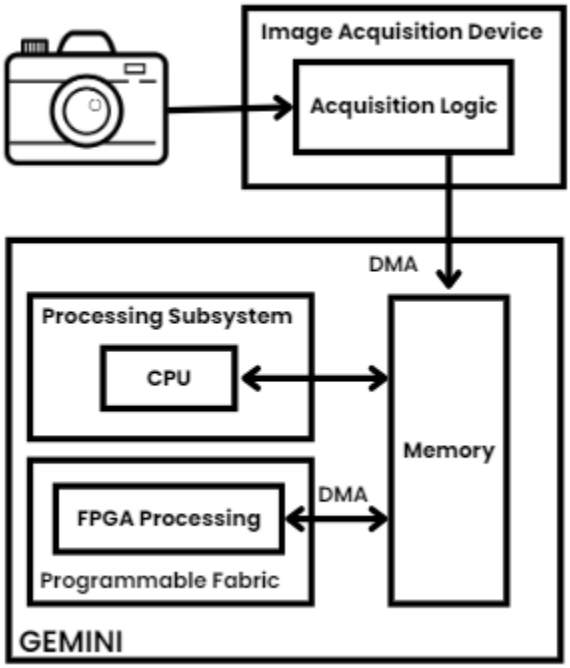

Figure 1: FPGA based Co-Processing

Gemini represents an ideal platform for the co-processing needs, boasting densities of up to 100K logic elements and incorporating a RISC-V based processor core. The integrated, hardened processor core with programmable fabric empowers users to seamlessly deploy their applications within a unified package, augmented by an effective routable architecture and multiple supporting I/O standard options. Complementing this architecture are enhanced embedded DSP block ensuring exceptional performance for compute-intensive co-processing tasks.

In terms of connectivity, Gemini supports a diverse array of peripherals, including PCI Express, triple-speed ethernet, and an extensive range of interfaces such as DDR3, DDR4, LPDDR4, RGMII, XGMII, LVTTL, LVDS, BLVDS, LVPECL, HSTL, and MIPI DPHY.

Moreover, Gemini boasts up to 6.3 megabits of embedded RAM, coupled with 2133 MT/s LPDDR4, alongside a comprehensive suite of additional I/O interfaces. Leveraging these features, Gemini excels in executing compute-intensive operations with efficiency, leveraging its FPGA logic fabric to alleviate processor workload. This capability facilitates the seamless offloading of tasks such as image processing and analytics, resulting in superior performance with lowered power consumption, thus positioning Gemini as a compelling solution for co-processing needs.

Fueling Intelligence in Edge Camera Solutions

In modern society, devices rely heavily on internet connectivity to exchange data with cloud servers. Some devices, like video cameras, generate large amounts of data during operation, while others, like

temperature sensors, produce smaller amounts individually but collectively pose challenges for managing data in the cloud. As a result, there's a growing need for devices that can process data locally, reducing reliance on cloud servers.

One such example is the smart cameras enabling the automation of repetitive tasks and thereby liberating human resources for more cognitively demanding endeavors. A prime example of smart camera utilization is in license plate recognition systems, which find application across diverse sectors, including security protocols aimed at thwarting unauthorized access and streamlined processes such as automated entry for subscribed vehicles at car wash facilities. It requires performing video analytics at the edge rather than sending raw video back to the cloud for processing.

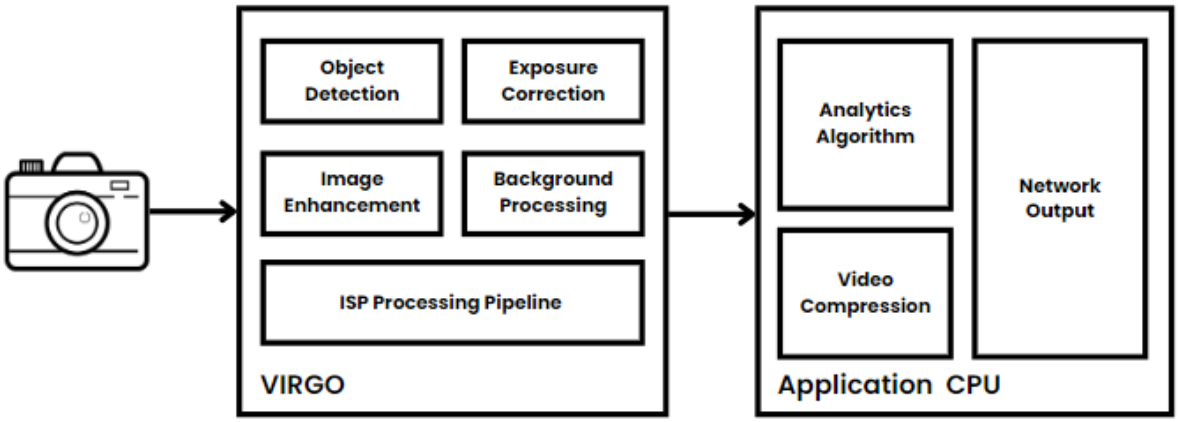

Figure 2: Virgo performing image processing tasks offloading CPU from compute intensive tasks

The Virgo FPGA presents users the choice for offloading their application processor workload to support local data processing. The FPGA would be responsible for a wide range of image processing tasks including object detection, exposure correction, object enhancement and more. The smart camera sensor captures the image. It is then enhanced for visibility using image processing leveraging the programmable fabric of FPGA. The processed output is then fed into the analytics algorithm running on the Application Processor Core. By transferring the most demanding computational tasks of the analytics algorithm to the parallel-processing FPGA architecture, the intelligent camera system boosts its performance without compromising on power efficiency and cost.

Empowering Visual Solutions in Industry

Machine vision encompasses a broad spectrum of applications across industrial domains wherein a fusion of hardware and software facilitates operational guidance to industrial devices, leveraging image capture and processing. Central to machine vision systems are computer hardware that analyze and interpret, and quantify diverse image characteristics facilitating informed decision-making process. FPGAs are pivotal component of such hardware used for various important roles including image signal processor, sensor bridge, co-processor and more.

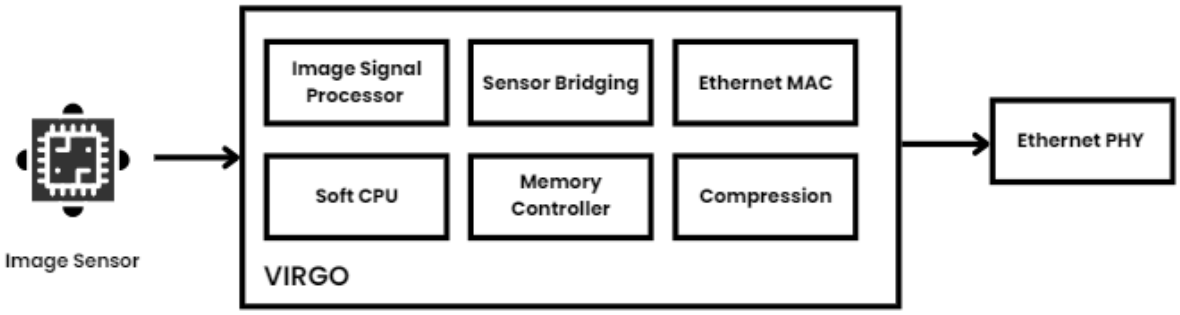

Figure 3: Virgo performing image signal processing or compression functions in industrial setting

The Virgo family of FPGAs enables the efficient handling of such tasks. Positioned between the image sensor and an Ethernet PHY, it receives the image data stream from the sensor. The FPGA then executes image processing tasks, such as compression using H.264 encoding. Leveraging its on-chip Block RAM and DSP blocks, the FPGA achieves optimal performance, particularly in Wide Dynamic Range (WDR) and image signal processing (ISP). Ultimately, the FPGA transmits the refined image data across the Ethernet network, as final step in the data processing pipeline.

Driving Machine Learning to Edge

In today's technological landscape, engineers designing products for modern embedded vision applications are increasingly integrating neural networks, artificial intelligence, and machine learning (AI/ML). The demand for hardware capable of running sophisticated algorithms, particularly those skilled in intricate pattern recognition and analysis, is rising. These hardware systems play a crucial role in interpreting data and enabling informed decision-making processes.

Machine learning, particularly through neural networks like deep learning, stands as a cornerstone for training computers to recognize various elements, such as images. This process demands substantial amounts of data and computational power, typically managed in large data centers equipped with high-performance GPUs and FPGAs.

Once trained, these models find application in everyday devices for tasks like image or speech recognition. However, at the edge of the network, where swift decision-making is paramount, inferencing techniques take center stage. These techniques leverage the learned insights to make quick judgments on new data.

In response, there's a growing demand for computationally-efficient solutions tailored for inferencing tasks at the network edge. Designers are actively pursuing ways to meet these demands while adhering to stringent criteria regarding power usage, size, and cost. This pursuit underscores the importance of striking a balance between computational efficiency and practical constraints in deploying machine learning at the network's edge.

In addressing these demands, the Virgo FPGA emerges as a fitting solution for the evolving AI market. Equipped with DSP blocks capable of executing fixed-point math functions akin to GPUs employing floating-point math but with reduced power consumption, the Virgo FPGA offers a compelling proposition. Its inherent parallel processing architecture confers a competitive advantage in terms of power efficiency, physical footprint, and cost-effectiveness.

In one practical deployment, the Virgo FPGA serves as an inferencing accelerator, executing pre-trained convolutional neural network (CNN) functions on data sourced from sensors. Leveraging this setup, the CNN engine running on FPGA identifies objects, face or gesture and relays the result to the system CPU, thereby achieving prompt and power-efficient object, face or gesture detection.

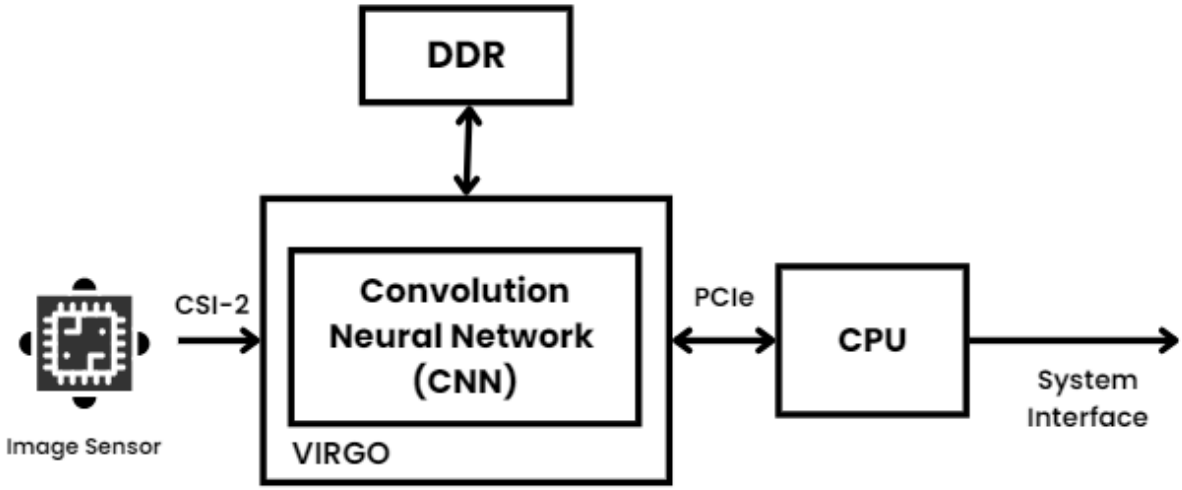

Figure 4: Virgo performing as a Convolution Neural Network Accelerator

Summary

Designers in the field are consistently exploring avenues to optimize costs, minimize power consumption, and shrink physical footprints while enhancing the intelligence of their edge applications. Simultaneously, they grapple with the ongoing challenge of adapting to the rapidly evolving performance standards and interface requirements imposed by next-generation sensors and displays utilized in edge environments. Rapid Silicon's Gemini and Virgo FPGA families addresses these multifaceted needs, offering designers a comprehensive solution. With a robust processing capacity of up to 100K LUTs, hardened application processing core and bolstered by transceiver support, these device families equip designers with indispensable co-processing capabilities and connectivity resources. Moreover, by delivering these features at a lower cost and power consumption than competing alternatives, these FPGAs provide developers with a decisive advantage in the competitive landscape.