Product Brief

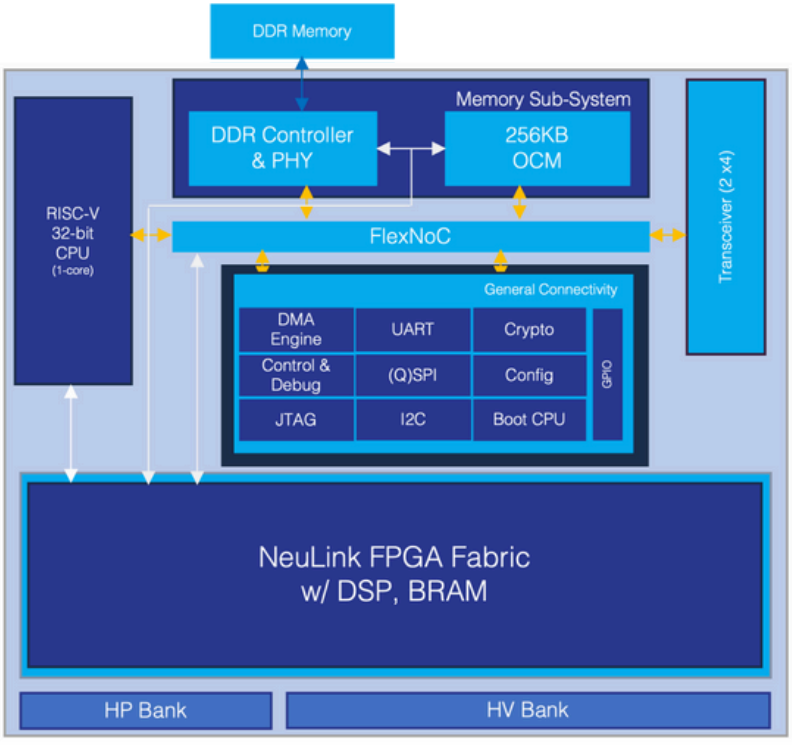
NEULINK SEMICONDUCTORS

Gemini+

Optimal Performance, Power and Connectivity

The New Standard for Emerging Embedded Applications

While power, cost, and performance have been the key characteristics in the embedded FPGA space for decades, integration shines bright in the new Gemini+ chip from NeuLink Semiconductors Built on TSMC's 16nm FF process, Gemini+ delivers the best performance-per-watt-per-dollar out of the gate. The modern design of Gemini+ features proven FPGA architectures including 6-input fracturable LUTs, DSP blocks, true dual-port block RAM, over 400 IO, supporting up to 2.5 Gbps LVDS IO and legacy 3.3V IO standards. This family also features hardened RISC-V, DRAM controller operating up to 2133 Mbps as well as hard Ethernet and USB controllers. This vast amount of IP integration is enabled via the high performance, low latency interconnect. The Gemini+ programmable logic devices bring a fresh, modern perspective to meet the embedded markets current and future needs.



Over 400 I/Os

GEMINI+ BLOCK DIAGRAM

THE INDUSTRY GAP

FPGA usage is too diversified for a single organization to service.

Larger FPGA vendors focus on data center, communications infrastructure and higher ASP products.

Existing mid-range FPGAs do not meet current and future standards and processing needs and are approaching end of life.

NEULINK FILLS THE GAP

IP and products designed from the ground up for optimal performance, power and cost.

Industry veterans and executives with combined 150+ years of experience and over 15 FPGAs and SoCs delivered successfully.

Leverage and promote the robust open source community to streamline development and support.

Bring innovation and customization to satisfy the diverse needs of the market.

A Modern FPGA Using Hardened Interconnect

Traditional PLDs have failed to meet the increasing need for IP integration in size and power-constrained embedded systems. Gemini+ is designed to eliminate the performance bottlenecks and interface bridging challenges with the use of hardened interconnect IP. Not only does this state-of-the-art IP natively support AXI and OCP, it also eliminates routing congestion, lowers latency, reduces both die area and power consumption, improves performance, and provides quality of service (QoS). Gemini+ with hardened interconnect is one of the many ways NeuLink Semiconductors has reimagined a modern, nimble FPGA that can quickly scale and adapt to the diverse and growing needs of tomorrow's embedded applications.

FABRIC ARCHITECTURE

- Up to 150K LE device densities
- Up to 325 18x20 Multiplier Blocks with built in Carry and Accumulate
- Up to 11.7 Mb of on-chip block RAM
- 6-input fracturable LUT with carry chain and registered outputs
- Multiply-accumulate DSP blocks
- True dual-port block RAM supporting FIFO modes
- 4-output PLLs capable of up to 3.2 GHz VCO clocking

INTEGRATED IP

- Hard 32-Bit RISC-V real-time application processor with custom instruction support operating up to 1066 MHz with 32 KB I/D cache and 64 KB program memory
- DRAM controller capable up to 2133 Mbps performance support DDR4, DDR3, LPDDR3, and LPDDR4
- Hardened interconnect allows for low latency, rapid integration of any AXI-capable IP
- Hard Triple Speed Ethernet controller for easy, high performance connectivity
- Up to 512 KB of dedicated on-chip RAM for extra storage

I/O CAPABILITIES

- Highest I/O density with up to 520 I/O
- High voltage I/O supporting up to 3.3V standards
- High performance I/O capable of up to 2.5 GHz LVDS performance

GET IN TOUCH WITH US

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