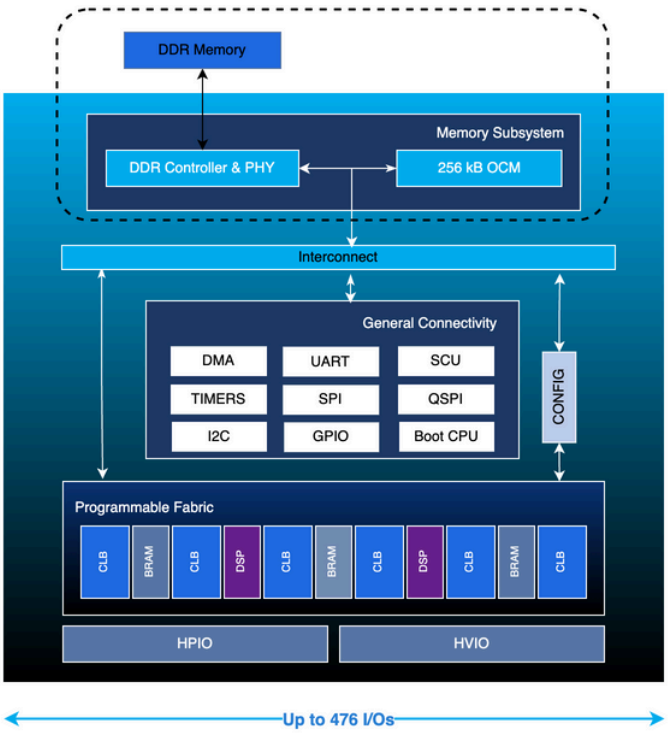
Product Brief

Virgo

Experience Maximized Connectivity, Optimized Power and Performance

Discover power and performance efficiency with dense I/Os in Virgo FPGAs. Built on TSMC's 16nm FinFET Compact (16FFC) process technology, Virgo delivers the best power efficiency and performance-per-dollar out of the gate. The proven Virgo FPGA architecture features 6-input fracturable LUTs, DSP blocks, True Dual port RAM, over 476 I/O, supporting up to 1.5 Gbps LVDS and legacy 3.3V I/O standards. The family also features a hardened DRAM controller operating up to 2133 MT/s as well as a hard Ethernet controller in larger devices on the roadmap.

Virgo devices serve as a go-to choice for connectivity and processing applications across diverse sectors including edge, industrial, and consumer electronics.



Virgo Functional Block Diagram

The FPGA Market Conundrum

The diverse applications of FPGAs pose a challenge for any single organization to adequately serve. While larger FPGA vendors concentrate on data center and communications infrastructure as well as higher ASP products, the midrange FPGA market remains underserved with limited options available for modern standards and processing needs.

NeuLink Bridges the Gap

Addressing industry needs, our IP and products are engineered from the ground up to deliver power efficiency, cost effectiveness and optimized performance. With a team of industry veterans and executives boasting over 150 years of combined experience and a track record of successfully delivering more than 15 FPGAs and SoCs, you can depend on our expertise.

Our FPGAs cater to the diverse needs of the market, conforming to standards and exceeding expectations.

NEULINK SEMICONDUCTORS

Power Your Embedded Applications with Virgo

Meet the demands of modern embedded applications with the I/O density, tight power footprint, and performance of Virgo FPGAs. Designed to excel in smaller power envelopes and shrinking form factors, Virgo FPGAs provide the perfect balance of power efficiency, connectivity options, and performance required for your needs.

Fabric Architecture

- From 28k to 100k Logic cell densities
- Up to 9.4 Mb of on-chip block RAM on the largest device
- Up to 208 18x20 Multiplier blocks on the largest device
- 6-Input fracturable LUT with carry chain and registered outputs
- True Dual Port RAM blocks
- Multiply Accumulate DSP blocks
- 4-output PLLs capable of up to 3.0GHz VCO clocking

Security

- Secure Firmware bootup
- Device LCM using OTP bits
- Authentication using ECDSA 256 and RSA 2048
- Encryption using AES-128 & AES-256 CCM mode
- Secure Hash SHA256

I/O Capabilities

- Highest I/O Density with up to 476 I/Os
- High Performance I/O capable of 1.5 GHz LVDS performance
- High Voltage I/O supporting up to 3.3V standards

EDA Tool (Raptor Design Suite)

- 50+ qualified soft IPs
- 20% area reduction with Yosys AI-driven enhancement
- User Configurable options for partitioning, packing, routing, timing, and area optimization
- Intuitive GUI
- Integrated HDL simulator engine
- GTKWave built-in waveform viewer
- VSCode IDE, RapidGPT integration

Interested in learning more about us?

Reach out to us at
www.neulinksemi.com/contact-us/