The Next-Generation of Intelligent, Embedded-Edge Programmable Devices

2021

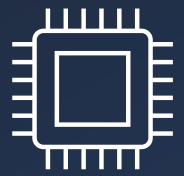
Rapid Silicon was founded in 2021

Headquarters
Silicon Valley

Other locations: Penang, Lahore

FPGA

Low to mid-range FPGA



130

Our team consists of 130 employees

150+

Our exec team has 150+ years of industry experience

Financing Funded by top semiconductor VCs

Applications

Variety of domain-specific FPGAs suited to diverse target applications

Open-Source

Industry's first open-source EDA tool

Production:
TSMC
#1 Fab in the world

Quality & Operations:
World Class manufacturing

Experienced Team Built by Industry Veterans

15+ FPGAs Delivered

SiFive · Brite Technology · intel · Open-Silicon · Silicon Federation

PEERNOVA · Infochips · ikanos · Q · Sibridge · VxTel

onsemi · MAGMA · applied micro · Hifn · ALTERA

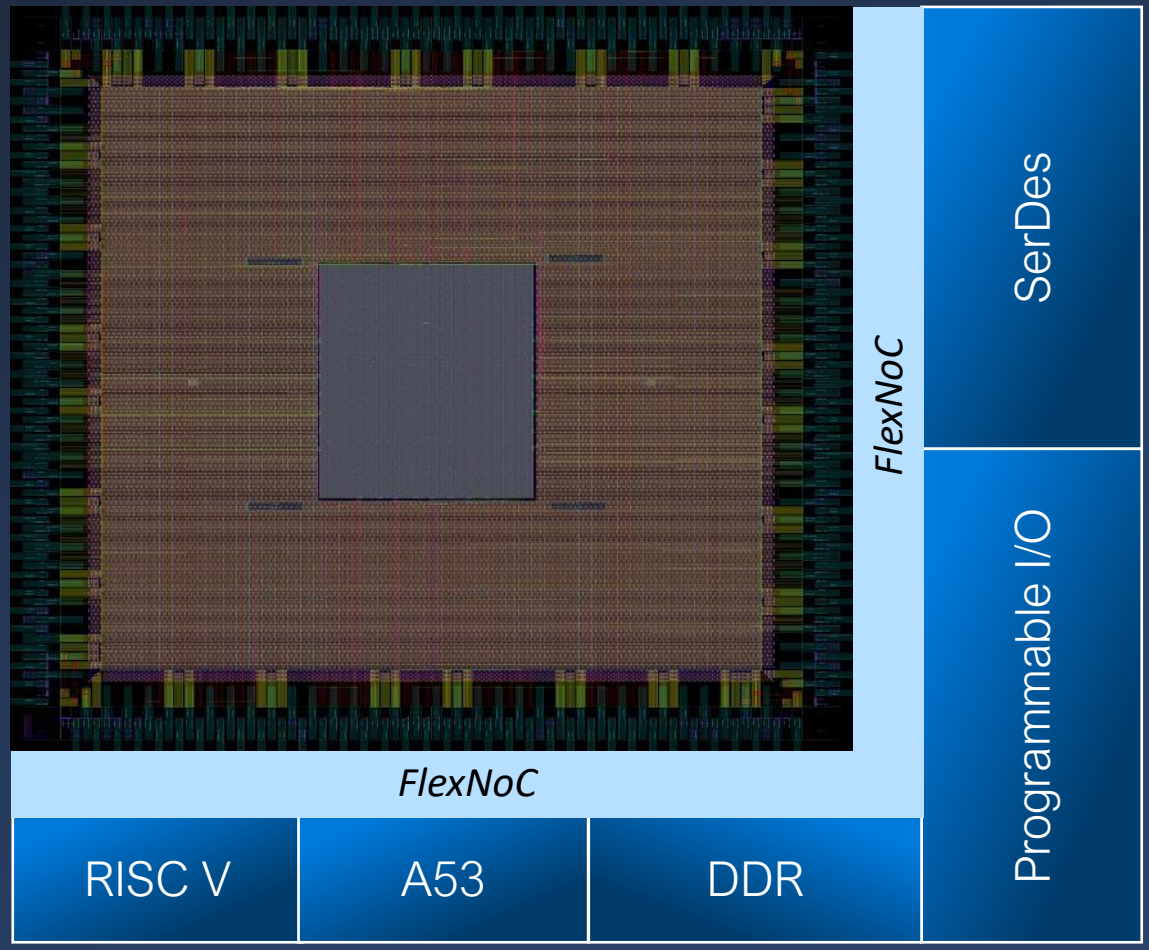
ATRENTA · synopsys · XILINX · AMD · leti

axessvision · EPFL · THALES · The University of Utah

Total Units Shipped	**10B+**
Executive Team PLD Experience	**150 years**
Complex SoC Tapeouts	**300+**
Advanced Nodes	**10+**

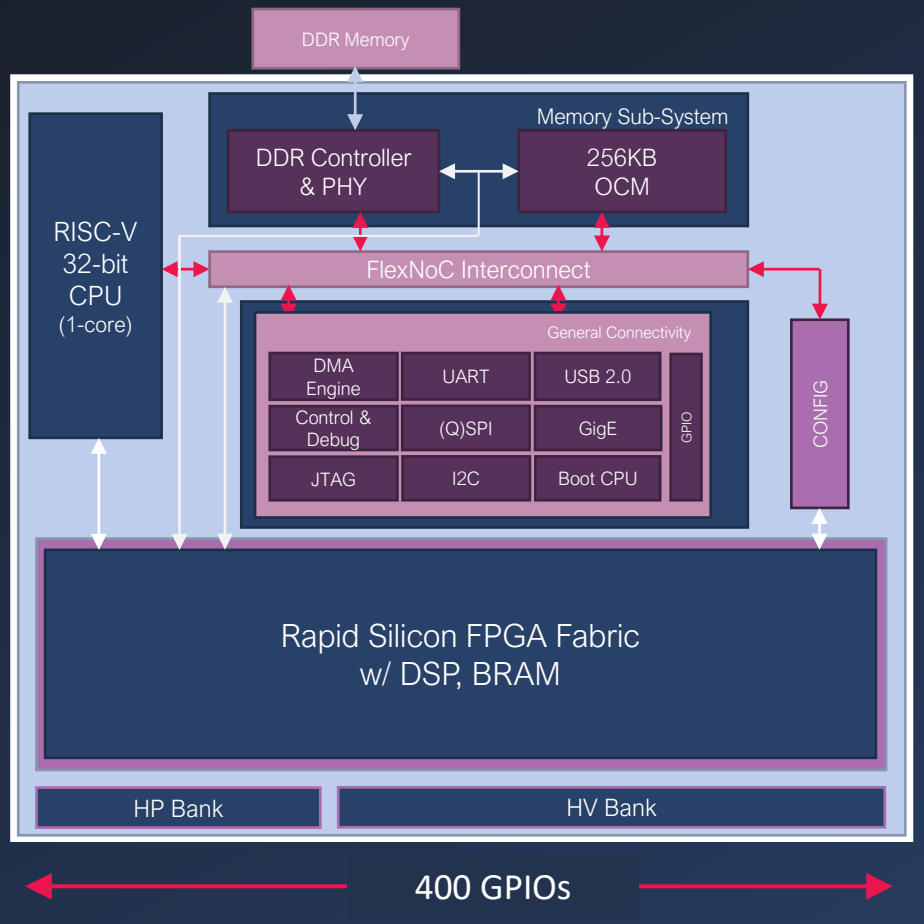
Rapid Silicon Product Differentiation

1. Use OpenFPGA to design core fabric for fast time to market
2. Utilizing industry standard, silicon-proven 3rd party IP libraries for time to market and reliability
3. FlexNoC enables easy IP integration to a wide range of IP to develop variants quickly
4. Singular Focus on Edge Products! No datacenter distraction



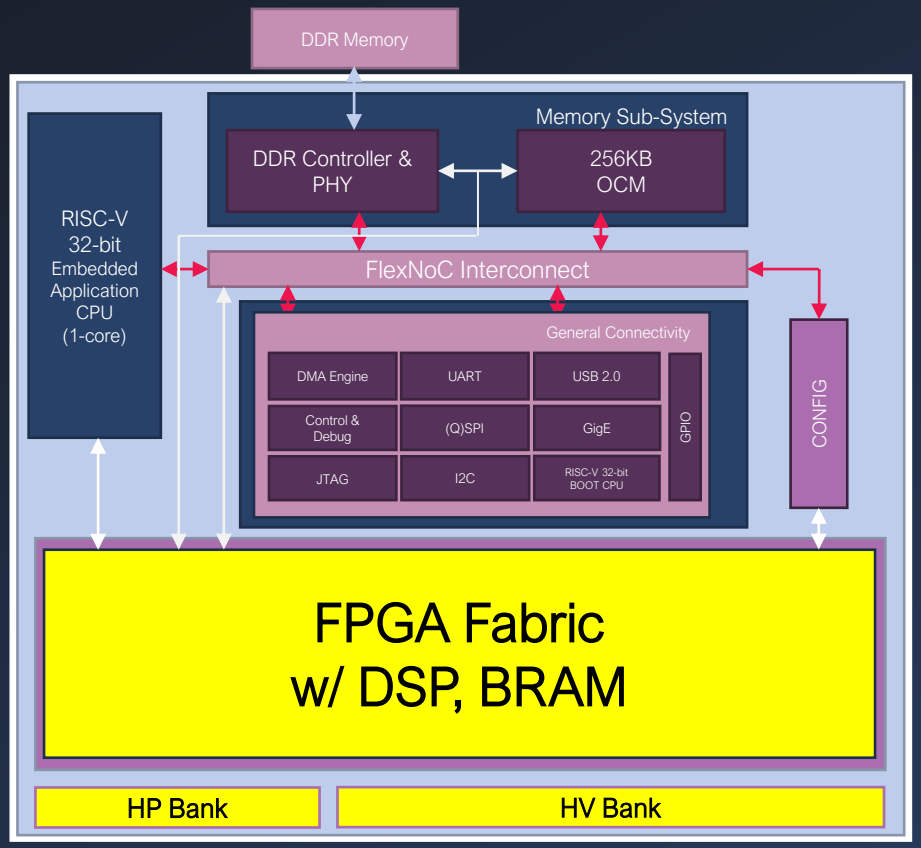
Introducing Gemini

The new standard for cost-effective Embedded FPGAs



- Built on proven TSMC 16nm FinFET process
- 30-100K Logic Density built on Open Standard 6-input LUT Logic Blocks
- Hardened 32-bit RISC-V processor running @ 533MHz
- Hardened FlexNoC and Connectivity Block
- Hard 32-bit Memory Controller
- 500+ I/O – Industry leading I/O-to-LC ratio

Gemini (Rapid Si) Fabric Domain



Fracturable 6-input LUT with carry chain

64-bit/128-bit AXI interface to Processing Domain running up to 400 MHz

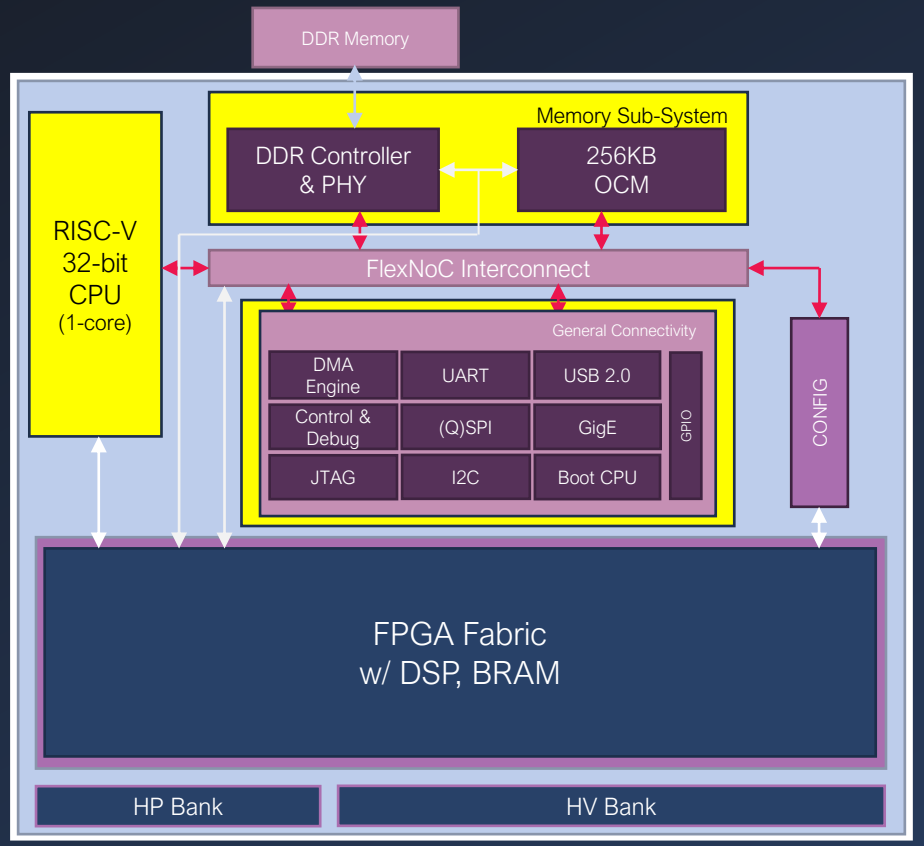
36Kb True Dual Port RAM

18x20 Multipliers w/ 64-bit accumulator and carry

General Purpose (HV) and High Performance (HP) I/O Banks

- LVCMOS, LVTTL,SSTL (I/II), PCI66/X, LVDS, LVPECL, BLVDS, RSDS
- 40-bit bank size
- Selectable drive strength, slew rate, ODT
- Native support for LVDS @ 1.2Gbps and MIPI @ 1.5Gbps

Gemini Processing Domain



RISC-V A45 Processor CPU Subsystem

- 16KB I/D Cache + 64K tightly integrated I/D Memory
- Memory Management Unit (MMU), Physical Memory Protection(PMP), and programmable Physical Memory Attribute (PMA)

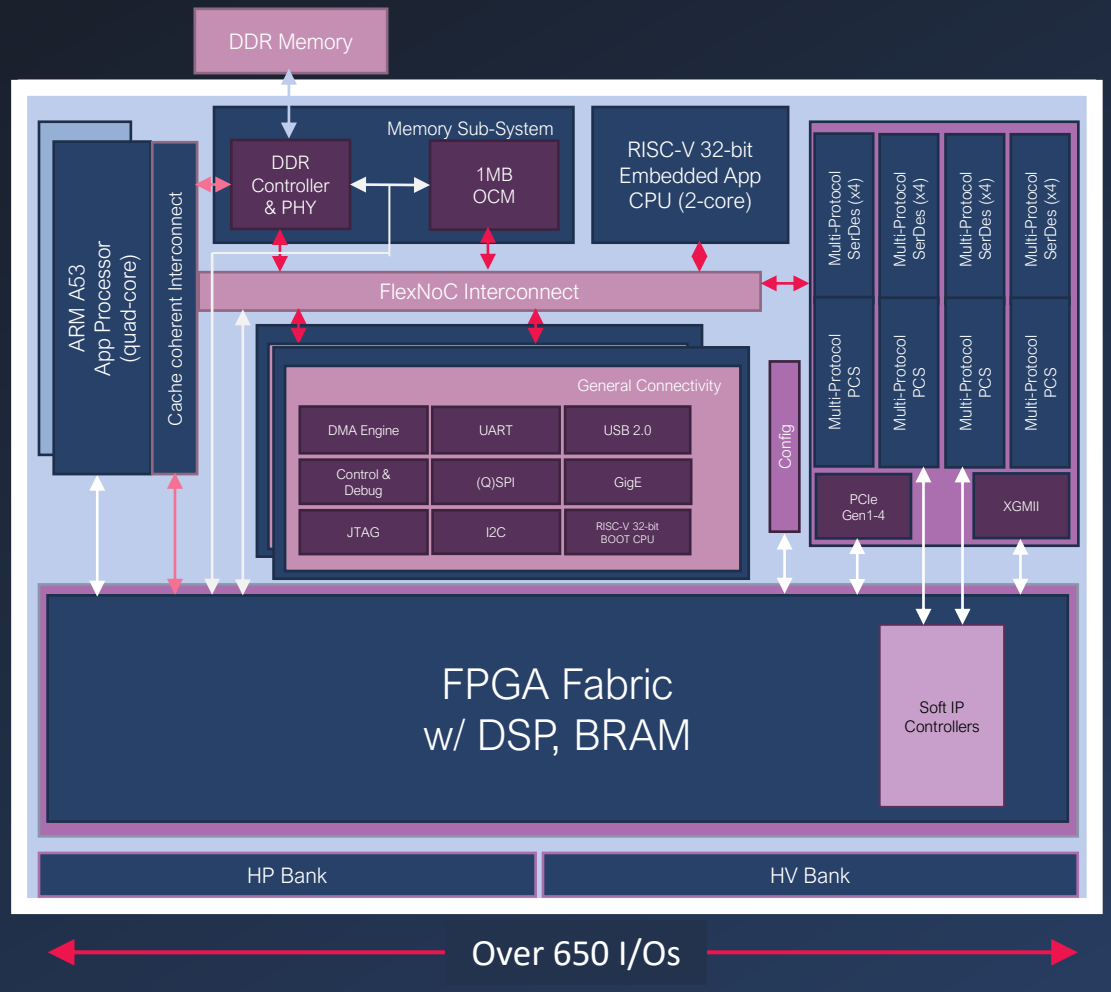
DDR3 / DDR4 Controller and PHY

- Data-rates up to 2133 Mbps
- 16-bit or 32-bit DDR memory interface

256KB On-chip Memory and Controller

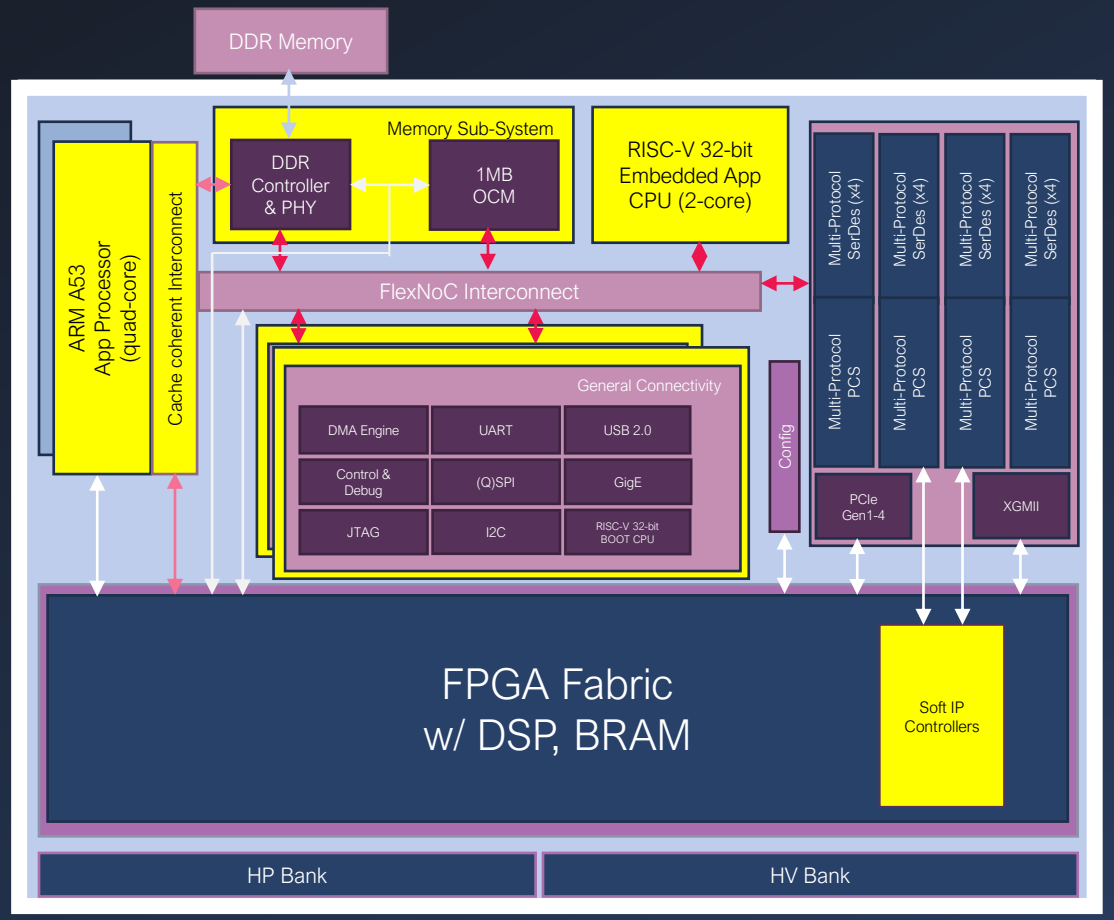
Orion for Signal Compute & Throughput

Application-Level Processing and High-Speed Transceivers - Built for Low Power



- Built on proven TSMC 16nm FinFET process
- 120-350K Logic Density
- Dual/Quad-core Arm Cortex-A53 Processors
- Hardened dual 32-bit RISC-V Processors
- Hardened FlexNoC and Connectivity Block
- Up to 24 Multi-Protocol16Gb Transceivers with hardened PCIe Gen 4 & Ethernet
- Hard 32-bit DDR Memory Controller
- Multiple Power Domains for Low Power
- Up to 650 I/O available

Orion Processing Domain



Dual/Quad-Core Arm Cortex-A53 Processors running up to 1.6GHz

Hardened dual 32-bit RISC-V processor running up to 533MHz

- Lock Step Capable

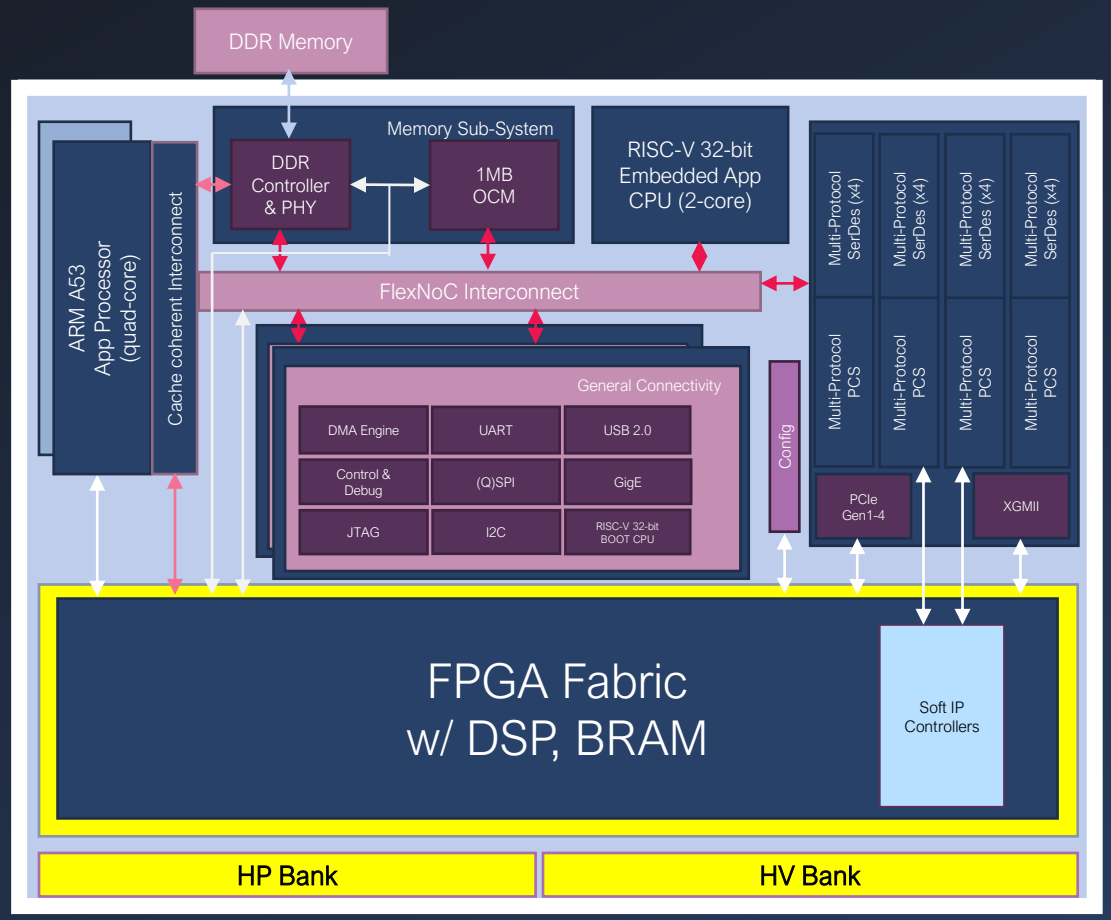
Support for UEFI, Zephyr RTOS, Linux OS

Hard DDR Memory Controller

- DDR4, LPDDR4/5 up to 2666 Mbps

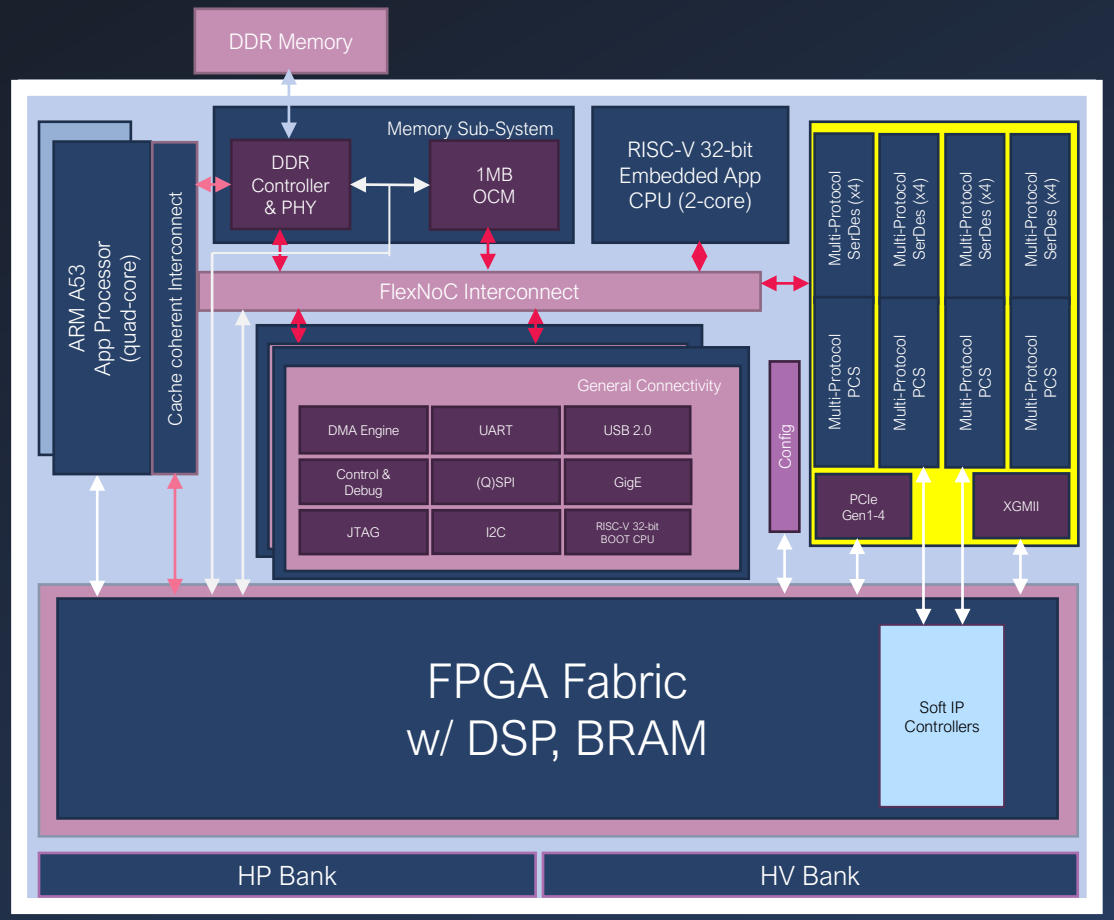
On-Chip Memory up to 1 MB

Orion Programmable Fabric Domain



- Fracturable 6-input LUT w/ carry chain
- 64-bit/128-bit AXI interface to Processing Domain running up to 400MHz
- 36Kb BRAM with FIFO support
- 18x20 DSP with 64-bit accumulator and carry
- 32-bit FPU w/ BFLOAT16 + INT8 + FP16/32 support
- General Purpose (HV) and High Performance (HP) I/O Banks
  - LVDS @ 1.6Gbps and MIPI Support @ 2.5Gbps
  - 40-bit banks with selectable drive strength, slew rate, ODT

Orion High Speed Interfaces



Up to 24, 16Gbps Transceivers

- Power and Area Optimized

Multi-Protocol PCS

- Hardened PCIe Gen 4 x8 support
- Hardened XGMII Ethernet Support

Large set of protocol support

- V-by-One HS, (Q)SGMII, IEEE 802.3 XAUI and 10G-KR, JESD204B/C, CPRI, HiGig, DP, (e)DP, SRIO

Integrated Fractional PLL

Adaptable PMA for data eye integrity

Introducing Vega embedded FPGA (eFPGA)

Unlock the Potential of Your SoC with Vega eFPGA: Flexible, Powerful, and Efficient!

- Customizable & Scalable architecture
- Logic – 6-input look-up-tables (LUTs) with integrated fast adders for efficient implementation of complex logic functions
- DSP – 18x20 multiplier, 64-bit accumulator to efficiently execute math functions such as FIR filters
- Block RAM – 36 Kb or 18 Kb True Dual Port RAM for improved system performance
- Designed for TSMC's 16nm FinFET process node
- High-Performance, Flexible I/O supporting up to 3.3V with support for LVDS and MIPI

Maximizing Benefits with Vega IP

Harnessing the Power of Vega eFPGA IP for Your Business

Customize Vega to Suit Your Needs

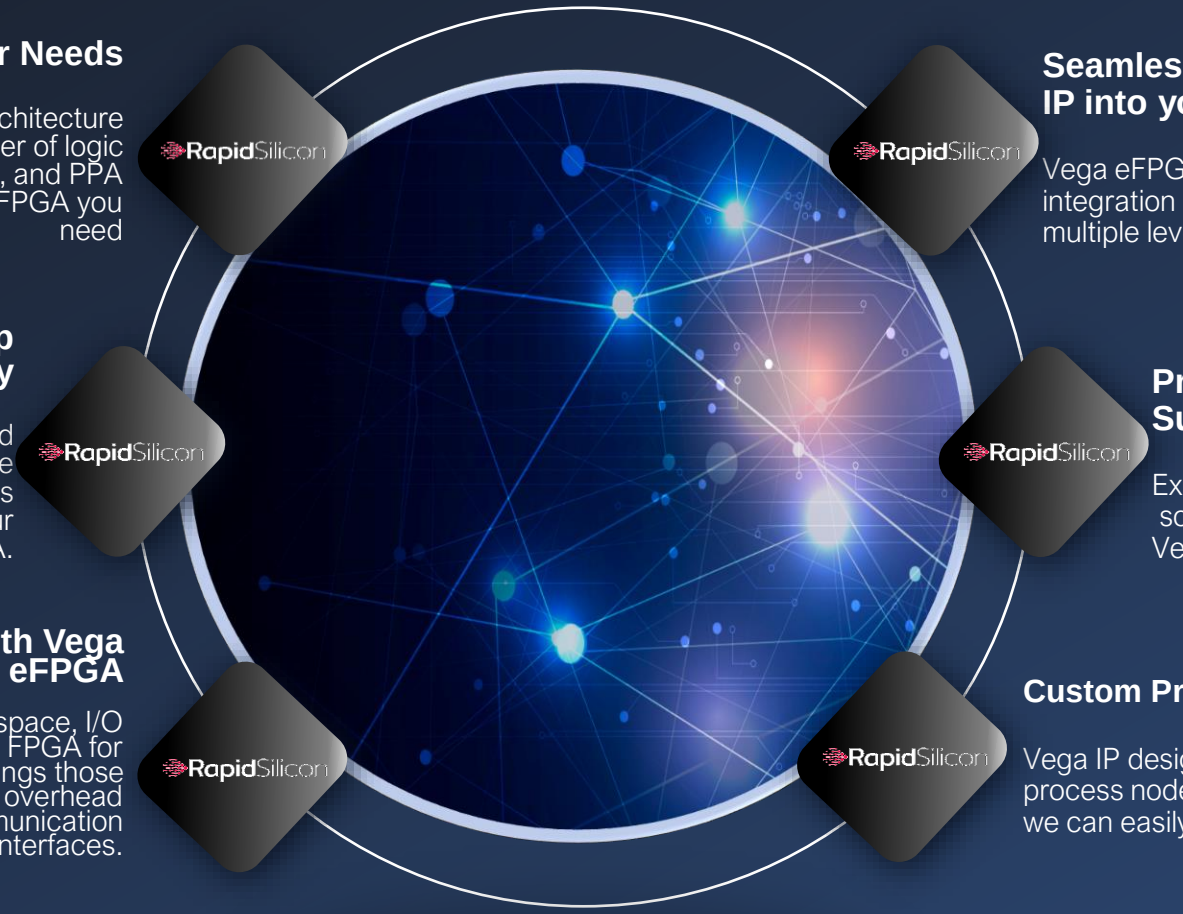
Leverage the power of our modular architecture to suit your needs. Specify the number of logic blocks, DSPs, BRAMs, interconnect, and PPA budget to help you architect the exact FPGA you need

Enhance Flexibility with On-Chip FPGA functionality

Eliminate the need for an on-board FPGA and reduce manufacturing costs, board space, time to market, and the need for multiple SoC variants with on-chip FPGA functionality. Empower your SoC with Vega eFPGA.

Accelerate Your Processor with Vega eFPGA

Eliminate the need for sacrifices in board-space, I/O latency, and bandwidth while using standard FPGA for processor acceleration. Vega eFPGA brings those accelerators on-chip, without the limitations or overhead of I/O pad-count or chip-to-chip communication interfaces.



Seamlessly Integrate and verify Vega IP into your SoC Design

Vega eFPGA is designed to provide seamless integration into your SoC, and can be verified at multiple levels for maximum reliability

Program Vega with Raptor Design Suite

Experience industry's first most capable open-source tool to implement your design using Vega eFPGA IP

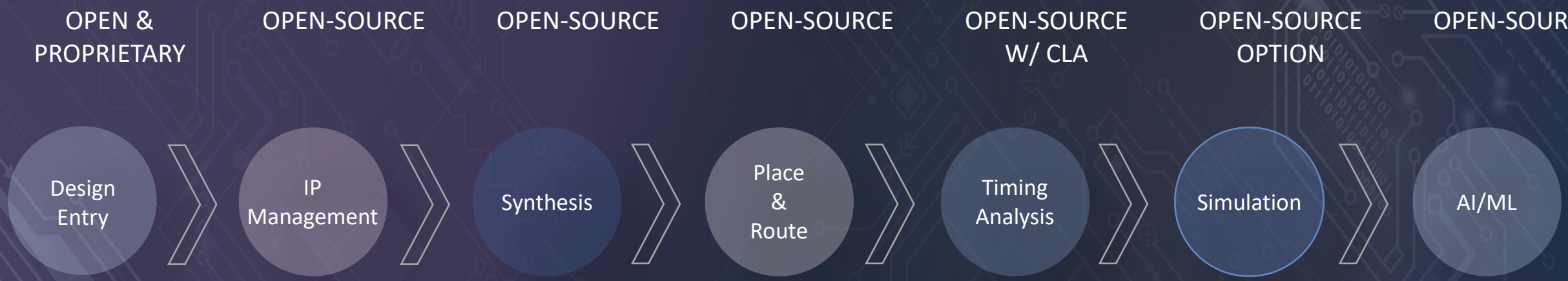
Custom Process Portability

Vega IP designed for TSMC's 16nm FinFET process node. For other process technologies, we can easily port Vega IP to meet your needs

Raptor
Design Suite

The only open-source commercial EDA tool

Raptor Design Suite: Industry's First Open-Source EDA Tool



FOEDAG / Verific

- Tcl backend, full design automation support
- Qt-based GUI frontend GTKWave integration

LiteX

- Python-based design builder
- Support for Python-to-RTL
- Library of 50+ qualified and verified open-source Soft IPs (AXI bridges, RiscV soft processors...)

Yoysys

- Verific design parsing for mixed language support, IEEE 1735 encryption
- Yosys optimized for RS architecture
- ABC-DE for device architecture mapping

OpenFPGA/VPR

- OpenFPGA started by Rapid Silicon CTO
- VPR is the most robust open-source place & route engine
- Verific Verilog parser added with IEEE 1735 encryption support

OpenSTA

- Industry standard – also used by AMD-Xilinx & MicroSemi

Verilator/GHDL/Icarus

- Verilator 2 states simulation can boot Linux in simulation < 1 minute
- QEMU for SW development
- GHDL support for VHDL designs
- Icarus support for 4 state and timed simulation

CFU IP

- Based on Google CFU playground
- Implements a custom CPU architecture for AI & ML Workloads
- Up to 10x faster than other implementations
- Innovating new, compact AI/ML models

RapidSilicon

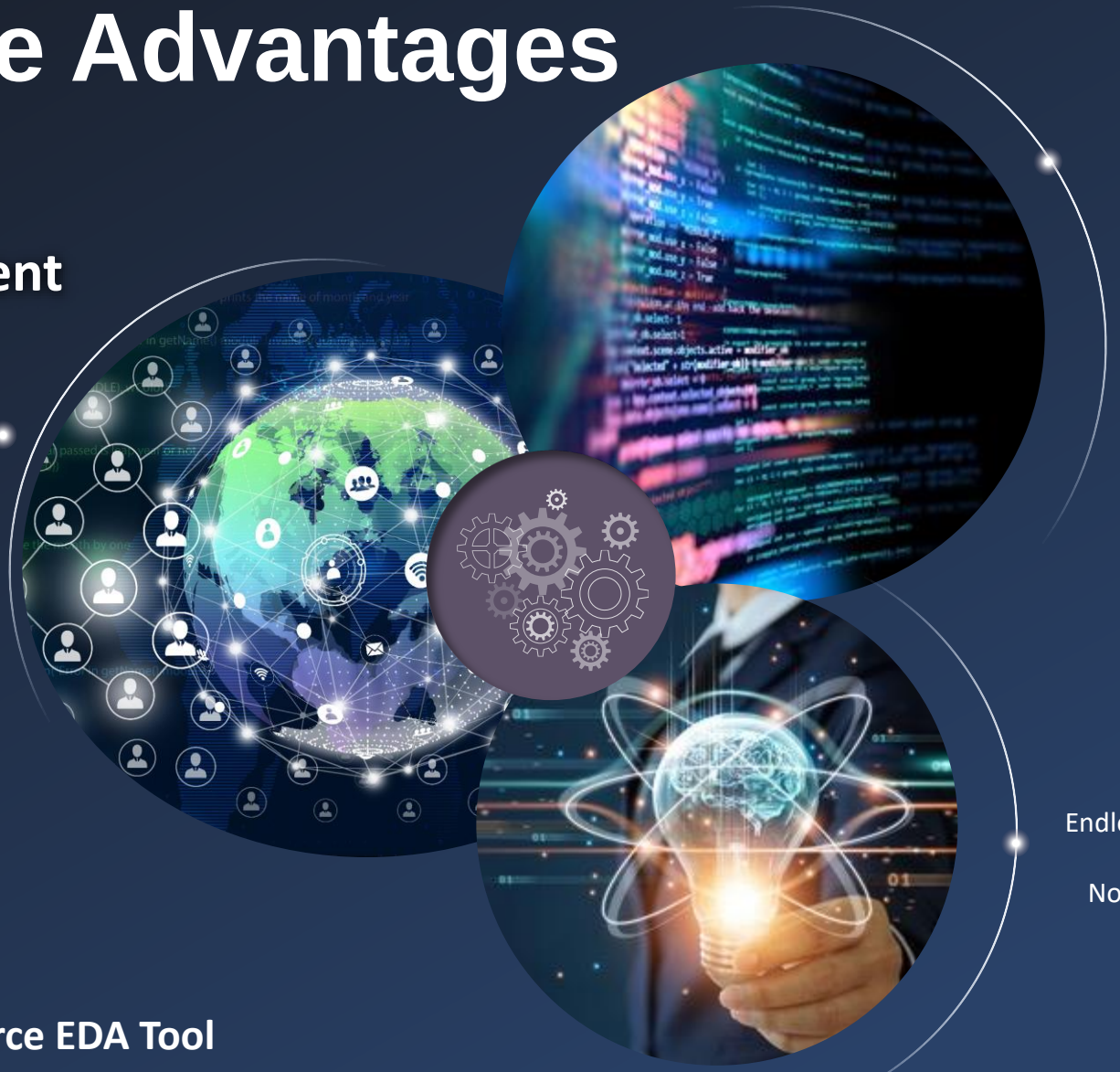
Open-Source Advantages

Community Engagement

Proven Historical Growth
(Linux and RISC-V)

Easy Access via GitHub

Increased Engagement → Support via Forums, Slack Channels…



Non-Proprietary

User Control

Enables Custom Modification

Google, Apple and many more moving to Open Source

Innovation

Endless & Continuous Improvement

No End-of-Life or Archived Tools

Focus on Differentiation

First Commercial-Grade Open-Source EDA Tool

Open-Source Gravitas

Industries are moving rapidly to open source – the FPGA industry is in the early days

gstreamer

DPDK
DATA PLANE DEVELOPMENT KIT

AUTOMOTIVE GRADE LINUX

OPEN Compute Project®

OpenCL™

CIVIL INFRASTRUCTURE PLATFORM

ASWF /* ACADEMY SOFTWARE FOUNDATION

CHIPS ALLIANCE

ELISA
ENABLING LINUX IN SAFETY APPLICATIONS

ROS

AI Based Enhancement to Yosys ABC

1. Yosys is an open-source implementation of ABC, a logic synthesis engine developed over decades

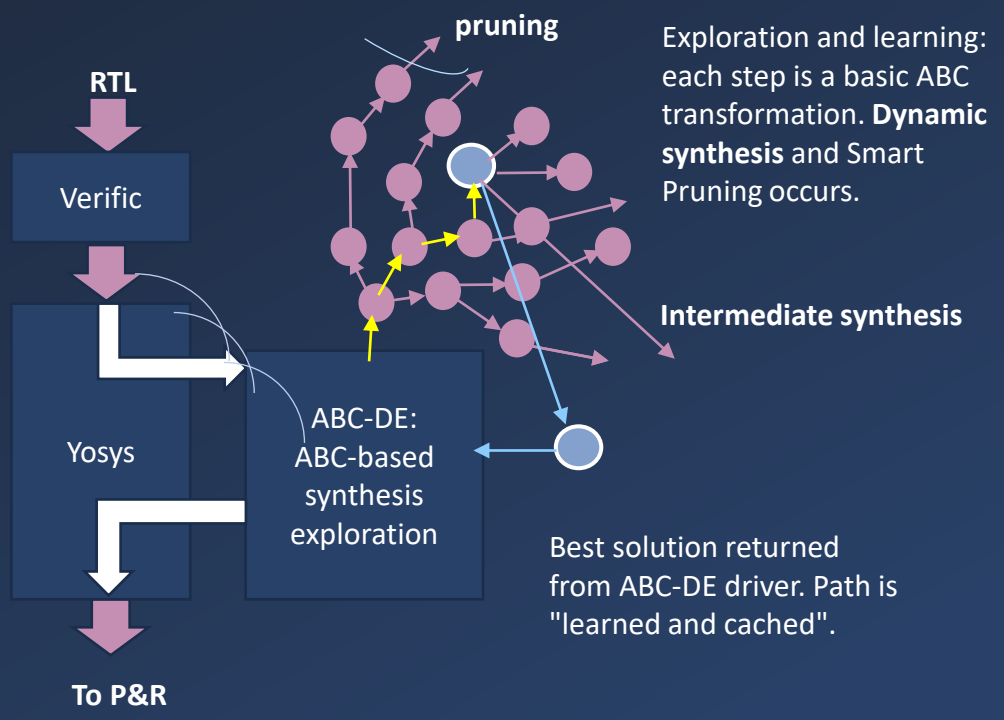
2. DE is AI-based design exploration addition to ABC, adaptive to the nature of the design, dynamically optimizing

3. Performs dynamic incremental transformations and mapping of boolean logic

   Up to 3x reduction in area

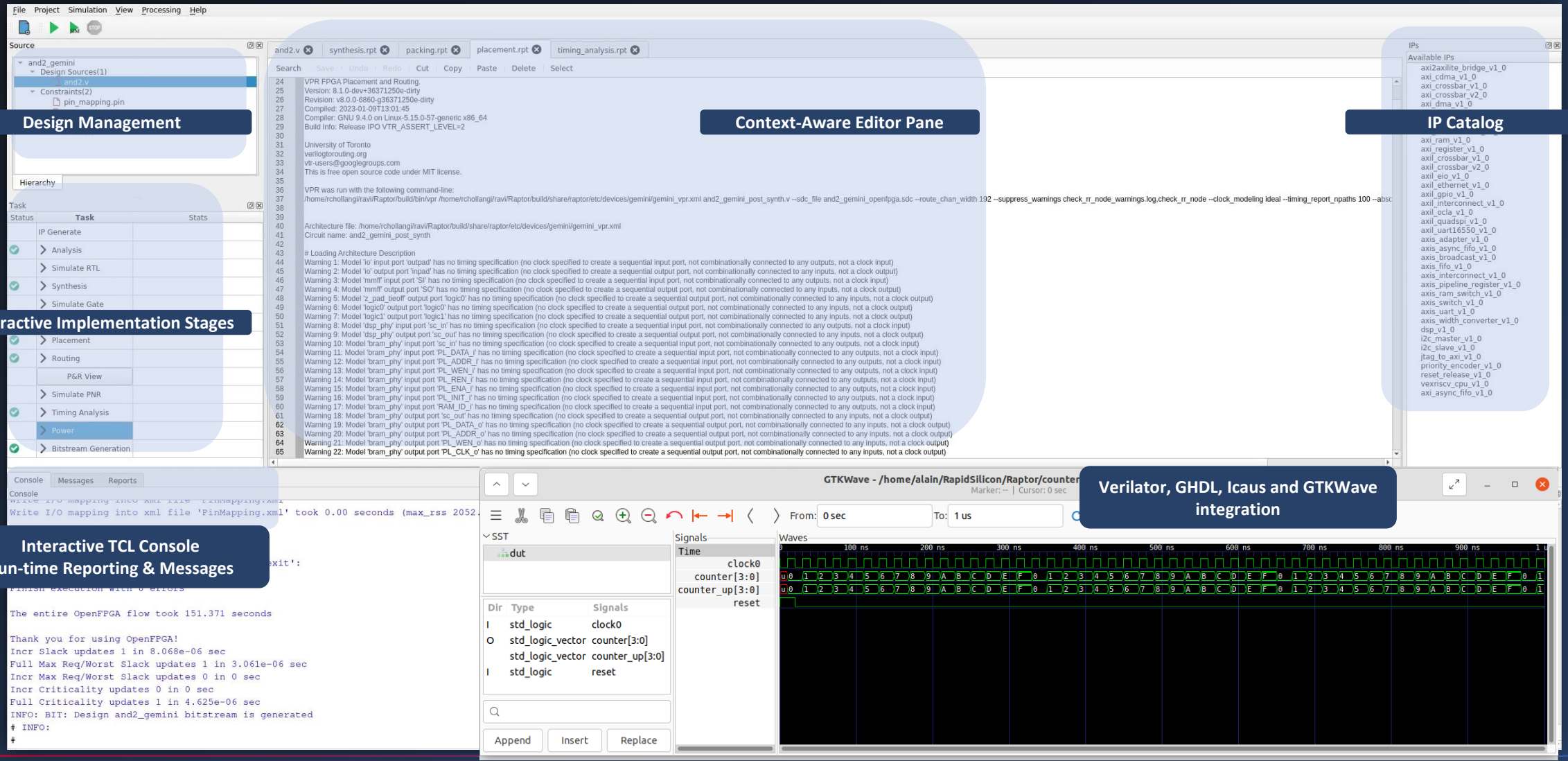
4. Benchmarked and proven in public EPFL competition

   31 unique Winners out of 46 benchmarks.



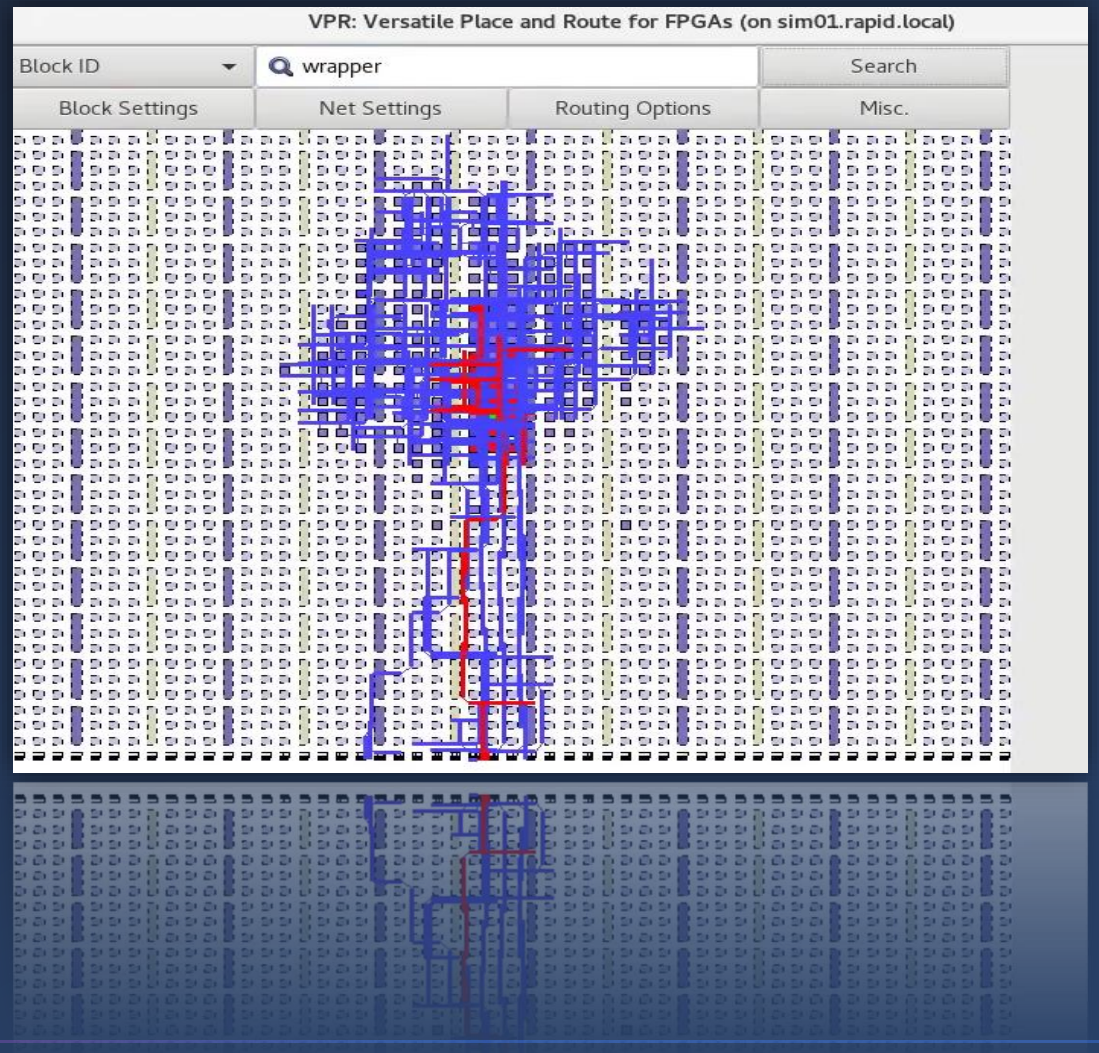
Rapid Silicon Flow (Yosys + ABC-DE)

Intuitive Raptor User Interface



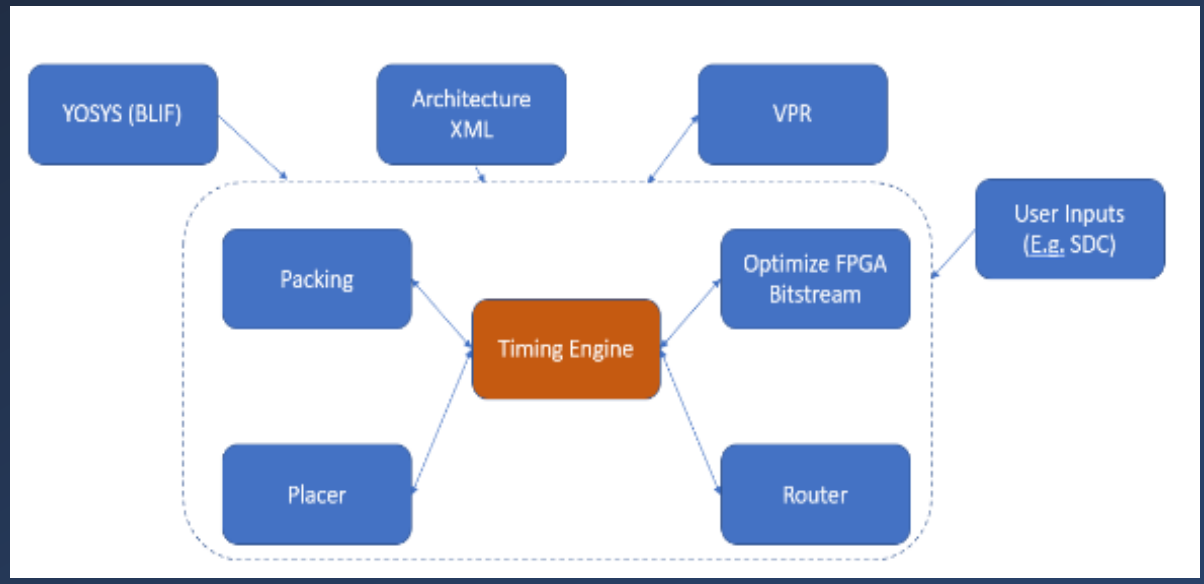
VPR - Versatile Place and Route

- Open-source Place & Route Tool, developed by University of Toronto, led by Vaughn Betz
- Used by several non-FPGA companies
- Supports parallel threads
- Annealing schedule driven
- User-configurable options for packing and routing
- Timing, Area and Balanced prioritization with re-route capability
- Fanout, Effort level and Initial seeding control



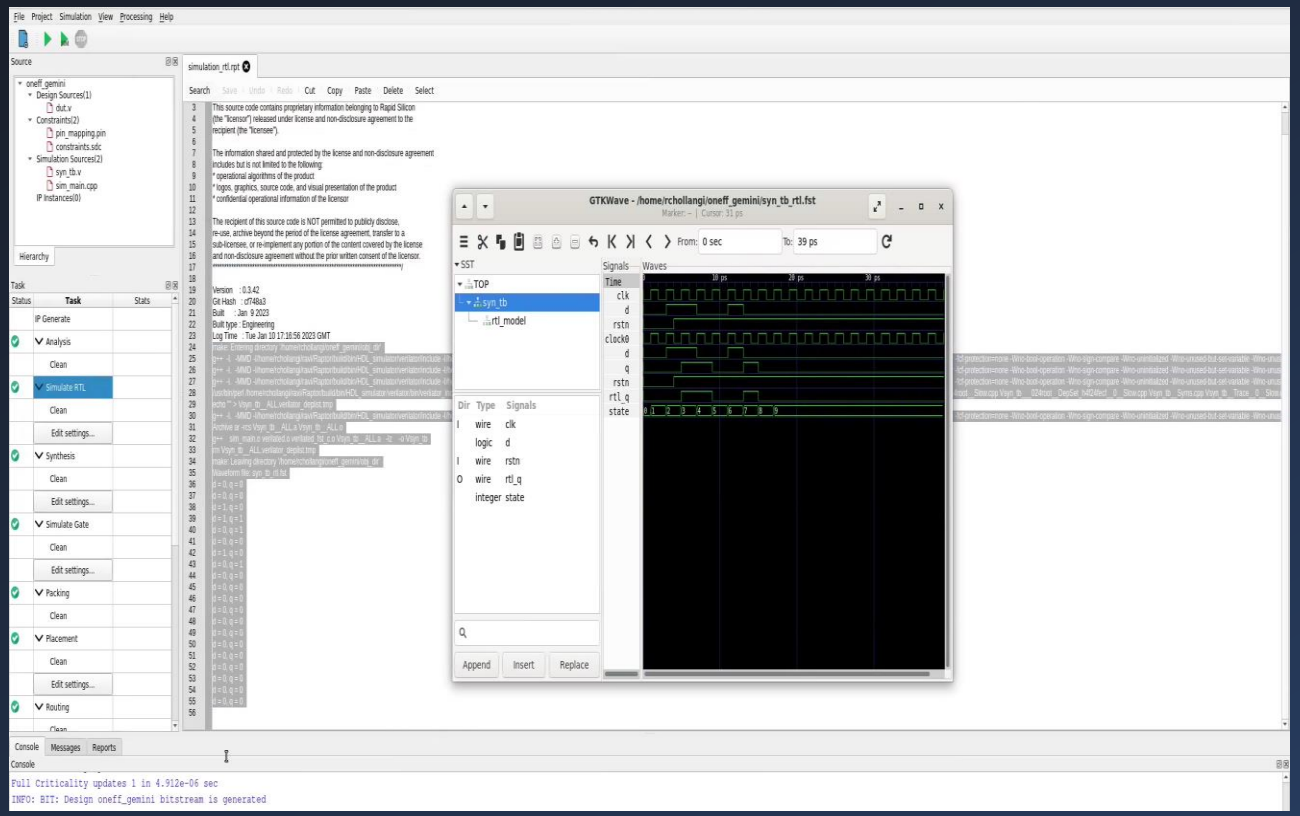
OpenSTA - Industry Standard Timing

- Supports standard file formats for timing analysis
- Used by many significant companies
- Rich TCL interface to read design, specify timing constraints and create timing reports
- Supports external delay calculator API
- Integrated RC effective capacitance algorithm for delay calculation
- Allows query based incremental updates of delays, arrival and required times



OpenSTA, best-in-class timing engine, used for timing analysis & optimization

Comprehensive simulation support



- Fully integrated simulator engine for Verilog and VHDL designs
- Verilator (fastest Verilog/SystemVerilog 2 states simulator)
- GHDL for VHDL simulation

  Icarus for 4 states and Timed simulation
- In-built GTKWave waveform viewer
- Supports RTL and Gate level simulations
- Multi-threaded simulations are supported
- 100% Open source

EPFL: Best in Class LUT6 Implementation

École polytechnique fédérale de Lausanne (EPFL) Combinatorial Benchmark Suite Competition

- 37 best solutions over 46 benchmarks
- Up to 3x reduction in size
- Optimal results for at least 2 designs

"…23 natively combinational circuits designed to challenge modern logic optimization tools."

30 unique wins, 2 category ties

- 2x more than next closest entrant
- Better than all other entrants in EDA industry
- Won in area hands-down! **(23 Best area** over **23 benchmarks)**

Full results here: benchmarks/best_results at master · lsils/benchmarks (github.com)

Best LUT-6 Implementations - 2022

The best LUT-6 implementations keep track of the best results of LUT-6 mapped benchmarks, both for size (# of LUTs) and depth (# of levels).

Best results for LUT-6 count

Arithmetic Benchmarks

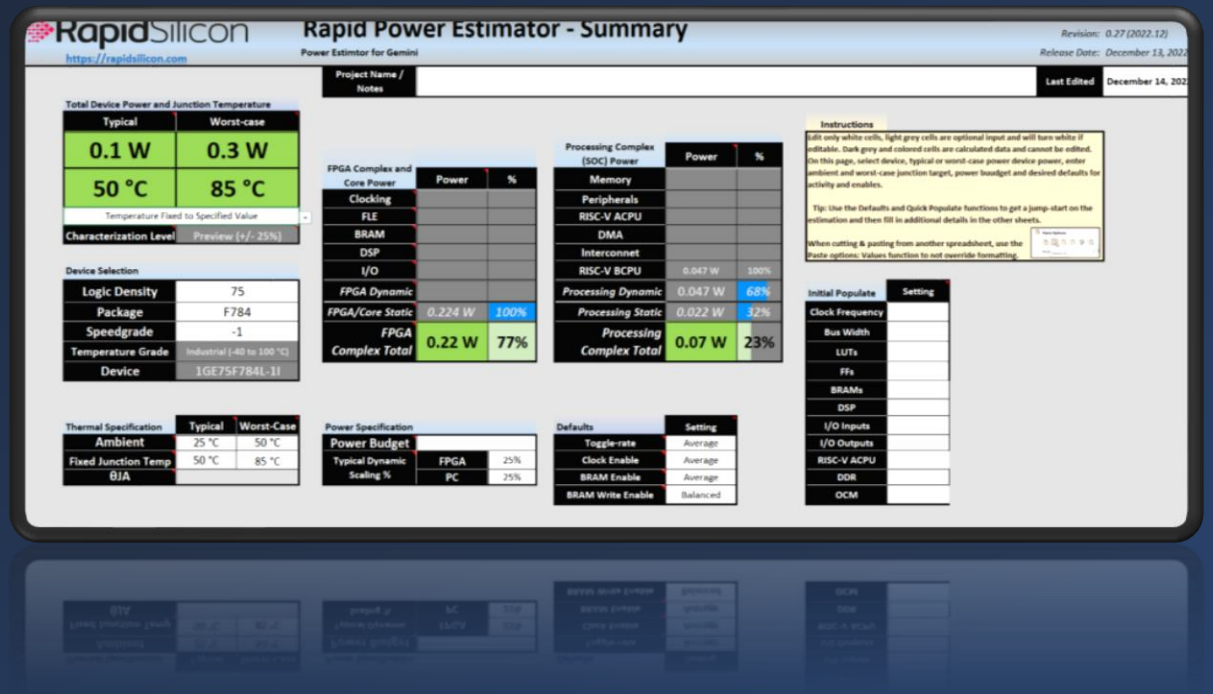
Benchmark name	Inputs	Outputs	LUT-6 count	Levels	Authors	Method
Adder	256	129	129	127	T. Besson	ABC-DE: ABC Design Explorer
Barrel shifter	135	128	512	4	R. K. Brayton & A. Mishchenko	ABC Extreme Mapper
Divisor	128	128	3101	1110	T. Besson	ABC-DE: ABC Design Explorer
Hypotenuse	256	128	39516	4560	A. Grosnit, C. Feng, X. Li, et al.	NAILS
Log2	32	32	6326	151	T. Besson	ABC-DE: ABC Design Explorer
Max	512	130	511	183	T. Besson	ABC-DE: ABC Design Explorer
Multiplier	128	128	4424	168	T. Besson	ABC-DE: ABC Design Explorer
Sine	24	25	1114	62	T. Besson	ABC-DE: ABC Design Explorer
Square-root	128	64	2994	1069	T. Besson	ABC-DE: ABC Design Explorer
Square	64	128	3071	108	T. Besson	ABC-DE: ABC Design Explorer

Random-Control Benchmarks

Benchmark name	Inputs	Outputs	LUT-6 count	Levels	Authors	Method
Round-robin arbiter	256	129	276	30	T. Besson	ABC-DE: ABC Design Explorer
Alu control unit	7	26	26	2	A. Grosnit, C. Feng, X. Li, et al.	NAILS
Coding-cavlc	10	11	54	6	T. Besson	ABC-DE: ABC Design Explorer
Decoder	8	256	264	2	L. Machado and J. Cortadella	Support-Reducing Decomp
I2c controller	147	142	182	7	T. Besson	ABC-DE: ABC Design Explorer
Int to float converter	11	7	20	3	T. Besson	ABC-DE: ABC Design Explorer
Memory controller	1204	1231	1735	14	T. Besson	ABC-DE: ABC Design Explorer
Priority encoder	128	8	94	20	T. Besson	ABC-DE: ABC Design Explorer
Lookahead XY router	60	30	19	5	T. Besson	ABC-DE: ABC Design Explorer

Rapid Power Estimator and Board Tool

- Early estimation based on Excel
  - Evaluating open-source spreadsheet tools
- Generally, first look at device architecture
  - Used prior to installation/use of Raptor
- Provide board-level power and pinout guidance / support
- Back-end power estimation under investigation



RPE is the view into RapidSilicon's Power Efficiency

Rapid Silicon is Alive and Thriving

Rapidly Progressing Test Chip and EDA Tools

MPW1 Test Chip Demo

Video

Open-Source EDA Tool Strategy

Video

Raptor EDA Demo

Video

CEO Message

Video

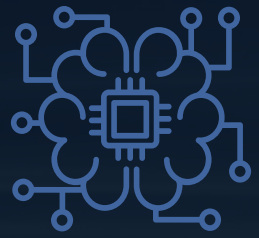
Summary

Accepting the Challenge to Build Next-Gen FPGAs and SoCs for Cost-Sensitive Markets

Experienced Team

150+ Years of Executive Team PLD Experience

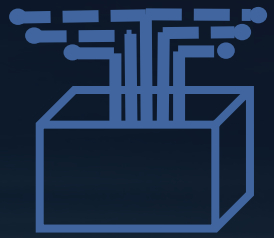
Incredible PLD Company Diversity



The Right Architecture

Leverage Open-Source and 3rd-Party IP for fast TTM

Utilize FlexNoC to quickly and easily add IP



Embracing Open-Source

First to Integrate OS Tool Chain for PLD Design

Rapid Tool Evolution and Improvement

Raptor Design Suite

Add FPGAs to an existing portfolio of stand-alone FPGAs (Production Silicon) or Embedded FPGAs.

- Off-the-shelf Core FPGA IP (eFPGA, Silicon proven IP)
- Tailored FPGA Core IP (DSP, BRAM, LUT, Routing, IOs, Secure configuration...)
- Design Services (Full SOC integration)
- Complete end-to-end Software stack
- Customizable Software stack mix-and-match with existing stacks

Interested in Learning More?

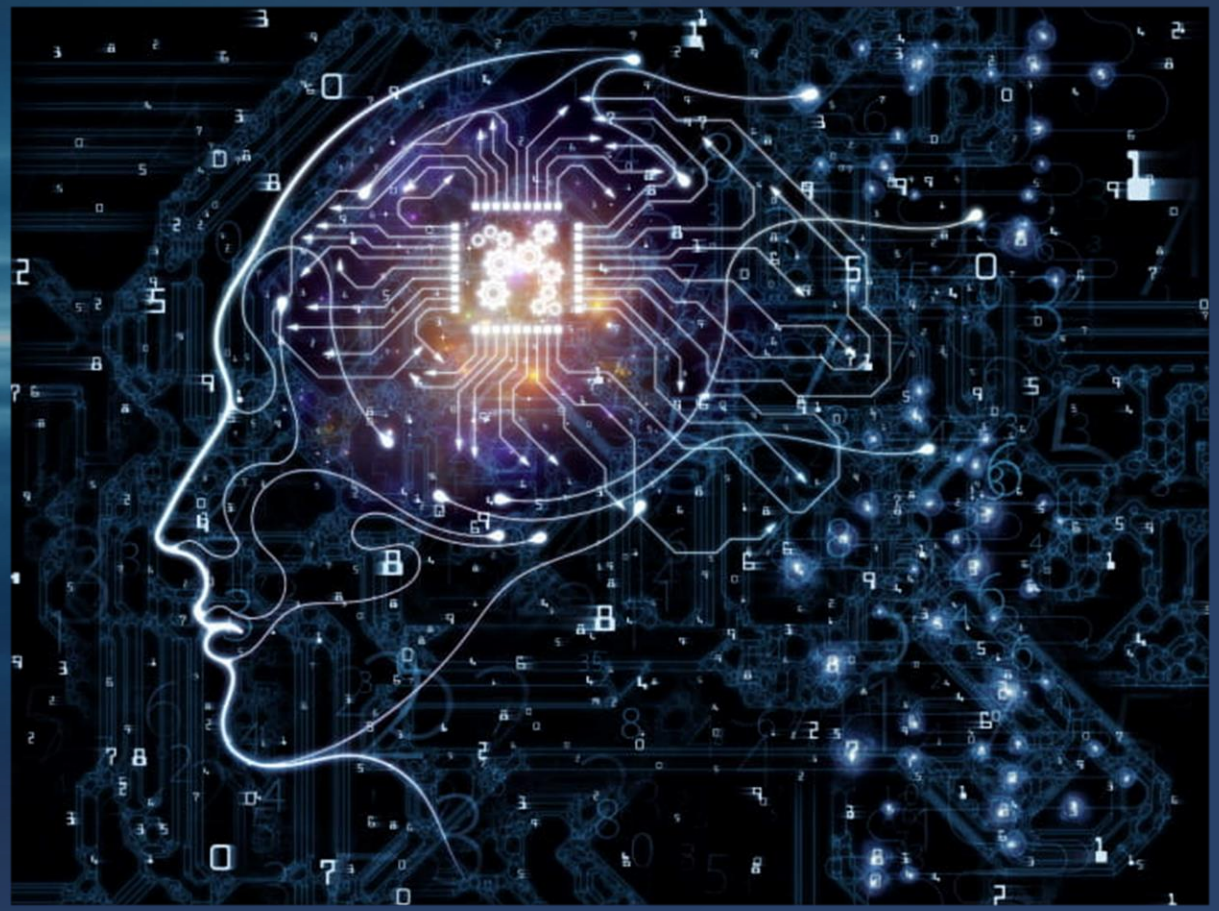
Join our Early Access Champions Program*

Updates on:

- Product Development
- Tool Flow
- Solutions

Early Access to Silicon & Dev Kits

Direct Technical Support



* Requires NDA and non-binding MOU

Thank you