Virgo Preliminary Data Sheet: Overview

DS-128 (v1.1) June 15th, 2024 **Product Data Sheet**

General Description

Rapid Silicon introduces the Virgo family of programmable logic devices, offering significant benefits with low power consumption, maximized connectivity, and optimized performance capabilities. Built on TSMC's 16nm FinFET Compact (16FFC) process node, Virgo family delivers high-performance logic based on 6-input look-up table (LUT), high-speed serial connectivity, and an optimized fabric architecture. These features make the Virgo family ideal for a wide range of applications across various markets.

Key Features

Configurable Logic Blocks (CLB)

- 6 Input Lookup tables (LUT)
- Flip-flops
- Adder

36Kb Block RAM

- True dual-port
- Configurable as dual 18Kb
- Dedicated 32-bit FIFO logic

DSP Blocks

- 18x20-bit multiply
- 64-bit accumulator
- Full 38-bit Multiplier Output

Programmable I/O Blocks

- Supports LVCMOS, LVDS, and SSTL
- 1.2V to 3.3V I/O
- Programmable I/O delay and SerDes

External Memory Interfaces

- A range of DRAM interfaces including DDR3, DDR4, and LPDDR4, achieving data rates up to 2133 MT/s
- ECC support

8-Channel DMA Controller

- Single DMA controller of 8 channels
- Supports 32 bits Address and Data bus width

Serial Transceivers

- Up to four dedicated receivers and transmitters
- Supports up to 10Gb/s data rates

Configuration and Security Unit

- Boot-up and configuration are managed by a dedicated boot processor core
- Secure firmware boot-up

Dedicated I/O Peripherals and Interfaces

- PCI Express Gen3
  - Root complex and End Point configurations
  - Up to x4 at Gen3 rates
- Watch Dog Timer with PWM
- SPI / QSPI Flash Controller
- I2C w/ selectable master/slave mode
- High-speed UART (up to 1Mb/s)
- JTAG TAP Controller
- Up to 240 high range I/Os
- Up to 120 high performance I/Os

Virgo Product Overview

The Virgo family boasts a wide range of interfaces, including PCI Express (Gen4), Ethernet (up to 10G), LVDS, and JESD204B, particularly in larger devices. These devices offer powerful programmable processing capabilities, featuring up to 100k logic cells, 208 multipliers (18x20), and 9.4 Mb of embedded memory while also providing bitstream security features. Additionally, they support a range of DRAM interfaces including DDR3, DDR4, and LPDDR4, achieving data rates up to 2133 MT/s in future roadmap devices.

The Raptor Design Suite empowers designers with a streamlined environment to implement their designs on Virgo devices. Its intuitive graphical user interface (GUI) simplifies navigation and reduces design flow complexity. Under the hood, the Raptor Design Suite leverages the power of open-source tools, providing a set of features for each stage of the design implementation process.

To optimize the design area, the Raptor Design Suite utilizes AI-driven synthesis techniques. It also offers user-configurable options for partitioning, packing, routing, timing, and area optimization, giving users granular control over the design process and enabling fine-tuning of implementation metrics.

Raptor also offers a fully integrated HDL simulator engine, allowing users to simulate their design directly within the suite. The built-in GTKWave waveform viewer simplifies result visualization, while multi-threaded simulation capabilities accelerate the process, significantly saving development time.

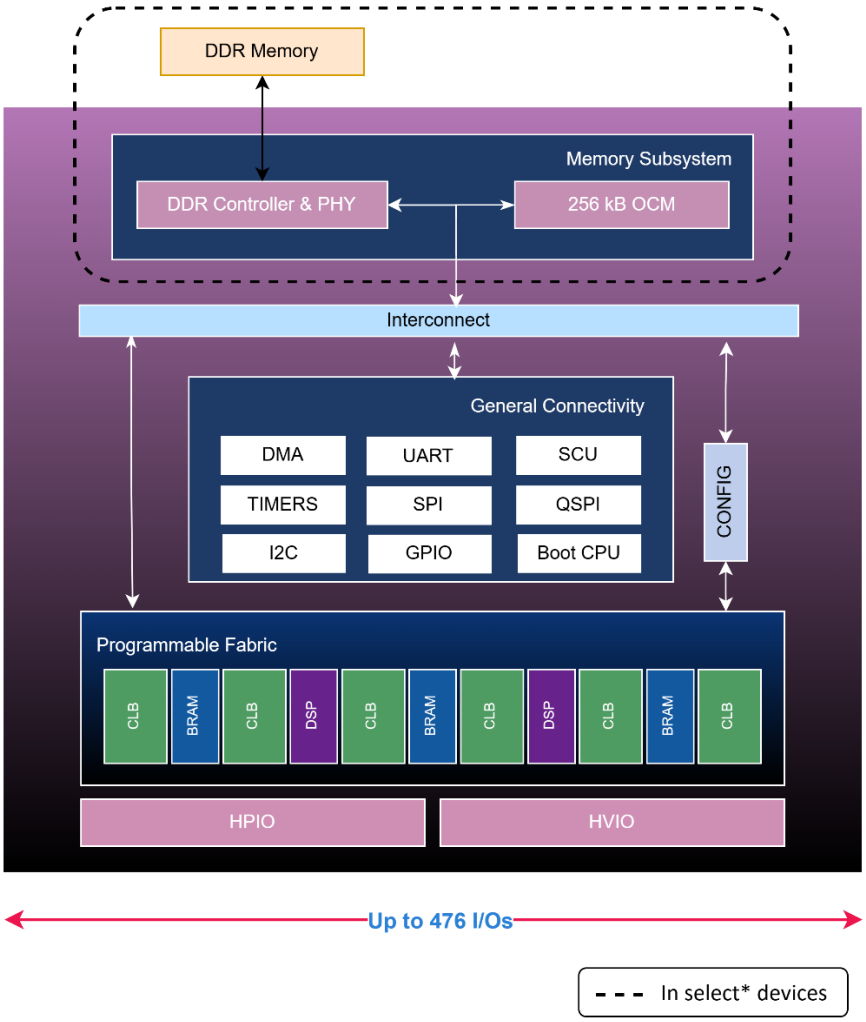

Figure 1: **Virgo Functional Block Diagram**

Table 1 provides an overview of the key features of each member of the Virgo FPGA family. The family comprises of four members, with Virgo-28K, in a 484-ball BGA package, being the first to be released. The remaining products will follow subsequently.

Table 1: **Virgo Family of FPGA devices**

	Virgo-28	Virgo-40	Virgo-100*
Logic Elements (k)	27	39	102
LUTs	17472	23808	63648
Flip Flops	34944	47616	127296
CLB	2184	2976	7956
Block RAM (Mb)	2.0	3.5	9.4
DSP	56	64	208
PLLs	2	2	4
Clocks	16	16	16
Hardened DDR Controller	N/A	N/A	32-bit
Transceiver (10G)	N/A	N/A	4
Hardened PCIe Gen3	N/A	N/A	1
High Voltage Banks	4	4	6
High Performance Banks	2	2	3
High Voltage IOs	160	160	240
High Range IOs	80	80	120
Configuration IOs	32	32	32
DDR I/O	N/A	N/A	84
Total I/O	272	272	476

FPGA Complex

The Virgo FPGA complex has programmable fabric that centers around the configurable logic blocks (CLBs), BRAM and DSP columns.

Configurable Logic Block

Each CLB consists of eight Fracturable Logic Elements (FLEs) housing six-input lookup tables (LUT6s) and storage elements. A CLB has 4×12 general inputs to drive 6 LUT inputs on each of 8 FLEs, as well as 6 special shared inputs for enables and resets, and carry chain input and output pins pre-connected to neighbors. It has 16 outputs which can be either combinational or sequential, and 8 outputs which are direct fast combinational connections. Each FLE combines look-up-tables (LUTs) and controllable data registers to store, retrieve, and process data synchronously.

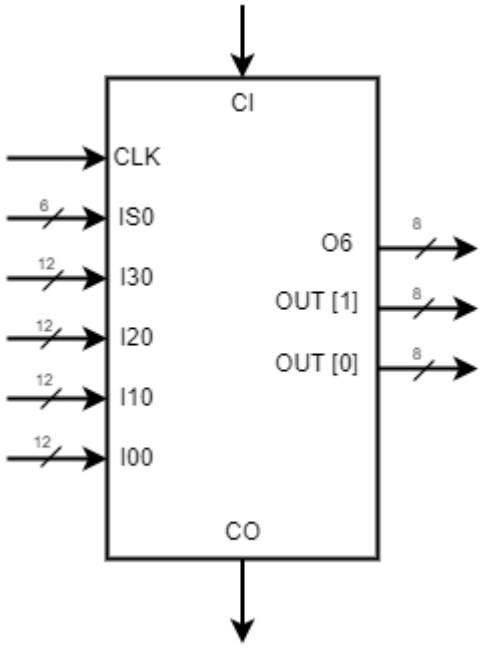

Figure 2: **Configurable Logic Block**

Block RAM

Virgo FPGA devices feature 36-kbit fracturable block RAMs, offering versatile configurability to accommodate a broad spectrum of functionalities. Each block RAM module can flexibly operate either as a singular 36-kilobit RAM or as two distinct 18-kilobit RAM blocks. Additionally, the block RAM modules include dedicated logic tailored for 32-bit FIFO implementation.

The true dual-port block RAM architecture comprises two fully independent access ports, labeled A and B. This enables data to be written to either port, or both simultaneously, and likewise, data can be read from either port, or both concurrently. Each write operation is synchronous, with each port equipped with its own dedicated address, data input/output, clock signals, and enables.

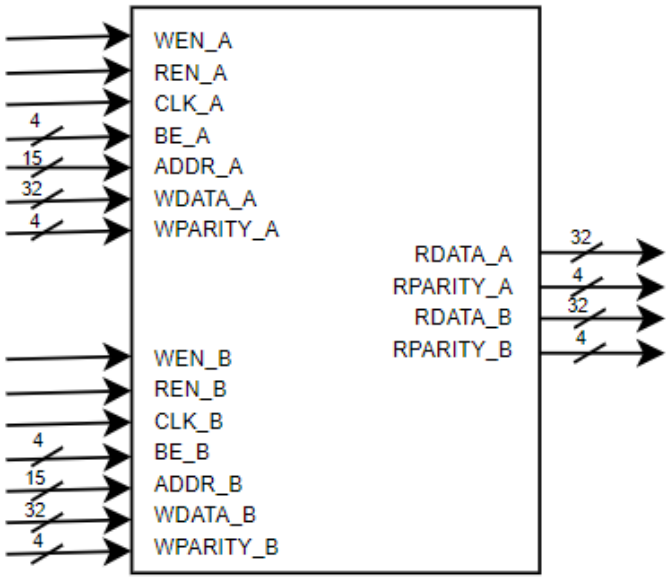

Figure 3: **True Dual Port Block RAM**

Below outlines the architectural summary of BRAM features:

- Memory configuration support as single-port, simple dual-port, and true dual-port
- Each RAM block support 18kbit
- Byte enable support to mask input data to write specific data bytes
- Parity Bits
- Simple Dual port mixed width support

The block RAM in Virgo devices supports the following write modes:

- WRITE_FIRST
- READ_FIRST
- NO_CHANGE

The BRAM configured as FIFO has following features:

- Synchronous or asynchronous mode
- First Word Fall Through (FWFT)
- Four push and pop side flags
    - Full/Empty
    - Full Minus 1 (almost full)/Empty Plus 1(almost empty)
    - Full/Empty Watermark – user specified watermark
    - Overrun/Underrun Error
- Push port supports 9- and 18-bit (and 36 bits for non-split) widths independent from pop width. (No byte enables).
- Pop port supports 9- and 18-bit (and 36 bits for non-split) widths independent from push width

Digital Signal Processing Blocks

Virgo incorporates dedicated Digital Signal Processor (DSP) blocks that are specifically designed to efficiently handle complex mathematical operations. These DSP blocks are equipped with multiply/accumulate functionality and associated logic, making them highly suitable for implementing a variety of mathematical functions, including finite impulse response (FIR) filters, fast Fourier transforms (FFT), and infinite impulse response (IIR) filters.

Some highlights of the DSP features include:

- 18x20-bit two's complement multiplier
- 64-bit accumulator
- Fracturable multiplier into two 9x10 multipliers each with 32-bit accumulator
- Full 38-bit output multiplied width
- Addition & Subtraction using accumulator (ACC+(A*B)) and (ACC-(A*B))
- Independent Signed and Unsigned operand support
- Right Shifting
- Rounding of shifted data
- Saturation (signed and unsigned) of shifted data
- Fixed Co-efficient support for FIR filtering
- Input and Output registration for pipelining

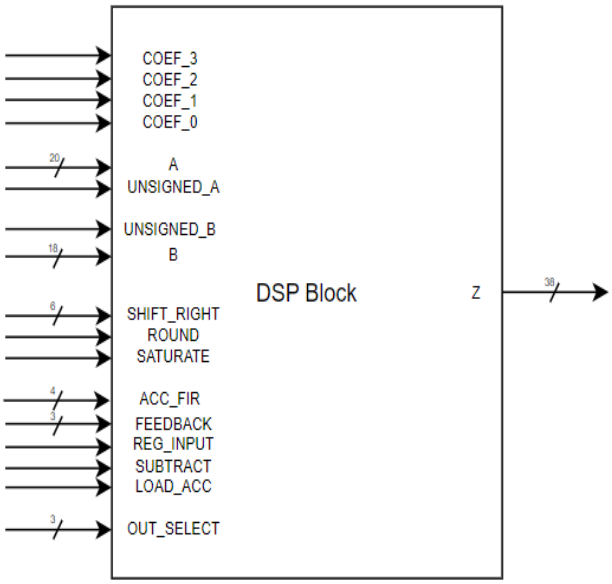

Figure 4: **Digital Signal Processor (DSP) Block**

The DSP supports both signed and unsigned operands of up to 72x72 bits producing an output of 144 bits. While multipliers in DSP support 20x18-bit operands, a wider implementation is achievable where DSP automatically generates the required additional logic.

Clock Network

Each IO bank has pins which can receive externally supplied clocks. These can route to SERDES/Gearbox functions in the IO banks directly, to PLLs as reference clocks, and/or directly to the FPGA fabric array.

There are multiple PLLs each of which can generate four different outputs with different divisors, using clock reference inputs from the IO banks. These outputs can drive functions in the IO banks and/or the clock trees in the FPGA fabric array.

The FPGA fabric array implements 16 global clock trees each of which can drive each resource in the array. The fabric array can forward these clocks to adjacent peripheral functions, possibly using FIFOs to manage data flow and phase relationships. Finally, the fabric array can produce generated clocks, which can be fed back to the array's clock trees.

I/O Complex (IOC)

The I/O complex in Virgo FPGA devices consists of two High Performance and four High Range I/O banks compliant with multiple high-speed Single-Ended and Differential I/O standards. The following subsections provide details on I/O features.

Each I/O bank supports 40 single ended I/Os. These I/Os can be configured as 20 differential pairs. Each bank contains dedicated clock capable pins.

I/O Types

The adaptable input/output (I/O) complex handles a range of connectivity offering a variety of I/O types, each best suited to a particular use case as follows:

- High-voltage I/O (HVIO) are dedicated I/O that supports the following 2.5V and 3.3V I/O standards:
  - LVCMOS: 8mA, 16mA
  - LVTTL
  - SSTL (Class I and II)
  - PCI 66
  - PCI-X 133
  - LVDS
  - LVPECL
  - BLVDS
  - RSDS

- High performance I/O (HPIO) operates at up to 1.5 GHz as SLVS (or 1.25 GHz without SLVS) and supports the following 1.2V through 1.8V standards:
  - LVCMOS 2mA, 4mA, 6mA, 8mA, 12mA, and 16mA
  - HSTL (Class I and II)
  - SSTL (Class I and II)
  - HSUL
  - POD
  - LVDS
  - DIFF_HSUL
  - DIFF_POD
  - SLVS
  - MIPI

I/O Distribution

The Virgo-28 FPGA device contains 272 dedicated and user configurable I/Os with distribution as follows:

1. Four High Range I/O bank contains a total of 160 I/Os
2. Two High Performance bank contains a total of 80 I/Os
3. Thirty-Two (32) dedicated configuration I/Os

Table 2: **Virgo FPGA I/O Pin Count per Device**

Device	I/O Type	F484A (0.8 mm) 19 x 19 mm
Virgo-28	Total	272
	HVIO	160
	HPIO	80
	Configuration I/O	32

* Package information being finalized for remaining Virgo family. Please reach out to us for further information at https://rapidsilicon.com/contact-us/

Pin Mapping

The following table describes the pins available in the Virgo-28 device and follows a specific nomenclature for identification.

Nomenclature

The programmable fabric GPIOs are named using the format below:
[BANK-TYPE]_[BANK-NUMBER]_[SE-IO-NUMBER]_[DIFFERENTIAL-PAIR-IO-NUMBER]_[P/N]

- HR = High Range Bank
- HR_X = The X represents the Bank Number. i.e. HR_1 mean HR Bank 1
- HR_X_Y = The Y represents the FPGA SE GPIO number
- HR_X_Y_Z = The Z represents FPGA GIO Differential Pair Number
- HR_X_Y_ZP = The differential pair positive terminal is identified by letter “P”
- HR_X_Y_ZN = The differential pair negative terminal is identified by letter “N”

Pin Table

Table 3: **Pin Specifications**

Pin No.	Pin Names	I/O	Function
A14	BOOT_CLK	I/O	System Reference Boot Clock
B15	BOOT_CLKSEL_0	I/O	Static pin
A15	BOOT_CLKSEL_1	I/O	Static pin
D13	BOOT_JTAG_TCK	I/O	JTAG Clock
C15	BOOT_JTAG_TDI	I/O	up to 40 Mbps
C14	BOOT_JTAG_TDO	I/O	up to 40 Mbps
D14	BOOT_JTAG_TMS	I/O	up to 40 Mbps
B13	BOOT_JTAG_TRSTN	I/O	up to 40 Mbps
D15	BOOT_M_0	I/O	Static pin
B16	BOOT_M_1	I/O	Static pin
C16	BOOT_M_2	I/O	Static pin
C13	BOOT_RST_N	I/O	Static pin

Pin No.	Pin Names	I/O	Function
A1 A4 A7 A10 A13 A16 A19 A22 AB1 AB4 AB7 AB10 AB13 AB16 AB19 AB22 D1 D22 G1 G22 K1 K22 N1 N22 T1 T22 W1 W22	No Connect	No Connection	No Connection

Pin No.	Pin Names	I/O	Function
AA2 AA3 AA7 AA8 AA15 AA16 AA20 AA21 B2 B3 B8 B14 B20 B21 D4 D5 D18 D19 E8 E11 E12 E15 F2 F6 F7 F9 F10 F11 F13 F14 F15 F16 F17 F21 G2 G8 G10 G11 G12 G13 G14 G15 G21 H4 H8 H9 H11 H13 H15 H19 J4	GND	GND	Shared digital and analog ground

Pin No.	Pin Names	I/O	Function
J6 J7 J8 J10 J12 J14 J16 J17 J19 K2 K7 K9 K11 K13 K15 K16 K21 K2 L6 L7 L8 L10 L12 L14 L15 L16 L17 L21 M6 M8 M9 M11 M13 M15 M17 N4 N7 N8 N10 N12 N14 N16 N19 P4 P7 P9 P11 P13 P15 P16 P19	GND	GND	Shared digital and analog ground

Pin No.	Pin Names	I/O	Function
R6 R8 R10 R12 R13 R14 R15 R17 T2 T7 T8 T9 T10 T11 T13 T14 T16 T21 U2 U8 U11 U12 U15 U21 V2 V21 W4 W5 W10 W13 W18 W19	GND	GND	Shared digital and analog ground
Y22	HP_1_0_0P	I/O	General Purpose I/O
AA22	HP_1_1_0N	I/O	General Purpose I/O
W21	HP_1_2_1P	I/O	General Purpose I/O
W20	HP_1_3_1N	I/O	General Purpose I/O
V16	HP_1_4_2P	I/O	General Purpose I/O
V17	HP_1_5_2N	I/O	General Purpose I/O
V18	HP_1_6_3P	I/O	General Purpose I/O
V19	HP_1_7_3N	I/O	General Purpose I/O
AB20	HP_1_8_4P	I/O	General Purpose I/O
AB21	HP_1_9_4N	I/O	General Purpose I/O
W17	HP_1_12_6P	I/O	General Purpose I/O
W16	HP_1_13_6N	I/O	General Purpose I/O
V15	HP_1_14_7P	I/O	General Purpose I/O
W15	HP_1_15_7N	I/O	General Purpose I/O

Pin No.	Pin Names	I/O	Function
Y18	HP_1_16_8P	I/O	General Purpose I/O
Y17	HP_1_17_8N	I/O	General Purpose I/O
Y19	HP_1_CC_18_9P	I/O	General Purpose I/O
AA19	HP_1_CC_19_9N	I/O	General Purpose I/O
AA17	HP_1_20_10P	I/O	General Purpose I/O
AA18	HP_1_21_10N	I/O	General Purpose I/O
AB18	HP_1_22_11P	I/O	General Purpose I/O
AB17	HP_1_23_11N	I/O	General Purpose I/O
Y16	HP_1_24_12P	I/O	General Purpose I/O
Y15	HP_1_25_12N	I/O	General Purpose I/O
V14	HP_1_26_13P	I/O	General Purpose I/O
W14	HP_1_27_13N	I/O	General Purpose I/O
Y14	HP_1_30_15P	I/O	General Purpose I/O
AA14	HP_1_31_15N	I/O	General Purpose I/O
AB12	HP_1_32_16P	I/O	General Purpose I/O
AA12	HP_1_33_16N	I/O	General Purpose I/O
Y13	HP_1_34_17P	I/O	General Purpose I/O
AA13	HP_1_35_17N	I/O	General Purpose I/O
Y12	HP_1_36_18P	I/O	General Purpose I/O
W12	HP_1_37_18N	I/O	General Purpose I/O
V13	HP_1_CC_38_19P	I/O	General Purpose I/O
V12	HP_1_CC_39_19N	I/O	General Purpose I/O
Y20	HP_1_10_5P	I/O	General Purpose I/O
Y21	HP_1_11_5N	I/O	General Purpose I/O
AB14	HP_1_28_14P	I/O	General Purpose I/O
AB15	HP_1_29_14N	I/O	General Purpose I/O
Y11	HP_2_0_0P	I/O	General Purpose I/O
W11	HP_2_1_0N	I/O	General Purpose I/O
AA10	HP_2_2_1P	I/O	General Purpose I/O
Y10	HP_2_3_1N	I/O	General Purpose I/O
AA11	HP_2_4_2P	I/O	General Purpose I/O
AB11	HP_2_5_2N	I/O	General Purpose I/O
AA9	HP_2_6_3P	I/O	General Purpose I/O
Y9	HP_2_7_3N	I/O	General Purpose I/O
W9	HP_2_8_4P	I/O	General Purpose I/O
V9	HP_2_9_4N	I/O	General Purpose I/O
Y7	HP_2_12_6P	I/O	General Purpose I/O
Y8	HP_2_13_6N	I/O	General Purpose I/O
AB5	HP_2_14_7P	I/O	General Purpose I/O

Pin No.	Pin Names	I/O	Function
AB6	HP_2_15_7N	I/O	General Purpose I/O
Y4	HP_2_16_8P	I/O	General Purpose I/O
AA4	HP_2_17_8N	I/O	General Purpose I/O
AA6	HP_2_CC_18_9P	I/O	General Purpose I/O
AA5	HP_2_CC_19_9N	I/O	General Purpose I/O
Y5	HP_2_20_10P	I/O	General Purpose I/O
Y6	HP_2_21_10N	I/O	General Purpose I/O
AB8	HP_2_22_11P	I/O	General Purpose I/O
AB9	HP_2_23_11N	I/O	General Purpose I/O
W7	HP_2_24_12P	I/O	General Purpose I/O
W6	HP_2_25_12N	I/O	General Purpose I/O
V8	HP_2_26_13P	I/O	General Purpose I/O
W8	HP_2_27_13N	I/O	General Purpose I/O
AB2	HP_2_30_15P	I/O	General Purpose I/O
AB3	HP_2_31_15N	I/O	General Purpose I/O
W2	HP_2_32_16P	I/O	General Purpose I/O
W3	HP_2_33_16N	I/O	General Purpose I/O
V7	HP_2_34_17P	I/O	General Purpose I/O
V6	HP_2_35_17N	I/O	General Purpose I/O
AA1	HP_2_36_18P	I/O	General Purpose I/O
Y1	HP_2_37_18N	I/O	General Purpose I/O
V5	HP_2_CC_38_19P	I/O	General Purpose I/O
V4	HP_2_CC_39_19N	I/O	General Purpose I/O
V11	HP_2_10_5P	I/O	General Purpose I/O
V10	HP_2_11_5N	I/O	General Purpose I/O
Y3	HP_2_28_14P	I/O	General Purpose I/O
Y2	HP_2_29_14N	I/O	General Purpose I/O
U16	HP_RCAL_1	I/O	General Purpose I/O
U7	HP_RCAL_2	I/O	General Purpose I/O
U20	HR_1_0_0P	I/O	General Purpose I/O
V20	HR_1_1_0N	I/O	General Purpose I/O
V22	HR_1_2_1P	I/O	General Purpose I/O
U22	HR_1_3_1N	I/O	General Purpose I/O
U17	HR_1_4_2P	I/O	General Purpose I/O
U18	HR_1_5_2N	I/O	General Purpose I/O
R22	HR_1_6_3P	I/O	General Purpose I/O
P22	HR_1_7_3N	I/O	General Purpose I/O
T19	HR_1_8_4P	I/O	General Purpose I/O
U19	HR_1_9_4N	I/O	General Purpose I/O

Pin No.	Pin Names	I/O	Function
T20	HR_1_12_6P	I/O	General Purpose I/O
R20	HR_1_13_6N	I/O	General Purpose I/O
R18	HR_1_14_7P	I/O	General Purpose I/O
R19	HR_1_15_7N	I/O	General Purpose I/O
R21	HR_1_16_8P	I/O	General Purpose I/O
P21	HR_1_17_8N	I/O	General Purpose I/O
L22	HR_1_CC_18_9P	I/O	General Purpose I/O
M22	HR_1_CC_19_9N	I/O	General Purpose I/O
P20	HR_1_20_10P	I/O	General Purpose I/O
N20	HR_1_21_10N	I/O	General Purpose I/O
N21	HR_1_22_11P	I/O	General Purpose I/O
M21	HR_1_23_11N	I/O	General Purpose I/O
M20	HR_1_24_12P	I/O	General Purpose I/O
L20	HR_1_25_12N	I/O	General Purpose I/O
P18	HR_1_26_13P	I/O	General Purpose I/O
P17	HR_1_27_13N	I/O	General Purpose I/O
M18	HR_1_30_15P	I/O	General Purpose I/O
M19	HR_1_31_15N	I/O	General Purpose I/O
H22	HR_1_32_16P	I/O	General Purpose I/O
J22	HR_1_33_16N	I/O	General Purpose I/O
J21	HR_1_34_17P	I/O	General Purpose I/O
H21	HR_1_35_17N	I/O	General Purpose I/O
K20	HR_1_36_18P	I/O	General Purpose I/O
K19	HR_1_37_18N	I/O	General Purpose I/O
L19	HR_1_CC_38_19P	I/O	General Purpose I/O
L18	HR_1_CC_39_19N	I/O	General Purpose I/O
T18	HR_1_10_5P	I/O	General Purpose I/O
T17	HR_1_11_5N	I/O	General Purpose I/O
N17	HR_1_28_14P	I/O	General Purpose I/O
N18	HR_1_29_14N	I/O	General Purpose I/O
J20	HR_2_0_0P	I/O	General Purpose I/O
H20	HR_2_1_0N	I/O	General Purpose I/O
E22	HR_2_2_1P	I/O	General Purpose I/O
F22	HR_2_3_1N	I/O	General Purpose I/O
C22	HR_2_4_2P	I/O	General Purpose I/O
B22	HR_2_5_2N	I/O	General Purpose I/O
D21	HR_2_6_3P	I/O	General Purpose I/O
E21	HR_2_7_3N	I/O	General Purpose I/O
K18	HR_2_8_4P	I/O	General Purpose I/O

Pin No.	Pin Names	I/O	Function
K17	HR_2_9_4N	I/O	General Purpose I/O
C20	HR_2_12_6P	I/O	General Purpose I/O
C21	HR_2_13_6N	I/O	General Purpose I/O
D20	HR_2_14_7P	I/O	General Purpose I/O
E20	HR_2_15_7N	I/O	General Purpose I/O
J18	HR_2_16_8P	I/O	General Purpose I/O
H18	HR_2_17_8N	I/O	General Purpose I/O
F19	HR_2_CC_18_9P	I/O	General Purpose I/O
G19	HR_2_CC_19_9N	I/O	General Purpose I/O
E18	HR_2_20_10P	I/O	General Purpose I/O
E19	HR_2_21_10N	I/O	General Purpose I/O
G18	HR_2_22_11P	I/O	General Purpose I/O
F18	HR_2_23_11N	I/O	General Purpose I/O
H17	HR_2_24_12P	I/O	General Purpose I/O
G17	HR_2_25_12N	I/O	General Purpose I/O
A21	HR_2_26_13P	I/O	General Purpose I/O
A20	HR_2_27_13N	I/O	General Purpose I/O
C18	HR_2_30_15P	I/O	General Purpose I/O
B18	HR_2_31_15N	I/O	General Purpose I/O
C17	HR_2_32_16P	I/O	General Purpose I/O
B17	HR_2_33_16N	I/O	General Purpose I/O
E17	HR_2_34_17P	I/O	General Purpose I/O
D17	HR_2_35_17N	I/O	General Purpose I/O
A18	HR_2_36_18P	I/O	General Purpose I/O
A17	HR_2_37_18N	I/O	General Purpose I/O
D16	HR_2_CC_38_19P	I/O	General Purpose I/O
E16	HR_2_CC_39_19N	I/O	General Purpose I/O
G20	HR_2_10_5P	I/O	General Purpose I/O
F20	HR_2_11_5N	I/O	General Purpose I/O
C19	HR_2_28_14P	I/O	General Purpose I/O
B19	HR_2_29_14N	I/O	General Purpose I/O
U3	HR_3_0_0P	I/O	General Purpose I/O
V3	HR_3_1_0N	I/O	General Purpose I/O
U1	HR_3_2_1P	I/O	General Purpose I/O
V1	HR_3_3_1N	I/O	General Purpose I/O
U6	HR_3_4_2P	I/O	General Purpose I/O
U5	HR_3_5_2N	I/O	General Purpose I/O
R1	HR_3_6_3P	I/O	General Purpose I/O
P1	HR_3_7_3N	I/O	General Purpose I/O

Pin No.	Pin Names	I/O	Function
U4	HR_3_8_4P	I/O	General Purpose I/O
T4	HR_3_9_4N	I/O	General Purpose I/O
T3	HR_3_12_6P	I/O	General Purpose I/O
R3	HR_3_13_6N	I/O	General Purpose I/O
R5	HR_3_14_7P	I/O	General Purpose I/O
R4	HR_3_15_7N	I/O	General Purpose I/O
R2	HR_3_16_8P	I/O	General Purpose I/O
P2	HR_3_17_8N	I/O	General Purpose I/O
M1	HR_3_CC_18_9P	I/O	General Purpose I/O
L1	HR_3_CC_19_9N	I/O	General Purpose I/O
N3	HR_3_20_10P	I/O	General Purpose I/O
P3	HR_3_21_10N	I/O	General Purpose I/O
M2	HR_3_22_11P	I/O	General Purpose I/O
N2	HR_3_23_11N	I/O	General Purpose I/O
M3	HR_3_24_12P	I/O	General Purpose I/O
L3	HR_3_25_12N	I/O	General Purpose I/O
P6	HR_3_26_13P	I/O	General Purpose I/O
P5	HR_3_27_13N	I/O	General Purpose I/O
M4	HR_3_30_15P	I/O	General Purpose I/O
M5	HR_3_31_15N	I/O	General Purpose I/O
H1	HR_3_32_16P	I/O	General Purpose I/O
J1	HR_3_33_16N	I/O	General Purpose I/O
H2	HR_3_34_17P	I/O	General Purpose I/O
J2	HR_3_35_17N	I/O	General Purpose I/O
K4	HR_3_36_18P	I/O	General Purpose I/O
K3	HR_3_37_18N	I/O	General Purpose I/O
L5	HR_3_CC_38_19P	I/O	General Purpose I/O
L4	HR_3_CC_39_19N	I/O	General Purpose I/O
T5	HR_3_10_5P	I/O	General Purpose I/O
T6	HR_3_11_5N	I/O	General Purpose I/O
N5	HR_3_28_14P	I/O	General Purpose I/O
N6	HR_3_29_14N	I/O	General Purpose I/O
J3	HR_4_0_0P	I/O	General Purpose I/O
H3	HR_4_1_0N	I/O	General Purpose I/O
E1	HR_4_2_1P	I/O	General Purpose I/O
F1	HR_4_3_1N	I/O	General Purpose I/O
C1	HR_4_4_2P	I/O	General Purpose I/O
B1	HR_4_5_2N	I/O	General Purpose I/O
E2	HR_4_6_3P	I/O	General Purpose I/O
D2	HR_4_7_3N	I/O	General Purpose I/O

Pin No.	Pin Names	I/O	Function
F3	HR_4_8_4P	I/O	General Purpose I/O
G3	HR_4_9_4N	I/O	General Purpose I/O
C3	HR_4_12_6P	I/O	General Purpose I/O
C2	HR_4_13_6N	I/O	General Purpose I/O
D3	HR_4_14_7P	I/O	General Purpose I/O
E3	HR_4_15_7N	I/O	General Purpose I/O
H5	HR_4_16_8P	I/O	General Purpose I/O
J5	HR_4_17_8N	I/O	General Purpose I/O
G4	HR_4_CC_18_9P	I/O	General Purpose I/O
F4	HR_4_CC_19_9N	I/O	General Purpose I/O
E5	HR_4_20_10P	I/O	General Purpose I/O
E4	HR_4_21_10N	I/O	General Purpose I/O
G5	HR_4_22_11P	I/O	General Purpose I/O
F5	HR_4_23_11N	I/O	General Purpose I/O
H6	HR_4_24_12P	I/O	General Purpose I/O
G6	HR_4_25_12N	I/O	General Purpose I/O
A2	HR_4_26_13P	I/O	General Purpose I/O
A3	HR_4_27_13N	I/O	General Purpose I/O
C5	HR_4_30_15P	I/O	General Purpose I/O
B5	HR_4_31_15N	I/O	General Purpose I/O
C6	HR_4_32_16P	I/O	General Purpose I/O
B6	HR_4_33_16N	I/O	General Purpose I/O
D6	HR_4_34_17P	I/O	General Purpose I/O
E6	HR_4_35_17N	I/O	General Purpose I/O
A5	HR_4_36_18P	I/O	General Purpose I/O
A6	HR_4_37_18N	I/O	General Purpose I/O
E7	HR_4_CC_19P	I/O	General Purpose I/O
D7	HR_4_CC_19N	I/O	General Purpose I/O
K5	HR_4_10_5P	I/O	General Purpose I/O
K6	HR_4_11_5N	I/O	General Purpose I/O
B4	HR_4_28_14P	I/O	General Purpose I/O
C4	HR_4_29_14N	I/O	General Purpose I/O
D11	BOOT_CONFIG_DONE_GPIO_0	I/O	Up to 200 Mbps
C11	BOOT_CONFIG_ERROR_GPIO_1	I/O	Up to 200 Mbps
C12	BOOT_GPT_RTC	I/O	Single-ended clock pin (32.768 KHz)
B12	BOOT_I2C_SCL	I/O	Single-ended clock pin (1 MHz)
C9	BOOT_I2C_SDA_GPIO_9	I/O	Up to 1 Mbps
C8	BOOT_PWM0_GPIO_10	I/O	Up to 200 Mbps
A8	BOOT_PWM1_GPIO_11	I/O	Up to 200 Mbps
A9	BOOT_PWM2_GPIO_12	I/O	Up to 200 Mbps

Pin No.	Pin Names	I/O	Function
B7	BOOT_PWM3_GPIO_13	I/O	Up to 200 Mbps
B10	BOOT_SPI_CS_GPIO_4	I/O	Up to 200 Mbps
D10	BOOT_SPI_DQ2_GPIO_7	I/O	Up to 200 Mbps
B9	BOOT_SPI_DQ3_GPIO_8	I/O	Up to 200 Mbps
C10	BOOT_SPI_MISO_DQ1_GPIO_6	I/O	Up to 200 Mbps
D9	BOOT_SPI_MOSI_DQ0_GPIO_5	I/O	Up to 200 Mbps
A12	BOOT_SPI_SCLK	I/O	Single-ended clock pin (100 MHz)
D8	BOOT_UART_CTS_GPIO_14	I/O	Up to 200 Mbps
C7	BOOT_UART_RTS_GPIO_15	I/O	Up to 200 Mbps
A11	BOOT_UART_RX_GPIO_3	I/O	Up to 200 Mbps
B11	BOOT_UART_TX_GPIO_2	I/O	Up to 200 Mbps
D12	TESTMODE	I/O	static pin
T15	VCC_AUX	PWR	Analog 1.8V
R9	VCC_AUX	PWR	Analog 1.8V
G9	VCC_AUX	PWR	Analog 1.8V
E13 E14	VCC_BOOT_IO	PWR	1.2/1.5/1.8V
H10 H12 H14 J9 J11 J13 K10 K12 K14 L9 L11 L13 M10 M12 M14 N9 N11 N13 P10 P12 P14	VCC_CORE	PWR	Core supply 0.8V
R11	VCC_HP_AUX	PWR	Analog 1.8V
U13 U14	VCC_HP_IO_1	PWR	1.2/1.5/1.8V
U9 U10	VCC_HP_IO_2	PWR	1.2/1.5/1.8V
N15	VCC_HR_AUX_1	PWR	Analog 1.8V
J15	VCC_HR_AUX_2	PWR	Analog 1.8V

Pin No.	Pin Names	I/O	Function
P8	VCC_HR_AUX_3	PWR	Analog 1.8V
K8	VCC_HR_AUX_4	PWR	Analog 1.8V
M16 R16	VCC_HR_IO_1	PWR	1.8/2.5/3.3V
G16 H16	VCC_HR_IO_2	PWR	1.8/2.5/3.3V
M7 R7	VCC_HR_IO_3	PWR	1.8/2.5/3.3V
G7 H7	VCC_HR_IO_4	PWR	1.8/2.5/3.3V
F12	VCC_PUF_PVT_OSC_BOOT_AUX	PWR	Analog 1.8V
T12	VCC_RC_OSC_FABRIC	PWR	Analog 1.8V
E9 E10	VCC_BOOT_IO	PWR	1.2/1.5/1.8V
F8	VCC_BOOT_AUX	PWR	Analog 1.8V

Q(SPI) Controller

The SPI controller is a part of the standard communication interface set. It can be used by the boot processor as well as by the FPGA logic. Some of the features of the SPI port include:

- Supports 1 device (1 select line)
- 3 modes of operation: indirect, memory-mapped and status flag polling. Memory-mapped mode allows direct booting from external flash memory
- Programmable data rate via clock dividers
- Quad I/O mode
- RX/TX FIFO length is 16 words
- Direct I/O mode
- Memory-mapped read accesses on the AHB bus
- Support SPI Slave mode
- Default value: CS2CLK = 0, CSHT = 2, SCLKDIV = 1
- 32-bit 133 MHz AHB slave port for memory-mapped external device access

DMA Controller

The Direct Memory Access Controller (DMAC) transfers data efficiently between devices on the AMBA® AHB™ bus. Some features of the DMA controller include:

- Available for use from system start
- Compliant with AMBA 2 AHB protocol specification
- Supports memory-to-memory, peripheral-to-memory, memory-to-peripheral transfers with scatter-gather support
- Support of round-robin arbitration with 2 priority levels
- Support of chain transfer
- 1 configurable DMA cores
- 8 DMA channels
- 9 DMA request/acknowledge pairs for hardware handshake
- 1 AHB master port for data transfers
- AHB address width: 32 bits
- AHB data width: 32 bits
- AHB 32-bit slave port for configuration
- One AHB 32-bit master port for embedded DMA engine
- 1-bit external interrupt signal

I2C Controller

The Inter-Integrated Circuit (I2C) Controller is a widely used communication interface designed for connecting low-speed peripherals. It is accessible by both the boot processor and the FPGA logic, ensuring flexible integration and control. Key features of the I2C Controller include:

- 3 speed modes from 100 Kbps to 1 Mbps
- 7- or 10-bit addressing mode
- Programmable master/slave mode
- Auto clock stretching
- Programmable clock/data timing
- Built-in DMA trigger
- Rx and Tx buffers with depth of 16 bytes
- Buffers implemented as FF FIFOs
- 32-bit APB slave port

UART Controller

The Universal Asynchronous Receiver/Transmitter (UART) controller is a critical component of the standard communication interface set, facilitating serial communication. It can be accessed both by the boot processor and the FPGA logic, making it highly versatile for various applications. Key features of the UART controller include:

- Two independent UART ports
- Programmable baud rates up to 128 Kbps

- Fractional baud rate support
- Programmable character widths of 5, 6, 7, or 8 bits per character
- Programmable 1, 1.5, and 2 STOP bit generation
- Programmable FIFO mode
- Programmable auto flow control using CTS, RTS signal
- Built-in DMA trigger
- Internal buffer with depth of 32 lines

General Purpose Timer

The General Purpose Timer provides versatile timing and counting functionalities essential for various applications. Some of the features of the general-purpose timer include:

- Multi-functional timer with 6 modes:
  - One 32-bit timer
  - Two 16-bit timers
  - Four 8-bit timers
  - One 16-bit Pulse Width Modulator (PWM)
  - One 16-bit timer and one 8-bit PWM
  - Two 8-bit timers and one 8-bit PWM
- Programmable source of timer clock
- External input pins for events/periods count
- Four multi-function timers in one module
- 32-bit APB slave port
- External real-time clock source

Configuration and Boot Control

The boot-up and configuration of the Virgo FPGA are managed by a dedicated boot processor core, specifically designed for executing the boot procedure. The boot mode is determined by three external pins, which are read during power-up to identify the boot source. Upon reset, the Boot CPU (BCPU) begins executing code from the Boot ROM at the location indicated by the three external boot select pins. The supported boot modes are JTAG and SPI Flash Mode, which are defined as follows:

- **JTAG Mode:** When the JTAG mode is selected, the host configuration software on the PC downloads the bootloader into the On-Chip Memory (OCM) of the Boot CPU. The BCPU then executes the bootloader, configuring the FPGA bitstream received along with the boot code. In JTAG mode, there's also an option to program the SPI flash with both the bootloader and the FPGA bitstream

- **SPI Flash Mode:** When the boot mode is set to SPI flash mode, the processor loads the bitstream and the bootloader from the SPI flash into the On-Chip Memory (OCM) and then executes it. The clock in the SPI flash mode is provided by Virgo. The SPI flash must be programmed before setting the Virgo BOOT_MODE pins to "SPI Flash Boot Mode". The on-board SPI flash may be programed using the JTAG mode.

Table 4: **Provides the boot pin configuration for boot mode selection.**

Boot Mode / Boot Pin	BOOT_M_0	BOOT_M_1	BOOT_M_2
JTAG	0	0	0
SPI Boot	0	0	1
Reserved	All other settings are reserved		

Security

- Secure firmware bootup
- Support for chain of trust, with BootRom as the root of trust
- Device Life Cycle Management supported using OTP bits
- FSBL (First Stage Boot Loader) and FPGA bitstream authentication and encryption/decryption supported
- Public Key Cryptography ECDSA 256 and RSA 2048
- Private Key Cryptography AES-128 CCM mode and AES-256 CCM mode
- Secure Hash SHA256

Electrical Characteristics

Table 5: **Electrical Characteristics**

Pin Name	Voltage	Voltage Range (V)	Comments
V_{CC_CORE}	0.8V	(+/- 5%) 0.76 – 0.84	Virgo-TC Core logic voltage supply
$V_{CC\_OLED,Dr}$	16.0V	(+/- 3%) 15.5 – 16.5	OLED driving voltage. Derived from 12V input supply
$VCC_{\_OLED\_3P3}$	3	(+/- 3%) 2.5 – 3.5	OLED Logic Power supply
V_{PWR_IN}	12.0V	(+/- 5%) 4.75 – 5.25	Direct 12V from power barrel.
$V_{CC\_BOOT\_IO}$	1.8/3.3V	(+/- 5%) 1.710 – 1.890	IO Bank 0 (BOOT) supply.
		(+/- 5%) 3.135 – 3.465	SoC GPIO supply
$V_{CC\_HP\_IO\_1}$	1.2/1.5/1.8V	(+/- 5%) 1.140 – 1.260	Selectable voltage for HP IO Bank 1 (FPGA HP bank 1) supply. A dedicated power plane shall be used.
		(+/- 5%) 1.425 – 1.575	
		(+/- 5%) 1.710 – 1.890	
$V_{CC\_HP\_IO\_2}$	1.2/1.5/1.8V	(+/- 5%) 1.140 – 1.260	Selectable voltage for HP IO Bank 2 (FPGA HP bank 2) supply. A dedicated power plane shall be used.
		(+/- 5%) 1.425 – 1.575	
		(+/- 5%) 1.710 – 1.890	
$V_{CC\_HR\_IO\_1}$	1.8/2.5/3.3V	(+/- 5%) 1.710 – 1.890	Selectable voltage for HR IO Bank 1 (FPGA HR bank 1) supply. A dedicated power plane shall be used.
		(+/- 5%) 2.375 – 2.625	
		(+/- 5%) 3.135 – 3.465	

Pin Name	Voltage	Voltage Range (V)	Comments
$V_{CC\_HR\_IO\_2}$	1.8/2.5/3.3V	(+/- 5%) 1.710 – 1.890	Selectable voltage for HR IO Bank 2 (FPGA HR bank 2) supply. A dedicated power plane shall be used.
		(+/- 5%) 2.375 – 2.625	
		(+/- 5%) 3.135 – 3.465	
$V_{CC\_HR\_IO\_3}$	1.8/2.5/3.3V	(+/- 5%) 1.710 – 1.890	Selectable voltage for HR IO Bank 3 (FPGA HR bank 3) supply. A dedicated power plane shall be used.
		(+/- 5%) 2.375 – 2.625	
		(+/- 5%) 3.135 – 3.465	
$V_{CC\_HR\_IO\_4}$	1.8/2.5/3.3V	(+/- 5%) 1.710 – 1.890	Selectable voltage for HR IO Bank 4 (FPGA HR bank 4) supply. A dedicated power plane shall be used.
		(+/- 5%) 2.375 – 2.625	
		(+/- 5%) 3.135 – 3.465	
V_{CC_AUX}	1.8V	(+/- 5%) 1.710 – 1.890	1.8V auxiliary bank power supply. A dedicated power plane shall be used.
$V_{CC\_BOOT\_AUX}$	1.8V	(+/- 5%) 1.710 – 1.890	1.8V auxiliary bank power supply. This power plane may be combined with V_{CC_AUX}.
$V_{CC\_HR\_AUX[1:4]}$	1.8V	(+/- 5%) 1.710 – 1.890	1.8V auxiliary bank power supply. This power plane may be combined with V_{CC_AUX}.

Ordering Information

Figure 5 shows the ordering information for the Virgo devices.

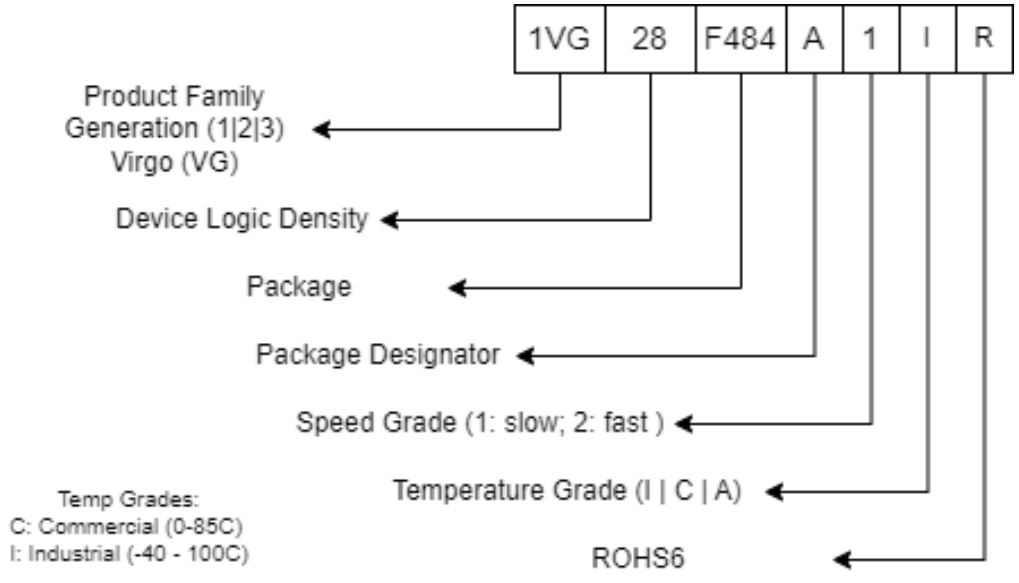

Figure 5: **Ordering Information**

Revision History

Revision	Date	Description
1.1	06-15-2024	Updated Version of the Datasheet
1.0	05-31-2024	Initial release of Virgo Datasheet

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