Lab Assignment 10

A Single-Cycle Implementation of the Datapath and Controller for a Reduced MIPS Instruction Set

1 Lab Tasks

a) You are required to describe a single-cycle data path and controller in Verilog for the following MIPS insruction set:

   (a) R Type: add, sub, or, xor, and, slt, sltu, jr.

   (b) I Type: addi, ori, andi, slti, lw, sw, beq, bneq.

   (c) J Type: j.

   A reference for different machine code fields corresponding to different instructions is given in WIKIPEDIA: MIPS Assembly Reference.

b) Write first the assembly code and then the machine code for a program that computes the greatest common divisor (GCD) of two numbers present in the main memory (not the register file) using the algorithm given below and stores the GCD in the register file as well as main memory.

```
done = 0;
A = First Number
B = Second Nubmer
while(!done ){
    if ( A < B ) swap A and B;
    else if ( B != 0 ) A = A - B;
    else done = 1;
}
Y = A
```

Use `initial` blocks with `readmemh` in the behavioral models of instruction memory and main memory to initialize them to your machine code for the GCD algorithm and two input numbers, respectively. The example of how to initialize memories is attached in the lab assignment post (thanks to Sajjad Ahmed and another student I don't know the name of for figuring out the synthesis problem with memories and its solution).

Use some instruction from the instruction set to stop the program counter at the end of your program.

c) Test the assembly code in ModelSim and check the register file's contents in ModelSim's memory view section. For a tutorial on how to do this, please follow ModelSim Tutorial, page 54.

d) Tie 16 LSBs of register file's `data1` port to seven-segment displays. Tie `ReadAddress1` port of the register file to switches through a multiplexer to allow either the processor or the user to take control of the port. You should not test seven-segment display driver in your test benches.

2 Questions

Answer the following questions:

a) Read the synthesis report and identify how many resources in the FPGA such as lookup tables (LUTs), input/output (IOs), etc., has been utilized. Is this resource usage equal to the resource usage of the circuit you designed on paper?

b) Burn the code on Spartan 3 board. After the execution of the GCD program, use a switch to provide address of different registers of the register file and display their contents on the seven-segment displays. Since only 16 LSBs of the register file output port is connected to seven-segment displays, only use numbers less than 2^{16} in main memory for testing the GCD code.

3 Instructions

a) A written report is required for this lab. The report should include the following:

   (a) A hand-sketched design partition of the system that clearly shows the datapath and the controller. The datapath may include multiplexers, demultiplexers, encoders, decoders, flip-flops, and should avoid gates as much as possible.

   (b) The device resource utilization summary from the synthesis report.

b) It is recommended that you bring your simulation in your laptop so that you can quickly get your assignment partially graded. Otherwise, you will have to share the computer in the lab and may have to wait. However, you will need to transfer your code to the lab computer using USB anyway for the synthsis and downloading the code to the FPGA.

c) The collaboration among students is encouraged, but blind code sharing/-copying is not allowed. If you are unable to explain anything in your code, it will be assumed you have copied it blindly. So make sure you know every thing you have written in your code. I am least concerned about how you have learnt something as long as you have learnt it well.