EEE3096S - Tutorial 4
Memo
2023

DAC Metrics [10 Marks]

1. The digital input 10100_2 is equal to decimal 20. Since V_{OUT} = 10 mV for this case, the proportionality factor as 0.5 mV. Thus, we can find for a digital input such as $11101_2 = 29_{10}$ as follows: V_{OUT} = (0.5 mV) × 29 = 14.5 mV. [5 Marks]
2. The step size is 10 mV/(2^{12} – 1) = 2.44 µV. Since $100000000000_2 = 2048_{10}$, the ideal output should be 2048 × 2.44 µV. The error can be as much as ± 0.5% × 10 mV = ± 0.05 mV. Thus, the actual output can deviate by this amount from the ideal 4.997 mV, so the actual output can be anywhere from 4.947 mV to 5.047 mV. **Note to markers**: consider rounding errors. [5 Marks]

DAC Design [15 Marks]

1. $Resolution_{PWM} = \frac{\log_{10}(\frac{F_{CLK}}{F_{PWM}})}{\log_{10}(2)}\ [Bits]$

   $10 = \frac{\log_{10}(72000000/X)}{\log_{10}(2)}$

   $10 * \log_{10}(2) = \log_{10}(72000000/X)$

   $10^{10*\log_{10}(2)} = 72000000/X$

   $X = \frac{72000000}{10^{10*\log_{10}(2)}} =$ **70312.5 Hz** [4 Marks]
2. $F_{PWM} = \frac{F_{CLK}}{(\text{ARR}+1)(\text{PSC}+1)}\ [Hz]$

   Let PSC = 0, then ARR = 1023 for F_{PWM} = 70.3 kHz [1 Mark]

3. http://sim.okawa-denshi.jp/en/OPseikiLowkeisan.htm

   Above link is an online filter design tool that can aid with marking.
   - Cut-off frequency should be between 5 kHz and 0.5*F_{PWM} [1 Mark]
   - Resistor and Capacitor values should be reasonable and from E12 series (or a combination thereof). [2 Marks]
   - Showing calculations [2 Marks]
   - Plots and circuit diagram [5 Marks]