EEE3096S: Embedded Systems II

LECTURE 17:

THE ADC (PART 2)

METRICS

Presented by:

STANLEY MBEWE

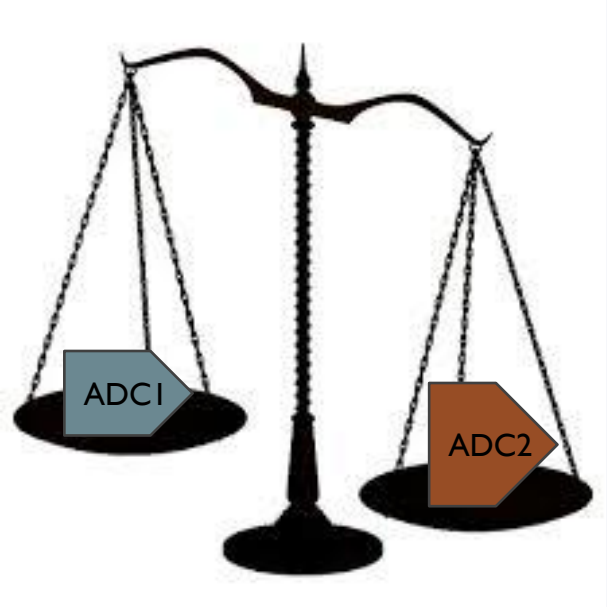
Electrical Engineering
University of Cape Town

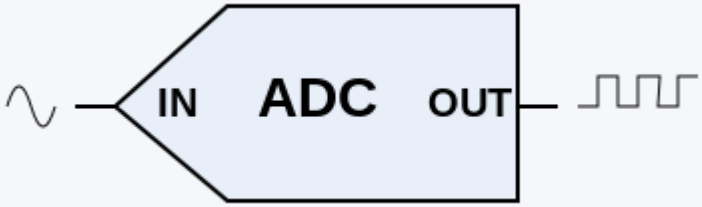
OUTLINE OF LECTURE

- ADC Resolution
- ADC/DAC Quantization
- Static Metric of an ADC
- Dynamic Metrics of an ADC

This presentation contains some slides adapted from course textbook "Embedded System Design Embedded Systems Foundations of Cyber-Physical Systems, and the Internet of Things" by Peter Marwedel

ADC Metrics





Analogue to Digital Convertors (ADCs)

ADC RESOLUTION

Resolution (in bits) : number of bits produced (2^n)

Resolution Q (in volts): difference between two input voltages causing the output to be incremented by 1 *

$$Q = \frac{V_{FSR}}{n}$$ (quantitation factor calculation)

where:

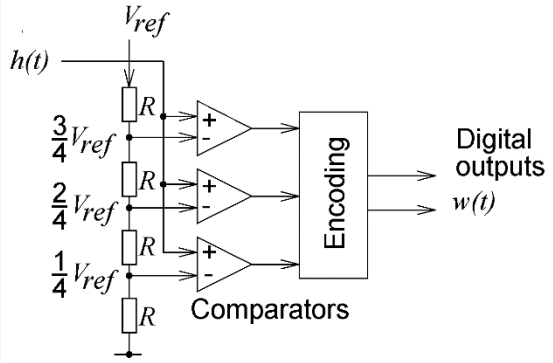
Q: resolution in volts per step

V_{FSR}: difference between largest and smallest voltage (Full Scale Range)

n: number of voltage intervals

Example:

$Q = V_{ref}/4$ for this flash ADC example

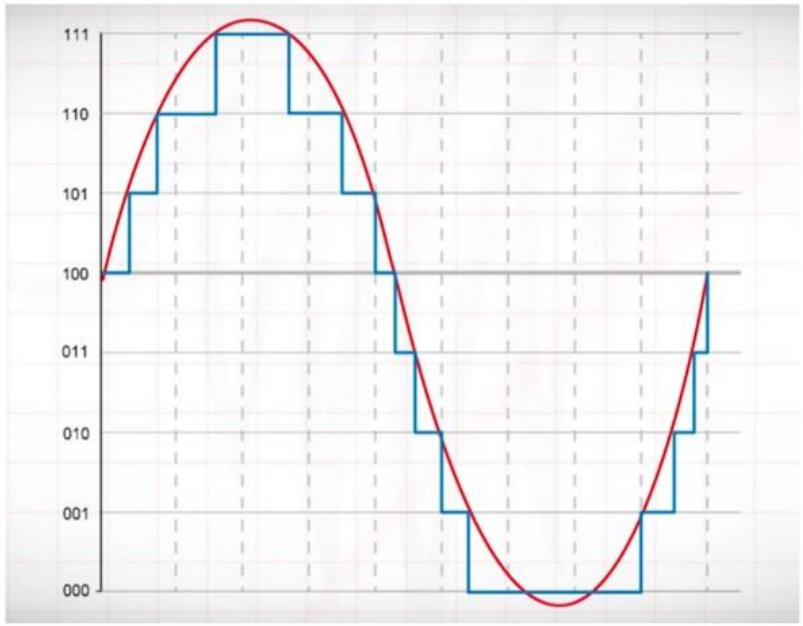


* i.e. this can be found practically using a voltage source that can be finely adjusted and see when the ADC value changes by 1. Obviously would need a little program running to somehow show the ADC's current reading.

Information source [1]: https://en.wikipedia.org/wiki/Analog-to-digital_converter

ADC/DAC QUANTIZATION

Quantization: Mapping analogue voltages to digital codes



3-bit ADC Digital Output Code Table

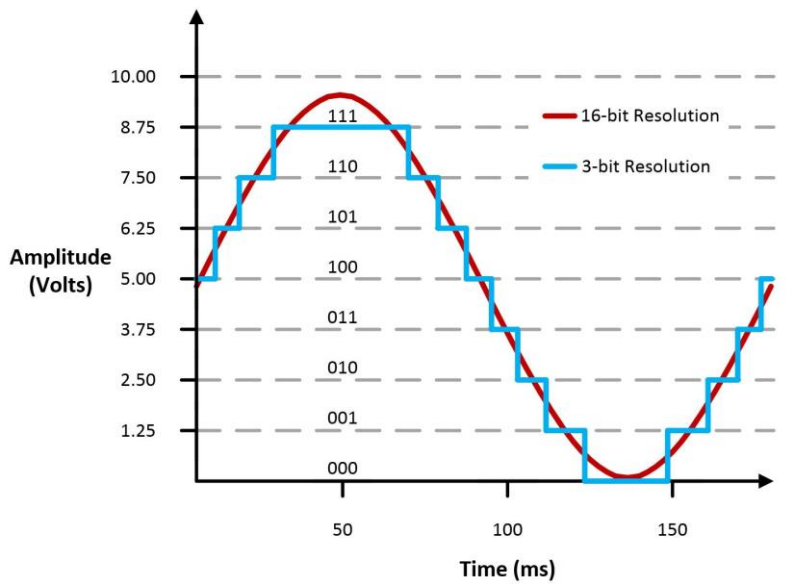
Analog Input Range (Normalized to V_{REF})	Digital Output Code
7/8 -> 8/8	111
6/8 -> 7/8	110
5/8 -> 6/8	101
4/8 -> 5/8	100
3/8 -> 4/8	011
2/8 -> 3/8	010
1/8 -> 2/8	001
0 -> 1/8	000

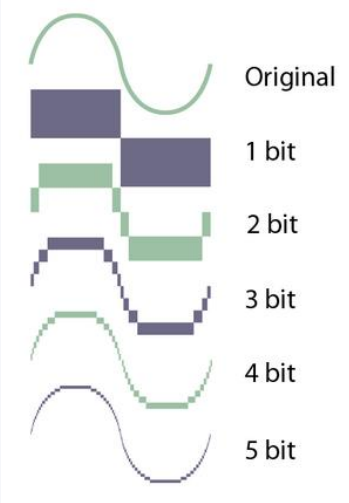
}1LSB Difference

Recommended video: https://www.youtube.com/watch?v=xX6ifWthjDA

RESOLUTION OF AN ADC

$$Number\ of\ Unique\ Codes = 2^N\ , where\ N\ is\ the\ number\ of\ bits$$





This answers the question "how many voltage levels can your ADC or DAC quantize?" i.e. the answer to this question would be 2^N in this case.

The resolution of an ADC or DAC is the number of bits, i.e. N, *not* 2^N.

RESOLUTION OF AN ADC

Source: https://www.youtube.com/watch?app=desktop&v=4EdKNahdJmU

Static Metrics

THE STATIC METRIC OF AN ADC

- The simplest but also very important ADC performance metrics is the
  - Static, DC (direct current, or zero-frequency constant input) performance of the devices.
  - i.e. does it read 0 when the input is 0V? *

* Note: you may need to interpret this differently depending on how your ADC is configure. For example, sometimes the configuration is such that 0 is output for –Vmax and 2^N-1 for +Vmax… in which case we'd need to see what gives for 0V (and you might have to look at the average of the middle codes to be more fair.

STATIC METRIC: OFFSET ERROR

OFFSET ERROR:

The offset error of an ADC, which is similar to the offset error of an amplifier, is defined as a deviation of the ADC output code transition points that is present across all output codes.

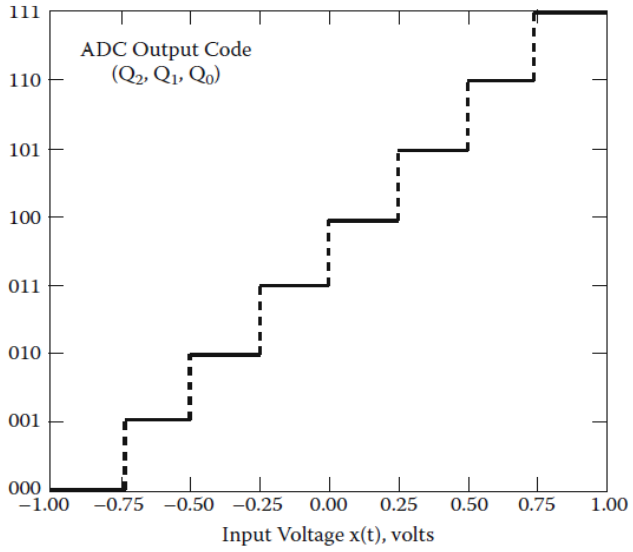


FIGURE 7-2 Conceptual ADC transfer function.

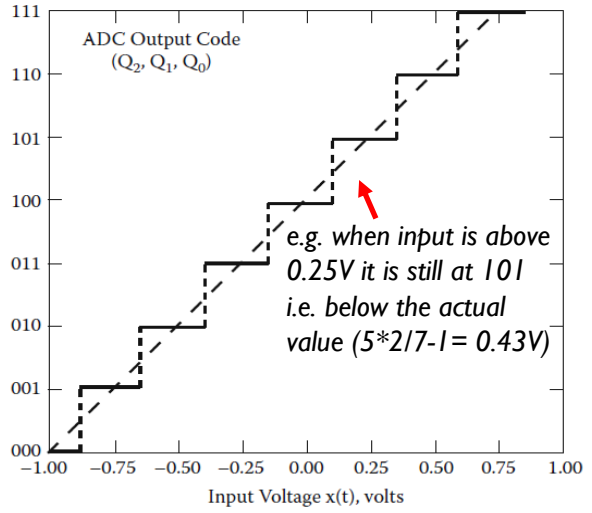
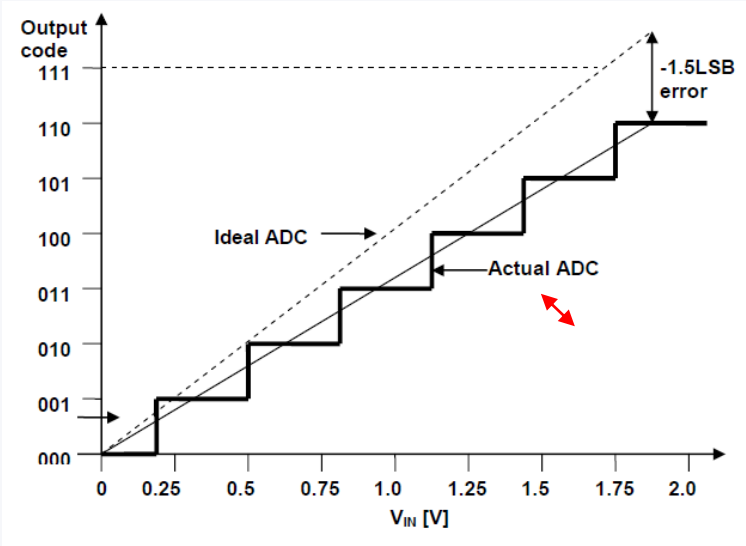


FIGURE 7-3 Ideal ADC transfer function.

[2]

STATIC METRIC: GAIN ERROR

- GAIN ERROR:
  - The gain error of an ADC is similar to the gain error of an amplifier.
  - Assuming ADC's offset error removed, then:
    - The gain error determines the amount of "rotational" deviation away from the ADC's ideal transfer function slope (i.e., the dashed diagonal line of the figure).
  - Once the gain error has been characterized, it may be possible to compensate for this error source.

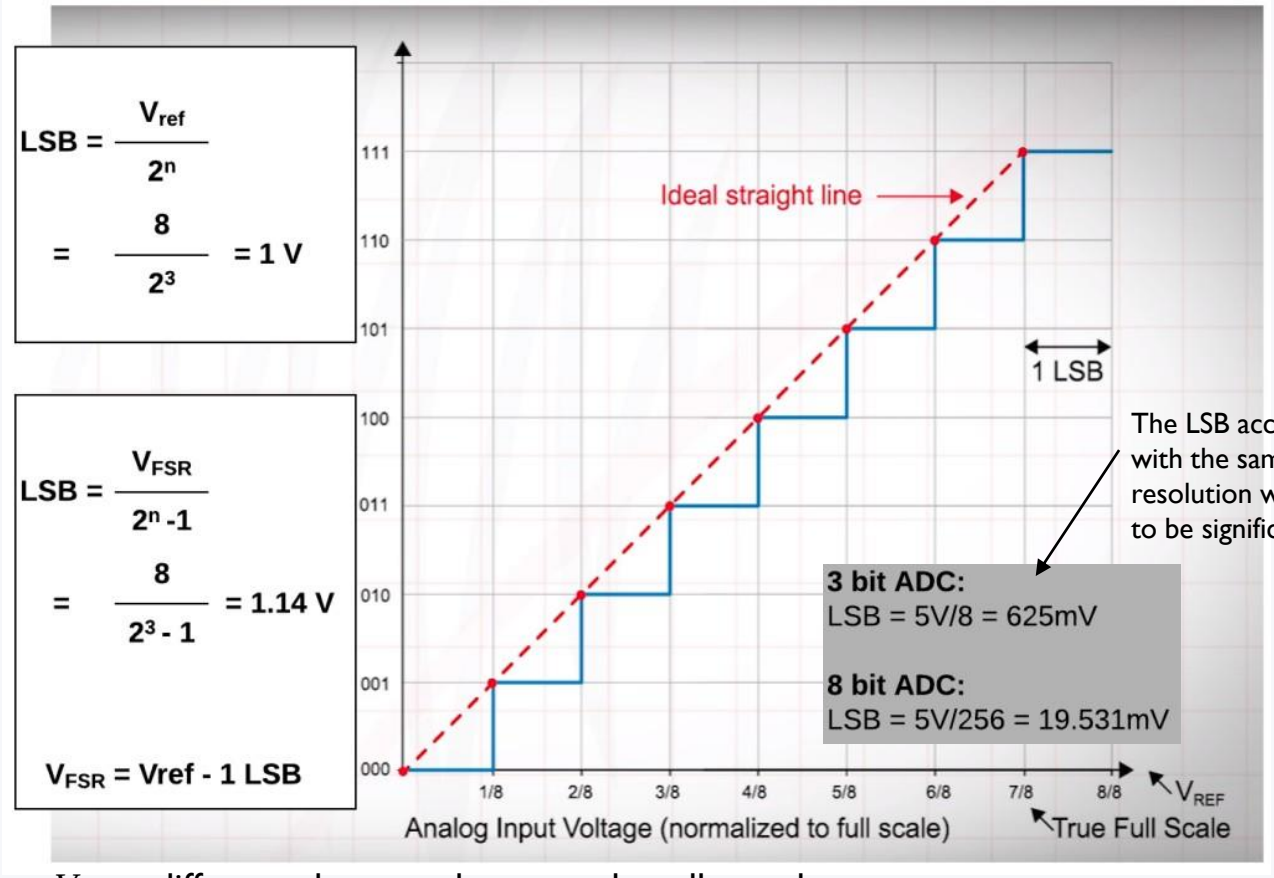


Recommended video: https://www.youtube.com/watch?v=ZfUz1s_jWmQ

Dynamic Metrics

ADC & DAC METRIC: LSB ACCURACY

This metric is used to compare how a LSB change in the code relates to the step change between the measured voltage Vref (blue line) and the desired ideal transfer function (dotted line). The LSB accuracy may not be consistent for all codes; it may change for different Vrefs (e.g. get wider, a bigger jump, as the voltage increases).



V_{FSR}: difference between largest and smallest voltage

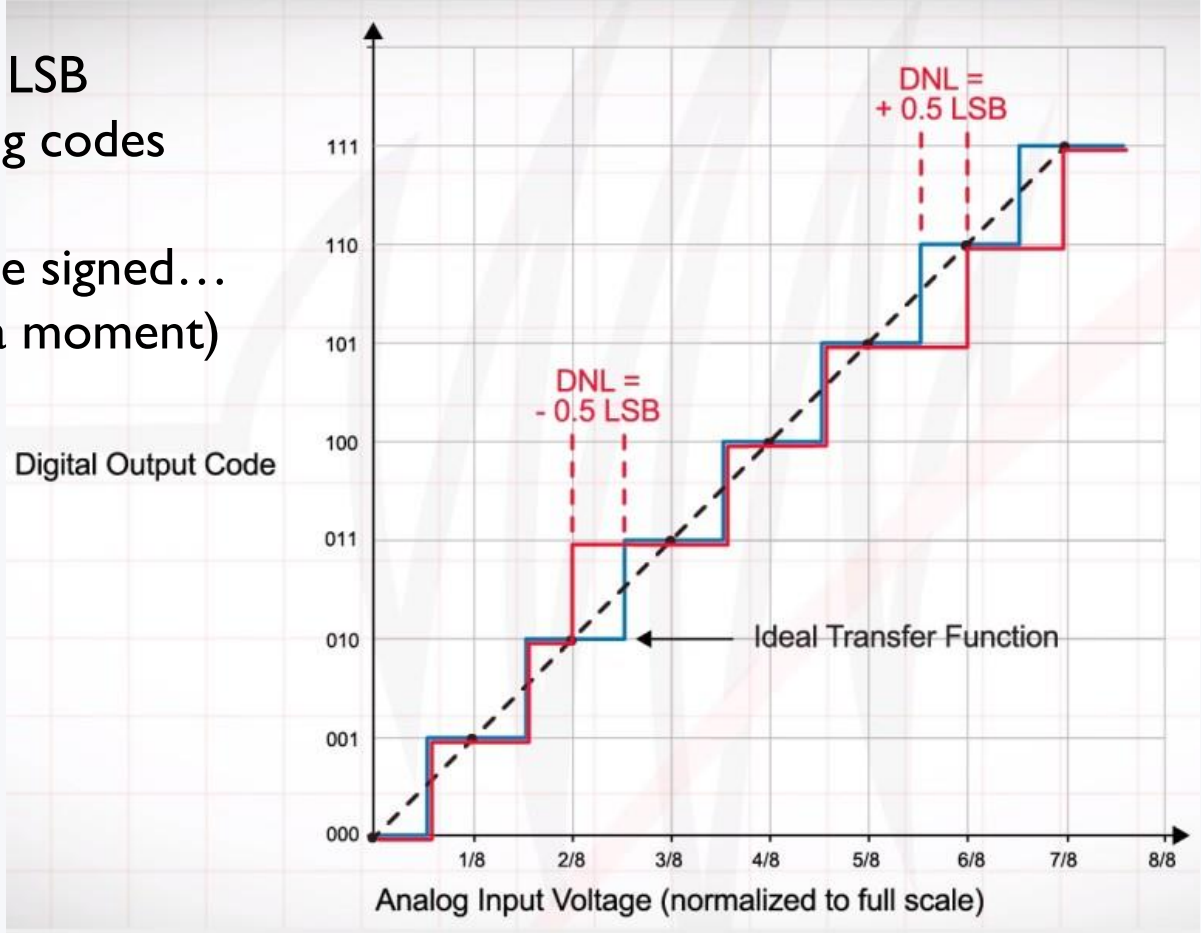
n: number of voltage intervals

ADC & DAC METRIC: LINEARITY (DNL)

Differential Non-Linearity (DNL):
The deviation between actual steps and ideal steps

DNL must be < ½ LSB
to ensure no missing codes

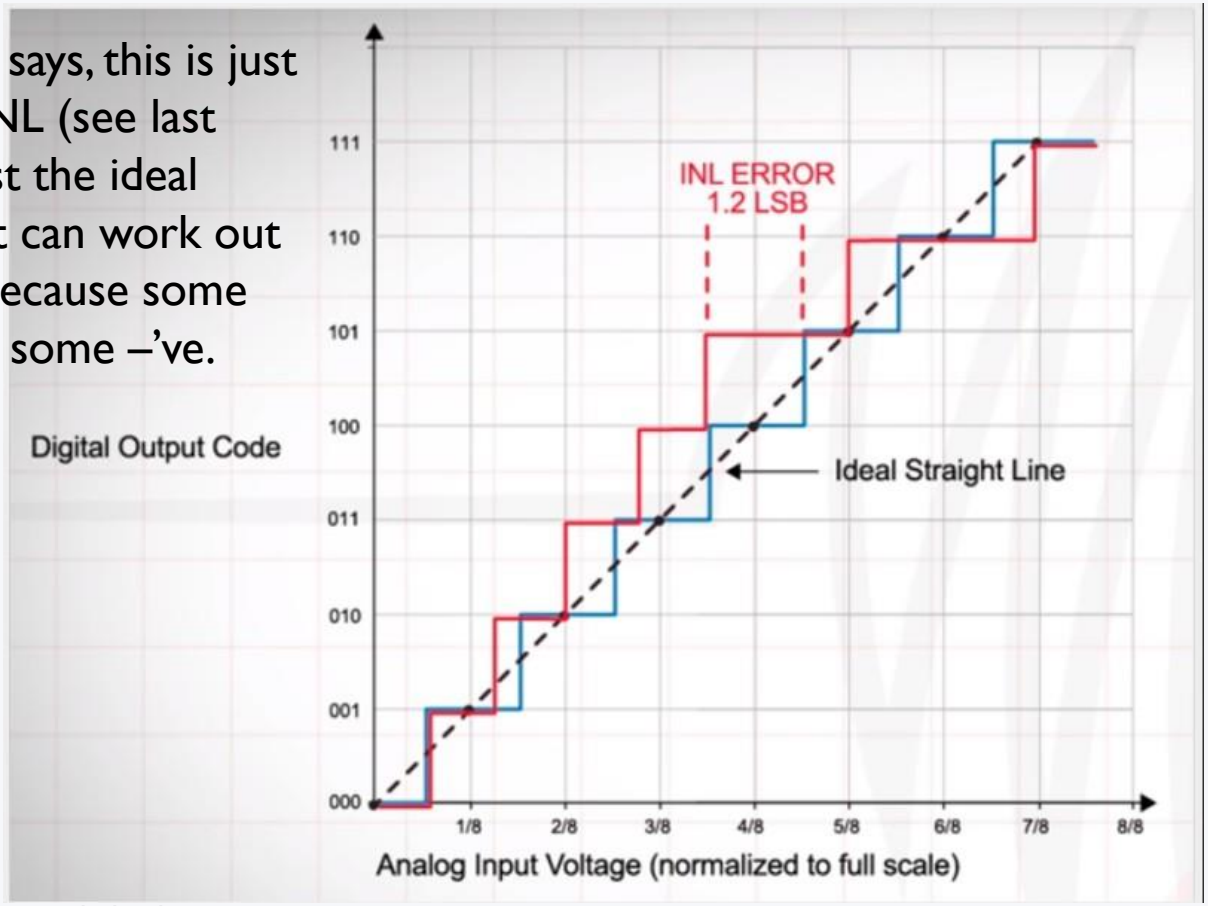
(The DNL should be signed…
we will see why in a moment)



ADC & DAC METRICS: LINEARITY (INL)

Integral Non Linearity (INL):
Integration of DNL error (accumulation of all DNL)

As the description says, this is just a sum of all the DNL (see last slide) errors against the ideal transfer function. It can work out to a low number because some DNLs may be +'ve some –'ve.



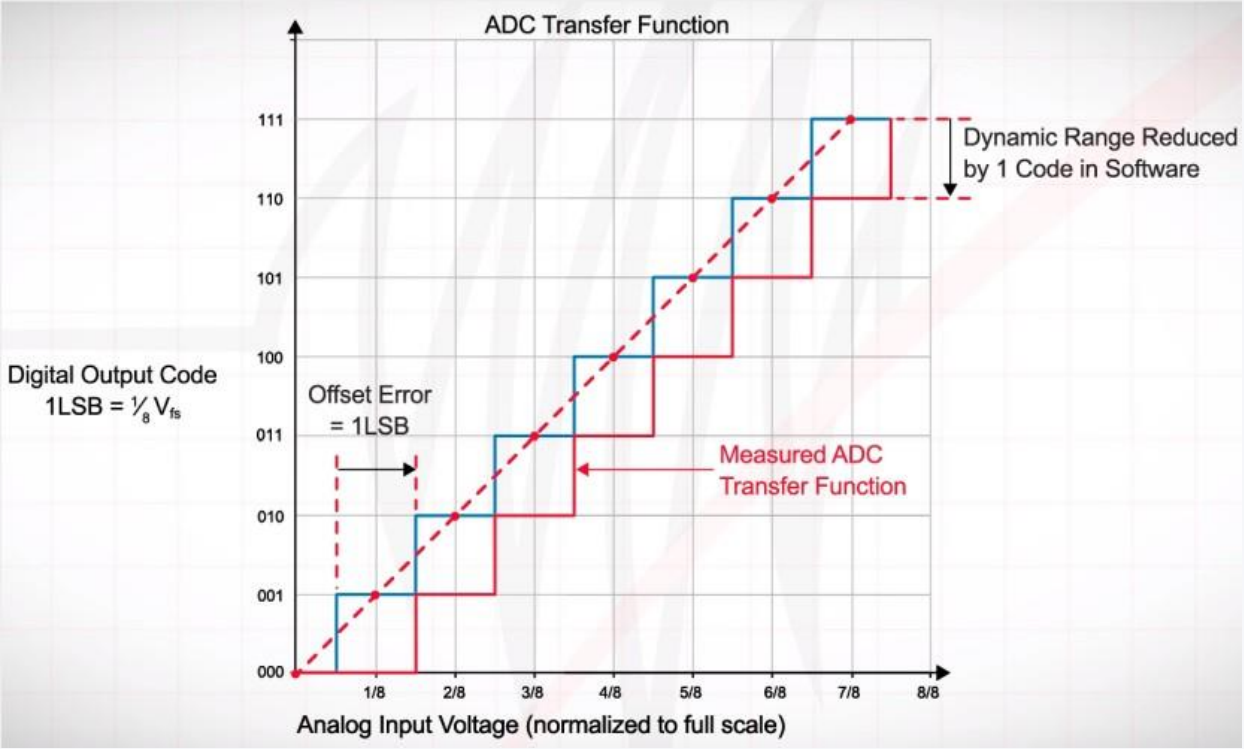
Information source and recommended video:
https://www.digikey.com/en/videos/m/microchip/adc-aspects---episode-1---quantization

OFFSET ERROR (RECAP)

Remember from earlier slide:

Offset error = Deviation of the output

Can easily be corrected using the microcontroller (reduces range of an ADC)



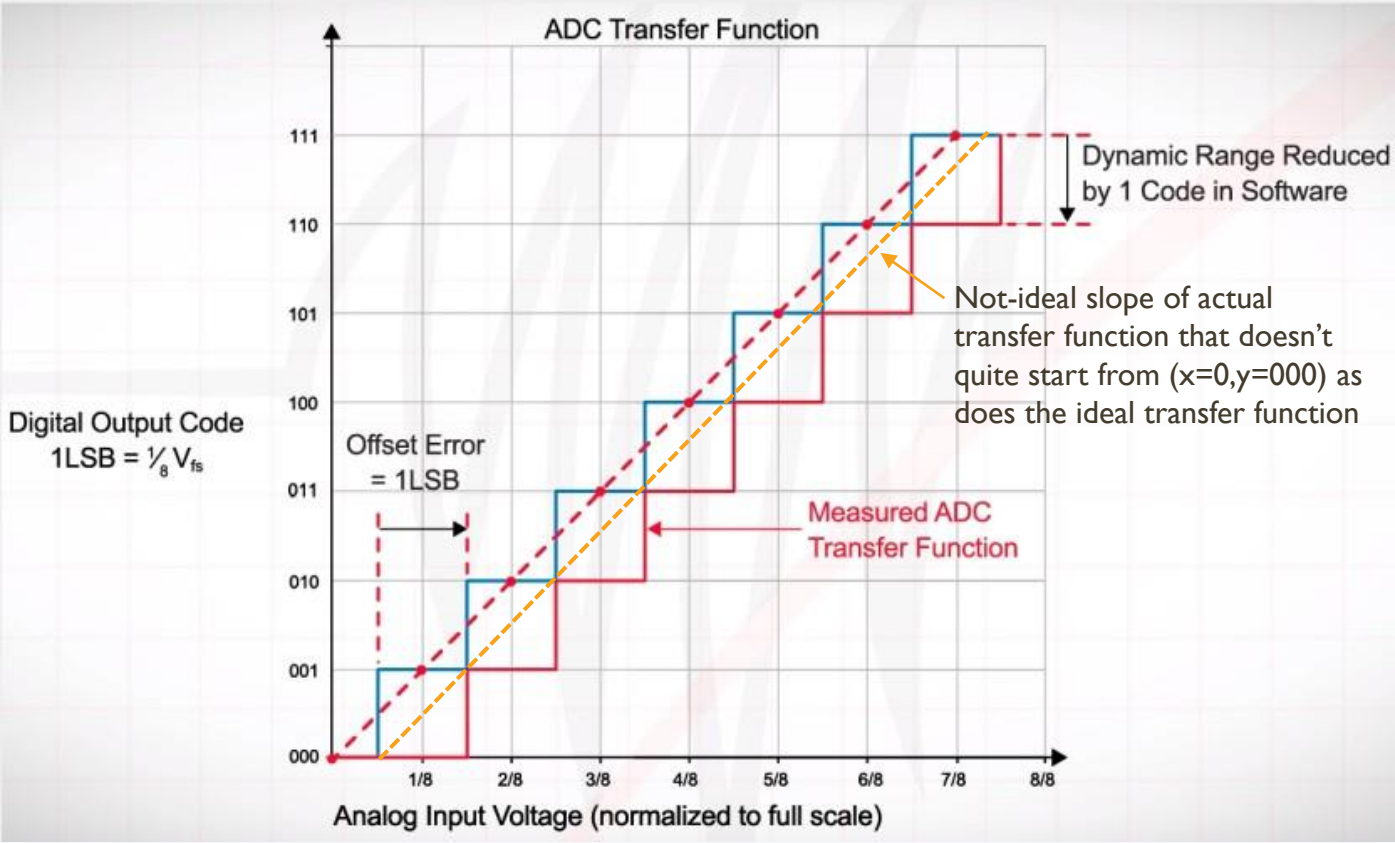
Offset error not to be confused with **full scale error**…

FULL SCALE ERROR

Definition Full scale error:

Offset error at the last transition

- ADC reaches its highest code before reaching its highest voltage
- Caused by both offset error + non-ideal slope of the transfer function

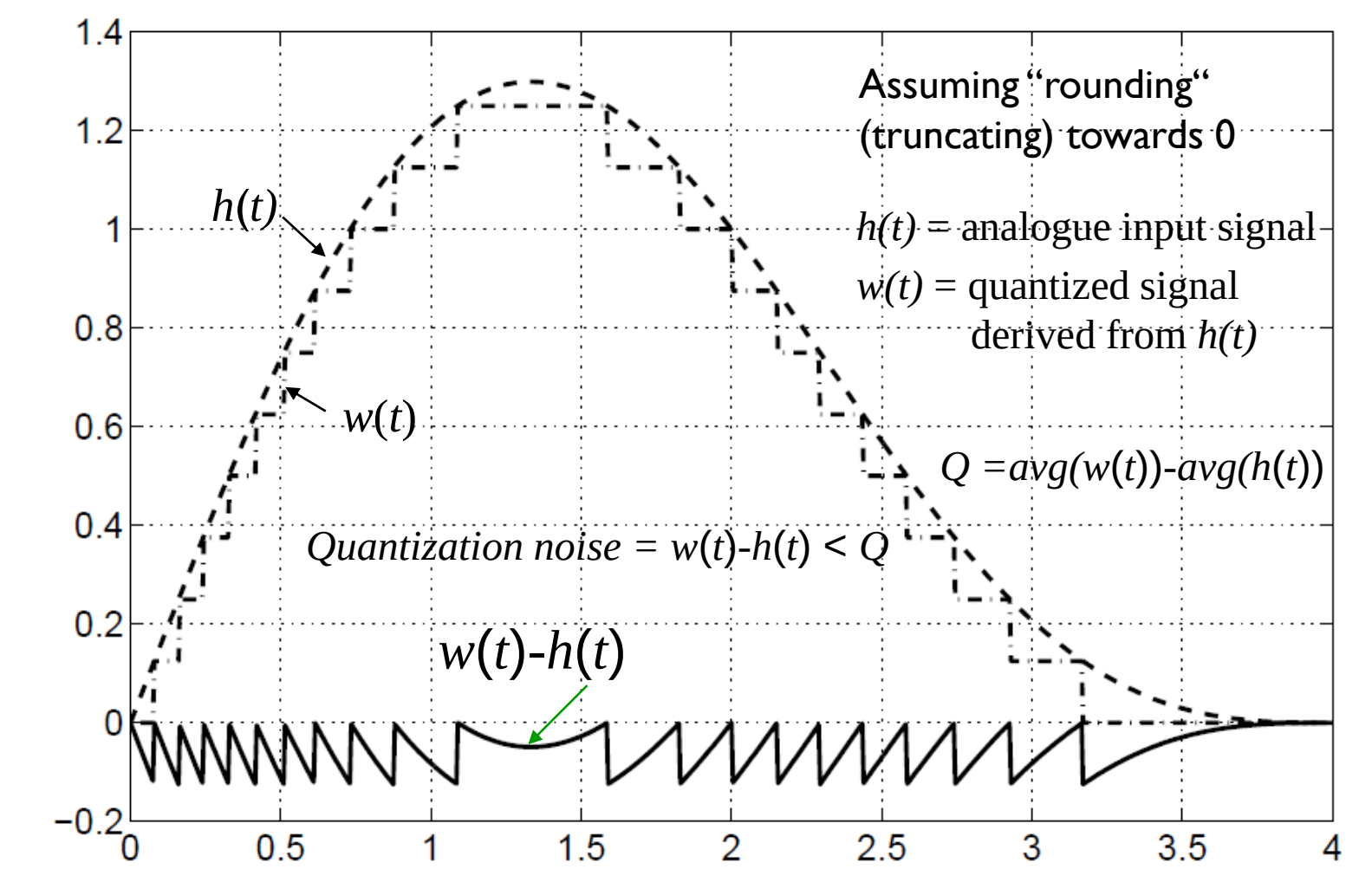


DYNAMIC MEASURES: EFFECTIVE NUMBER OF BITS (ENOB)

- Effective number of bits (ENOB)
  - The resolution of an ADC is specified by the number of bits used to represent the analogue value, in principle giving $\mathbf{2}^{N}$ signal levels for an N-bit signal.
  - The ENOB indicates how many bits effectively contribute towards representing the sampled input.

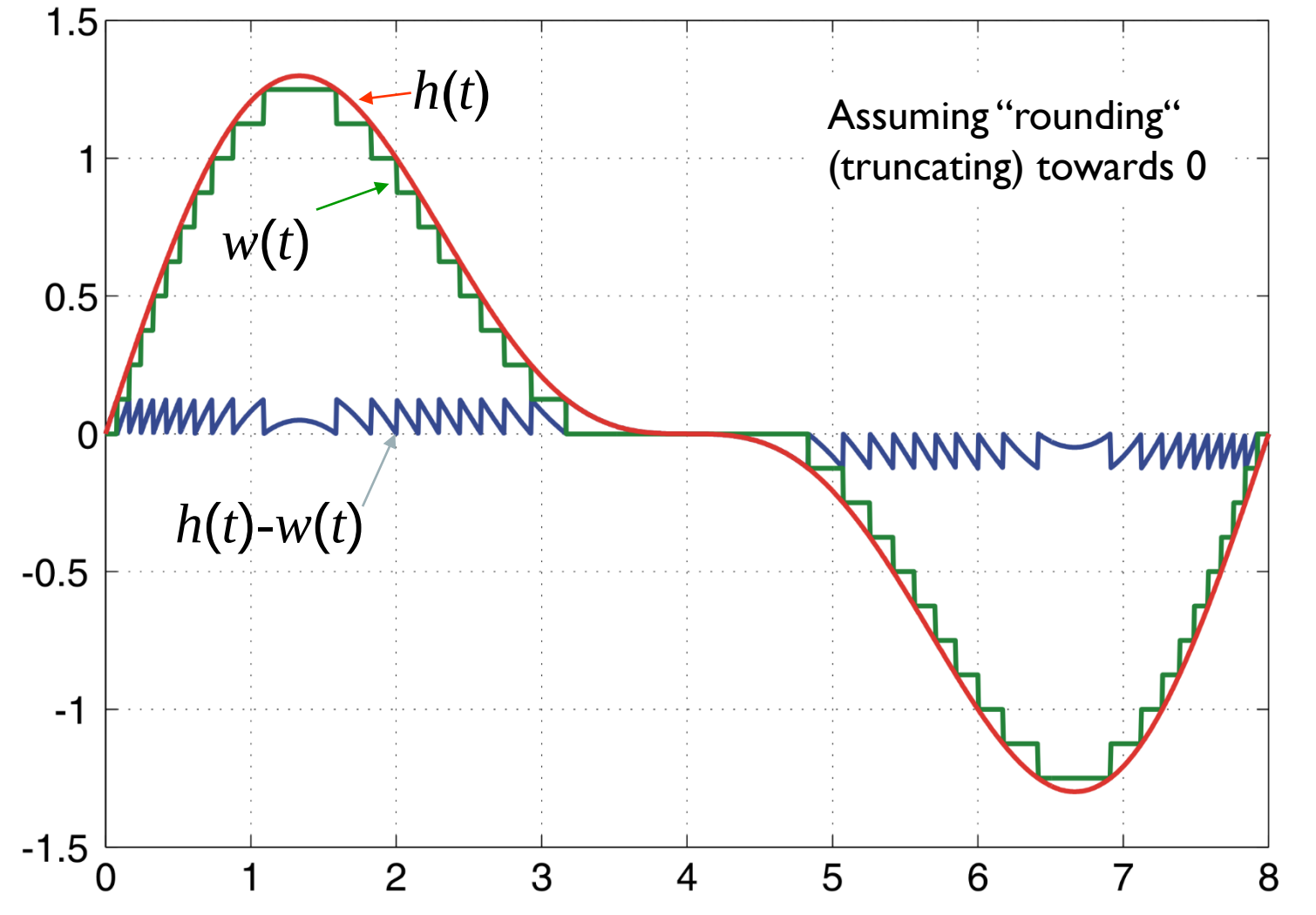
Bad ENOBs are like bad apples for an embedded engineer
(they can spoil the rest of your processing package)

QUANTIZATION NOISE



So, if I asked you to graph how the difference between the input signal (i.e. *h(t)*) and the quantization transfer (i.e. *w(t)*) looks you would be able to show that pretty easy now.

QUANTIZATION NOISE



h(t) = analogue input signal *w(t)* = quantized signal derived from *h(t)*

QUANTIZATION NOISE IMPACTS SNR

- In SNR, the quantization noise adds to other noise that may be hindering the channel.
- SNR = signal/noise

SNR in bB = $10\log_{10}$(signal/noise)

SNR in bB = $20\log_{10}$(V signal/ Vnoise) *

SNR_Q in dB = $20\log_{10}(n/\alpha Q)$

α characterizes how well w(t) tracks h(t)

α=0 → h(t) = w(t) α=1 → w(t) a little off from h(t)

clearly α=0 → perfect (infinite) SNR α=1 → strong signal

* For voltage the power is proportional to V^2 hence the x2 for in the 2nd equation (see net slide)

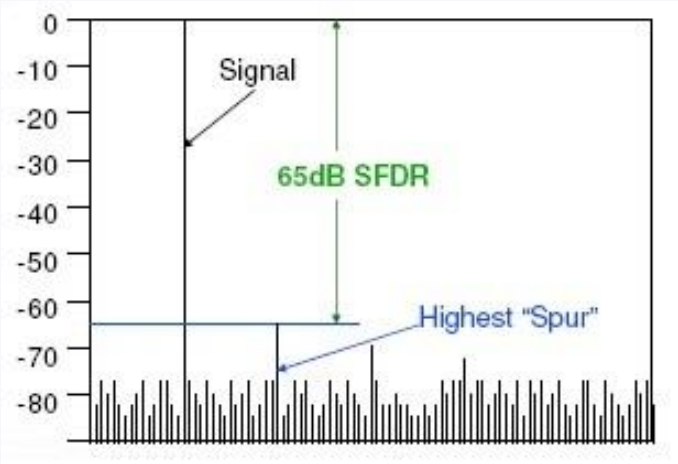
SPURIOUS-FREE DYNAMIC RANGE (SFDR)

Spurious-free Dynamic Range (SFDR):

- This is a frequency-domain measurement that determines the minimum signal level that can be distinguished from spurious components, and includes all spurious components over the full Nyquist band regardless of their origin
- SFDR for a ADC typically decreases as sampling rate increases. (It is generally indicate as a power or S/N ratio value)

This can be calculated for sampling real systems by sampling a known sinusoidal reference (or carrier signal) with minimum interference, sample it for a period and perform a Fourier transfer to find the difference between the max. of the spurious signals and the full-scale range (P_{FS} corresponds to the maximal power measured). Note: must put the spectrum in dBs i.e. $10\log_{10}(P_S/P_{REF})$.

Example of measuring SFDR



noise spurs are at the bottom of the plot