EEE3096S - Tutorial 3
Memo
2023

Question 1 [10 Marks]

Can be quite flexible on this - if it is well explained can get the marks.

1. The resolution of the ADC is 8-bit… but let's check that more closely. If we are using ramp.csv data, we can work out the MAX which is 244, and the MIN which is 14. The digitization range is effectively 244 – 14 + 1 = 231. So, the effective resolution is 231 codes and to get the number of bits it is **$\log_2(231) = 7.85$**.
   You could say the precise resolution is 7.85, however you can't really have a fraction of a bit so we would have to round it up and say that its resolution is 8 bits.

2. We could plug in the equation: $Q = V_{FSR}/n$
   We're using the Voltage ranges 0 to 2.50 V, so V_FSR = 2.5. There are 231 unique codes produced. So, voltage Q = 2.5V/231 = 0.0108 V.
   This would technically be the more correct answer. Alternatively, an acceptable solution is using n as 2^(n_adc_bits) = 256, in which case the quantization resolution would be 2.5/(2^8) = 0.0098 (which is pretty close – technically in this case though some of the codes are not effective, e.g. going much above 2.5 V and things get clamped rendering those last couple of codes the same which effectively reduces the quantization resolution of the system – at least that is the case if one is considering the surrounding circuitry, if one was looking just at the ADC without consideration for the circuit that links to it, then the quantization according to the devices specifications would probably be 0.0098).

   Another potential solution is to take saturation into account, as then the ramp only increases for a period of 1.84 ms (about 160 ns of saturation) for each period. Assuming the 0-2.5V ramp takes exactly 2 ms, this results in the voltage range of the ramp being (1.84/2)*2.5 = 2.297 V. If you then divide this by the number of steps between the min and max values, Q = 2.297/231 = 9.945 mV.

Question 2 [10 Marks]

Can be quite flexible on this - if it is well explained can get the marks.

1. The average code value given a 0 V input appears to be 14.87, i.e., it reads this code value for 0V. If the full-scale range (0 to 231) correspond to 2.5 V then the offset error appears to be on average 14.87/231 x 2.5 V = 0.1609 V (which is a bit of a nastily large offset considering the FSR; it is 6% of the available quantizing resolution). If using the full 8-bit quantizing, i.e., 0.0098 V, this corresponds to 14.87/256 x 2.5 V = 0.145 V – which doesn't appear as bad; this answer will also be accepted. [5 marks]

2. From the Figure, the highest spur is at 5 in the Fourier plot. The test signal, P_REF, is providing an amplitude of 26 in the plot. Accordingly, SFDR = (magnitude of fundamental) – (magnitude of largest spur) SFDR is: 26 – 5 = 21
   We can also a power measure in which the 80 kHz frequency is a reference power. Let the reference power measure of the 80 kHz signal be 0 dB; then, the power of the spur is: $10\log_{10}(5/26) = -7.16$ dB [5 marks]

Question 3 [10 Marks]

1. Frequency – Number of cycles per second.
   Duty cycle – Percentage that the PWM signal is high for a single cycle. [1 Mark]
2. Duty cycle – changes effective power being dissipated. [1 Mark]
3. Persistence of vision is a visual/optical illusion that occurs when the visual perception of something does not cease for some time after the light emanating from it stops reaching the eye. In other words, its an optical illusion whereby we can see light for a short period of time after it is turned off. In the context of PWM, this helps us to simplify circuit designs as we can reduce the power usage of displays by rapidly turning them on and off and they will continuously appear on. [2 Marks]
4. https://www.electronics-tutorials.ws/waveforms/555-circuits-part-1.html
   Assign marks for calculations [2 Marks], labelling components and figures [2 Marks], graphs showing that the circuit works [2 Marks]. To vary duty cycle, one or more of the resistors (R_B, R_B) should be replaced with a potentiometer.