# EEE3096S - Tutorial 4
## 2023

## Digital to Analog Converters

Submit a single PDF (named correctly with "**EEE3096S 2023 Tutorial 4 Hand-in STUDNUM1 STUDNUM2.pdf**") answering the following questions. If you pull from any sources, be sure to correctly cite them.

### 1 Learning Objective

By the end of this practical, you will have:

- Theoretical understanding of DACs.
- Experience with signal generation and low-pass filtering.

Preparatory notes: Read the lecture slides on DACs before you begin.

### 2 DAC Metrics

1. DACs opeate on the general premise that $V_{out} = K * \text{digitalinput}$. Calculate the output voltage $V_{out}$ of a 5-bit DAC if the digital input is 0b11101, given that the output is 10 mV for a digital input of 0b10100. [5 Marks]
2. A common DAC metric is full-scale error, which is the maximum deviation from its ideal value expressed as a percentage of its full scale. Calculate the range of possible outputs for an input of 0b100000000000 using a 12-bit DAC with a full-scale output of 10 mV, and a full-scale error of ±0.5% FS. [5 Marks]

Provide clear explanations (and/or working) for both of your answers.

### 3 DAC Design

In Practical 4 we will be building our own "cheap and nasty" PWM DAC signal generator with a maximum output frequency of 5 kHz. To do this, we need to keep the following in mind:

- We want $F_{PWM}$ to be significantly larger than our bandwidth $F_{BW}$ so that we can design a low-pass filter that will allow our signal through but attenuate the high frequency PWM harmonics.
- Raising $F_{PWM}$ degrades the DACs resolution according to the following:

$$\text{Resolution}_{PWM} = \frac{\log_{10}(\frac{F_{CLK}}{F_{PWM}})}{\log_{10}(2)} \quad [\text{bits}]$$

- The formula to be used in configuring the timer module in PWM mode to control the PWM output frequency is

$$F_{PWM} = \frac{F_{CLK}}{(ARR + 1)(PSC + 1)} \quad [Hz]$$

1. Calculate the maximum PWM frequency for a 10-bit DAC. Assume, in this case, that we are using a clock frequency of 72 MHz and the full 10-bit resolution. [4 Marks]
2. Pick values for ARR and PSC to guarantee the required 10-bit resolution. [1 Mark]
3. Design a Sallen-key low-pass filter that will allow our signal to pass through but attenuate the high-frequency PWM harmonics. We will limit our bandwidth to 5 kHz. Test your filter's performance in LTSpice (or similar) with a 1 kHz signal, a 5 kHz signal and a 20 kHz signal. Show any calculations, and include screenshots of your circuit as well as its output for the 1 kHz, 5 kHz and 20 kHz inputs. [10 Marks]
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