EEE3096S - Tutorial 3
2023

ADC Metrics and PWM

1 Learning Objective

By the end of this tutorial, you should have:

- an understanding of ADC metrics and how this should help you quantify the performance of an ADC device; and
- some basic experience with using data sampled from an ADC in order to find the ADC metrics

Note: You should know the basics of sampling from your Signals courses and/or the lecture slides for this course, but remember that Google is your friend! The following overview may also help: https://www.studocu.com/row/document/east-west-university/digital-signal-processing/lab1-study-of-sampling-quantization-and-encoding/46416091

2 ADC Metrics

Consider the following scenario and then respond to the questions that follow.

Scenario:

Consider that you're in lockdown. You and your colleague are working remotely to implement sampling in the system you are tasked do build. As it happens, neither of you have access to the physical platform, but being a smart engineer you hooked it up to the internet as well as a remotely controlled signal generator and power switch before abandoning the office. So you both have access to the platform, which happens to be running embedded Linux and is connected via ssh.

You know is that it's an 8-bit, low-cost, SPI-based ADC that is not of the best quality. You can assume that you've got the code to program it.

But you need to answer a few questions in order to decide on processing solutions to implement. Various data files have been obtained from tests that were run which will help you to characterise the ADC. The ADC is set up to receive a $0 - 2.55$ V signal, to convert that to 8-bit values. The ADC is sampling at 1 MHz and it understandably has a DC offset of some sort and saturates at some point.

2.1 Question 1

First off, the most obvious thing first: we know it's an 8-bit ADC but that doesn't mean it gives that perfect resolution. Consider that a ramp waveform has been linked up to test things. The ramp is running at 500 Hz, and we sample every 1 us.

We've set up the voltage range to go from 0 to 2.50 V, but we also know that the device saturates at some point below 2.55 V; as such, setting the signal generator's maximum voltage above 2.5 V would not make sense.

The captured data is shown in Figure 1 below. Based on this, answer the following sub-questions:

1. What is the resolution (in bits) of the ADC, based on the samples obtained from the experiment? [5 marks]
2. What is the Q (Quantizing) resolution (in Volts) for this system? (i.e., do some inspections to determine the difference between two input voltages causing the digitised output to be incremented by 1). [5 marks]

Provide clear explanations (or working) for both your above answers.

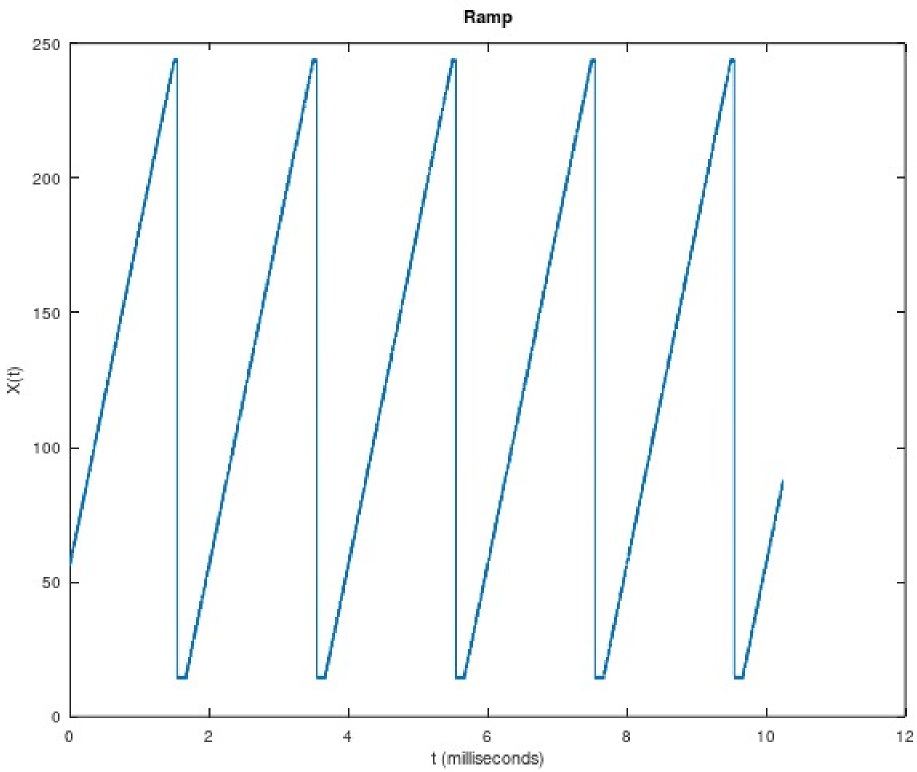

Figure 1: Testing of feeding a ramp into the ADC

2.2 Question 2

For this case, we have fed 0 V into the ADC (or as good as the remotely-controlled signal generator can do 0 V — which is pretty good). Based on Figure 2, clearly it is not exactly zero or perfectly behaved.

Answer the following based on this recording:

1. What is the direct current (DC) offset error of the ADC when it is connected to 0 V? [5 marks]

2. A further test was done in which the signal generator was told to generate a frequency of 80 kHz. The frequency plot generated from an FFT is shown in Figure 3. Use this data determine the Spurious-free Dynamic Range (SFDR), providing your answer as either power or SNR. [5 marks]

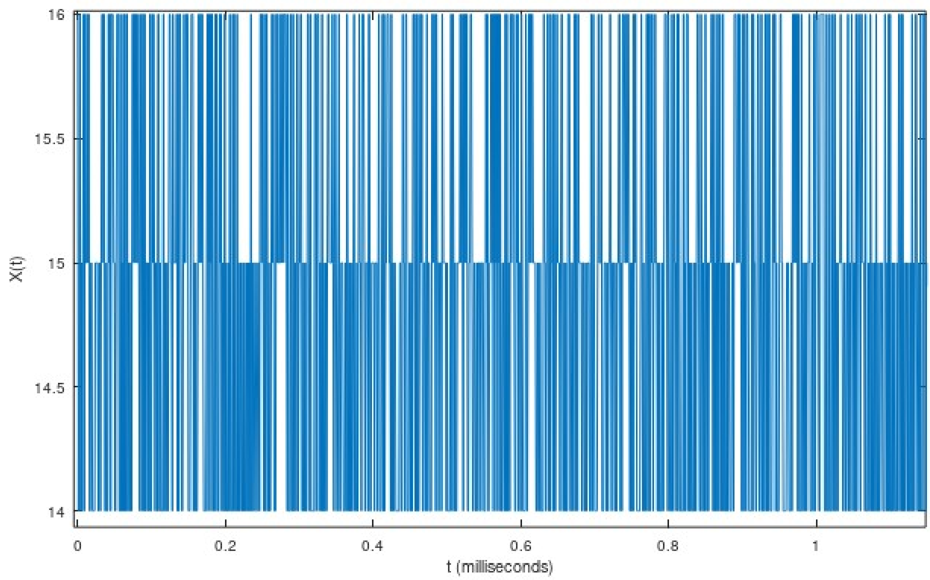

Figure 2: Testing at 0 V input, a zoomed in view of the captured data

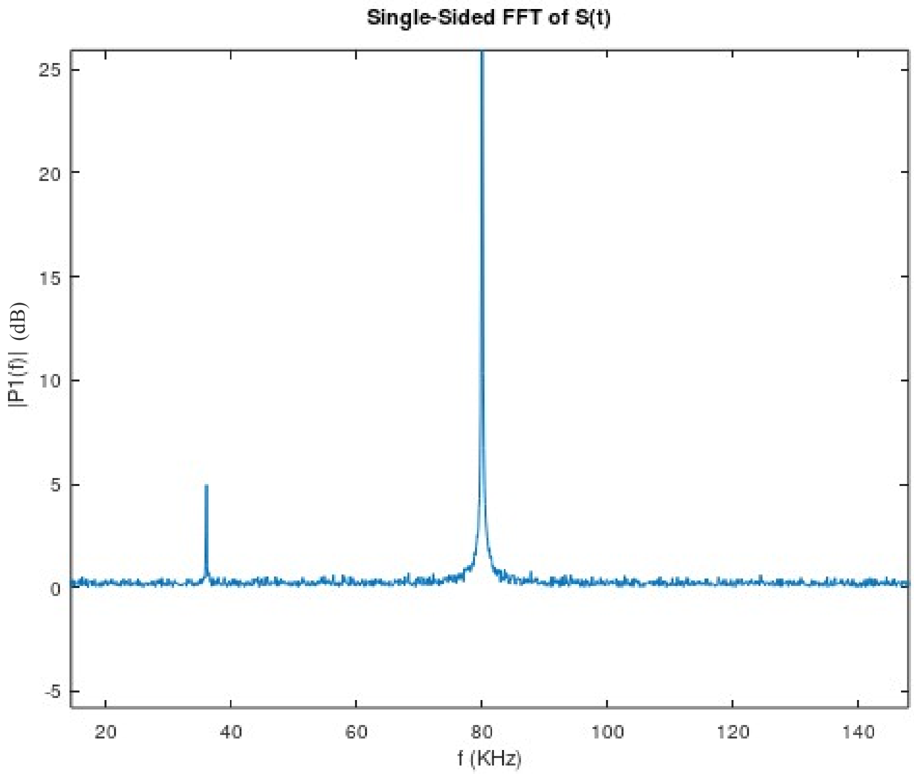

Figure 3: Testing with 80 kHz input, a zoomed in view of the frequency plot

3 PWM

A PWM signal is a square wave for which the frequency and duty cycle can be adjusted by the controller. By adjusting the frequency (the number of repeating cycles per second) and the duty cycle (the percentage of time that the square wave is high versus low), the resulting average voltage of the waveform can be adjusted. By changing the average voltage the controller is able to adjust the average power delivered to a load.

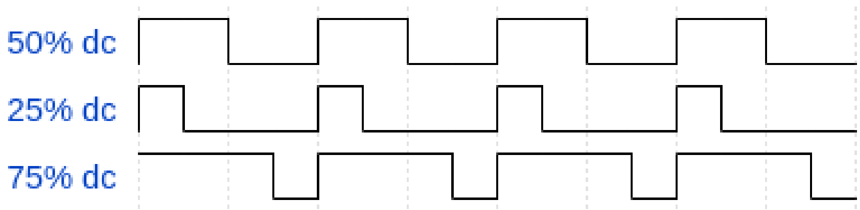

Figure 4: Fixed frequency, changing duty cycle PWM

3.1 Question 3

1. What is the difference between PWM frequency and duty cycle? [1 mark]
2. Which parameter should you change if you are trying to increase the brightness of an LED being driven by a PWM signal? [1 mark]
3. Explain the concept of persistence of vision in the context of PWM and why this can be useful in simplifying circuit designs. [2 marks]
4. Design a 555 timer-based circuit for generating a PWM signal with variable duty cycle. Remember that Google is your friend. Make sure to include screenshots from a simulator such as LTSpice. [6 marks]

Submit a single PDF (named correctly as "**EEE3096S 2023 Tutorial 3 Hand-in STUDNUM1 STUDNUM2.pdf**) with your answers to the above. If you pull from any sources, be sure to correctly cite them.