

GPL95100UA

16-bit High-end Interactive LCD Toy & Game Controller

Jan. 16, 2019

Version 1.0

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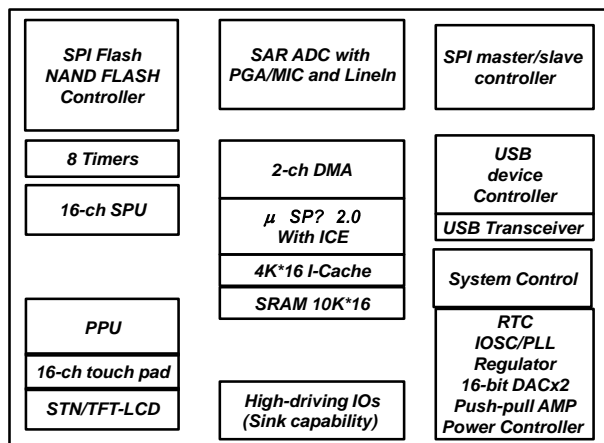
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16-bit High-end Interactive LCD Toy & Game Controller with $\mu'nSP^{\circledR}$ 2.0

1. GENERAL DESCRIPTION

GPL95100UA, a highly integrated System-on-a-Chip (SoC), is a cost-effective and high performance micro-controller solution for game, education and interactive learning applications. It equips a $\mu'nSP^{\circledR}$ 2.0 CPU with 8KB I-cache, picture process unit (PPU), 16-channel sound process unit (SPU), SPI Flash controller, NAND FLASH Memory controller with ECC/BCH, two channel DMA controller, USB device, mono STN-LCD and TFT-LCD interface, interrupt controller, and many other useful features. Providing a complete set of common system peripherals, GPL95100UA minimizes overall system costs and saves many additional components that other microcontrollers may require. The GPL95100UA development system integrates several powerful tools such as system with C language, assembly compiler, linker, source debugger, and project management function.

2. BLOCK DIAGRAM



3. FEATURES

- **Built-in 16-bit $\mu'nSP^{\circledR}$ 2.0 microprocessor with:**
 - operating speed up to 96MHz.
 - operating voltage from 2.9V to 5.5V.
- **Memories**
 - 4K*16-bit I-cache
 - 10K*16-bit RAM, stack area included.
 - Linear mapping and executing program on the external SPI FLASH memory. Both 2-IO mode and 4-IO mode are supported.
 - NAND FLASH controller with 1-bit ECC and 4-bit/8-bit BCH
- **I/O Ports**
 - Max. 58 General Programmable I/O ports (GPIO).
 - Each incorporates with pull-up resistor, pull-down resistor or floating input as programmer's settings on the corresponding registers
 - 13 high driving I/O ports with LED driving capability and 40mA current sink
- **Clock Management**
 - Internal oscillator: 8MHz $\pm 1.5\%$ (typ), @ 2.7V~3.6V
 - 32768Hz Crystal input @ 1.62V~1.98V
 - PLL (Phase-Lock Loop): 8MHz~96MHz, step=4MHz @ 2.7V~3.6V
- **Flexible Power Management (Operating/ Power down/ Wait/ Halt Mode)**
 - Operating mode: High performance@96MHz high speed
 - Deep Halt mode: 3.3V/1.8V off and only RTC on with approx. 5uA current consumption.
 - Wait mode: CPU clock off and system clocks all on
 - Halt mode: CPU and system clocks are all off. Only RTC, 32768Hz-XTAL, and LDOs modules are active
- **Picture Process Unit (PPU)**
 - 3 Text layers + 256 Sprites
 - QVGA output
 - Line-base operation
 - Up to 1024 x 1024 Text Size
- **TFT-LCD controller**
 - UPS051 (serial RGB)
 - UPS052 (serial RGB dummy),
 - Parallel RGB
 - I80 (8-bit/16-bit system bus) I/F type

- CCIR601/CCIR656.
- **Supports various LCD resolutions: 160x128, 220x176, and 320x240**
- **Mono and 16-gray STN-LCD controller interface**
- **Sound Process Unit (SPU)**
 - 16 hardware PCM/ADPCM channels
 - Cache supporting for directly accessing 16-channel wave table on external SPI Flash, 2-channel A1800 playback
- 16-channel capacitive touch detection
- Two-channel DMA controller.
- 29 sources Interrupt Controller.
- Universal Serial Bus (USB) 2.0 full speed compliant device with built-in transceiver.
- Watchdog timer.
- Independent power real-time clock.
- 11-output x 8-input matrix key scan controller.
- Eight 16-bit timers.
- Six re-loadable timers/counters support comparison, PWM, capture and BAM (4-bit angle modulation)
- SPI master/slave controller.
- Power controller with on power-on key and one system power enable output pad.
- Built-in 5.5V to 3.3V regulator, 3.3V to 1.8V regulator, Regulator for touch pad macro and regulator for ADC
- Low voltage reset(LVR)(2.4V trigger/2.6V release for 3.3V)
- IOSC, 96MHz PLL
- **DAC/Amplifier:** 16-bit stereo L and R DAC output that can be added external amplifier. Or mix L_R internally then through a push pull amplifier output, which can driver external speaker directly.
- **ADC: Two 12-bit ADCs**
 - One for MIC in with PGA and digital AGC
 - One for 8-channel line-in

4. SIGNAL DESCRIPTION

Left Side

Pad No	Package No	Name	Group	Type	Normal Function Description	GPIO Group
-	1	NC	NC	I/O	Leave it unconnected	
-	2	NC	NC	I/O	Leave it unconnected	
1	3	V18_RTC	RTC	P	RTC power output if V50_LDO is provided. RTC power input if V50_LDO is not provided.	
2	4	VSS_PLL	PLL	G	PLL ground	
3	5	V33_PLL	PLL	P	3.3V PLL power	
4	6	IOE0	ADC	I/O	IOE0 or ADC line in 0 or external input interrupt (EXT0_INT)	
5	7	IOE1	ADC	I/O	IOE1 or ADC line in 1	
6	8	IOE2	ADC	I/O	IOE2 or ADC line in 2	
7	9	IOE3	ADC	I/O	IOE3 or ADC line in 3	
8	10	IOE4	ADC	I/O	IOE4 or ADC line in 4	
9	11	IOE5	ADC	I/O	IOE5 or ADC line in 5	
10	12	IOE6	ADC	I/O	IOE6 or MIC input or UART_RX	
11	13	IOE7	ADC	I/O	IOE7 or ADC voltage reference output or UART_TX	
12	14	VSS_ADC	ADC	G	ADC ground	
13	15	V33_ADC	ADC	P	3.3V ADC power This power can be provided by internal regulator out and then connect capacitor to ADC ground only.	
14	16	RESETB	SYS	I	Reset pin, low active.	
15	17	ICECK	ICE	I	ICE clock input. Default is input pull low.	
16	18	ICEDA	ICE	I/O	ICE data Default is input pull low.	
17	19	IOD0	SPI FLASH I/F	I/O	Default is SPI FLASH DATA0	
18	20	IOD1	SPI FLASH I/F	I/O	Default is SPI FLASH CLOCK	
19	21	DVSS	Digital Ground	G	Digital ground	
20	22	IOD2	SPI FLASH I/F	I/O	Default is SPI FLASH DATA3	
21	23	IOD3	SPI FLASH I/F	I/O	Default is SPI FLASH CSB	
22	24	IOD4	SPI FLASH I/F	I/O	Default is SPI FLASH DATA1	
23	25	IOD5	SPI FLASH I/F	I/O	Default is SPI FLASH DATA2	
24	26	V33_DVCC	Digital 3.3V	P	3.3V I/O power for PortD	
25	27	TEST	SYS	I	Test mode control signal. Input floating This pin must be tied with ground under normal operation.	
26	28	IOC0	NAND I/F	I/O	IOC0 or NAND FLASH ready or UART_TX or TFT data0(i-80)	
27	29	IOC1	NAND I/F	I/O	IOC1 or NAND FLASH REB or UART_RX or TFT data1(i-80)	
28	30	IOC2	NAND I/F	I/O	NAND FLASH CSB or I2C_CLK or TFT data2(i-80)	
-	31	NC	NC	I/O	Leave it unconnected	
-	32	NC	NC	I/O	Leave it unconnected	

Bottom Side

Pad No	Package No	Name	Group	Type	Normal Function Description	GPIO Group
-	33	NC	NC	I/O	Leave it unconnected	
29	34	IOC3	NAND I/F	I/O	IOC3 or NAND FLASH data 7 or I2C_SDA or TFT data3(i-80)	
30	35	IOC4	NAND I/F	I/O	IOC4 or NAND FLASH data 6 or TFT data4(i-80)	
31	36	IOC5	NAND I/F	I/O	IOC5 or NAND FLASH data 5 or TFT data5(i-80)	
32	37	IOC6	NAND I/F	I/O	IOC6 or NAND FLASH data 4 or TFT data6(i-80)	
33	38	IOC7	NAND I/F	I/O	IOC7 or NAND FLASH data 3 or TFT data7(i-80)	
34	39	IOC8	NAND I/F	I/O	IOC8 or NAND FLASH data 2 or external input interrupt(EXT1_INT)	
35	40	V33_DVCC	Digital 3.3V	P	3.3V I/O power for PortC	
36	41	DVSS	Digital Ground	G	Digital ground	
37	42	IOC9	NAND I/F	I/O	IOC9 or NAND FLASH data 1	
38	43	IOC10	NAND I/F	I/O	IOC10 or NAND FLASH data 0 or TFT TE input	
39	44	IOC11	NAND I/F	I/O	IOC11 or NAND FLASH CLE or TFT OEB(i-80)	
40	45	IOC12	NAND I/F	I/O	IOC12 or NAND FLASH ALE or TFT R/S(i-80)	
41	46	IOC13	NAND I/F	I/O	IOC13 or NAND FLASH WEB or TFT CSB(i-80)	
42	47	IOC14	NAND I/F	I/O	IOC14 or NAND FLASH WPB or TFT WEB(i-80)	
43	48	V18_DVCC	Digital 1.8V	P	1.8V digital power	
44	49	IOA0	High driving IO	I/O	IOA0 or TFT TE input(i-80) or external input interrupt(EXT0_INT)	
45	50	IOA1	High driving IO	I/O	IOA1 or TFT OEB(i-80) or TFT DE or SPI1 DO	
46	51	IOA2	High driving IO	I/O	IOA2 or TFT R/S(i-80) or TFT HSYNC or SPI1 CSB	
47	52	IOA3	High driving IO	I/O	IOA3 or TFT CSB(i-80) or TFT VSYNC or SPI1 CLK	
48	53	IOA4	High driving IO	I/O	IOA4 or TFT WEB(i-80) or TFT clock or SPI1 DI	
49	54	IOB0	High driving IO	I/O	IOB0 or TimerA CCP or TFT D0(CCIR)	
50	55	IOB1	High driving IO	I/O	IOB1 or TimerB CCP or TFT D1(CCIR)	
51	56	V50_IOAB	IO power	P	PortA/B power	
52	57	VSS_IOAB	Ground	G	PortA/B ground	
53	58	IOB2	High driving IO	I/O	IOB2 or TimerC CCP or TFT D2(CCIR)	
54	59	IOB3	High driving IO	I/O	IOB3 or TimerD CCP or TFT D3(CCIR)	
55	60	IOB4	High driving IO	I/O	IOB4 or Timer PWM0 or TFT D4(CCIR) or SPI1 DO	
56	61	IOB5	High driving IO	I/O	IOB5 or Timer PWM1 or TFT D5(CCIR) or SPI1 CSB	
57	62	IOB6	High driving IO	I/O	IOB6 or Timer PWM2 or TFT D6(CCIR) or SPI1 CLK	
58	63	IOB7	High driving IO	I/O	IOB7 or Timer PWM3 or TFT D7(CCIR) or SPI1 DI	
-	64	NC	NC	I/O	Leave it unconnected	

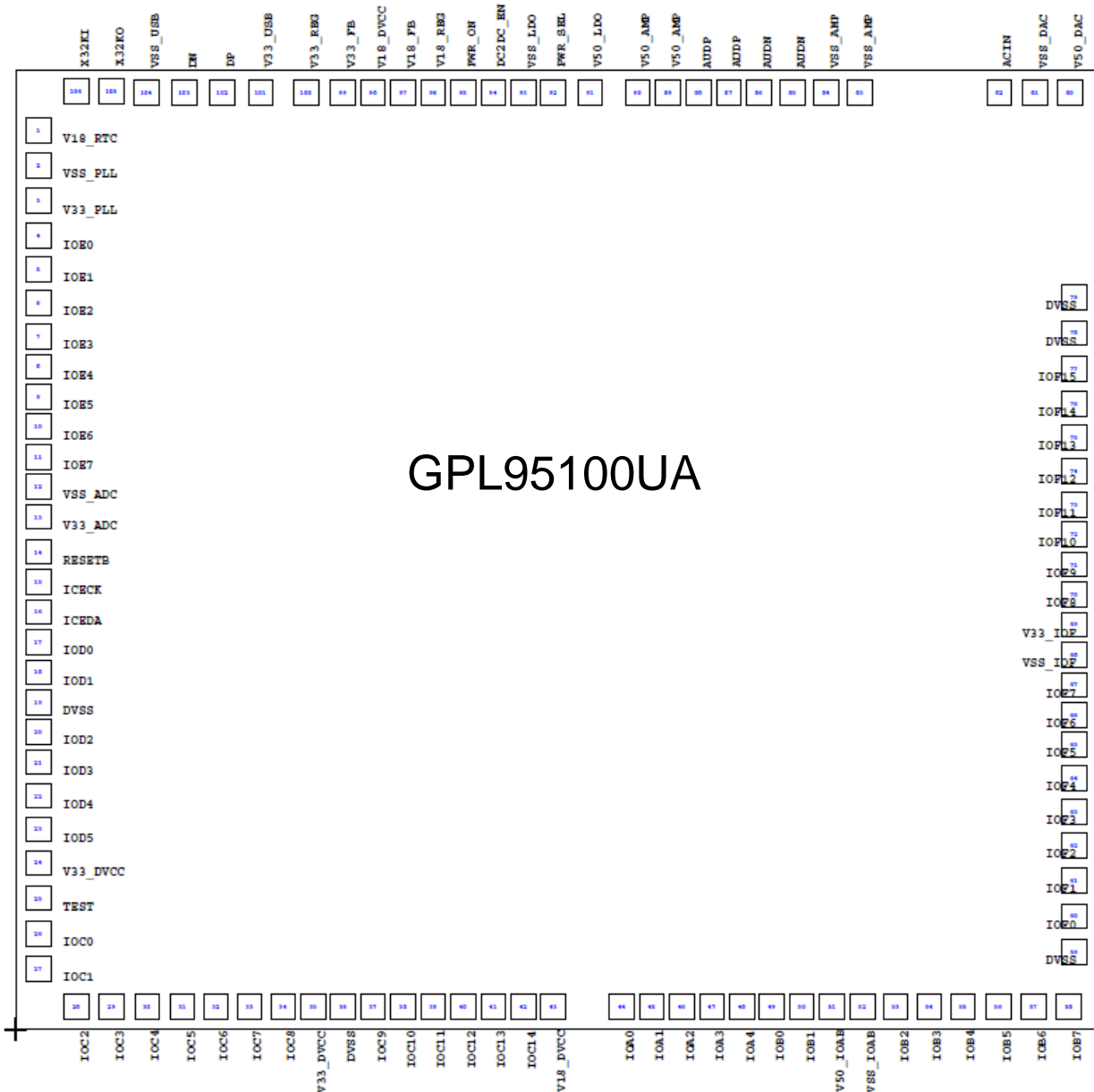
Right Side

Pad No	Package No	Name	Group	Type	Normal Function Description	GPIO Group
-	65	NC	NC	I/O	Leave it unconnected	
-	66	NC	NC	I/O	Leave it unconnected	
-	67	NC	NC	I/O	Leave it unconnected	
-	68	NC	NC	I/O	Leave it unconnected	
-	69	NC	NC	I/O	Leave it unconnected	
59	70	DVSS	Digital Ground	G	Digital ground	
60	71	IOF0	Touch	IO	IOF0 or Touch pad 0 or TFT B3(CCIR) or TFTD0(CCIR) or SPI1 DO	
61	72	IOF1	Touch	IO	IOF1 or Touch pad 1 or TFT B4(CCIR) or TFTD1(CCIR) or SPI1 CSB	
62	73	IOF2	Touch	IO	IOF2 or Touch pad 2 or TFT B5(CCIR) or TFTD2(CCIR) or SPI1 CLK	
63	74	IOF3	Touch	IO	IOF3 or Touch pad 3 or TFT B6(CCIR) or TFTD3(CCIR) or SPI1 DO	
64	75	IOF4	Touch	IO	IOF4 or Touch pad 4 or TFT B7(CCIR) or TFTD4(CCIR) or SPI0 DO	
65	76	IOF5	Touch	IO	IOF5 or Touch pad 5 or TFT G2(CCIR) or TFTD5(CCIR) or SPI0 CSB	
66	77	IOF6	Touch	IO	IOF6 or Touch pad 6 or TFT G3(CCIR) or TFTD6(CCIR) or SPI0 CLK	
67	78	IOF7	Touch	IO	IOF7 or Touch pad 7 or TFT G4(CCIR) or TFTD7(CCIR) or SPI0 DI	
68	79	VSS_IOF	Touch	G	PortF ground	
69	80	V33_IOF	Touch	P	3.3V power for PortF .	
70	81	IOF8	Touch	IO	IOF8 or Touch pad 8 or TFT G5(CCIR) or TFT TE input(i-80)	
71	82	IOF9	Touch	IO	IOF9 or Touch pad 9 or TFT G6(CCIR) or TFT OEB(i-80) or TFT DE(CCIR)	
72	83	IOF10	Touch	IO	IOF10 or Touch pad 10 or TFT G7(CCIR) or TFT R/S(i-80) or TFT HSYNC(CCIR)	
73	84	IOF11	Touch	IO	IOF11 or Touch pad 11 or TFT R3(CCIR) or TFT CSB(i-80) or TFT VSHYNC(CCIR) or UART TX	
74	85	IOF12	Touch	IO	IOF12 or Touch pad 12 or TFT R4(CCIR) or TFT WEB(i-80) or TFT CLK(CCIR) or UART RX	
75	86	IOF13	Touch	IO	IOF13 or Touch pad 13 or TFT R5(CCIR) or I2C CLK	
76	87	IOF14	Touch	IO	IOF14 or Touch pad 14 or TFT R6(CCIR) or I2C SDA	
77	88	IOF15	Touch	IO	IOF15 or Touch pad 15 or TFT R7(CCIR) or external input interrupt(EXT1_INT)	
78	89	DVSS	Digital Ground	G	Digital ground	
79	90	DVSS	Digital Ground	G	Digital ground	
-	91	NC	NC	I/O	Leave it unconnected	
-	92	NC	NC	I/O	Leave it unconnected	
-	93	NC	NC	I/O	Leave it unconnected	
-	94	NC	NC	I/O	Leave it unconnected	
-	95	NC	NC	I/O	Leave it unconnected	
-	96	NC	NC	I/O	Leave it unconnected	

Top Side

Pad No	Package No	Name	Group	Type	Normal Function Description	GPIO Group
-	97	NC	NC	I/O	Leave it unconnected	
-	98	NC	NC	I/O	Leave it unconnected	
-	99	NC	NC	I/O	Leave it unconnected	
80	100	V50_DAC	DAC_AMP	P	DAC power (up to 5.5V)	
81	101	VSS_DAC	DAC_AMP	G	DAC ground	
82	102	ACIN	DAC_AMP	AI	DAC ACIN	
83	103	VSS_AMP	DAC_AMP	G	Audio AMP ground	
84	104	VSS_AMP	DAC_AMP	G	Audio AMP ground	
85	105	AUDN	DAC_AMP	AO	Audio AMP output N/DAC output channel L	
86	106	AUDN	DAC_AMP	AO	Audio AMP output N/DAC output channel L	
87	107	AUDP	DAC_AMP	AO	Audio AMP output P/DAC output channel R	
88	108	AUDP	DAC_AMP	AO	Audio AMP output P/DAC output channel R	
89	109	V50_AMP	DAC_AMP	P	Audio AMP power	
90	110	V50_AMP	DAC_AMP	P	Audio AMP power	
91	111	V50_LDO	LDO	P	DC 5V power input	
92	112	PWR_SEL	LDO	AI	Internal 3.3V regulator power source selection 1: Using External 3.3V power device(ex: LDO) 0: Using internal 3.3V LDO	
93	113	VSS_LDO	LDO	G	LDO ground	
94	114	DC2DC_EN	LDO	AO	External DC-DC system power enabling pin Leave it unconnected if not used.	
95	115	PWR_ON	LDO	AI	Power-on key, high active. Default is input pull low	
96	116	V18_REG	LDO	P	Internal V1.8 LDO regulator output	
97	117	V18_FB	LDO	AI	LDO18 feedback	
98	118	V18_DVCC	Digital 1.8V	PWR	1.8V digital power input	
99	119	V33_FB	LDO	AI	LDO33 feedback	
100	120	V33_REG	LDO	P	Internal V3.3 regulator output	
101	121	V33_USB	USB	P	3.3V USB power input	
102	122	DP	USB	I/O	DP pin of USB PHY	
103	123	DN	USB	I/O	DN pin of USB PHY	
104	124	VSS_USB	USB	G	USB ground	
105	125	X32KO	RTC	AO	32768Hz X'TAL output	
106	126	X32KI	RTC	AI	32768Hz X'TAL input	
-	127	NC	NC	I/O	Leave it unconnected	
-	128	NC	NC	I/O	Leave it unconnected	

4.1. PAD Assignment



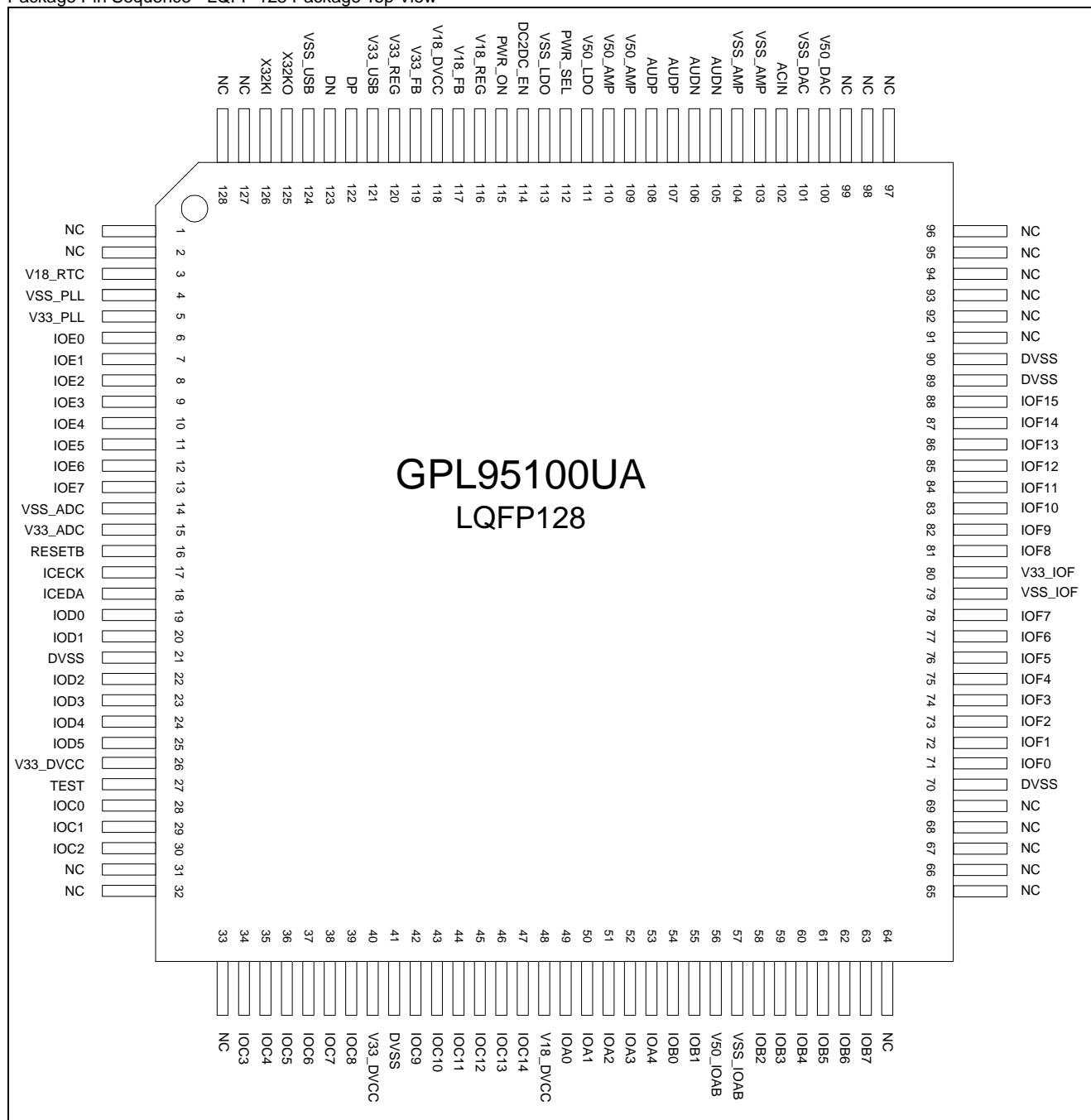
This IC substrate should be connected to VSS

Note1: To ensure IC functions properly, please bond all of VDD and VSS pins.

Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

4.2. Pin Map

Package Pin Sequence - LQFP 128 Package Top View



5. FUNCTIONAL DESCRIPTIONS

5.1. CPU

GPL95100UA comes with a 16-bit μnSP^{TM} 2.0 CPU and sixteen registers: R1 - R4 (General-purpose registers), PC (Program Counter), SP (Stack Pointer), Base Pointer (BP), SR (Segment Register) and R8 - R15 (General-purpose register). The interrupt includes three FIQs (Fast Interrupt Request) and eight IRQs (Interrupt Request), plus one software-interrupt, BREAK. GPL95100UA also has an 8K bytes I-cache which can significantly enhance the p overall performance.

5.2. Memory

5.2.1. Internal SRAM

The amount of SRAM is 10K-word (including stack), ranged from 0x0000 through 0x27FF with access speed of one CPU clock. Since this SRAM is located in CPU's local bus, the system bus will not be occupied when this SRAM is accessed by CPU. This SRAM can be accessed by CPU/PPU/DMA /LCD.

5.2.2. SPI FLASH memory

The memory space of SPI FLASH is from 0x9000 and it is linear mapping, the range is dependent on the density of the external SPI Flash. Other bus masters such as PPU, SPU and DMA can access SPI FLASH directly. Both 2-IO and 4-IO mode are supported for system performance enhancement. The controller is configurable for various SPI FLASH providers with different timing format. The maximum SPI FLASH clock is up to 96MHz(PCB dependent).

5.3. PLL, Clock, Power Mode

5.3.1. PLL (Phase Lock Loop)

An internal 8MHz oscillator and a 96MHz PLL are embedded in GPL95100UA.

5.3.2. System clock

The system clock can be selected from 32768 or 8M or 96M (determined by fast PLL's output frequency) by register setting. Furthermore, a clock divider which can divide clock up to 1/128 is provided to reduce the power consumption.

5.4. Power Savings Mode

The GPL95100UA provides four power modes: Operating, Deep Halt, Wait, and Halt.

Mode	CPU	System	RTC	POWEREN	After wakeup
Operating	ON	ON	ON	ON	-
Deep Halt	OFF*	OFF*	ON	OFF*	Reset System
Wait	OFF	ON	ON	ON	Next Instruction
Halt	OFF	OFF	ON	ON	Next Instruction

*OFF: In Deep Halt mode, OFF is power off; in other modes, OFF means clock off.

Entering Deep Halt/Wait/Halt mode is implemented by writing a specific value to a designated port. The wakeup source can be key-change keys or RTC wakeup.

5.5. Picture Process Unit

GPL95100UA equips a powerful process engine which has the following features.

Item	Features
Text Layer	<ol style="list-style-type: none"> 1. Maximum of three text layers at the same time. 2. Supports text size up to 1024x1024. 3. Supports Text scale effect. 4. Text1 and text2 support horizontal/ vertical compression effect. 5. Supports horizontal movement effect. 6. Supports 64-level alpha blending.
Sprite	<ol style="list-style-type: none"> 1. Maximum 256 sprites at the same time. 2. Each sprite support 64-level rotate function. 3. Each sprite supports 64-level zoom in/out function from 1/32 to 8.75 times. 4. Each sprite supports 64-level alpha blending. 5. Each sprite supports 3 kinds of mosaic effect. 6. All above function can combine at the same time.
Color	<ol style="list-style-type: none"> 1. Text layer and sprites support 4/16/64/256-color palette and RGB1555/ RGB565/ YUYV/ RGBG bitmap mode. 2. 1024 palette entry for text layers and sprites. 3. Supports 16-bit level of palette index color.
Other Features	Supports sprite DMA function.

5.6. Sound Process Unit

GPL95100UA equips a 16-channel SPU. Each channel of SPU supports PCM8/ PCM16/ ADPCM36. For software application, GPL95100UA also supports the wide-band (sample rate \geq 16KHz) low bit rate algorithm.

5.7. Video Output Interface

5.7.1. STN-LCD Interface

The STN-LCD driver interface supports LCD resolution up to 320 x

240 and supports 1/4-bit data bus for monochrome/gray-scale STN. Memory interface type CSTN is also supported.

5.7.2. TFT-LCD Interface

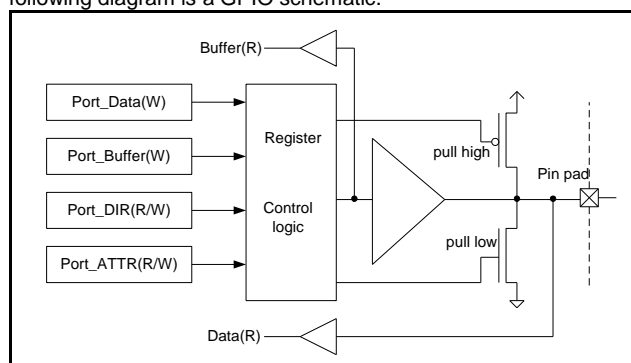
GPL95100UA supports TFT-LCD controller. The LCM interface including parallel RGB (5-6-5), serial delta RGB, serial stripe RGB, CPU (MPU) type, and CCIR601/CCIR656. The horizontal resolution of TFT controller maximum reaches 320 pixels, and the vertical resolution of TFT controller maximum reaches 240 pixels. The TFT controller mainly provides four timing control pins and 8 or 16 data pins to control external TFT panel. Those are VSYNC, HSYNC, DE, DCLK, and DATA.

5.8. Interrupt

GPL95100UA has 29 interrupt sources, grouped into FIQ (Fast Interrupt Request) and IRQ (Interrupt request). The priority of FIQ is higher than IRQ. FIQ is the high-priority interrupt and IRQ is the low-priority interrupt. An IRQ can be interrupted by a FIQ, but not by another IRQ. A FIQ cannot be interrupted by any other interrupt sources. Some of the interrupt source can be programmed as FIQ or IRQ by register setting.

5.9. GPIO

Five I/O ports are available in GPL95100UA: IOA, IOB, IOD, IOE, and IOF. IOA and IOB provide high current sink capable for LED applications. IOE are shared with ADC and IOF are shared with touch pads. Each I/O pin has its normal function and is described in the signal description section. When the normal function of the I/O is disabled, it will switch to GPIO function automatically. The following diagram is a GPIO schematic.



5.10. Timer / Counter

The GPL95100UA provides eight 16-bit timers/counters, TimerA to TimerH. The clock source of each timer can be set individually. For TimerA to TimerH, an INT will be sent to CPU when timer overflows. In addition, BAM, Capture, Comparison and PWM functions are also provided by TimerA ~ TimerE.

Clock Source A	Clock Source B
Fosc/2	2048Hz
Fosc/256	1024Hz
32768Hz	256Hz
8192Hz	Time Base B
4096Hz	Time Base A
1	0
Another Timer	1
INT1	INT2

GPL95100UA is embedded with a time base controller which is used to generate the slow and precisely interrupt from 32768Hz crystal. The following table shows the available time base.

TimeBase A	TimeBase B	TimeBase C
--	8Hz	128Hz
1Hz	16Hz	256Hz
2Hz	32Hz	512Hz
4Hz	64Hz	1024Hz

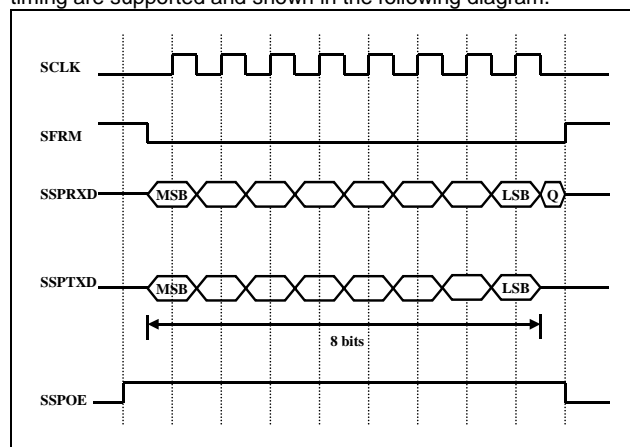
5.11. Watchdog

The purpose of watchdog is to monitor whether the system operates normally. Within a specific period, watchdog must be cleared. If not, CPU assumes program has been running into an abnormal condition. As a result, the CPU will reset the system to the initial state and start running the program all over again. In GPL95100UA, the clearance period is software programmable. If watchdog is cleared before expiration, the system will not be reset.

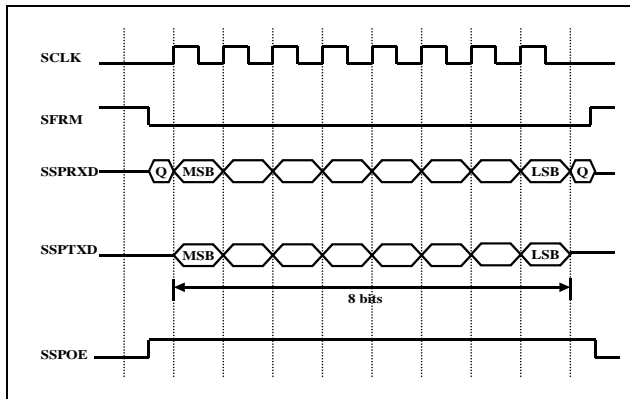
5.12. Serial Interface

5.12.1. Serial Peripheral Interface (SPI)

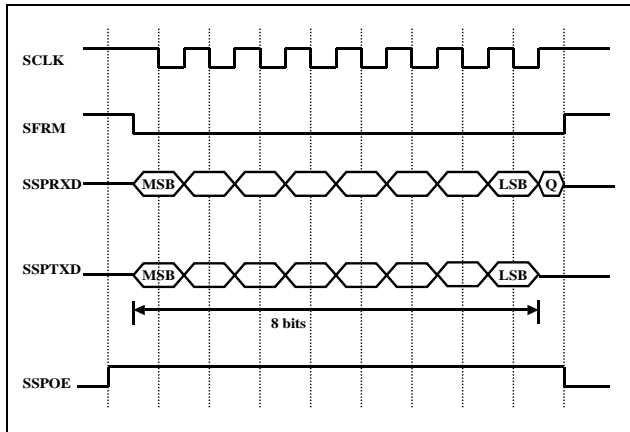
The SPI interface is a master interface that enables synchronous serial communication with slave/master peripherals. Two 8-byte FIFOs are used for transmitting and receiving data. Four types of timing are supported and shown in the following diagram.



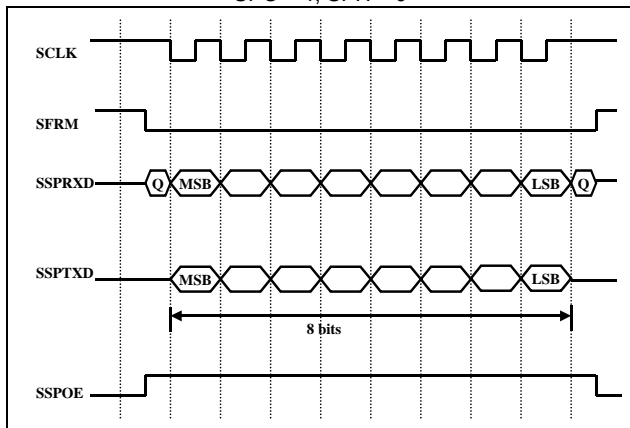
SPO = 0, SPH = 0



SPO = 0, SPH = 1



SPO = 1, SPH = 0



SPO = 1, SPH = 1

5.12.2. USB Device Function

GPL95100UA provides USB device function which is compatible with USB 1.1 and USB 2.0 full speed standard. An USB transceiver is built-in for devices function. A FIFO with size of 128x8 is used for bulk-in and bulk-out transfer and an 8-byte FIFO is used for pipe transferring control. Interrupt IN/OUT pipes are also supported. The DMA transferring is enabled for bulk-in/out to maximize the transfer performance.

5.13. IDE Tools Function

The IDE includes the following functions:

- 1). C compiler, Assembler, and Linker
- 2). Single step trace
- 3). Break point (break point for debug)
- 4). Run (execution)

5.14. Real Time Clock (RTC)

The RTC block provides the alarm function, schedule function, and hour/minute/second/half-second interrupt function.

5.15. Analog Control

5.15.1. DAC/AMP control

A 16-bit stereo DAC (2ch) is embedded in GPL95100UA. For both left and right channels, a 16x16 FIFO is used to avoid sound glitch when CPU is busy. The left and right channels do not need to have the same sample rate. A single DMA channel can use the stereo playback. A push-pull AMP is built in for speaker applications.

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Rating

Rating	Symbol	Value	Unit
Supply Voltage 1	V33_DVCC V33_IOF V33_PLL V33_ADC V33_USB	-0.3 to 4.0	V
Supply Voltage 2	V18_DVCC V18_RTC	-0.3 to 2.16	V
Supply Voltage 3	V50_IOAB V50_DAC V50_AMP V50_LDO	-0.3 to 5.5	V
Input Voltage	V _{IN}	-0.3 to 4.0	V
Operating Temperature	T _A	0 to 70	°C
Storage Temperature	T _{STG}	-40 to +150	°C

6.2. DC Characteristics

Characteristic	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Operating Voltage 1	V33_DVCC V33_IOF V33_PLL V33_ADC V33_USB	2.7 3.0 ¹	3.3	3.6	V	-
Operating Voltage 2	V18_DVCC V18_RTC	1.62	1.8	1.98	V	-
Operating Voltage 3	V50_IOAB V50_DAC V50_AMP V50_LDO	2.9 3.3 ¹	3.6	5.5	V	-
Operating Current	I _{OP}	-	55 ²	-	mA	@96MHz, 3.3V, all clocks on
Power Down Current	I _{PD}	-	5	25	μA	All power off except RTC
Halt mode Current	I _{HALT}	-	40	85	μA	3.3V, system clock off, Internal Power on, RTC ON
High Input Voltage	V _{IH}	0.7*V _{source} ³	-	V _{source} ³	V	-
Low Input Voltage	V _{IL}	V _{SS}	-	0.8	V	-
Output High/Low Current (I/O)	I _{OH}	-	4 ⁴	-	mA	IO is 3.3V, VOH=0.7*VDDIO and IO driving set as 4mA.
	I _{OL}	-	7 ⁴	-	mA	IO is 3.3V, VOL=0.3*VDDIO and IO driving set as 4mA.
IO Input Pull-Low Resistor	R _{PL}	-	95K	-	OHM	IO 3.3V on PA/PB/PD/PE/PF
	R _{PL}	-	70K	-	OHM	IO 4.5V on PD/PE/PF

Characteristic	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
IO Input Pull-High Resistor	R _{PH}	-	95K	-	OHM	IO 3.3V on PA/PB/PD/PE/PF IO 4.5V on PD/PE/PF
	R _{PH}	-	70K	-	OHM	IO 4.5V on PA/PB
Crystal Frequency	-	-	32768	-	Hz	-
System Clock	F _{SYS}	256Hz	48	96	MHz	-

Note1: When USB function is enabled, the minimum voltage of operation voltage 1 is 3.0V and 3.3V for operating voltage 3.

Note2: Operating current depends on software code. In this test case, all clocks are on and system is in idle mode.

Note3: Vsource may be V33_DVCC, V33_IOF, V33_ADC or V50_IOAB.

Note4: IO driving can be setup by program. There are 4mA/8mA/12mA/16mA can be setup and default driving is 4mA.

6.3. Audio DAC Characteristics

Characteristic	Limits			Unit	Condition
	Min.	Typ.	Max.		
Resolution	-	16	-	Bit	-
Full Scale Output Voltage	-	0.6*VDDDA	-	Vp-p	-
THD+N (f = 1kHz)	-	0.1	-	%	-
Noise at No Signal	-	-90	-	dBrA	-
Frequency Response	20	-	19200	Hz	-

6.4. SAR ADC Characteristics

Characteristics	Symbol	Limits			Unit
		Min.	Typ.	Max.	
SAR ADC Input Voltage Range	VIN_RANGE	2.7	-	3.6	V
Resolution of ADC	RESO	12	12	12	bit
Signal-to-Noise Plus Distortion of ADC from Line in	SINAD (Note 1)	58	60	62	dB
Effective Number of Bit	ENOB (Note 2)	9.0	9.66	10	bit
Integral Non-Linearity of ADC	INL	-	+/-3	-	LSB (Note 3)
Differential Non-Linearity of ADC	DNL	-	+/-2	-	LSB
No Missing Code		10	11	12	bit
AD Conversion Rate=ADCCLK/16	F _{CONV}	-	-	125K	Hz

Note1: The SINAD testing condition at VINLp-p = 0.8 * V33_AD, F_{CONV} = 62.5KHz, Fin = 1.0KHz Sine waves at V33_AD = 3.0V from ADC input.

Note2: ENOB = (SINAD - 1.76) / 6.02.

Note3: LSB means Least Significant Bit (at 12-bit resolution).

6.5. LDO18 Characteristics

Characteristics	Symbol	Unit			Unit
		Min.	Typ.	Max.	
Input Voltage	VREGI	2.7	3.3	3.6	V
Maximum Current Output	IREGO	-	140	280	mA
Output Voltage	VREGO	1.33 ¹	1.8	1.995	V
Standby Current	IREGS	-	3	-	-

Note1: To save more power, it is recommended switching to 1.4V before entering the halt mode and switching to 1.8V in normal operation mode.

6.6. LDO33 Characteristics

Characteristics	Symbol	Unit			Unit
		Min.	Typ.	Max.	
Input Voltage	VREGI	2.9	3.6	5.5	V
Maximum Current Output	IREGO	-	350	700	mA
Output Voltage	VREGO	2.85	3.3	3.465	V
Standby Current	IREGS	-	3	-	-

7. RECOMMENDED BOARD LAYOUT

7.1. Power and Ground

All digital power and ground should be connected. The decoupling capacitor of 0.1 μ F and 10 μ F should be connected to each power pin of the IC as the following diagram. The power of analog parts should be connected from power source with high quality.

7.2. Analog Section

A specific AGND ground plane, connected by a single trace to the GND ground, should be provided. No digital signal should cross the AGND plane. AVREF_ADC should be connected to a 1 μ F capacitor.

8. ORDERING INFORMATION

8.1. Ordering Information

Product Number	Package Type
GPL95100UA - NnnV - C	Chip Form
GPL95100UA - NnnV - QL09x	Halogen Free Package

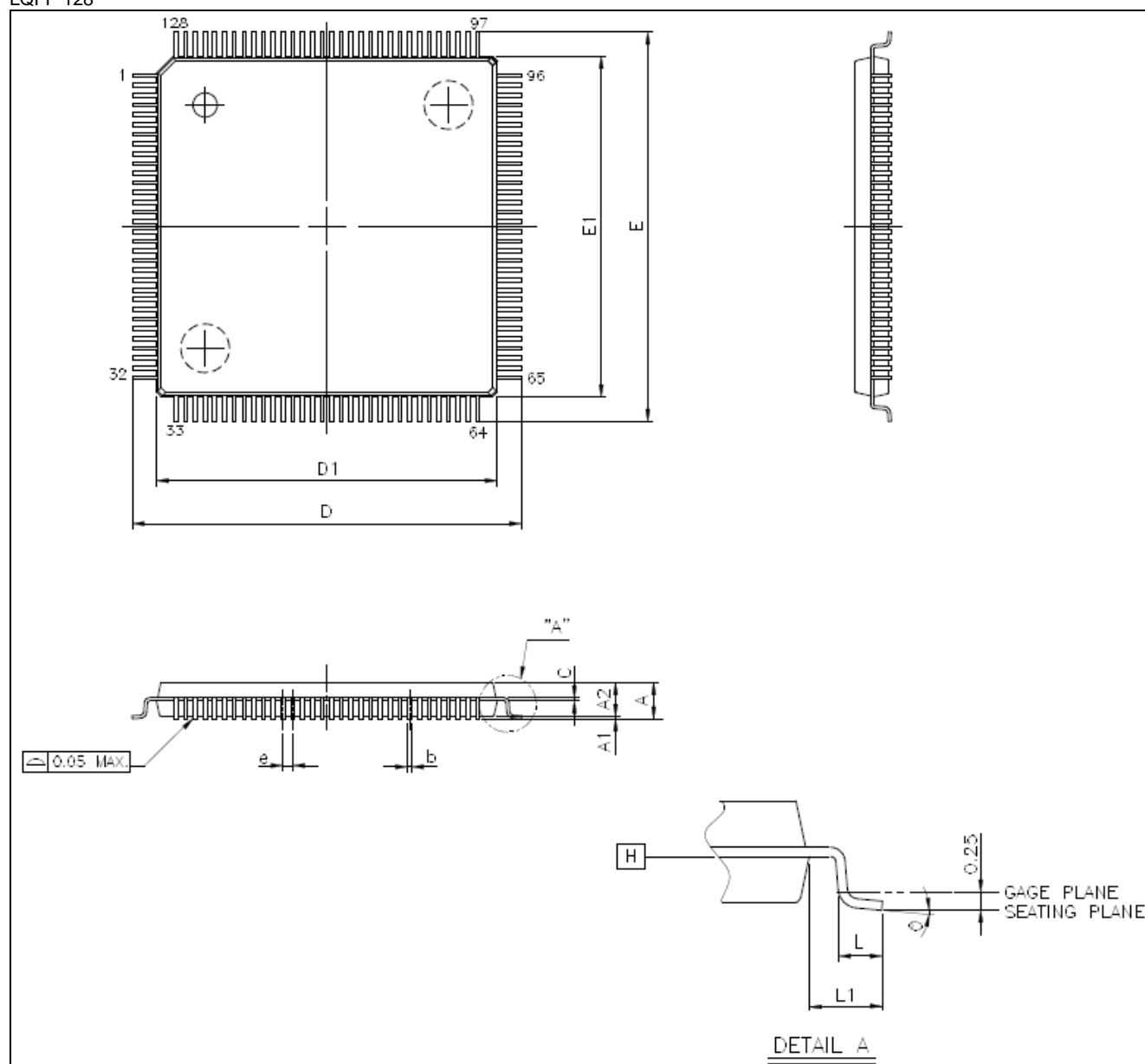
Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

Note3: Package form number (x = 1 - 9, serial number).

8.2. Package Information

LQFP 128



Symbol	Millimeter		
	Min.	Nom.	Max.
A	--	--	1.60

Symbol	Millimeter		
	Min.	Nom.	Max.
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.13	0.16	0.23
C	0.09	--	0.20
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

9. DISCLAIMER

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10. REVISION HISTORY

Date	Revision #	Description	Page
Jan. 16, 2019	1.0	1. Modify NAND Flash controller support 4-bit BCH to 4-bit/8-bit BCH	4
		2. Modify DAC descriptions from "Two 16-bit DACs (R2R DAC for L-R speaker), 1x14-bit push-pull AMP " to "16-bit stereo L and R DAC output that can be added external amplifier. Or mix L_R internally then through a push pull amplifier output, which can driver external speaker directly."	5
		3. Modify 8 timers for PWM to 6 timers for PWM	5
		4. Modify Audio DAC Characteristics	17
		5. Add SAR ADC Characteristics	17
Oct. 24, 2016	0.3	1. Modify Timer from 5 sets to 8 sets.	4
		2. Modify operating voltage low bond to 2.9V/2.7V	4
		3. Modify LVR voltage descriptions.	5
		4. Modify pin descriptions.	6-9
		5. Modify chapter 5.4 Halt mode POWEREN to OFF.	12
		6. Remove IOC from chapter 5.9	13
		7. Modify Chapter 6. Electrical Specifications.	16-17
Jun. 16, 2016	0.2	1. Remove velocity key descriptions.	5
		2. Fix typo in signal description chapter	6-9
		3. Modify pin description and pin name	7,10,11
Mar. 18, 2016	0.1	Preliminary version.	22