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MAXIMIZING THE EFFECTIVENESS OF YOUR SMD ASSEMBLIES

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IR Application Note –994 (Rev. 5)

Title: Maximizing the Effectiveness of Your SMD[1] Assemblies

Topics Covered:

- Section I: How we Measure $R_{th\ (JA)}$
- Section II: Thermal Characterization of Surface Mount Packages
- Section III: Attachment to board
- Section IV: Solder Pastes
- Section V: Heat Profiles
- Section VI: Rework

Section I: How we measure $R_{th\ (JA)}$

Herein is described the device mounting and heat sinking used and the test methods employed to measure Thermal Resistance of the various packages. Standard printed circuit boards were developed to which devices were solder-mounted for measuring thermal resistance. FR-4 material with 2 oz. Cu was used. Board dimension were 4.75 inches by 4.5 inches and backside of board had full metal pattern. Three different PCB metallization patterns were tested: one with 1 sq inch of Cu area, the second one with Cu trace minimized so as to cover only as much area as taken up by the Device Under Test (DUT) and necessary lead mounting pads (described as "modified minimum pattern"), and the last one is the "absolute minimum" pattern with the metallized area sized only as needed to mount each lead. (See the figure 1.)

Thermal Resistance was measured according to industry practice by first performing a reference temperature estimate; a temperature sensitive electrical parameter (TSEP) such as Vsd is measured and compared with a calibration value to determine Tj. Then a heating pulse of known power is applied followed by a second TSEP measurement. That measurement was compared to a calibration table to estimate junction temperature and calculate the temperature rise due to the heating pulse. From the familiar equation:

$$\Delta T = R_{TH} \times P_D \qquad \text{(equation 1)}$$

And where:

$\Delta T = T_J - T_{Ref}$ Temperature difference (C) between junction temperature and reference temperature (here ambient, case temperature or package lead),

R_{TH} = Thermal Resistance (C/W) between junction and reference point (again ambient, case temperature or package lead),

P_D = Power dissipated (W)

We can calculate the thermal resistance by plugging in the measured values of temperature rise and power. In this way measurements were taken on representative samples of all packages listed in the table below.

Package type	R_{th} (Sample Size 3 pc/package type)						
	1sq"		Modified Minimum		Minimum		Typ $R_{th(JL)}$ *
	Typ $R_{th(JA)}$	Max $R_{th(JA)}$	Typ $R_{th(JA)}$	Max $R_{th(JA)}$	Typ $R_{th(JA)}$	Max $R_{th(JA)}$	
u-3	169.2	230.0	237.1	308.2	263.6	342.6	139.3
TSOP6 (Dual)	73.4	125.0	134.7	175.1	170.7	222.0	35.5
TSSOP8	60.9	83.0	106.4	138.3	117.0	152.1	35.5
u-6	47.1	75.0	112.5	146.3	124.9	162.4	14.7
u-8	39.9	70.0	102.4	133.2	126.1	163.9	17.0
TSOP6 (Single)	47.3	62.5	112.0	145.6	118.5	154.0	17.0
SO-8 (Dual)	54.5	62.5	73.1	95.1	94.7	123.1	28.7
SOT-223	27.2	60.0	49.0	63.7	66.1	86.0	4.9
SO-8	33.5	50.0	66.3	86.2	70.6	91.8	10.6
D-Pak	20.2	26.3	42.0	54.6	59.5	77.3	2.0
D2-Pak	18.0	23.3	33.6	43.7	36.7	47.7	1.6

NOTE:
A specific thermal test board was used for Direct FET package due to the uniqueness of the Direct FET connections to the PCB. Therefore thermal resistance results are illustrated by providing two tables. However, in order to improve document readability, the graphical illustrations remain grouped together.

Package type	R_{th} (Sample Size 3 pc/package type)						
	1sq"		Modified Minimum		Minimum		Typ $R_{th(JL)}$ *
	Typ $R_{th(JA)}$	Max $R_{th(JA)}$	Typ $R_{th(JA)}$	Max $R_{th(JA)}$	Typ $R_{th(JA)}$	Max $R_{th(JA)}$	
Small-can DirectFET	32.1	60.0	49.2	64.0	68.1	88.5	NA
Mid-can DirectFET	32.3	60.0	55.6	72.3	62.2	80.9	NA

Figure 1.

1 This application note applies only to surface mountable type devices. Through-hole devices such as TO-220, TO-247, Fulpak, etc are excluded and not covered by this note.

Section II: Thermal Characterization of Surface Mount Packages

Table 1 shows typical and Maximum $R_{th\ (JA)}$ and typical $R_{th\ (JL)}$ values of the SMD packages presently offered by International Rectifier. For $R_{th\ (JC)}$ values, please refer to the appropriate data sheet.

Measurements are provided for devices mounted on three different PCB patterns: 1 square inch ("1 sq"), modified minimum area, and minimum area, as described graphically in Figure 1.

Based on the Max $R_{th\ (JA)}$ values in Table 1 please see in Figures 2-4 the graphs of power dissipation vs. ambient temperature for each type of PCB pattern.

Note that generally the larger packages with exposed heat sinks (D2-Pak, D-Pak & SOT-223) have the highest Power Dissipation capabilities.

Note also that the larger the metallized PCB pattern area, the lower will be the thermal resistance. Measurements at 3 different PCB pattern Areas reflect this sensitivity.

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D2-Pak	18.0	23.3	33.6	43.7	36.7	47.7	1.6

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	Typ $R_{th(JA)}$	Max $R_{th(JA)}$	Typ $R_{th(JA)}$	Max $R_{th(JA)}$	Typ $R_{th(JA)}$	Max $R_{th(JA)}$	
Small-can DirectFET	32.1	60.0	49.2	64.0	68.1	88.5	NA
Mid-can DirectFET	32.3	60.0	55.6	72.3	62.2	80.9	NA

Table 1: R_{th} typical and max values for various SMD packages

NOTES:
1. * The $R_{th\ (JL)}$ & the $R_{th\ (JA)}$ 1sq" were measured at the same time. R_{th} reference to drain lead.
2. See Section I for details of measurement conditions.
3. The PCB contributes greatly to the total $R_{th.}$ If PCB material properties or dimensions vary significantly from those used by IR, actual $R_{th\ (actual)}$ results may also vary.

Figure 2: Mod Min Power Dissipation (T_ambient)

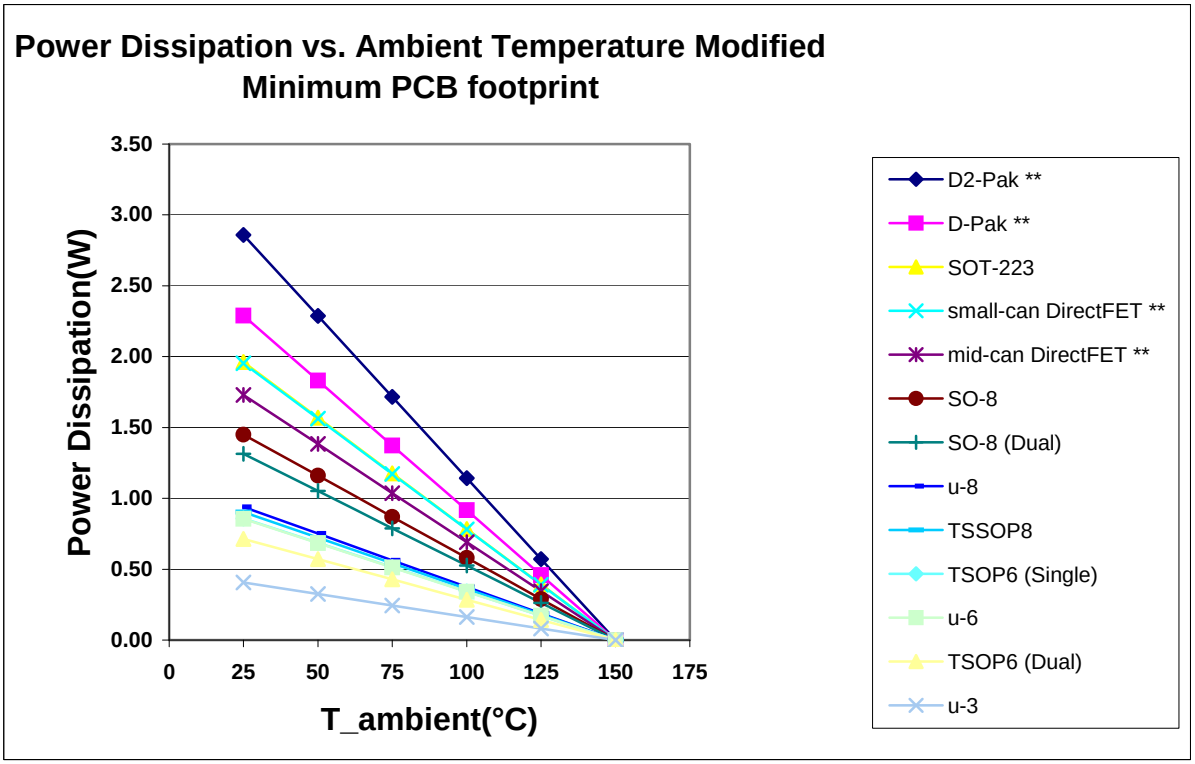


Figure 3: 1 sq" Power Dissipation (T ambient)

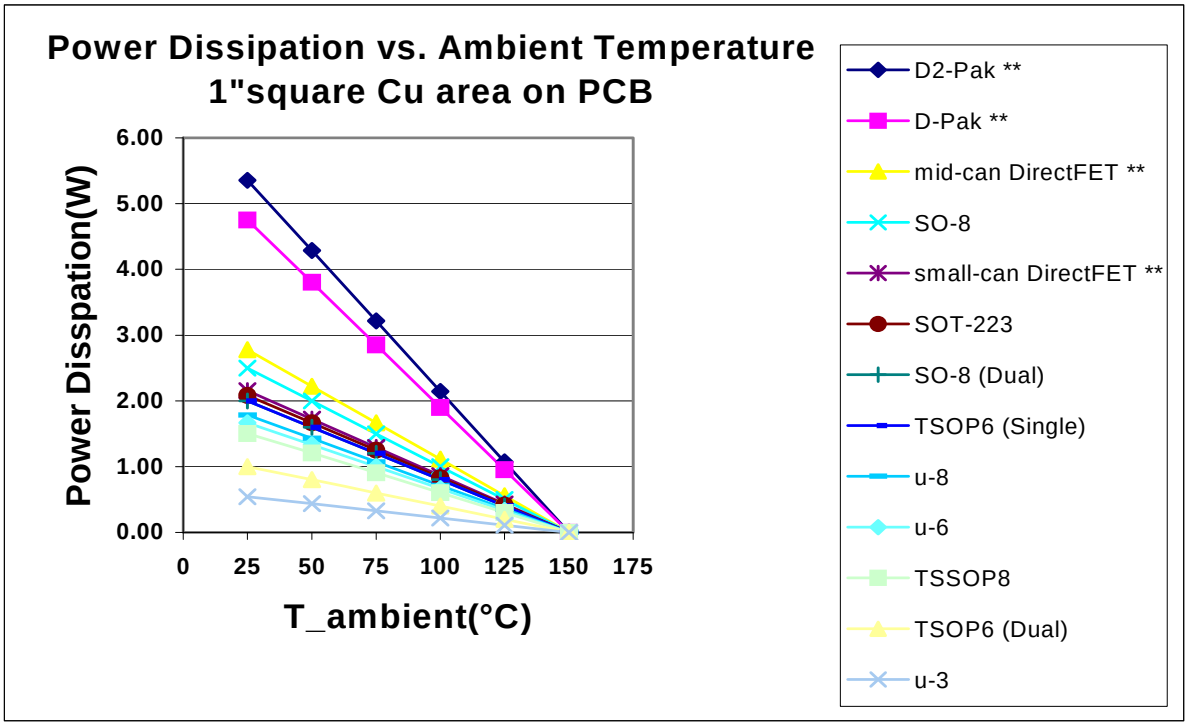
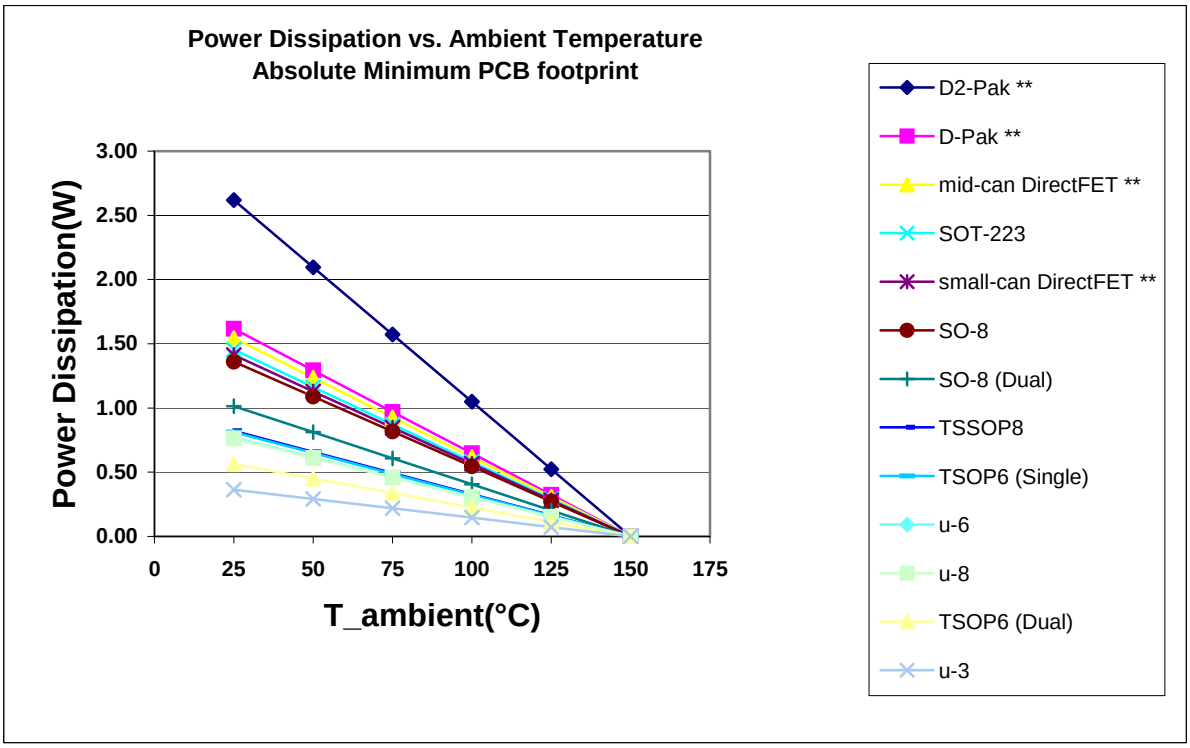


Figure 4: Absolute Min Power Dissipation (T ambient)



Section III: Attachment to board:

Most designers and technicians in the electronic industry are familiar with printed circuits that are provided with holes to support leaded components during the soldering process. Surface mount components on the other hand are by definition leadless and rely on the strength of the solder joint alone for mechanical as well as electrical connection. Many PCB assemblies require the mounting of devices on both sides of the board. The reflow process is typically performed once. Both sides of the board are pasted at the same time. Components are then placed on the topside only. An adhesive is then applied to the topside to hold the components in place. The board is then inverted 180 degrees and the second side is populated with components. At that point the populated board is ready for the thermal process that will melt the solder paste and attach the components to the board. After the mounting process is complete the adhesive serves no further purpose.

The adhesives used must provide sufficient tenacity to prevent component movement during handling and soldering. At the same time, the adhesive should provide a bond that can be broken with minimal disturbance to the populated board in order to replace incorrect components before soldering. It must also be capable of maintaining adhesion during the preheat cycle and it should not become a deterrent to solder flow during the reflow or wave soldering process. Typical adhesives of this type are made from non-activated resins (R), which can be used in forming gas atmosphere to reduce oxides. Some are mildly activated resin (RMA), which can be used in normal factory environment. The activation in this case is used to reduce small amounts of oxidation of the solderable surfaces and the solder particles in the paste.

Section IV: Solder Pastes:

There are a wide variety of solder pastes available for surface mounting applications. Typical solder pastes are composed of a homogeneous mixture of pre alloyed solder powder with a specific grain size. Fluxes are also provided in the solder paste mixture as a necessary component of the surface mounting process.

In today's densely populated assemblies, pin spacing of SMD components has significantly been reduced. Pin spacing of less than 0.4mm is common which poses problem such as solder bridging, insufficient solder on the lead and device placement accuracy. Solder stencil thickness, dimension and registration accuracy, solder paste composition and particle size are all critical to successful soldering of these assemblies.

With the advanced state of the art of fine pitch device technology, a simple guideline for the choice of solder paste is outside the scope of this document. The customer should seek expert guidance from the solder paste vendor and PCB board fabricator for detailed, application specific recommendations.

Section V: Heat profiles
Reflow Soldering Heat Profiles

A major problem associated with surface mounting of electronic components, especially those with mismatched internal expansion coefficients is the thermal shock of the soldering process. The advent of lead free assemblies has driven the requirement to develop and implement new handling techniques for surface mounting devices. Typical lead free solders have higher melting point temperatures than the traditional Pb based solders. Whereas previously, assemblies could be mounted at peak reflow temperatures in the range of 220°C to 245°C, Pb free assemblies require reflow temperatures in the range of 245°C to 260°C. The higher peak reflow temperatures require careful control of the reflow environment to prevent over temperature conditions that can severely degrade the reliability of surface mount devices. Caution must be taken when choosing the reflow profile in order to optimize the thermal stresses that are applied to either Pb based or Pb free assemblies.

In addition to the over temperature considerations, under temperature conditions can in turn result in a failure of the mechanical attachment of the device during the reflow profile. A carefully controlled preheat and post-cooling sequence is necessary. Properly controlling the preheat cycle will remove any volatile component of the solder paste such as alcohol or water by evaporation prior to the solder fusing cycle. This will reduce the chances of forming void or solder ball.

This thermal conditioning can be applied in several ways such as using Infrared/Convection ovens, Vapor Phase, or Wave Solder equipments. The recommended thermal conditioning methods are the Infrared/Convection Soldering Temp / Time Profile and wave solder described below:

A) Infrared/Convection Soldering Temp/Time Profile.

The critical parameters are shown in table 2 by solder paste type and device volume.

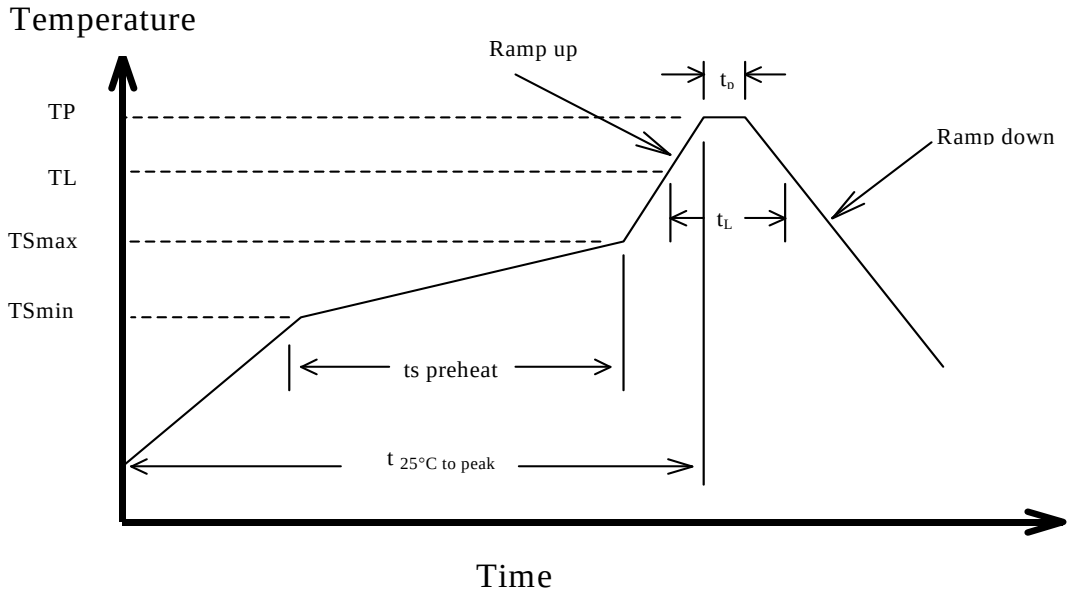


Table 2

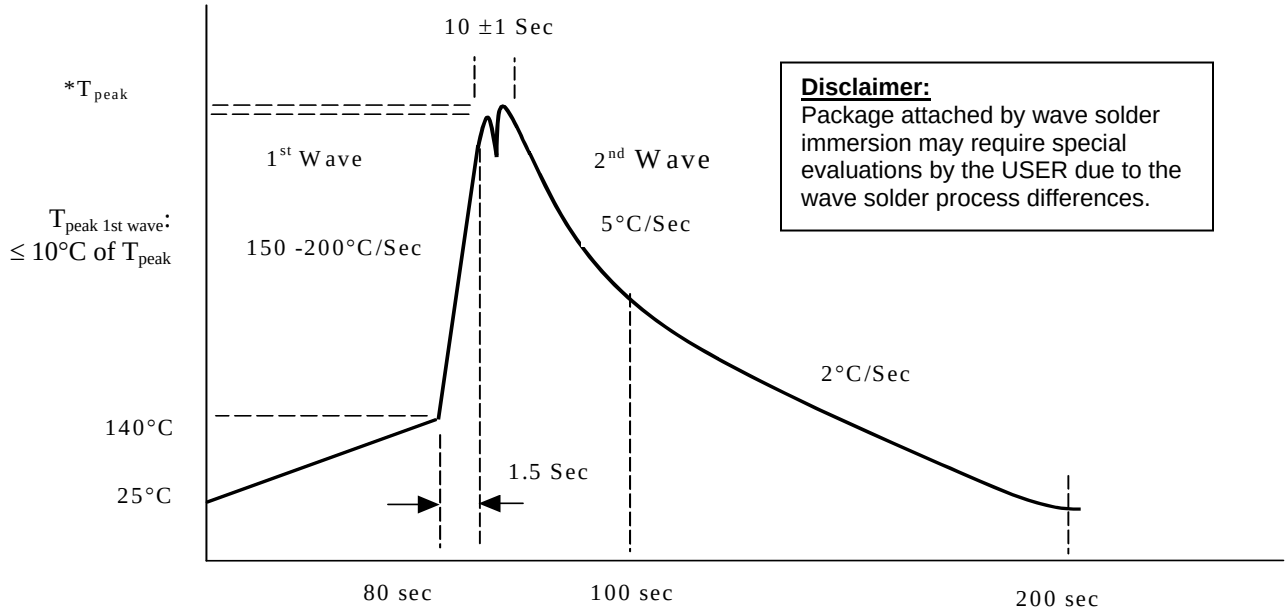
Profile Feature	Sn-Pb Eutectic Assembly		Pb Free[2] Assembly	
	*Large Body	**Small Body	*Large Body	**Small Body
Ave ramp up rate (TL to Tp)	3°C/Sec maximum		3°C/Sec maximum	
Preheat • Temp Min (Tsmin) • Temp Max (Tsmax) • Time (min to max) ts	100°C 150°C 60 – 120 sec		150°C 200°C 60 - 180 sec	
Tsmax to TL Ramp up rate	-		3°C/Sec maximum	
Time maintained above: • Temp (TL) • Time (tL)	183°C 60 – 150 sec		217°C 60 – 150 sec	
Peak Temperature (Tp)	225°C +0/-5°C	240°C +0/-5°C	260°C +0/-5°C[3]	
Time within 5°C of actual peak temperature (tp)	10 – 30 sec	10 – 30 sec	10 – 30 sec	
Ramp-down rate	6°C/sec maximum		6°C/sec maximum	
Time 25°C to Peak temperature	6 minute maximum		8 minute maximum	

- Large Body: TO-220, D2pak and larger (Package Thickness ≥2.5 mm or Package Volume ≥ 350 mm^3
- Small Body: Dpak, Ipak and smaller (Package Thickness < 2.5 mm or Package Volume < 350 mm^3))

Table 2

[2] Devices that are lead free have the suffix “Pbf” in the part number. If unsure of the status of a device, contact the Sales Representative or the factory.
[3] The recommended peak reflow temperature for some large body packages (i.e. PLCC-44 / MQFP64) is 250°C +0/-5°C. If unsure, contact the sales representative for details.

B) Wave Soldering Temp/Time Profile.



Double Wave Soldering Temperature/Time Profile

Wave Solder Evaluation for Various Packages

Package	Reflow Temp	REMARKS
DPAK	235	***Non-Pb-Free****
SOICN-8L	240	***Non-Pb-Free***
SOICW-28L	240	***Non-Pb-Free***
SOICN-14L	240	***Non-Pb-Free***
D2PAK	225	***Non-Pb-Free***
SOICW-16L	240	***Non-Pb-Free***
D2PAK	260	**Pb-Free**
DPAK	260	**Pb-Free***
SOICN-14L	260	**Pb-Free**
SOICN-16L	260	**Pb-Free**
SOICN-8L	260	**Pb-Free**
SOICW-16L	260	**Pb-Free**

* Contact manufacturer for further information

Pb-Free/Eutectic Reflow Recommendation

Package	Package Body	Reflow 1 Pb-Free @	Reflow 2 Eutectic @
DPAK	S	260	245
D2PAK	L	250	225
TO-220	L	250	225
TO-247	L	250	225
TO-262	L	250	225
D-61-8	L	250	225
PDIP-8	L	250	225
PDIP-14	L	250	225
PDIP-16	L	250	225
PDIP-20	L	250	225
PDIP-28	L	250	225
SOICN-8	S	260	245
SOICN-14	S	260	245
SOICN-16	S	260	245
SOICW-16	S	260	245
SOICW-20	S	260	245
SOICW-28	S	260	245
Micro-3/SOT 23	S	260	245
Micro-6/TSOP 6	S	260	245
Micro-8	S	260	245
SMA	S	260	245
SMB	S	260	245
SMC	S	260	245
MLP-6 3x3	S	260	245
MLP-20 4x4	S	260	245
MLP-28 5x5	S	260	245
MLP-48 7 x 7	S	260	245
TSSOP8	S	260	245
SSOP 20	S	260	245
TSSOP24	S	260	245
PLCC44	L	250	225
SOT 223	S	260	245
MQFP 64	L	250	225

Thickness> 2.5 mm or volume > 350 mm^3, reflow 250+0/-5C (Pb-Free), 225 +0/-5C (SnPb Eutectic)

Thickness < 2.5 mm and volume < 350 mm^3, reflow 260 +0/-5C (Pb-Free), 240 +0/-5C (SnPb Eutectic)

Section VI: Rework

The primary problem in replacing soldered SMDs on substrates is how to apply sufficient heat to simultaneously fuse all the connections on the component to be replaced without overheating the adjacent components on the substrate itself. Soldering irons with specially shaped tips are usually used for this purpose and because of the multiplicity of SMD package styles a corresponding variety of soldering tips is required. These tips also must have a gripping function so that when the solder is reflowed the device can be extracted from the board assembly.
When a new device is to be mounted into an SMD assembly, the tool must perform the reverse procedure. The new part must be fluxed prior to local reflow as described.