Electronic Devices

Lab Report

GUID:2839915 UESTC ID:2022190504031 Name: He WenXiao

Abstract

This is the report of the 3 lab sessions of the course Electronic Devices. Lab session 1 was about exploring the characteristics of forward basis and reverse basis of diodes. Lab session 2 required conducting a basic research on Bipolar Junction Transistor(BJT). Lab session 3, however, was a coursework regarding the Junction Field-effect Transistor(JFET). All of these three components are essential to modern electronic engineering. These three lab sessions provided valuable hands-on experience and a deeper understanding of fundamental semiconductor devices.

Introduction

Semiconductor

A substance that can conduct electricity is named a conductor, on the contrary, a substance that can not conduct electricity is named insulator. Semiconductors, however, have conducting properties which are between conductor and insulator. Due to their unique characteristics, semiconductors-related technologies are widely applied in electronic industries such as ICs(integrated circuits) production.[1]

Doping

The majority of semiconductors are silicon. Unfortunately, the pure silicon's conductivity is too small($\sigma \approx 1.56 \times 10^{-3} S/m$). Therefore, doping is required for industrial practices. There are two types of doping. N-type means adding elements whose valence electrons are more than that of silicon such as phosphorus. P-type indicates adding elements whose valence electrons are less than that of silicon, for example, boron. A very small amount of doping can significantly increase the conductivity of semiconductors.

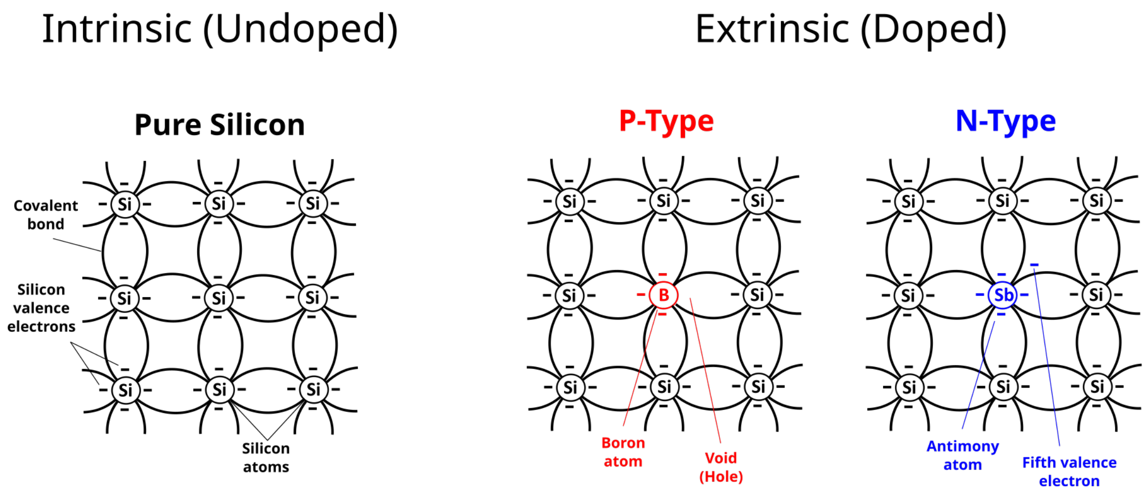


Figure 1: Doping

PN junction and diodes

A diode is constructed with a P-type semiconductor and a N-type Semiconductor connected in series.

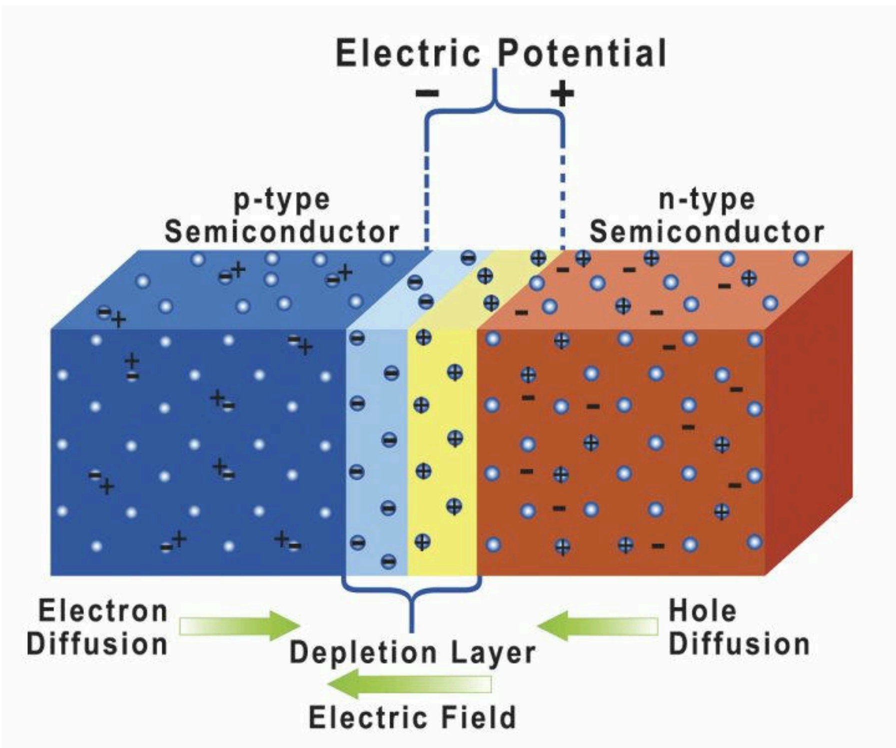


Figure 2: PN junction

The region where two types of materials contact forms the PN junction[2]. The holes which carry positive charges in P-type semiconductors can move freely, while the electrons which carry negative charges in N-type semiconductors can move freely. They both initially flow to another type because of concentration difference. As the holes and electrons carry different types of charges, they will neutralize in region near the contact forming the depletion layer. As these carriers continued to move, the holes that have entered N-type semiconductor and the electrons that have entered T-type semiconductor will form an electric field from N region to P region. This electronic will prevent more carriers from diffusion. A stable depletion layer will establish with this negative feedback mechanism[3]. When a positive voltage is applied between the P region and N region like Figure 3, the external voltage can promote the carriers' diffusion, thinning the depletion layer. The current can be easily established.

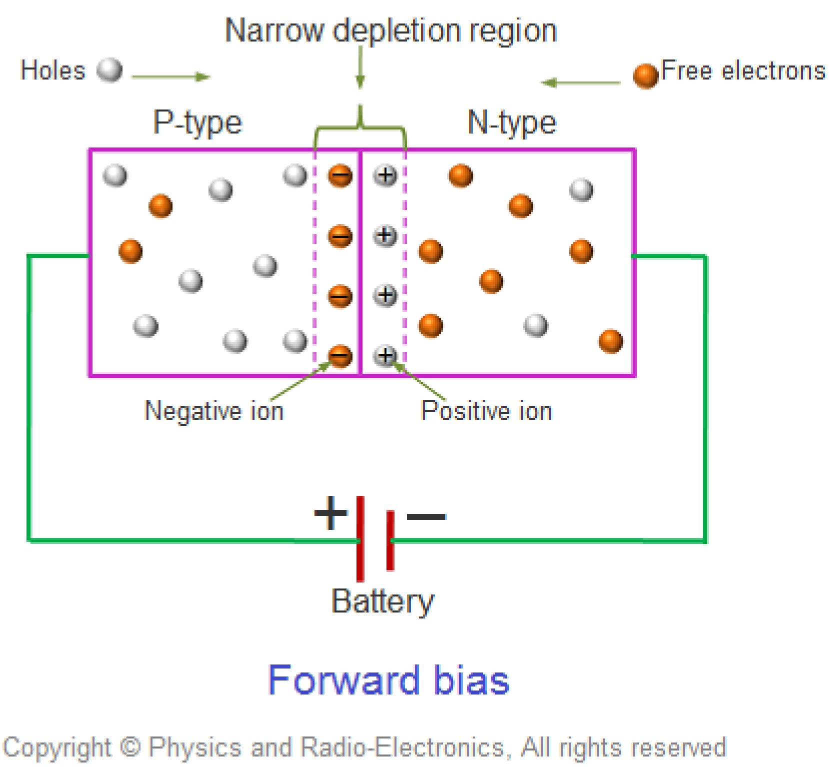


Figure 3: Forward bias

The opposite setup in Figure 4, which is called reverse bias, will thicken the depletion layer and prevent current from establishing.

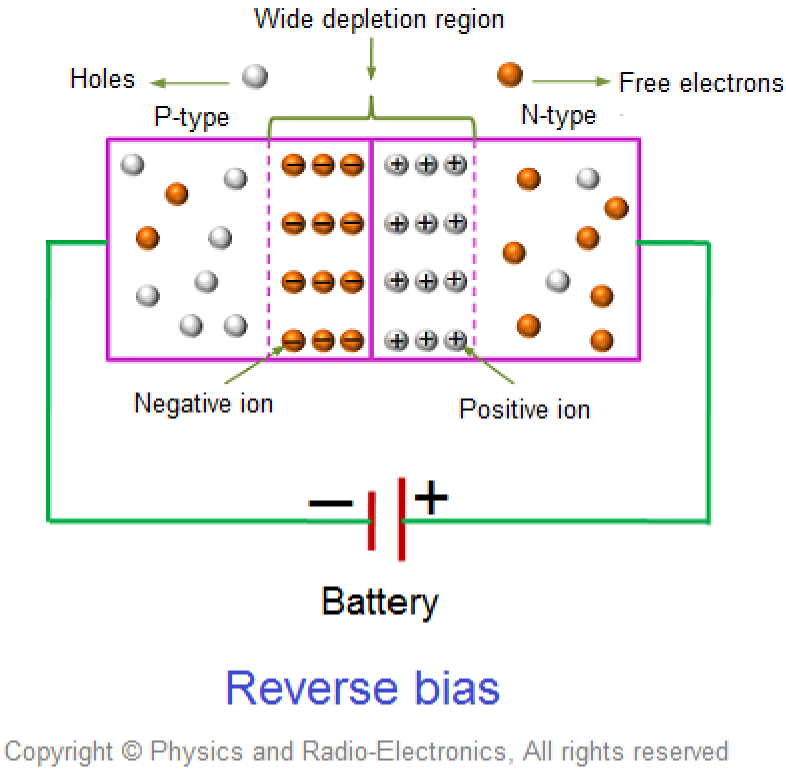


Figure 4: Reverse bias

This explains the one-way conduction property of diodes.

Bipolar Junction Transistor(BJT)

The bipolar junction transistors(BJTs) consists of three blocks of semiconductors. Depending on permutations, it can categorized as NPN(Figure 5) and PNP(Figure 6).BJT can be used to amplify the current or work as a switch to control the current. The two terminals of BJT are called emitter and collector, the pole connected to the central region is called the base. A BJT contains two PN junctions. The BJT have four working states—cutoff, active, saturation and breakdown.

Working states	PN junction near emitter	PN junction near collector
Cutoff	Reverse biased	Reverse biased
Active	Forward biased	Reverse biased
Saturation	Forward biased	Forward biased
Breakdown	Reversed biased	Breakdown

Table 1: Working states of BJT

This lab session focused on the active and saturation regions. In active regions, the BJT satisfies:

$$I_E = I_B + I_C$$

$$I_C = \beta I_B$$

$$V_{\text{CE}} > V_{\text{ce satuation}}$$

Ideally, in this region, I_C only depends on I_B regardless of V_{CE}.

When $I_B \approx 0$, $I_C \approx 0$, BJT is in the cutoff region.

In saturation region, I_C mainly depends on V_{CE} and it can be complex.

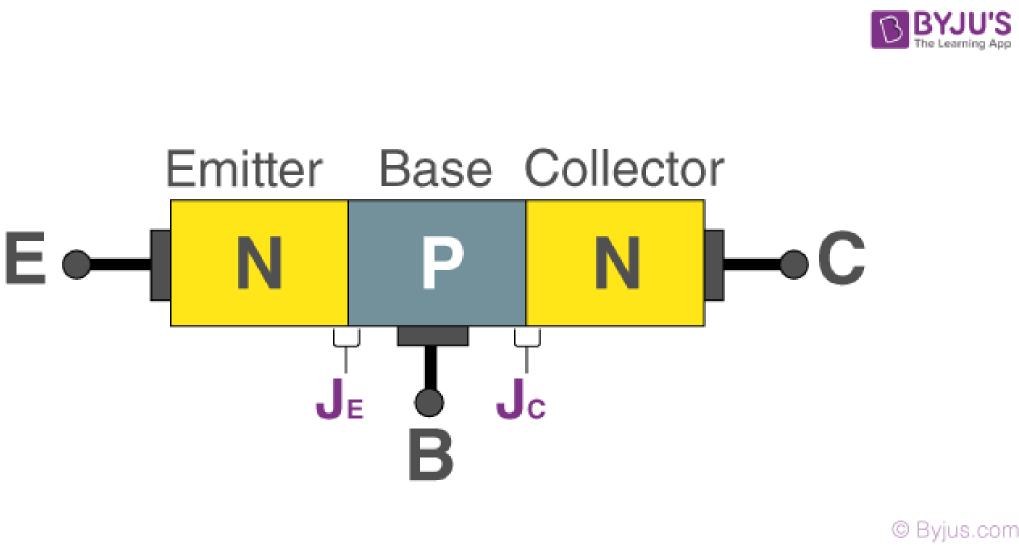


Figure 5: NPN BJT

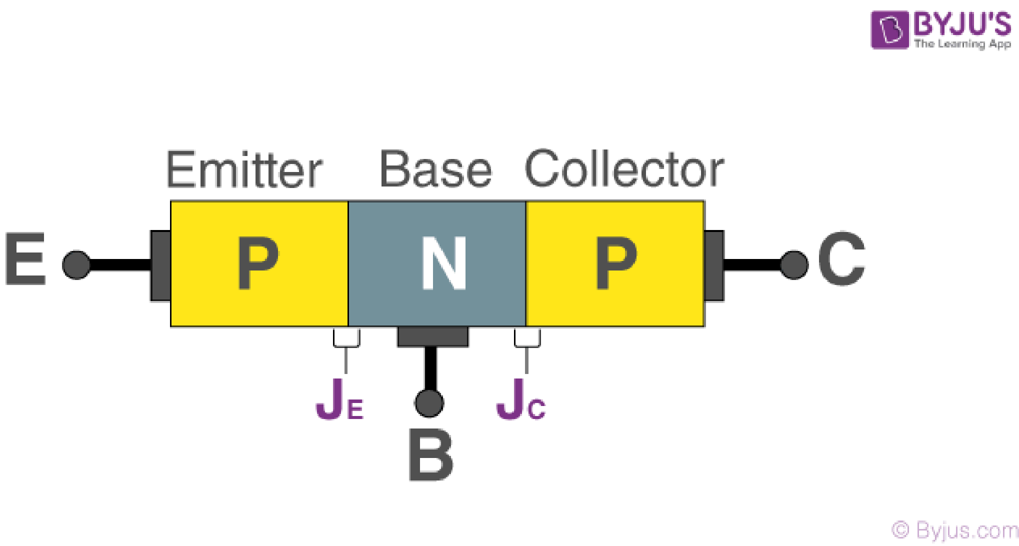


Figure 6: PNP BJT

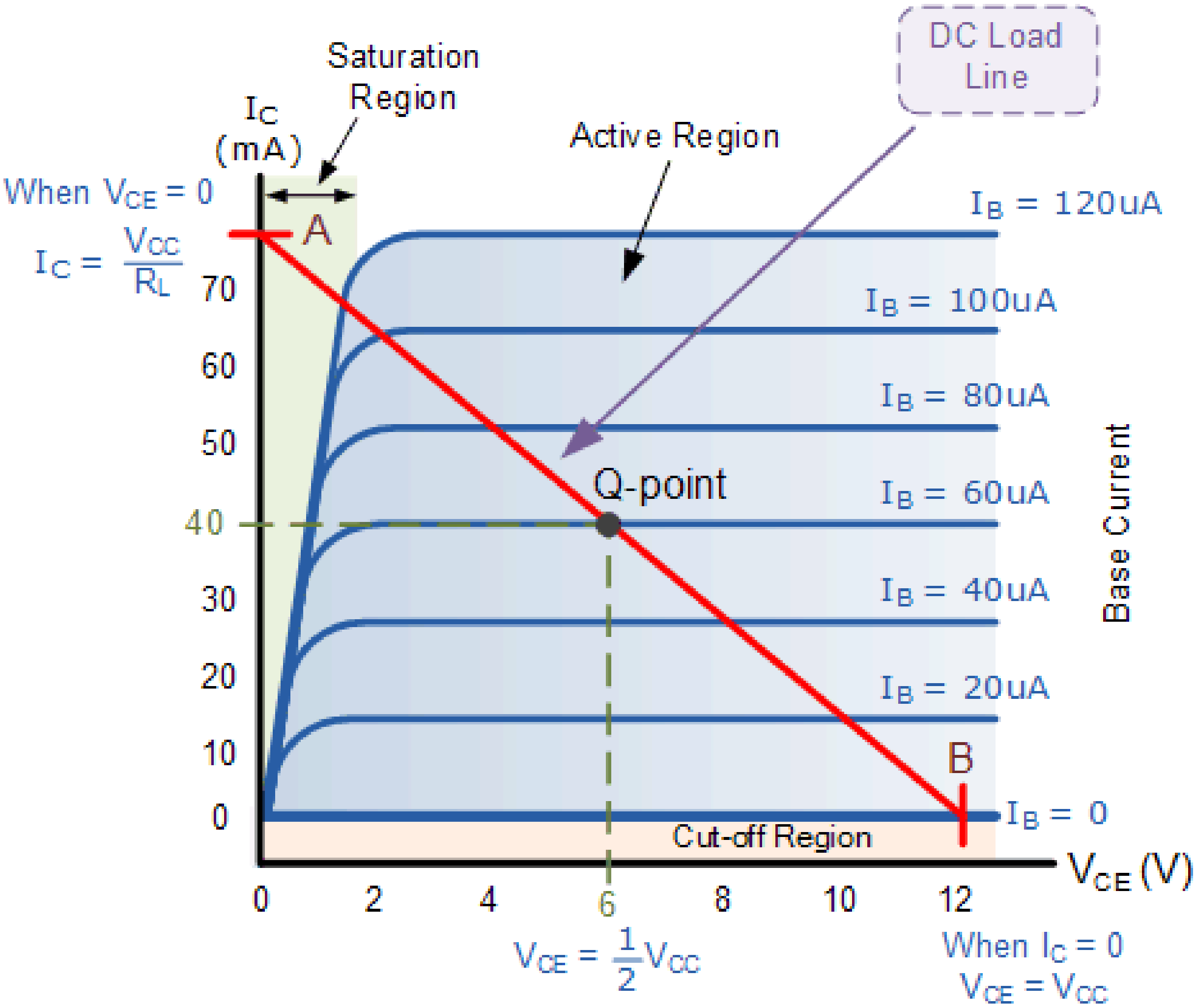


Figure 7: Working regions of BJT

Junction Field-effect Transistor(JFET)

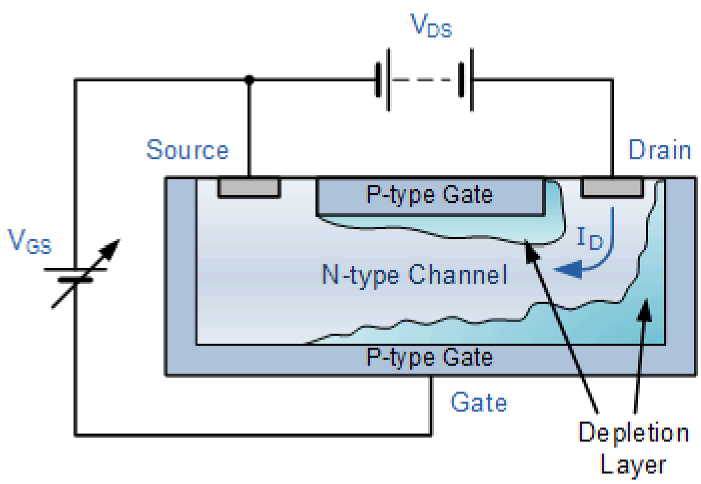


Figure 8: JFET

A typical JFET has the structure like Figure 8. SimilarlyS depending on materials' permutations, there is N-channel and P-channel JFET[4].

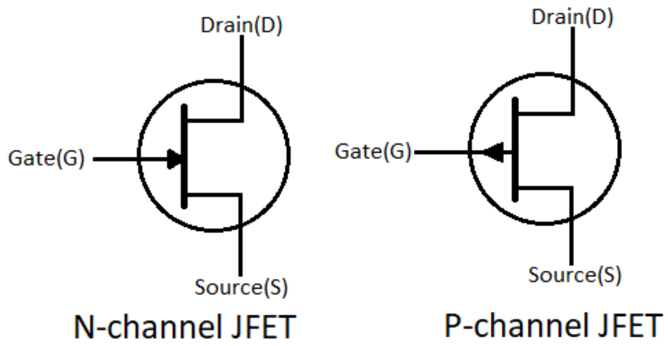


Figure 9: Symbols of two types of JFET

In a certain working condition(e.g certain temperature), a JFET has a unique V_P. The working states and its relevant information is listed in Table 2.

Linear Region	Condition
Cutoff	$V_{\text{GS}} \leq V_p$
Linear	$V_{\text{GS}} > V_P, V_{\text{DS}} < V_{\text{GS}} - V_P$
Saturation	$V_{\text{GS}} > V_P, V_{\text{DS}} \geq V_{\text{GS}} - V_P$

Table 2: JFET Working regions

Methods

For lab session 1, I built a simple circuit that connecting a diode to a variable voltage source and measure the current across the diode.

For lab session 2 and lab session 3, I used LTSpice to perform simulation and used Jupyter notebook to analyze the data.

Results

Lab session 1

Forward biased

- Simulation

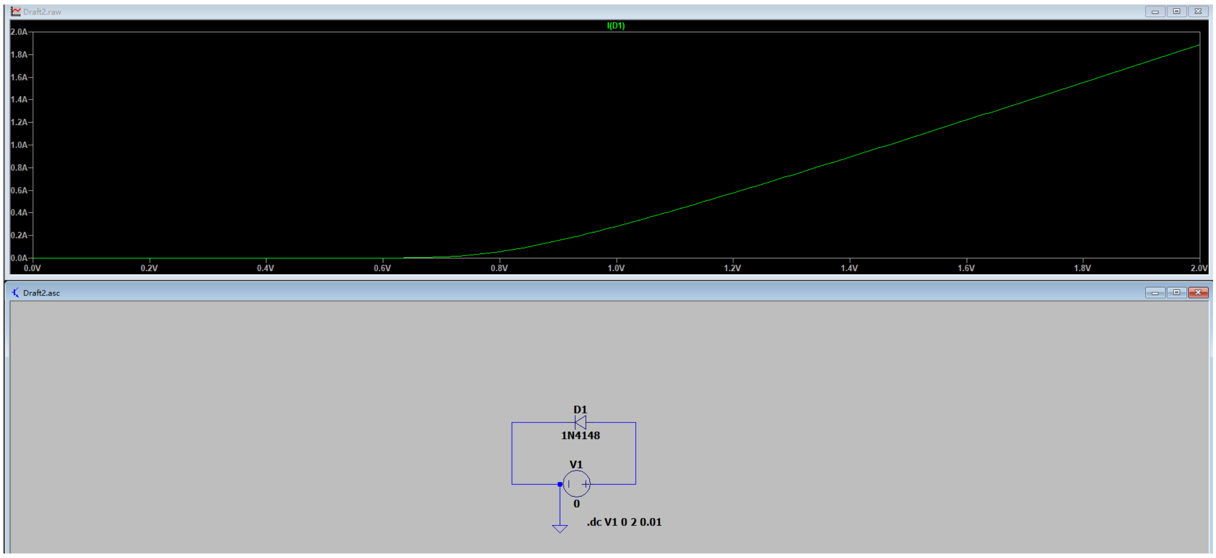


Figure 10: Forward biased

The threshold voltage is $V_F \approx 676$ mV

- Real circuit

The voltage-current relationship is shown in Table 3 and Figure 11.

Voltage(V)	Current(A)
0.3	0.012
0.4	0.02
0.5	0.045
0.6	0.105
0.7	0.18
0.9	0.35
1.1	0.529
1.2	0.623
1.3	0.717
1.4	0.812
1.5	0.907
1.6	1.002
1.7	1.098
1.8	1.194
1.9	1.29
2.0	1.387

Table 3: Forward biased

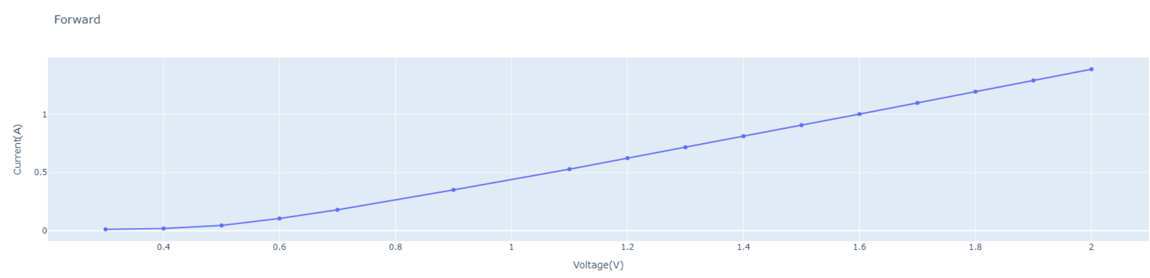


Figure 11: Forward biased

The threshold voltage is $V_F \approx 0.6V$. It is clearly shown that when the forward biased volatge exceeds a certain threshold value, the current will increase rapidly.

Reversed biased

- Simulation

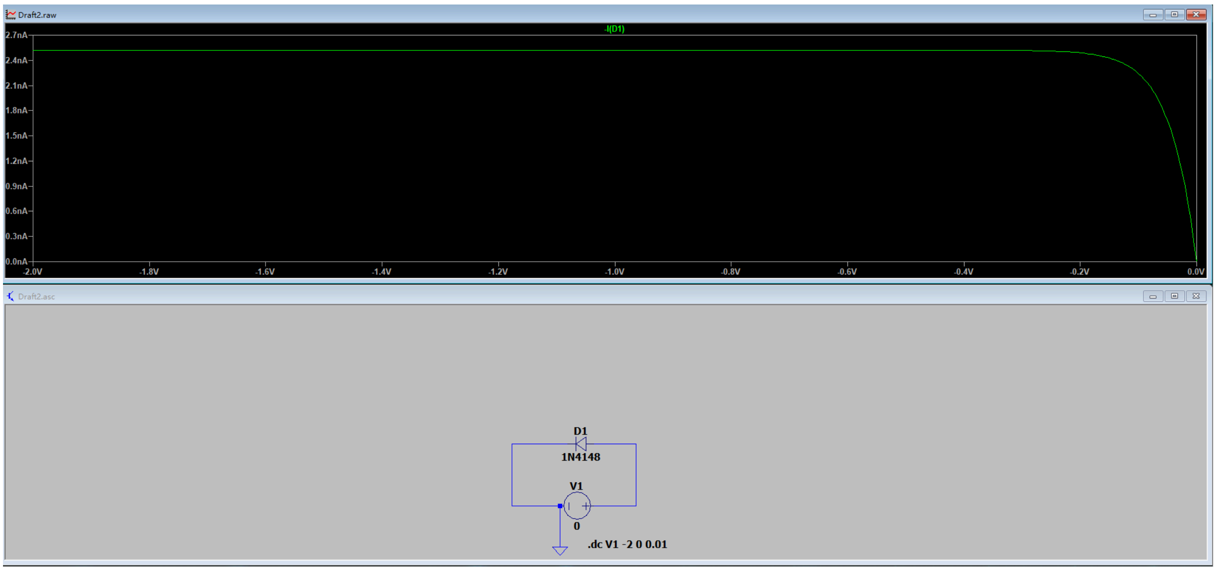


Figure 12: Reversed biased

The breakdown voltage is $V_R \approx 210$ mV

- Real circuit

The voltage-current relationship is shown in Table 4 and Figure 13.

Voltage(mV)	Current(A)
733	0.16
826	0.18
910	0.18
1002	0.183
1134	0.184
1190	0.188
1267	0.191
1375	0.193
1468	0.203
1561	0.208
1654	0.209
1747	0.209
2210.0	0.21
2670.0	0.21
4530.0	0.48
4720.0	0.48

Table 4: Reversed biased

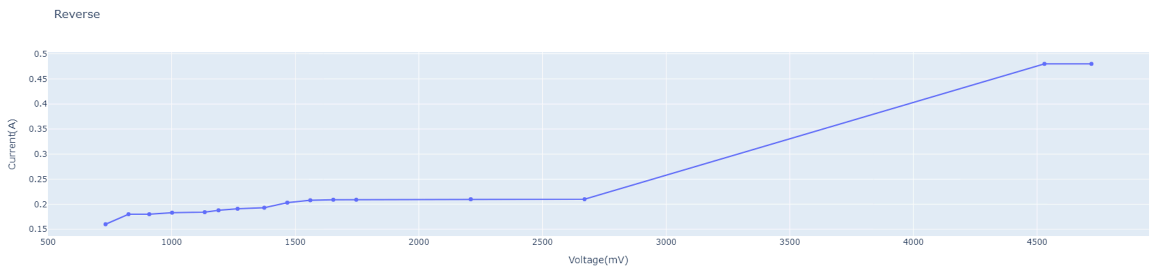


Figure 13: Reversed biased

The breakdown voltage is $V_R \approx 2670$ mV In the reversed biased case, when the voltage exceeds the breakdown voltage, the current will increase rapidly.

Problem 4

$$V_{\text{bi}} = \frac{kT}{a} \ln\left(\frac{N_A N_D}{n_i^2}\right) \approx 0.582V$$

$$W=\sqrt{\frac{2\varepsilon_r\varepsilon_0}{q}\left(\frac{N_A+N_D}{N_AN_D}\right)V_{\mathrm{bi}}}\approx 1.2\times 10^{-7}m$$

Problem 5

$$V_{\mathrm{bi}}=\frac{kT}{a}\ln\left(\frac{N_AN_D}{n_i^2}\right)\approx 0.902V$$

$$W=\sqrt{\frac{2\varepsilon_r\varepsilon_0}{q}\left(\frac{N_A+N_D}{N_AN_D}\right)V_{\mathrm{bi}}}\approx \frac{1}{04}\times 10^{-8}m$$

$$E(0)=\frac{qN_AW}{\varepsilon_r\varepsilon_0}\approx 1.57\times 10^{6}V/\ \mathrm{cm}$$

Lab session 2

I established a Spice model shown in Figure 14

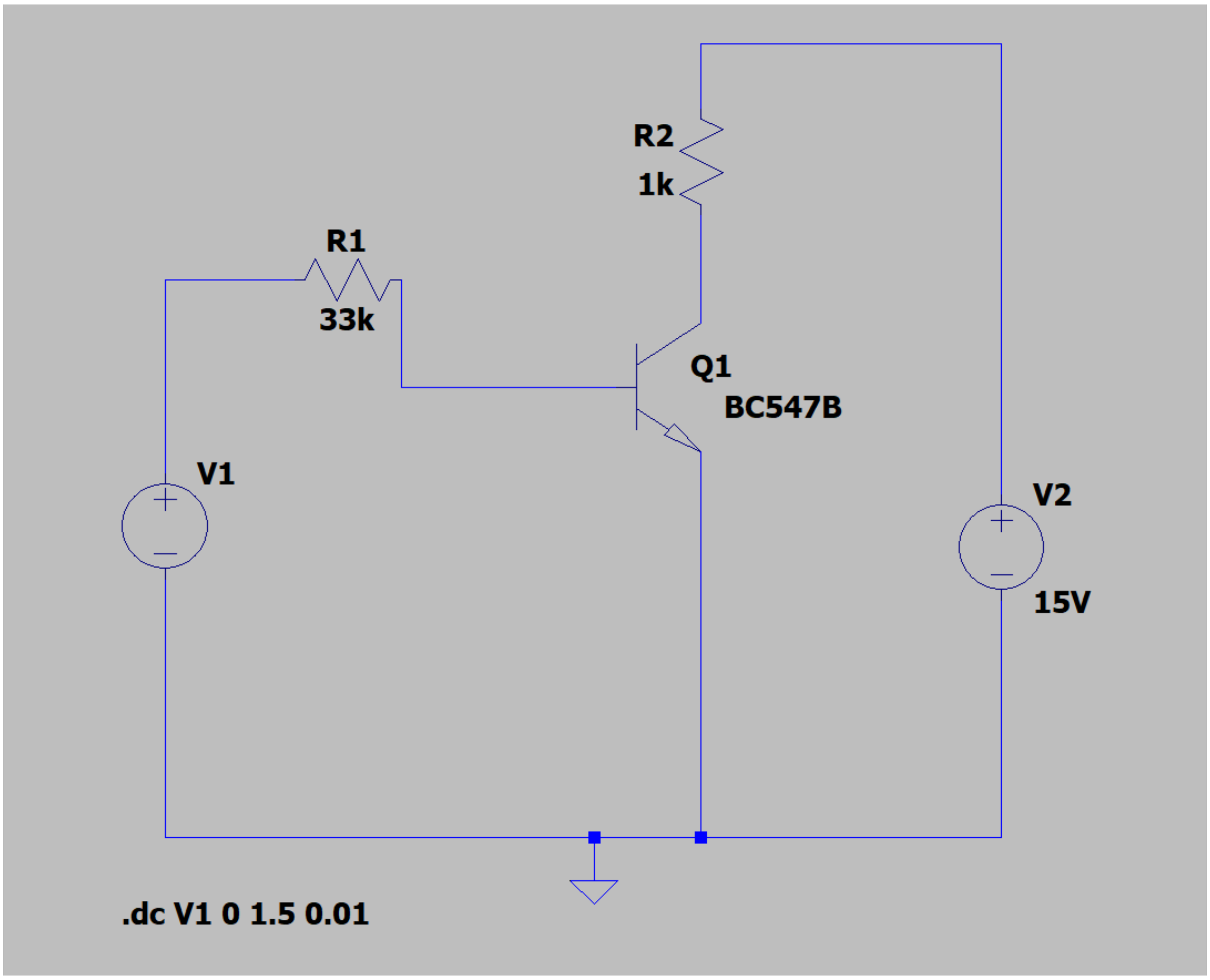


Figure 14: Lab session 2 circuit

For task 1, I observed the relations between I_C and V_{BE} when V_{CC} is equal to a series of values. Four figures was selected and displayed in Figure 15

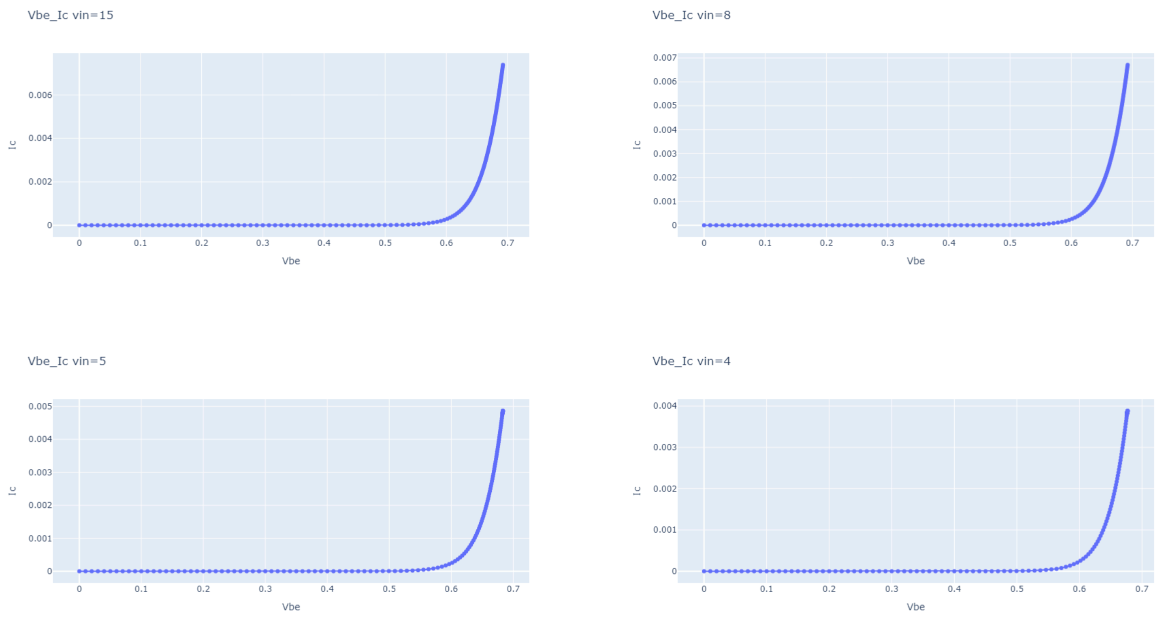


Figure 15: Lab session 2 task1

For task 2, I set V_{CC} to be 5V. Then, V_{BE} was adjusted to approximately 1.241 V ensuring that V_{CE} was close to 5V. Then, V_{CC} was modified while V_{BE} was fixed to make V_{CE} to be 0,0.2,1,3,5,10 V. I_C is measured meanwhile. The results are shown in Table 5 and Figure 16.

$V_{\mathrm{CE}(V)}$	$I_C(\mathrm{mA})$
0	0
0.2	0.171
1	0.935
3	2.88
5	4.64
10	4.99

Table 5: Lab session 2 taks2

Figure 16: Lab session 2 task2

Lab session 3

I established a Spice model shown in Figure 17.

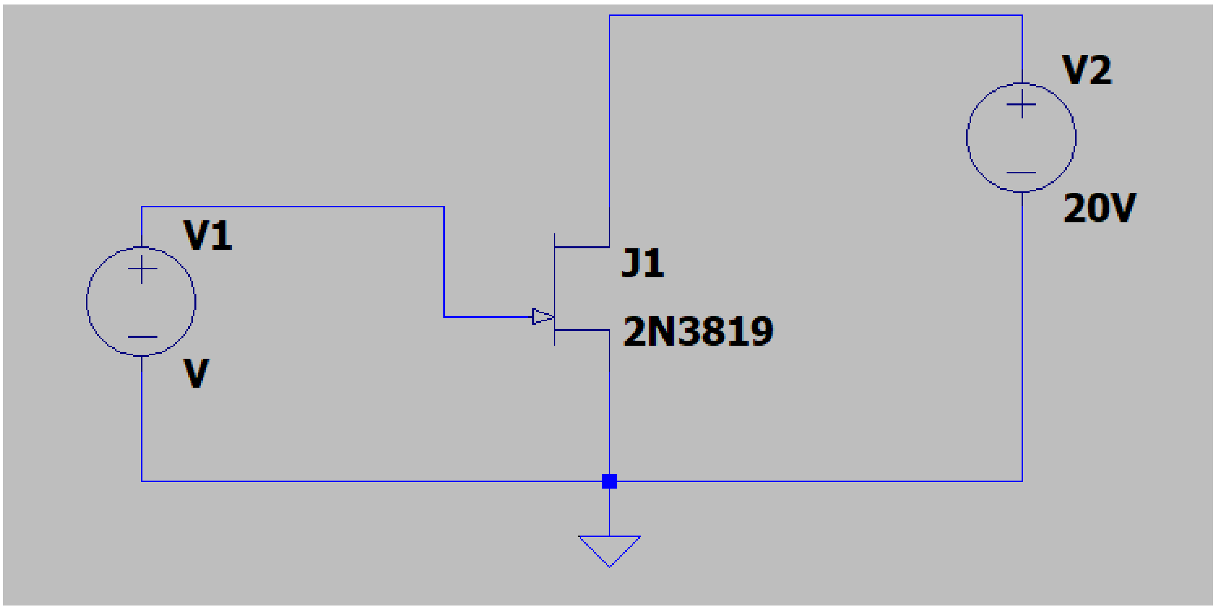
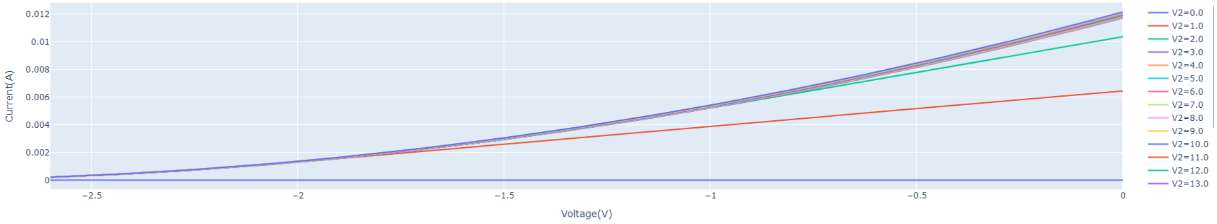
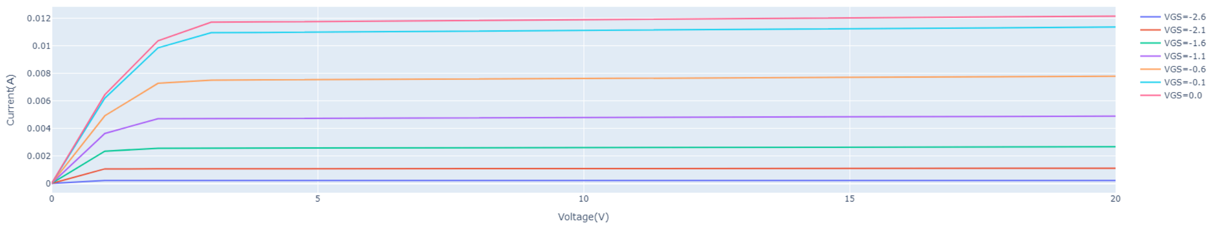


Figure 17: Lab session 3 circuit

The two figures of task 1 are shown in Figure 18.



(a) $I_D - V_{\mathrm{GS}}$



(b) $I_D - V_{\mathrm{DS}}$

Figure 18: Lab session 3 task1

For task 2, I was required to choose a proper operation point Q. When a small signal is applied, $V_{\mathrm{GS}} > 0$ should be avoided, thus, the medium of previous values $V_{\mathrm{GS}} = -1.1V$ or $V_{\mathrm{GS}} = -1.6V$ should be selected.

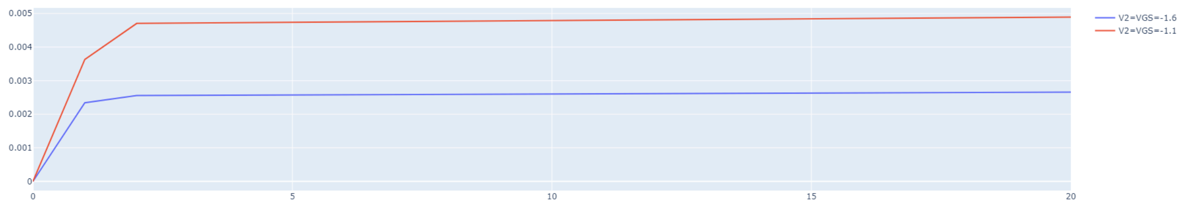


Figure 19: Lab session 3 task 2

For task 3, as the supply voltage is 20V, I should connect the the selected operation point Q and (20,0). The absolute value of slope is the value of R_D.

$$R_D \approx 1577\Omega$$

The voltage of the battery3 required to bias the gate is V_{GS} in case $\approx 1.6V$.

For task 4. R_D is integrated and the circuit is displayed in Figure 20. A sine wave is applied.

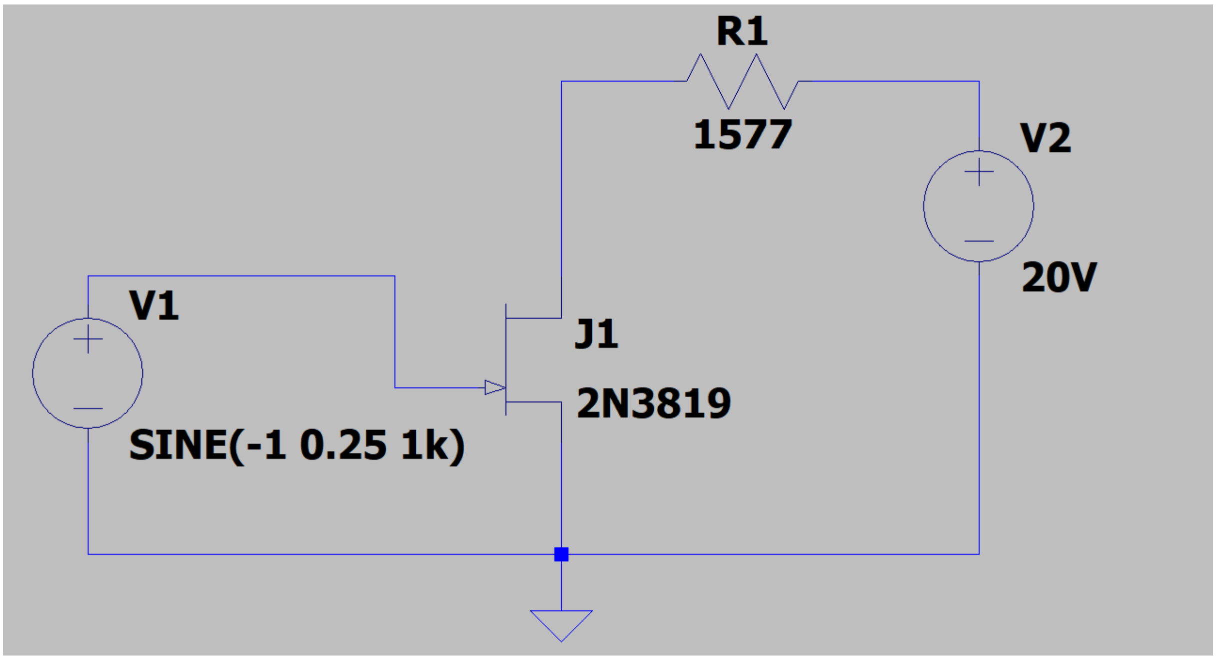


Figure 20: Lab session 3 taske4 circuit

The response to a sine wave of 1kHZ $V_{\mathrm{pp}} = 0.25V$ is shown in Figure 21.

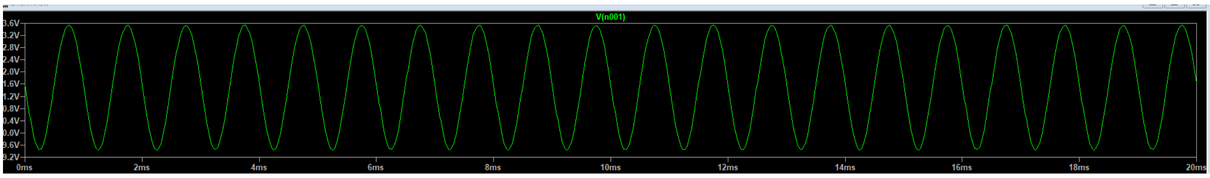


Figure 21: Response

Discussion

Lab session 1, the diode lab is relatively easy to obtain ideal result. However, for small current, especially when it is setup with the reversed biased. It is hard to get an accurate current measurement as the instrument's limit.

Regarding lab session 2 and 3, being familiar with simulation software and plotting platform like plotly in this report is essential.

Conclusion

Diode, BJT, and JFET are classic semiconductor devices based on the PN-junction, and they have become foundational building blocks in electronics. These devices can function as both switches and amplifiers, offering a variety of applications in circuits.

References

[1] Hitachi High-Tech, “What are semiconductors?,” Online. Available: https://www.hitachi-hightech.com/global/en/knowledge/semiconductor/room/about/. [Accessed: Dec. 6, 2024].

[2] Toshiba, “What is a pn Junction?,” Online. Available: https://toshiba.semicon-storage.com/us/semiconductor/knowledge/e-learning/discrete/chap1/chap1-6.html. [Accessed: Dec. 6, 2024].

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