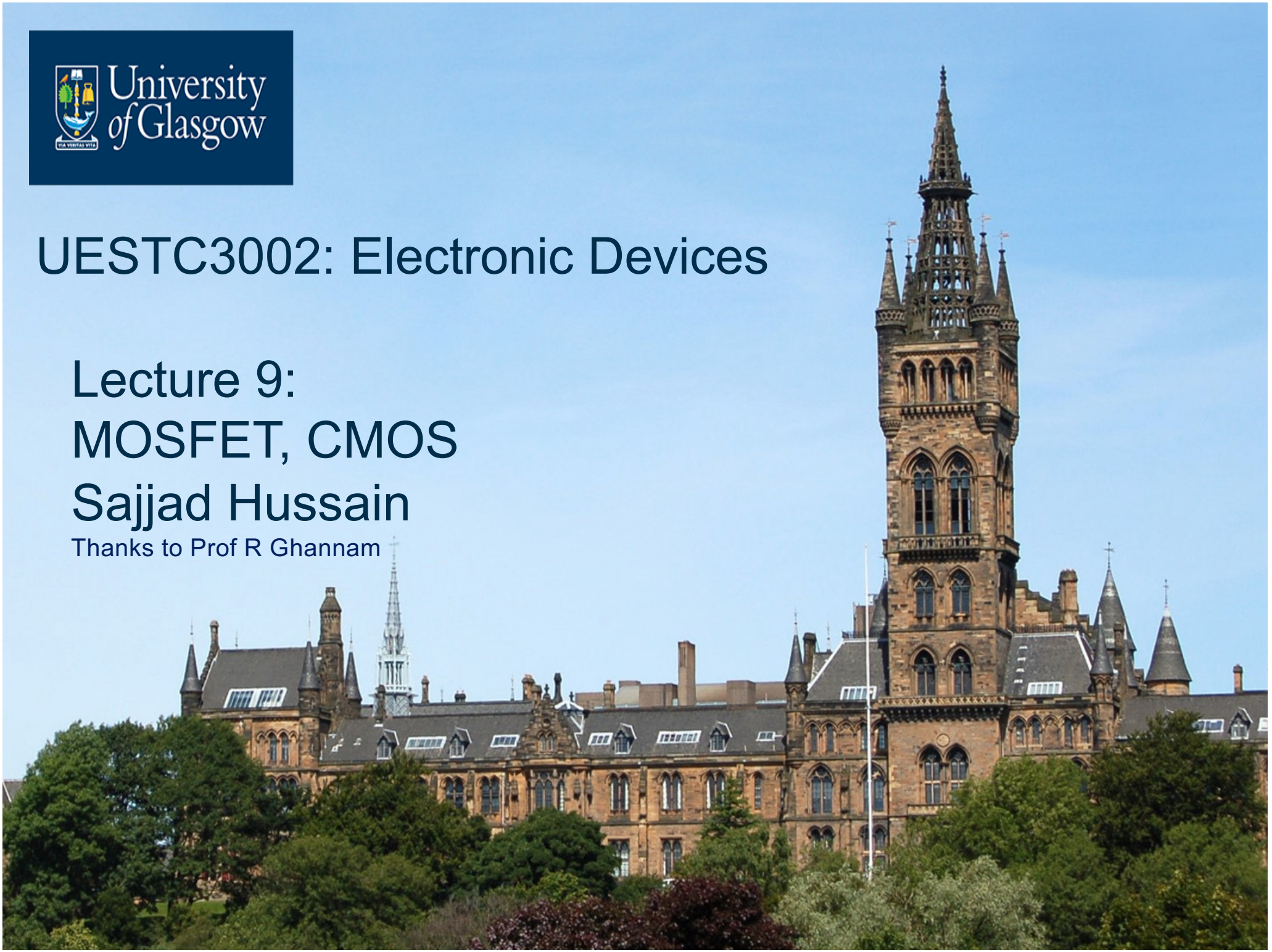


University of Glasgow

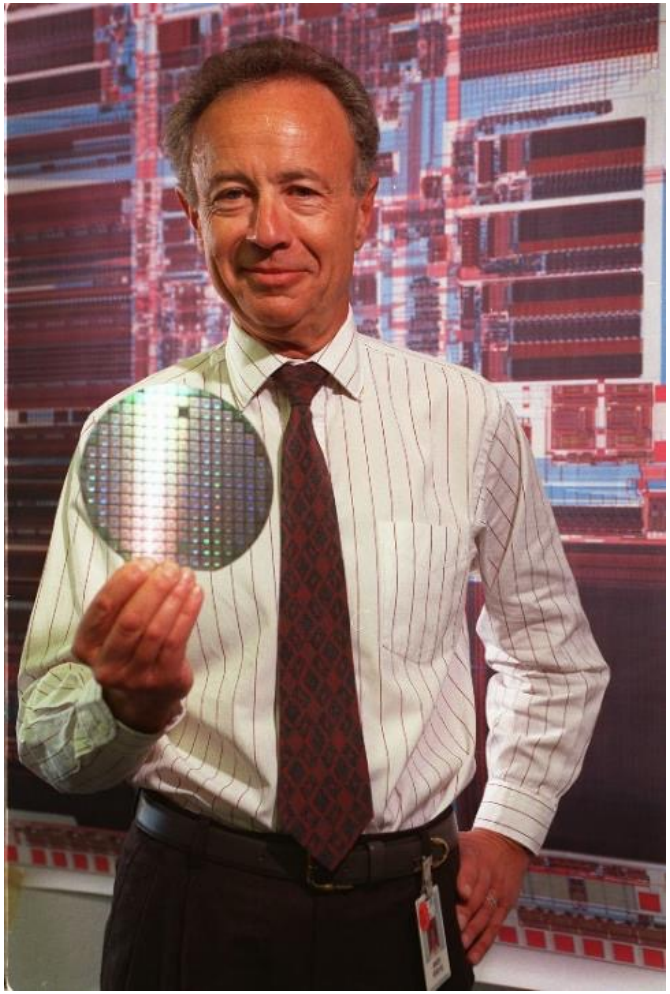
UESTC3002: Electronic Devices

Lecture 9:
MOSFET, CMOS

Sajjad Hussain

Thanks to Prof R Ghannam

MOSTs (Metal-Oxide-Semiconductor Transistors)



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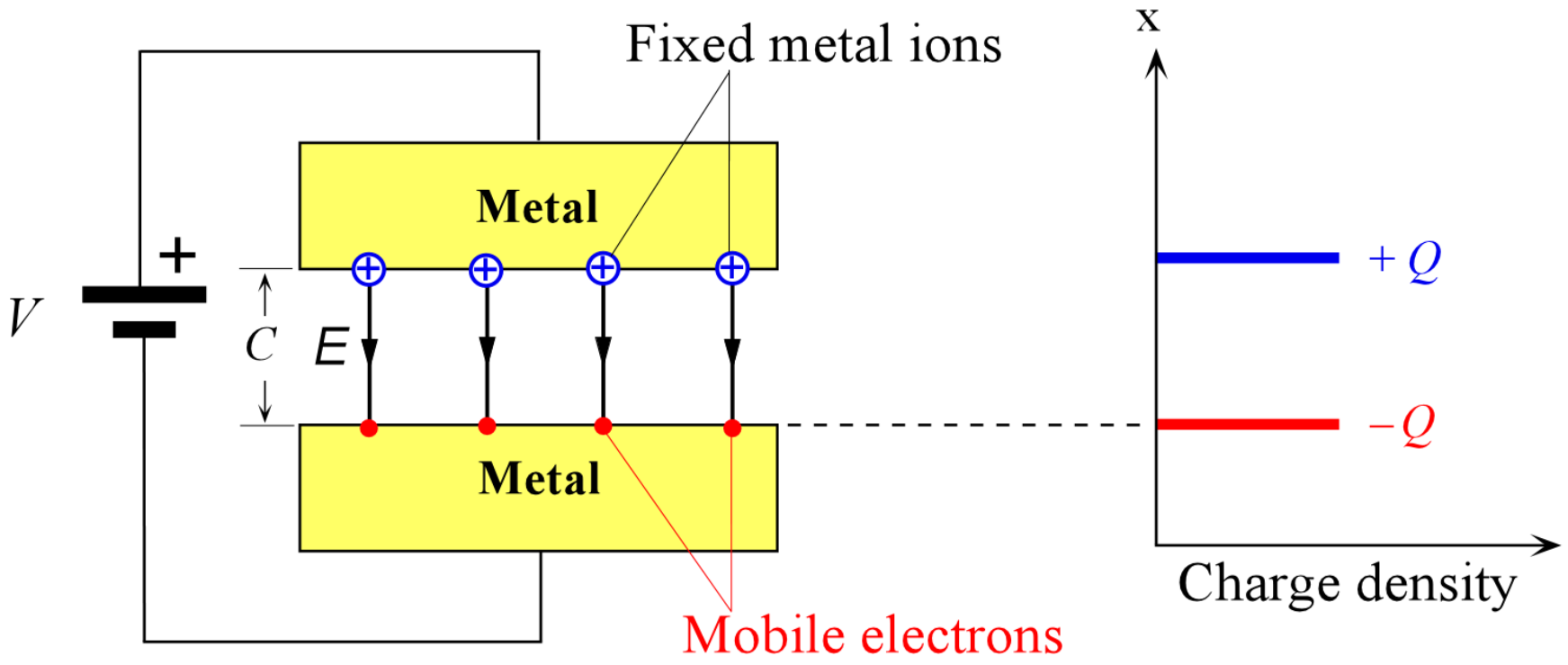
- Modern integrated circuits (ICs) contain billions of Transistors. Most are MOSTs.
- Andrew S. Grove (1936–2016) played a key and influential role in the development of the microprocessor technology at Intel.
- When Robert Noyce and Gordon Moore founded Intel in 1968, they hired Andrew Grove to lead the technology development.
- The well-known 386 and Pentium PC chips were actually developed at Intel under Andrew Grove's leadership.
- He became Intel's President in 1979 and CEO in 1987 until 1998, which was followed by his position as Chair of the board until 2005.
- His book Physics and Technology of Semiconductor Devices published in 1967 by Wiley is still among the best reads in understanding the fundamentals of semiconductor materials and devices.
- In this photo, Andrew Grove is holding an Intel 0386 microprocessor at Intel headquarters in Santa Clara, California.

MOS: Metal-Oxide-Semiconductor (MOS)



Applying a voltage between two metal plates separated by an insulator results in the build-up of charges +Q and –Q on the plates and an E-field. In a metal-air-metal capacitor, all the charges reside on the surface and the E-field does not penetrate into the metal.

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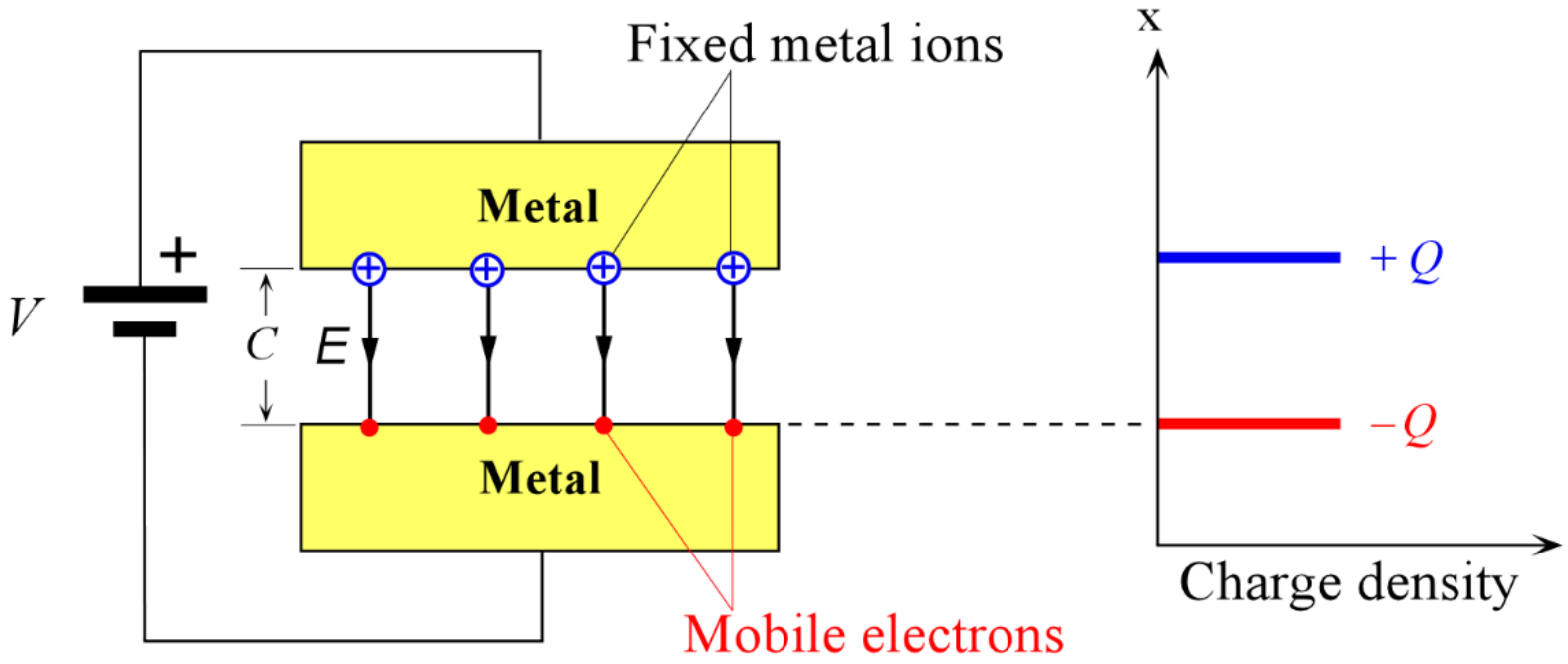
MOS: Metal-Oxide-Semiconductor



- There will be that many number of positive metal ions and electrons on the surface.
- The charges $+Q$ and $-Q$ can therefore be generated by the electrons and metal ions at the surface alone. The E-field terminates at the metal surface.

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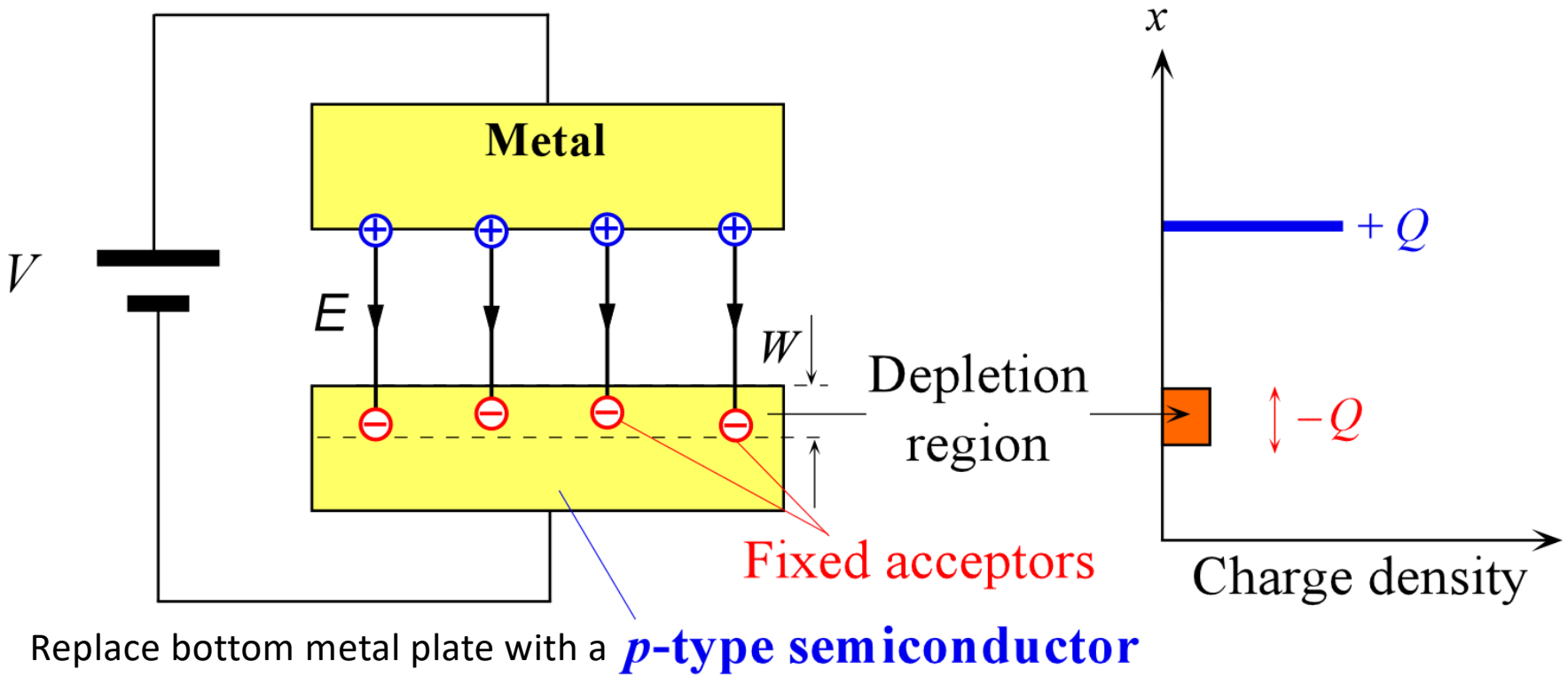
MOS: Metal-Oxide-Semiconductor



Insufficient number of negative acceptors at the surface to generate the charge $-Q$. Therefore, we must **expose negative acceptors in the bulk**.

The field penetrates into the semiconductor.

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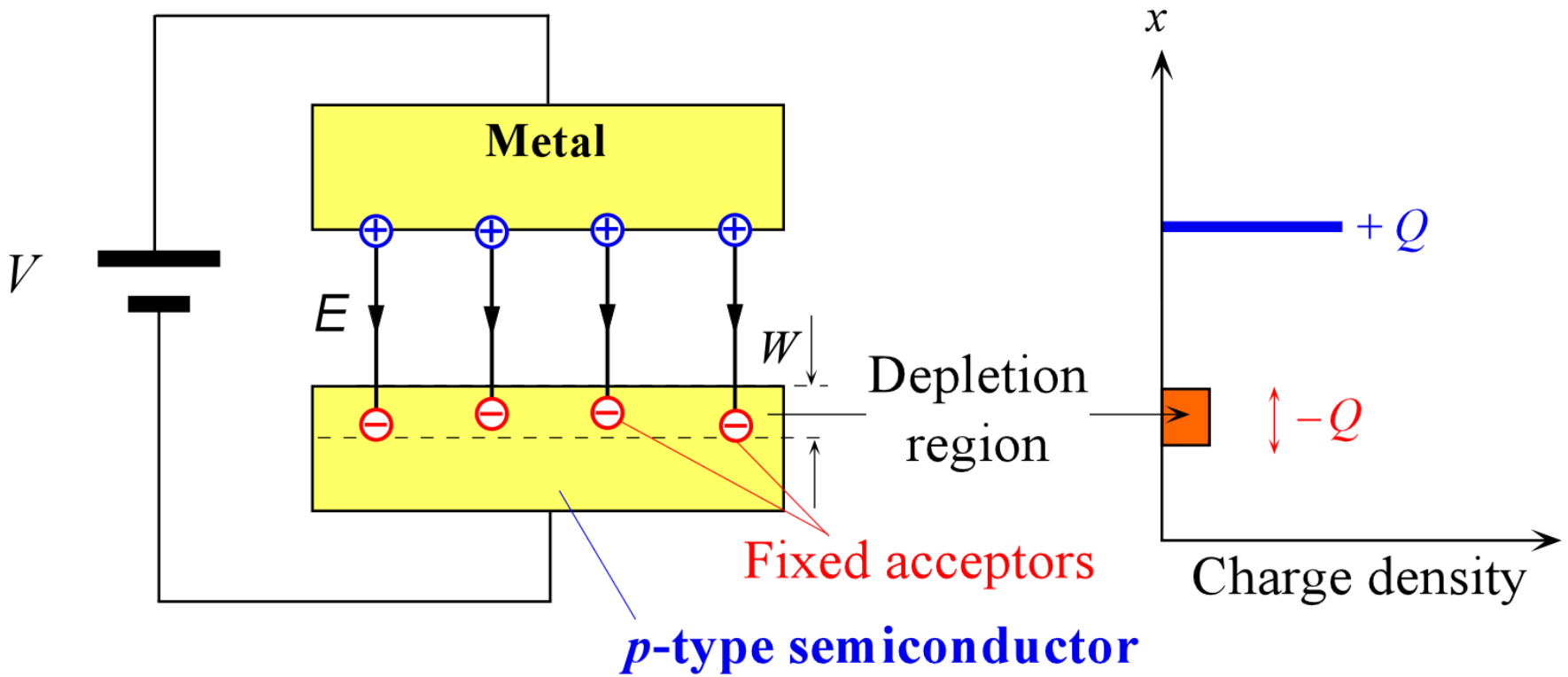
MOS: Metal-Oxide-Semiconductor



A positive voltage creates a depletion layer by forcing the positively charged holes **away** from the metal/insulator/semiconductor interface, **leaving exposed a carrier-free region of immobile**, **negatively** charged **acceptor ions**. The region into which the field penetrates is therefore depleted of its equilibrium concentration of holes.

This is a **depletion layer**. We can estimate **W** since $Q = qAWN_a$

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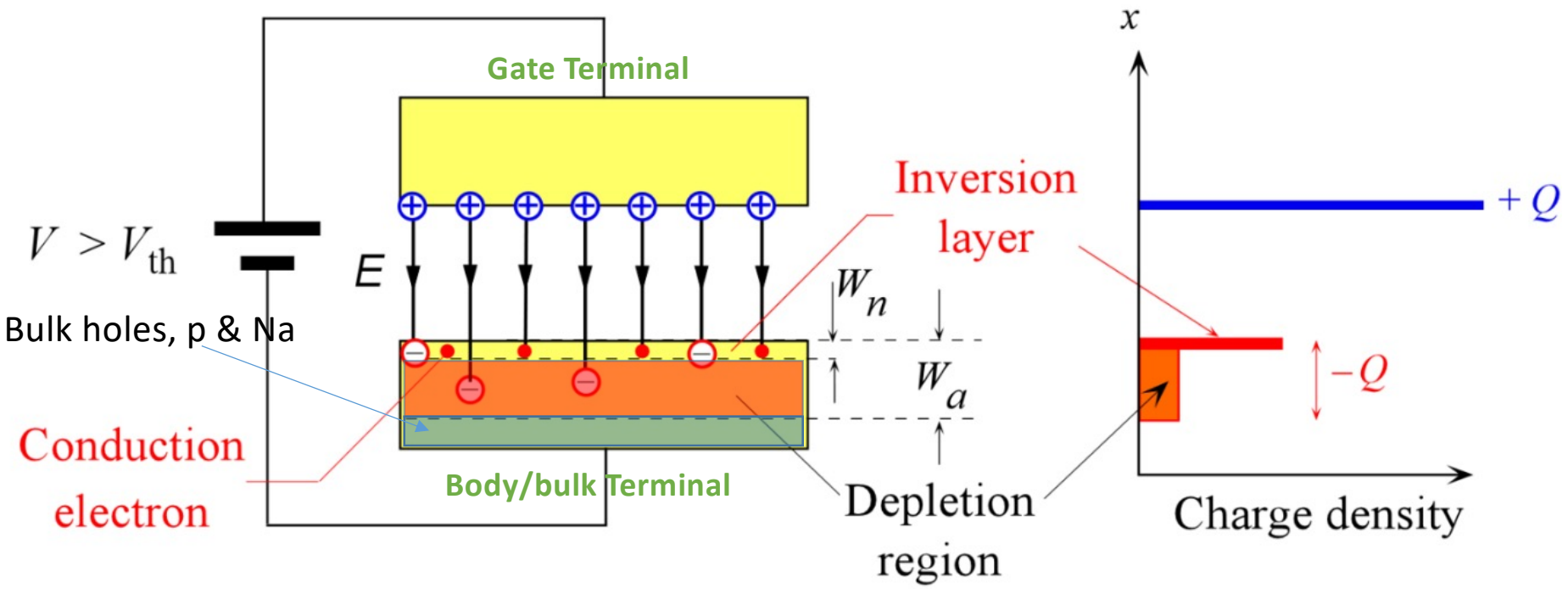
MOS: Metal-Oxide-Semiconductor



If V is high enough, **a high concentration of negative charge carriers forms in an *inversion layer* located in a thin layer next to the interface between the semiconductor and the insulator**. Conventionally, the gate voltage at which the volume density of electrons in the inversion layer is the same as the volume density of holes in the body is called the threshold voltage. $V > V_{th}$, an **inversion layer** is created near the surface in which there are conduction electrons

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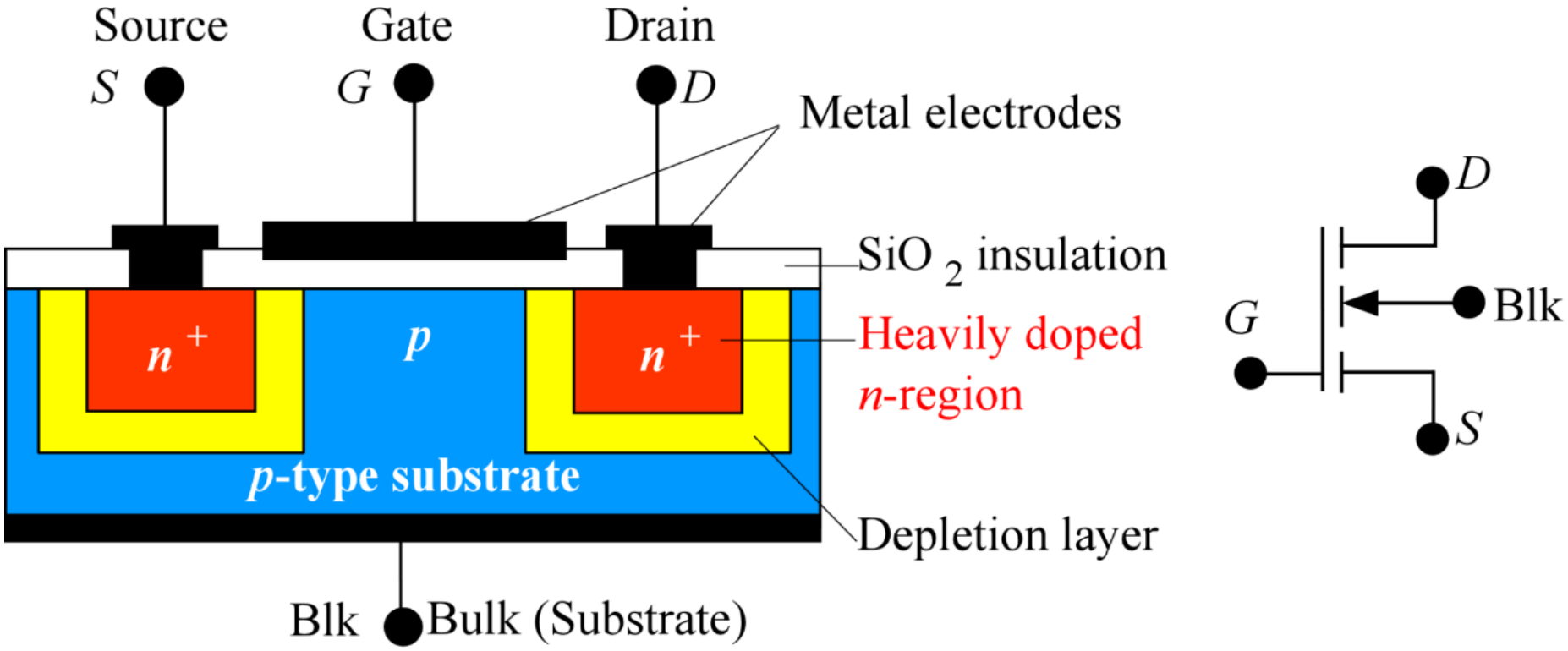
MOS: Metal-Oxide-Semiconductor

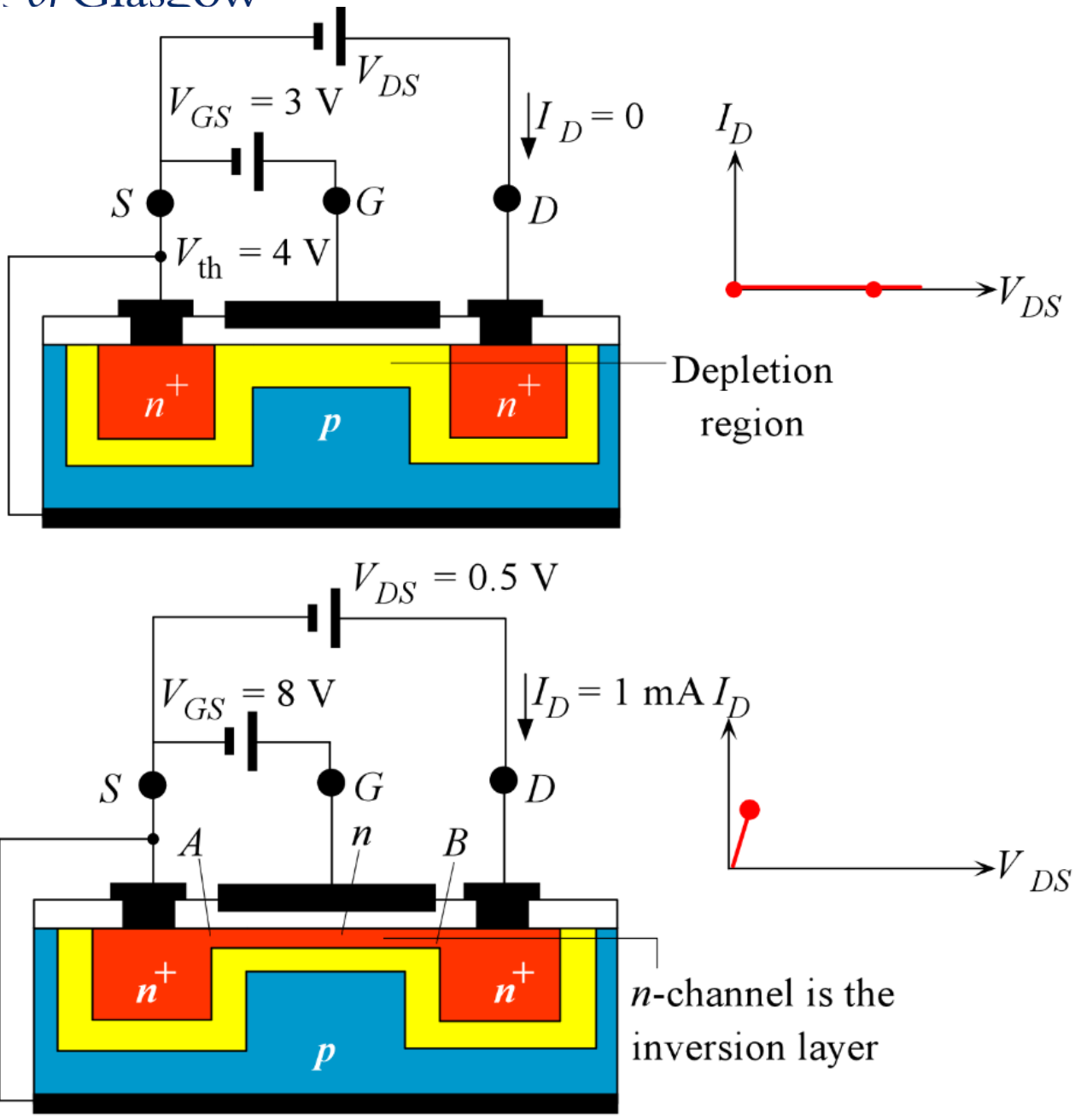
- In addition to the Body/bulk and the Gate terminal in a MOS capacitor, a MOSFET has two additional terminals called Source and Drain.
- Each of these is connected to individual highly doped regions that are separated by the bulk region.
- These regions can be either p or n type, but they must both be of the same type and of opposite type to the body region.
- The source and drain (unlike the bulk) are highly doped as signified by a "+" sign after the type of doping.

Enhancement MOSFET



If the MOSFET is an n-channel or nMOS FET, then the source and drain are "n+" regions and the body is a "p" region. If the MOSFET is a p-channel or pMOS FET, then the source and drain are "p+" regions and the body is a "n" region. The source is so named because it is the source of the charge carriers (electrons for n-channel and holes for p-channel).

Enhancement MOSFET



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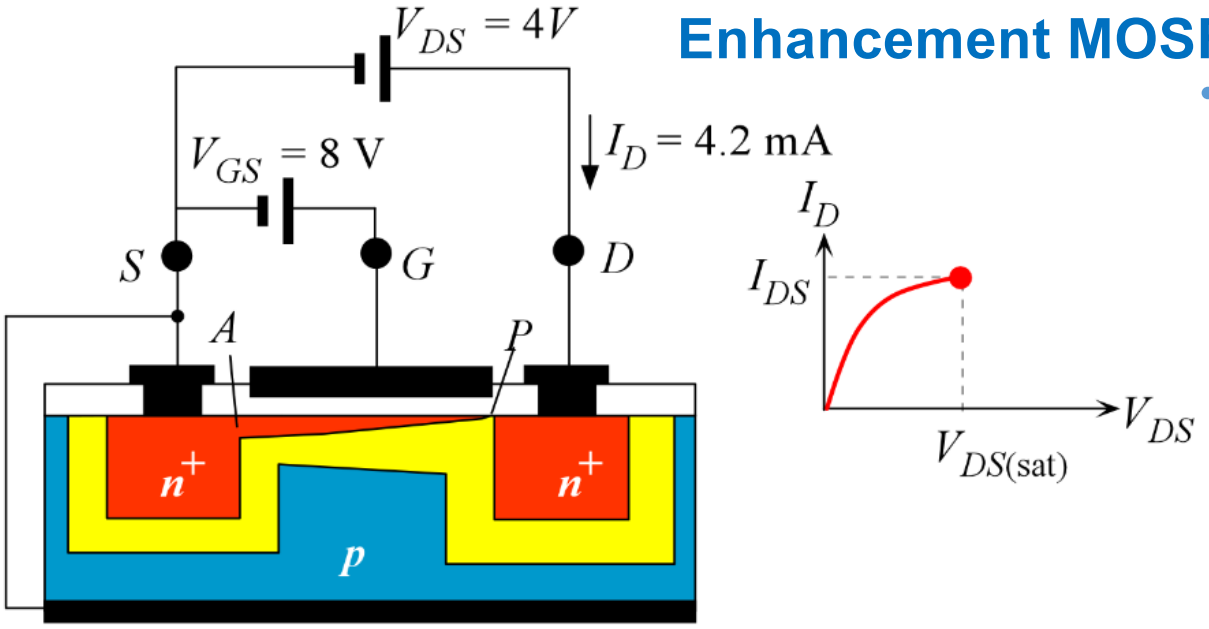
Below threshold $V_{GS} < V_{th}$ and $V_{DS} = 0$. Depletion layer forms due to expulsion of holes. Now, increasing V_{GS} beyond threshold (V_{DS} =0) results in an inversion layer to form in the p-type semiconductor, which links the two n+ regions of source and drain.

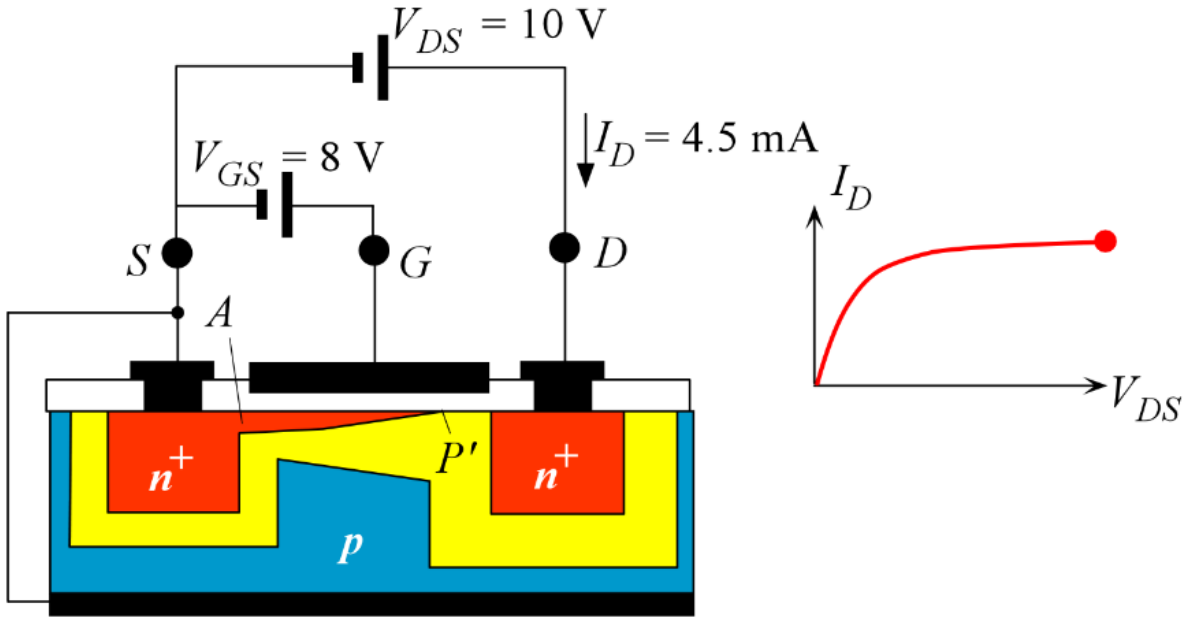
Above threshold $V_{GS} > V_{th}$ and by applying a small V_{DS} ($V_{DS} < V_{DS(sat)}$) a current I_D flows, which is limited by the resistance of the n-channel:

$$I_D = \frac{V_{DS}}{R_n}$$

The current, I_D increases linearly with V_{DS} in this region.

Enhancement MOSFET





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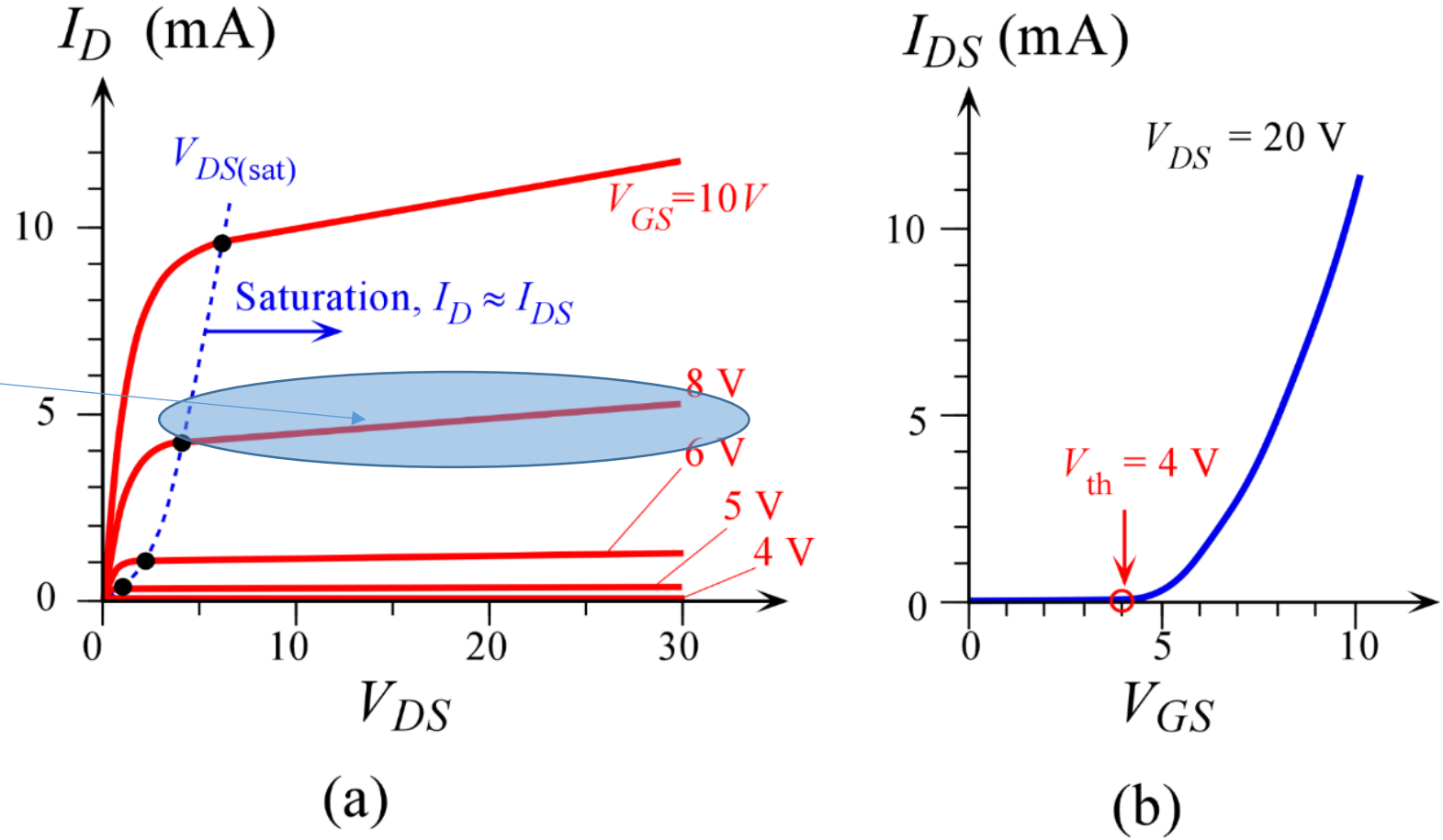
- **Above threshold $V_{GS} > V_{th}$ and $V_{DS} = V_{DS(sat)}$** . As V_{DS} is increased, voltage at B (V_{GD}) decreases since $V_{GD} = V_{GS} - V_{DS}$. There is less inversion near the drain and the channel gets narrower as well as R_{ch} increasing. When V_{GD} is just $\leq V_{th}$ we start to expose the depletion layer and pinch-off is obtained. Thus, $V_{DS} = V_{DS(sat)}$ and $V_{GD} = V_{GS} - V_{DS(sat)} = V_{th}$

- **Above threshold $V_{GS} > V_{th}$ and $V_{DS} > V_{DS(sat)}$** additional V_{DS} drops across depletion layer, which extends to P'. Resistance of channel changes slightly and I_{DS} becomes:

$$I_D \approx I_{DS} \approx V_{DS(sat)}/R_{AP'(n-ch)}$$

Enhancement MOSFET

Only slight increase in I_{DS} with increasing V_{DS} above $V_{DS(sat)}$



(a) Typical I_D vs V_{DS} characteristics of an enhancement MOSFET (V_{th} = 4 V) for various Fixed voltages V_{GS}.

(b) Provided that $V_{DS} > V_{DS(sat)}$, I_{DS} (output in source-drain circuit) is totally dependent on V_{GS}. Thus, variations in V_{GS} lead to changes in $I_{DS.}$ Remember, I_{DS} only exists when $V_{GS} > V_T$

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Enhancement NMOSFET

Called enhancement, since a gate voltage is required to ***enhance*** a conducting channel between source and drain.

Enhancement NMOSFET constant

Units of AV^{-2}

$$K = \frac{Z\mu_e\varepsilon}{2Lt_{ox}}$$

Sometimes referred to as C_{ox} (oxide capacitance)

where μ_e is the electron drift mobility in the channel, L and Z are the length and width of the gate controlling the channel, and ε and t_{ox} are the permittivity ($\varepsilon_r\ \varepsilon_o$) and thickness of the oxide insulation under the gate respectively.

Enhancement MOSFET in LINEAR REGION

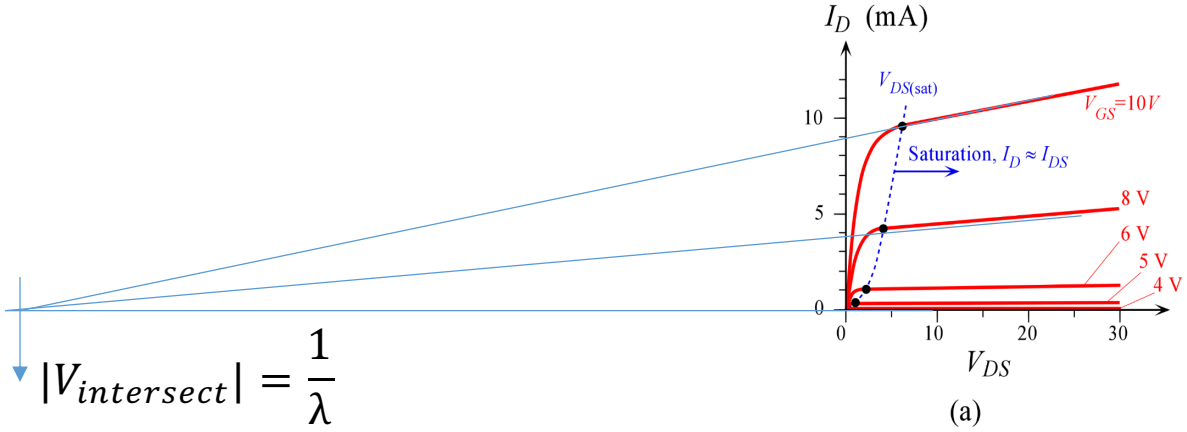
$$I_{DS} = K[2(V_{GS} - V_{th})V_{DS} - V_{DS}^2]$$

Enhancement NMOSFET

Enhancement MOSFET in SATURATION REGION

$$I_{DS} = K\left(V_{GS} - V_{\text{th}}\right)^2\left(1 + \lambda V_{DS}\right)$$

Where λ is the channel-length modulation parameter, which is a constant that is typically 0.01 V^{-1}. It can be determined by extending I_D vs V_{DS} lines and finding the intersect at - V_{DS}



Enhancement NMOSFET

- **The MOSFET transconductance is**

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{2I_D}{V_{GS} - V_{th}} = \frac{2I_D}{V_{ov}},$$

where $V_{ov} = V_{GS} - V_{th}$ is called the **overdrive voltage.**

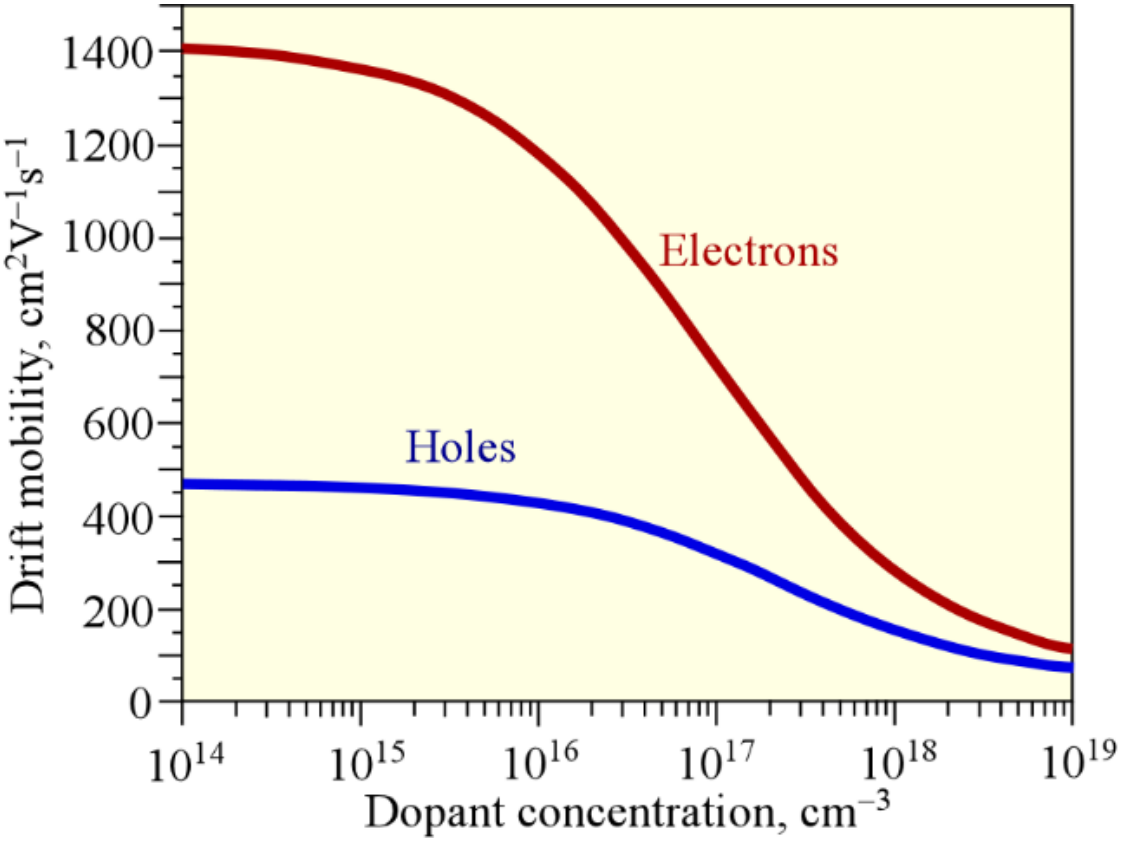
- We can calculate the voltage gain A_V using transconductance g_m.
- Remember the voltage gain:

$$A_V = -g_m R_D$$

MOSFET – Example 1

THE ENHANCEMENT NMOSFET A particular enhancement NMOS transistor has a gate with a width (Z) of 50 μm, length (L) of 10 μm, and SiO_2 thickness of 450 Å. The relative permittivity of SiO_2 is 3.9. The p-type bulk is doped with 10^{16} acceptors cm^{-3}. Its threshold voltage is 4 V. Estimate the drain current when $V_{GS} = 8$ V and $V_{DS} = 20$ V, given $\lambda = 0.01$. Due to the strong scattering of electrons near the crystal surface assume that the electron drift mobility μ_e in the channel is half the drift mobility in the bulk.

The variation of the drift mobility with dopant concentration in Si for electrons and holes at 300 K.



MOSFET as an Amplifier – Example 2

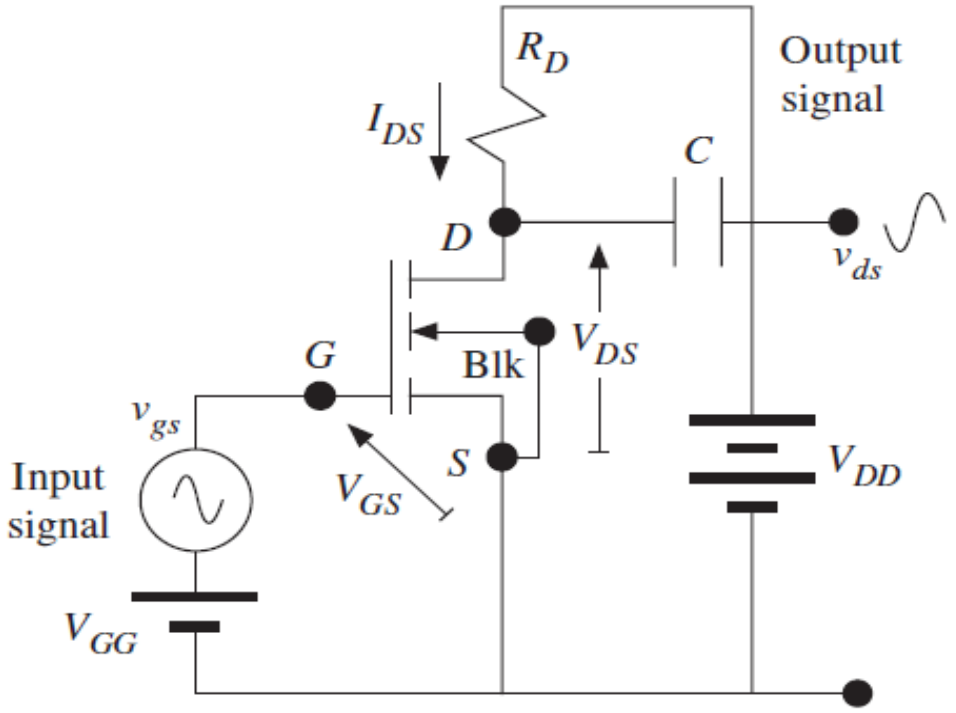
The Enhancement NMOSFET amplifier Consider an n-channel Si enhancement NMOS that has a gate width (Z) of 150 μm, channel length (L) of 10 μm, and oxide thickness (t_{ox}) of 500 Å. The channel has $\mu_e = 700\ cm^2\ V^{-1}\ s^{-1}$ and the threshold voltage (V_{th}) is 2 V ($\varepsilon_r = 3.9$ for SiO_2).

a. Calculate the drain current when $V_{GS} = 5$ V and $V_{DS} = 5$ V and assuming $\lambda = 0.01$.

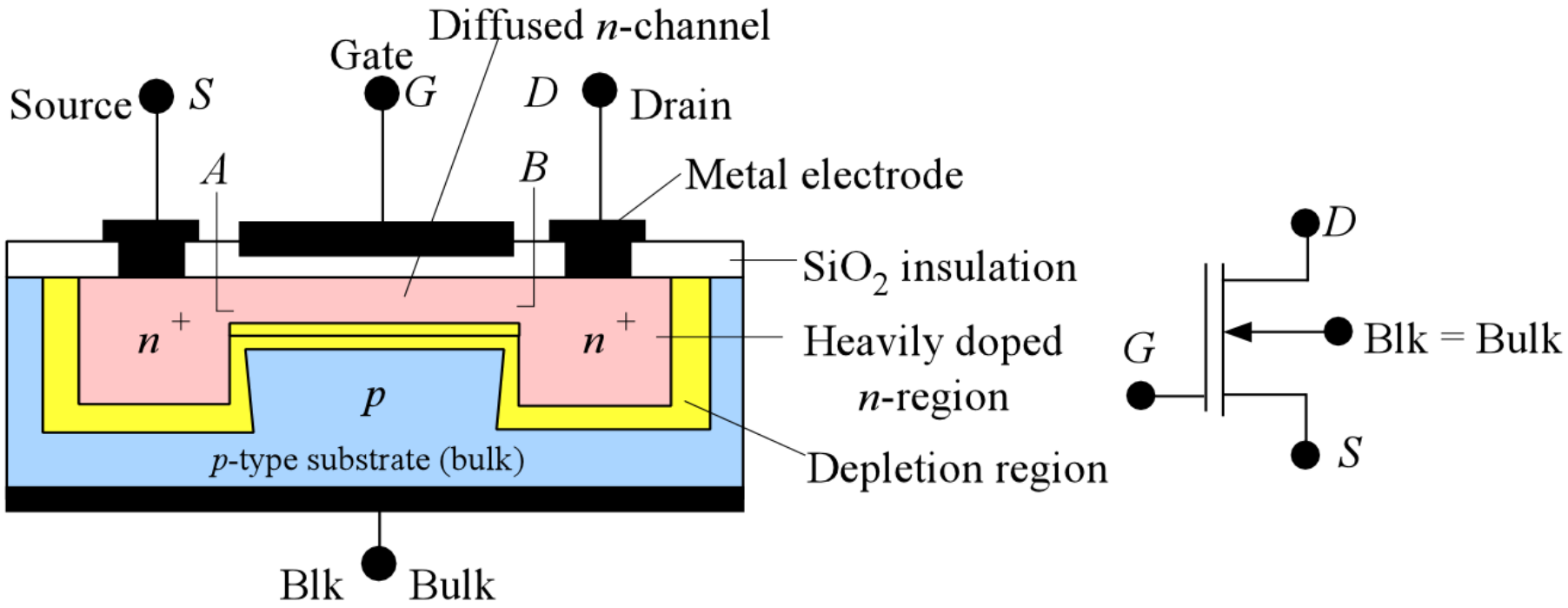
b. What is the small-signal voltage gain if the NMOSFET is connected as a common source amplifier with a drain resistance R_D of 2.2 kΩ, the gate biased at 5 V with respect to source ($V_{GG} = 5$ V) and V_{DD} is such that $V_{DS} = 5$ V? What is V_{DD}? What will happen if the drain supply is smaller?

c. Estimate the most positive and negative input signal voltages that can be amplified if V_{DD} is fixed at the above value in b.

d. What factors will lead to a higher voltage amplification?



Depletion MOSFET



Unlike enhancement-mode transistors, which are "normally-off" devices, depletion mode MOSFETs are "normally-on".

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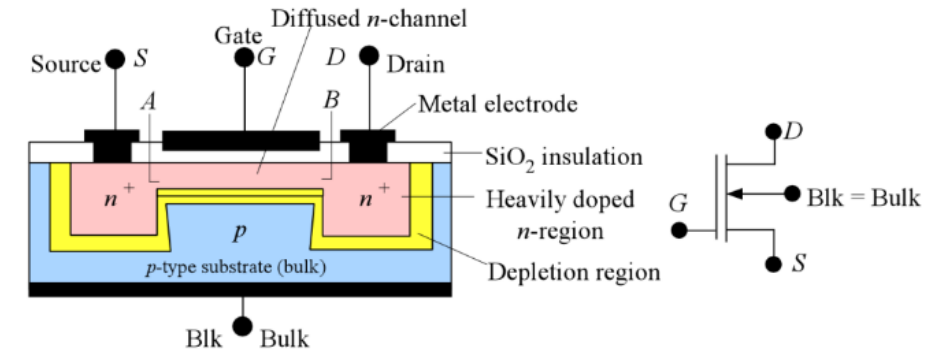
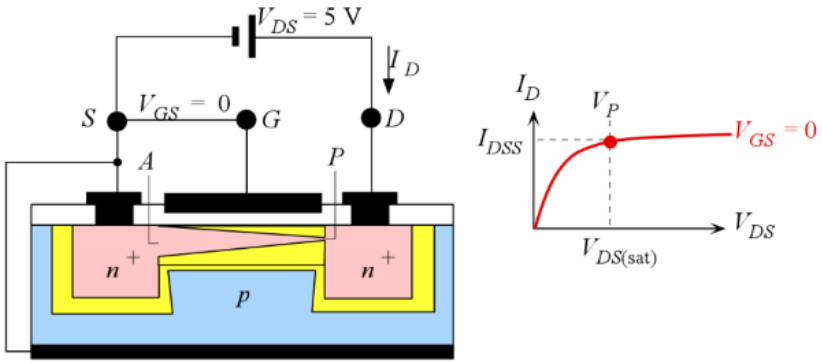
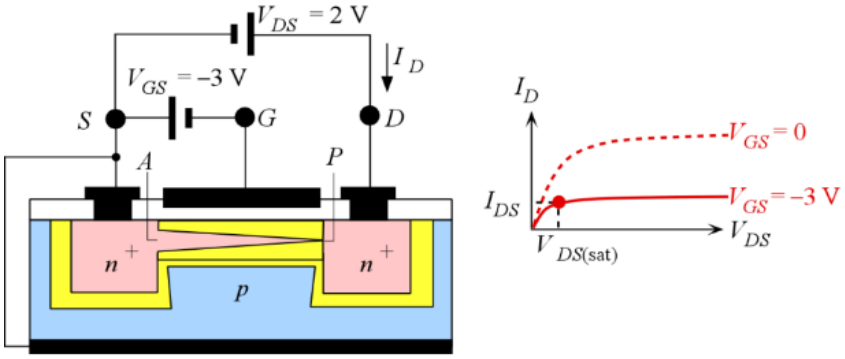
Depletion MOSFET

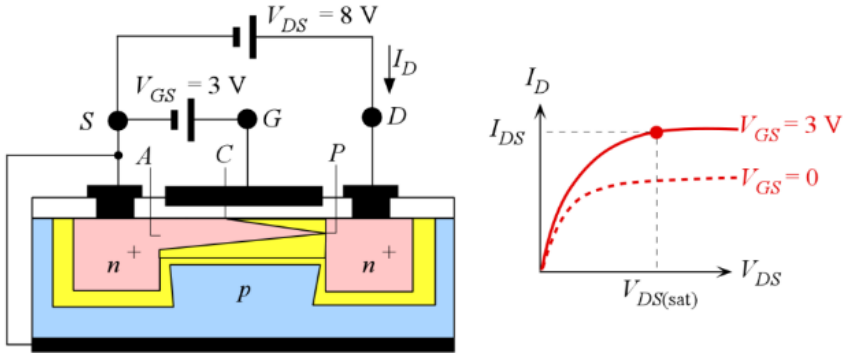




$V_{GS} = 0$, I_D increases with V_{DS} . Eventually at $V_{DS} = V_{DS(\text{sat})}$, the channel is pinched off and I_D becomes saturated at I_{DSS}.



Depletion mode: When V_{GS} is negative, the channel has a lower conductance and pinch-off occurs at a lower V_{DS}



Enhancement mode: When V_{GS} is positive, the channel has a higher conductance and pinch-off occurs at a higher V_{DS}

MOSFET Summary

When a positive voltage is applied to the gate, electrons are induced in the semiconductor below the gate oxide. Those electrons form a conductive *channel* between the source and the drain and a current may flow. Since the gate field controls the carrier concentration in the channel and hence the current, the transistor is also called *field-effect transistor* (FET).

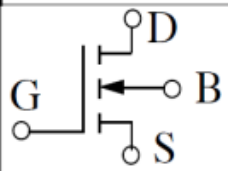
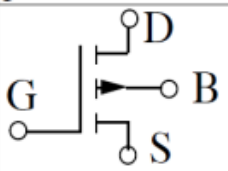
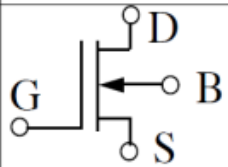
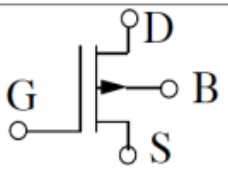
You may also found in the books the following abbreviations:

- MOSFET,
- MOST,
- IGFET,
- MISFET.

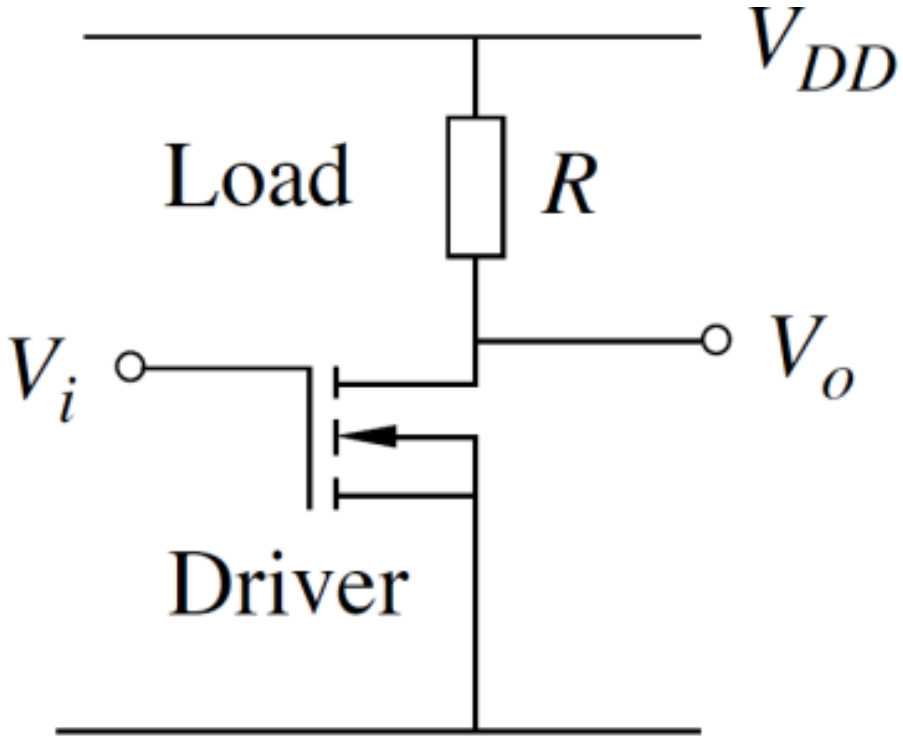
MOS transistor classification:

Channel type	Channel	Source and drain	Substrate
n-channel MOST	electrons	*n*-type	*p*-type
p-channel MOST	holes	*p*-type	*n*-type

Channel mode	
Enhancement mode	At V_G=0 no channel exists
Depletion mode	Channel exists without applying V_G

	n-channel	*p*-channel
Enhancement		
Depletion		

MOSFET Switching

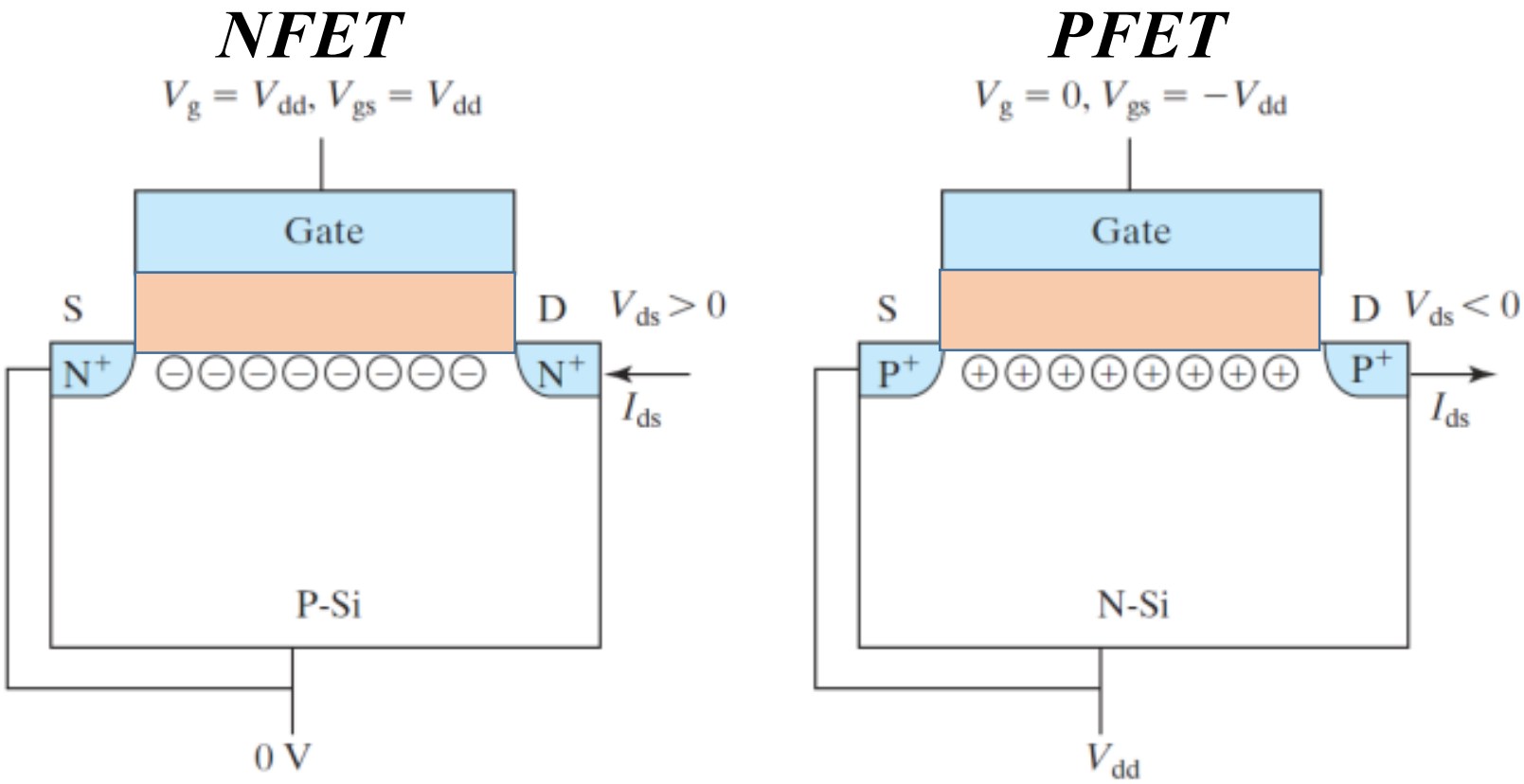


- Majority of MOSFETs are used in digital applications.
- Logical levels "0" and "1" correspond to the *on* and *off* states of the transistor.
- The basic MOSFET switching circuit is the MOS invertor shown opposite.

- The current through the load resistor R is given by $\frac{V_{DD}-V_o}{R}$ which determines the load line.
- The typical value for the load resistor is R=1 MΩ.
- A *dc* current flows through the invertor when the driver is ON. This causes a significant power dissipation in an integrated circuit with millions invertors.

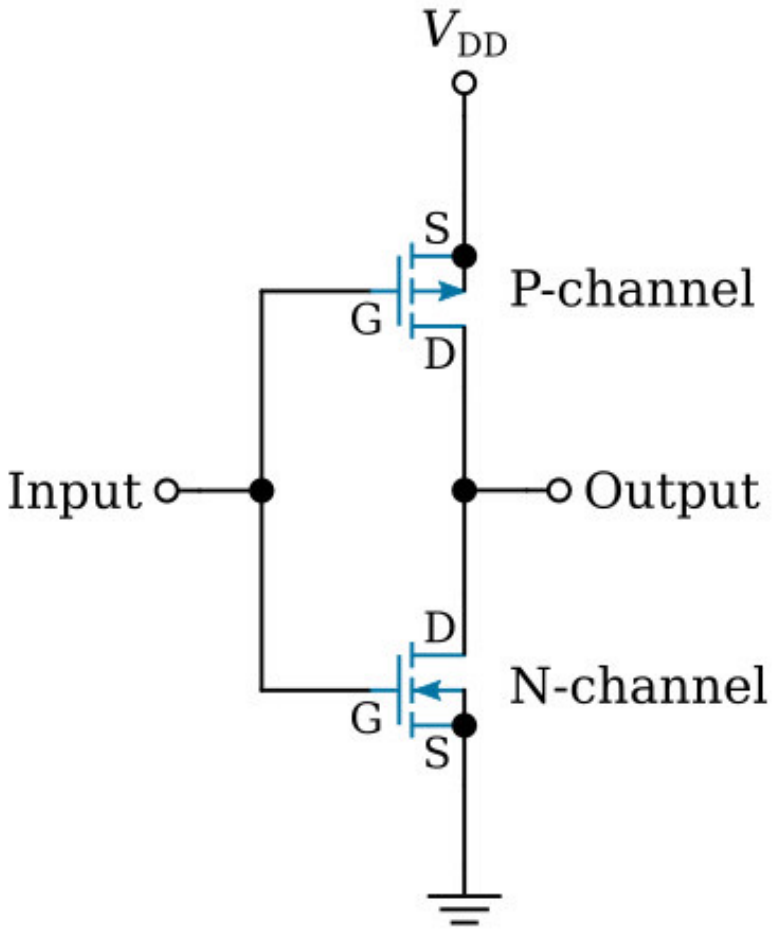
CMOS

- One of the most popular MOSFET technologies available today is the CMOS (Complementary MOS) technology.
- CMOS is one of the most popular technology in the computer chip design industry.



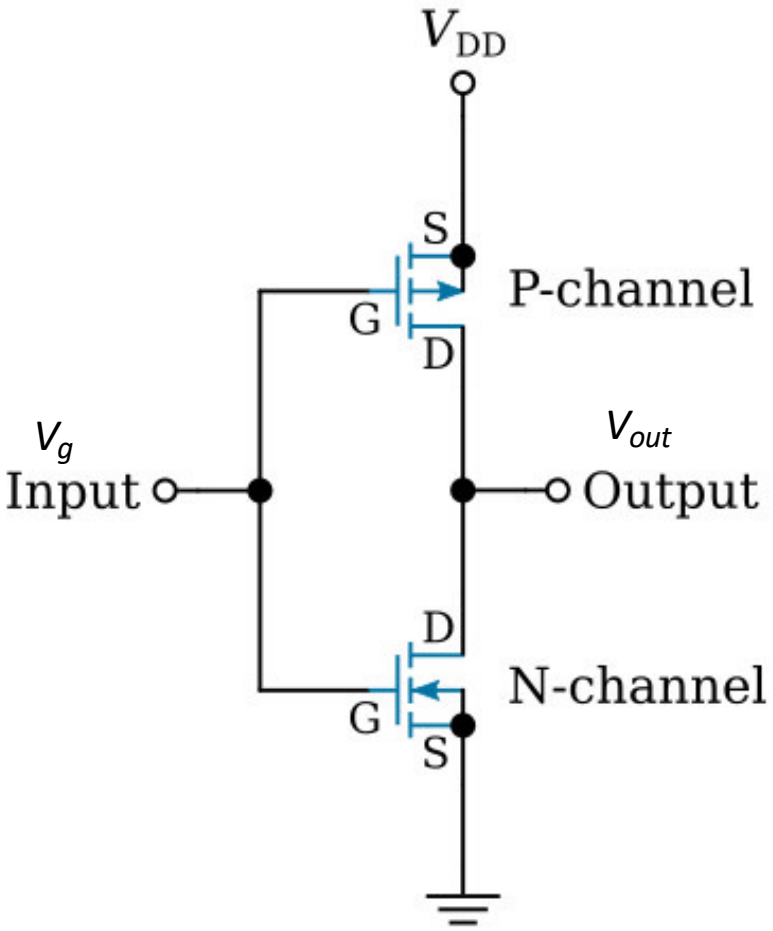
When $V_g = V_{dd}$, the NFET is on and the PFET is off.
When $V_g = 0$, the PFET is on and the NFET is off.

CMOS



The complementary nature of NFETs and PFETs makes it possible to design low-power circuits called **CMOS** or **complementary MOS** circuits.

CMOS



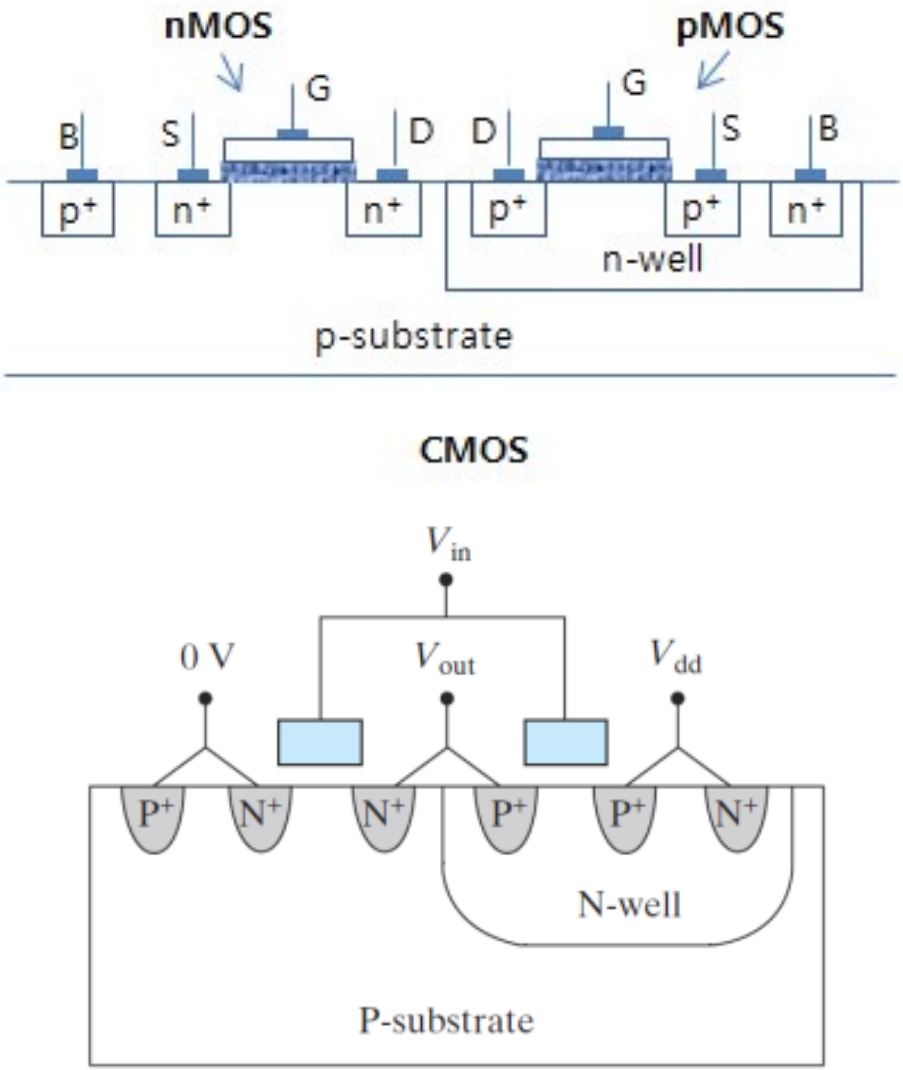
When *input voltage* $V_g = V_{dd}$, the NFET is on and the PFET is off (think of them as simple on–off switches), and the output node is pulled down to the ground ($V_{out} = 0$).

When *input voltage* $V_g = 0$, the NFET is off and the PFET is on; the output node is pulled up to V_{dd}.

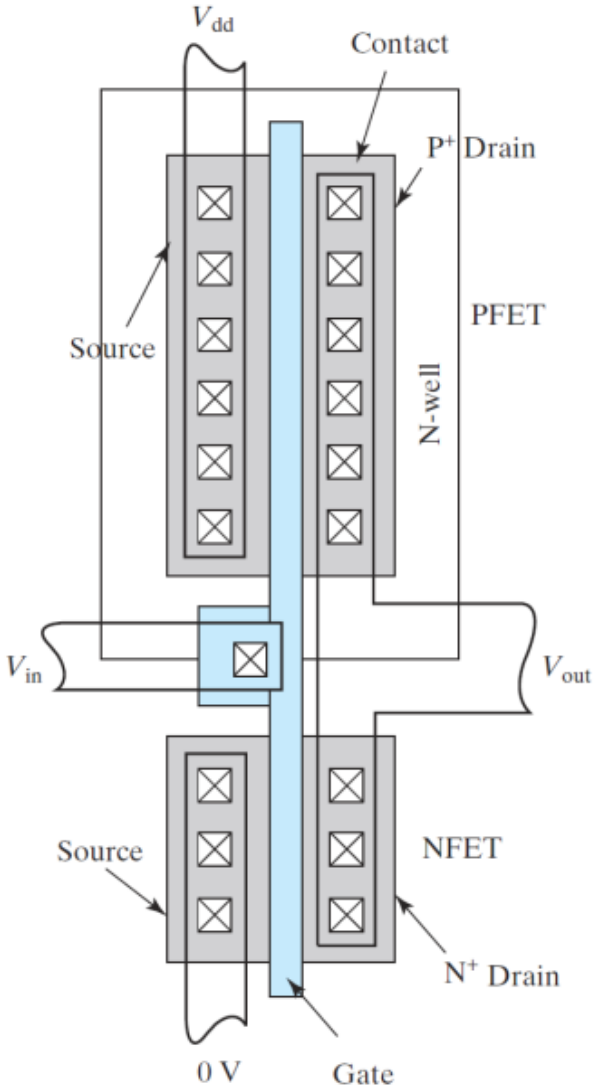
In either case, one of the two transistors is off and there is no current flow from V_{dd} through the two transistors directly to the ground. Therefore, CMOS circuits consume much less power than other types of circuits.

A CMOS inverter is made of a PFET ***pull-up device*** and a NFET ***pull-down device***. $V_{out} = ?$ if $V_{in} = 0$ V.

CMOS

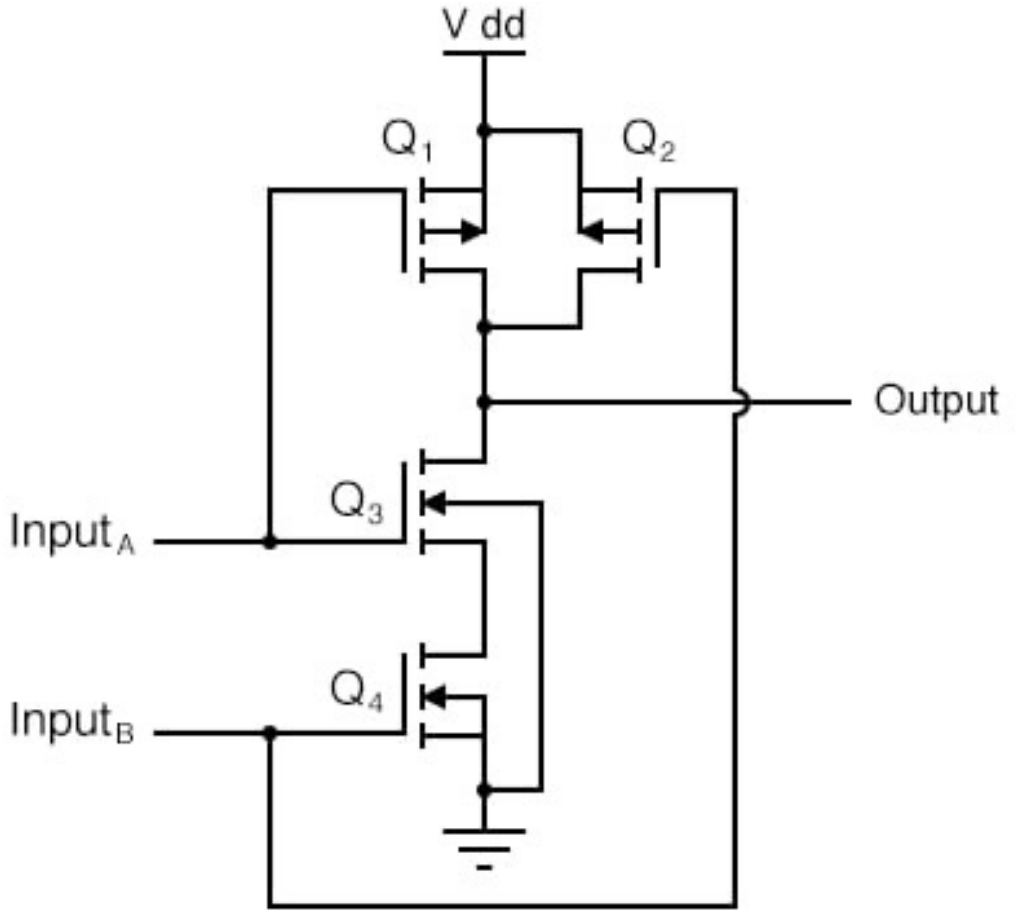


NFET and PFET can be fabricated on the same chip.



Basic layout of a CMOS inverter

CMOS as logic gate



What logic is implemented through this circuit of CMOS combination?