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UESTC 3002/HN3008: Electronic Devices

Lecture 2.1: *p-n Junction (1)*

WORLD CHANGING GLASGOW

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Lecture 2.1: *p-n Junction (1)*

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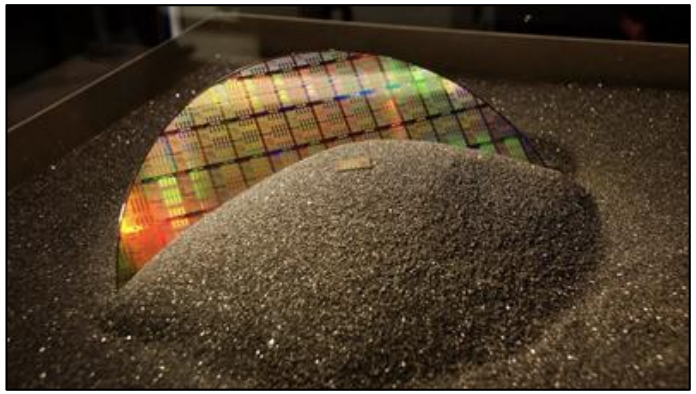
Reading: Chapter 5, Solid State Electronic Devices 7E, Ben G. Streetman, Sanjay K. Banerjee

In today's lesson



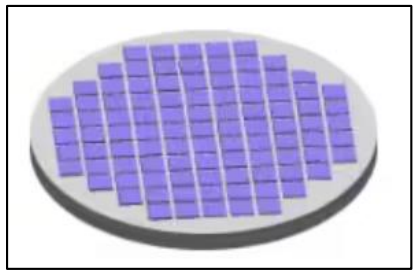
- Semiconductor Manufacturing
- How p-n junction is formed?
- Characteristics of the p-n junction
- Forward-bias and reverse-bias
- Diode Equation
- Class Task: Real-World Application Case Study (Teams of 4-5)

"The only thing that distinguishes the man who makes semiconductors from those who don't is the vision to see their possibilities"
— *William Shockley, Beyond the Semiconductor: A Memoir*

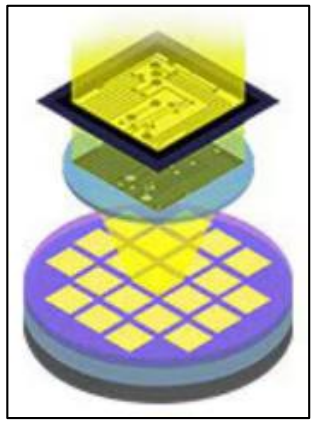
Source: newport.com

Semiconductor Manufacturing Process

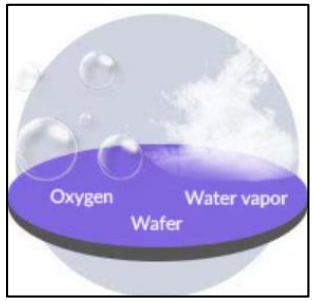
Wafer Manufacturing → Oxidation → Photolithography → Etching → Deposition and Ion Implantation → Metal wiring → Electrical Die Sorting → Packaging



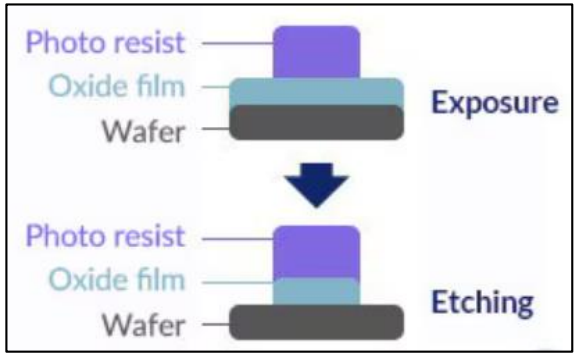
The main material used for making semiconductors integrated circuits



The process of drawing circuits on the wafer



The process of making the foundation of the transistor by forming a silicon oxide film on the wafer surface. Protects and blocks leakage current between circuits



The process of making patterns that form the semiconductor. Removing parts other than necessary circuit patterns

Source: semiconductor.samsung.com

Semiconductor Manufacturing Process

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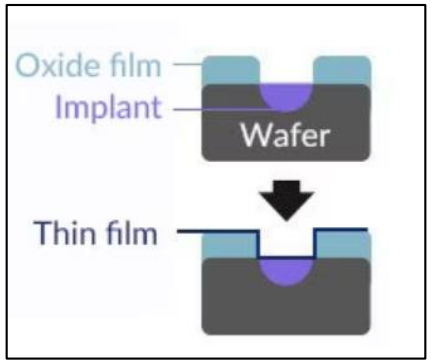
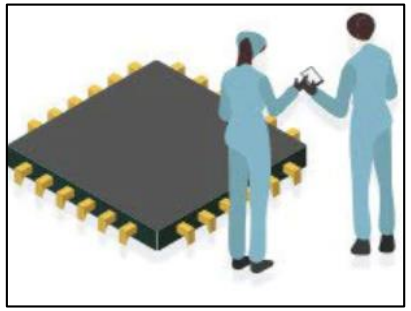


Deposition: making a thin film that protects, distinguishes and connects each circuit.
Ion Implantation: giving electrical properties to semiconductors



Checking whether each chip has reached the desirable quality level through electrical property testing

The process of linking the metallic wires so that electrical signals are delivered well

The process of making paths for chips to exchange signals externally, and forming them to be safely protected from various external environments

Source: semiconductor.samsung.com

Fabrication of p-n junction

Oxidation – protects the wafer's surface

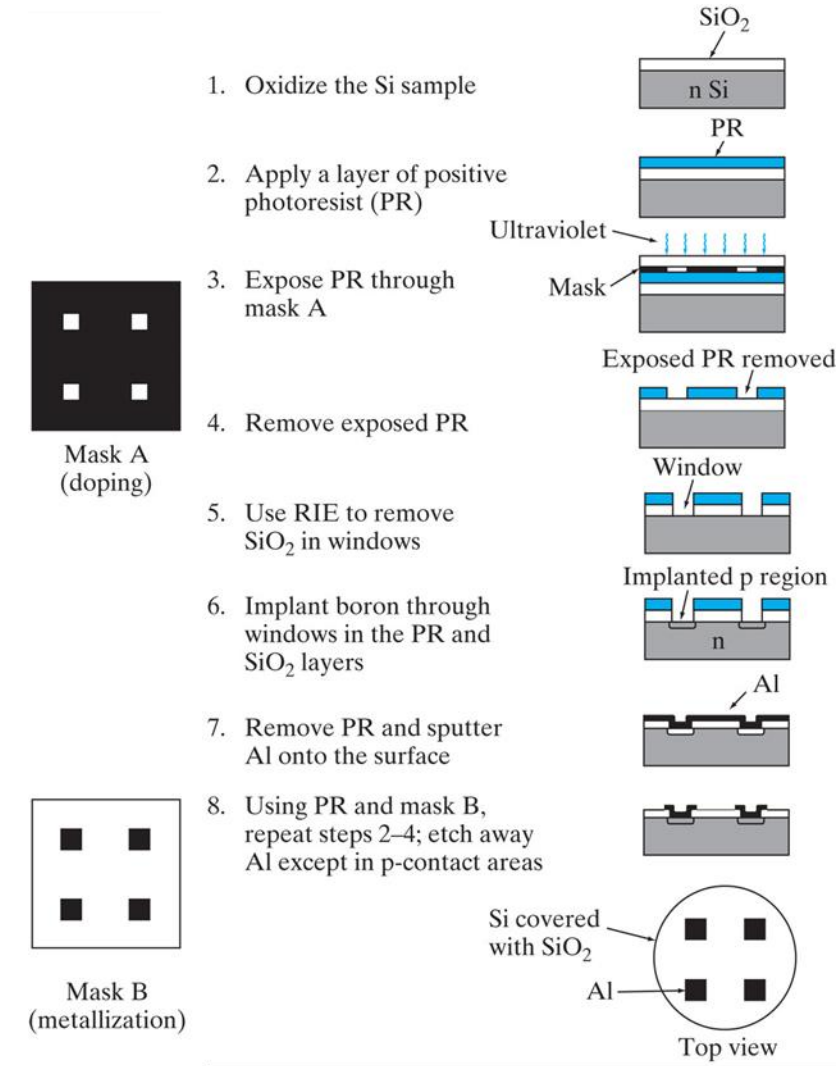
Photolithography – drawing circuits onto a wafer

Etching – completion of circuit pattern

Deposition & Ion Implantation – electrical properties

Metal Wiring – electrical highways

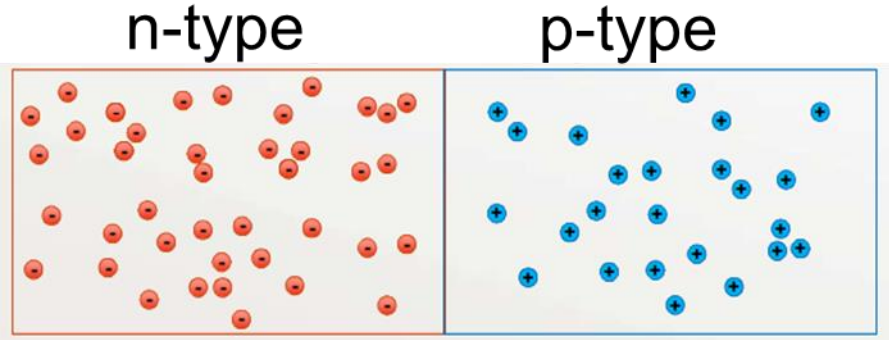
EDS – Testing for the desired quality



Simplified description of steps in the fabrication of p-n junctions.

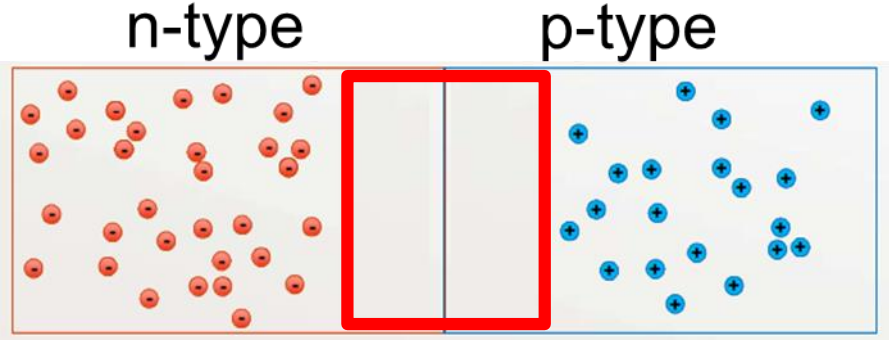
Source: Solid State Electronic Devices 7E, Ben G. Streetman, Sanjay K. Banerjee

p-n junction



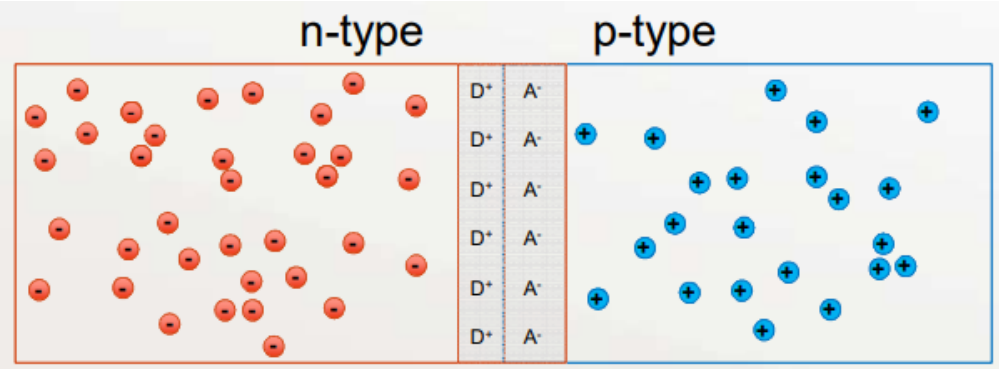
Concentration Gradient → Diffusion

- Diffusion Driven by Concentration Gradient
- Holes diffuse from the p-type region to the n-type region, followed by recombination.
- Electrons diffuse from the n-type region to the p-type region, followed by recombination.



depletion region

Depletion Region

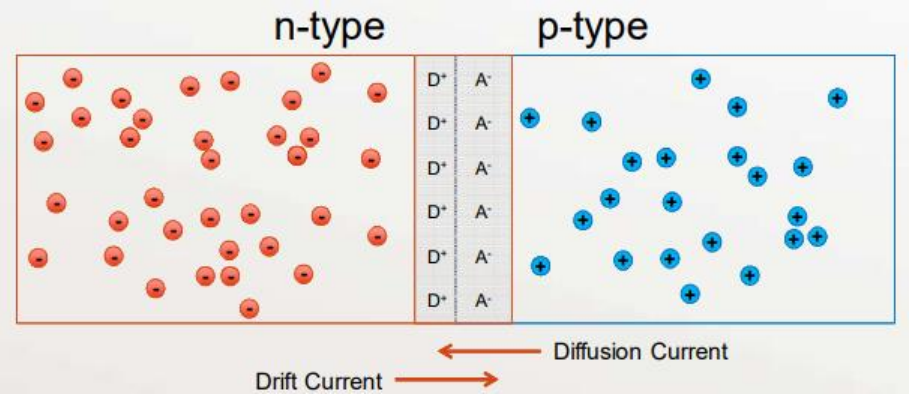


Depletion Region ⇔ Space Charge Region
(Interchangeable Terms)

- Depletion region contains essentially no mobile charge carriers.
- Ionized dopants remain fixed and contribute to a net charge, which is why the depletion region is also called the space charge region.
- Built-in voltage across the p-n junction.

Charge Separation → Voltage V

Steady State: Diffusion = Drift



Typical built-in voltages

Semiconductor	V_{bi} (V)
Si	0.78
Ge	0.37
GaAs	1.21

- Built-in voltage → drift current (in the opposite direction as diffusion)
- Steady state: where diffusion current equals drift current

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_D N_A}{n_i^2}\right)$$

$$\frac{kT}{q} = 25mV, at\ T = 300K$$

k Boltzmann constant (1.38×10^{-23} J/K)
T is the absolute temperature in Kelvin (300 K)
q charge of an electron (1.6×10^{-19}C)

N_A, N_D typical values 10^{16} to 10^{19} cm^{-3}
depend on the application and the desired electrical characteristics

Depletion Width

- The depletion region's width affects the diode's behaviour, including its capacitance and the characteristics of the electric field.
- At steady state

$$W = \sqrt{\frac{2\epsilon_0 \epsilon_r V_{bi}}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)}$$

For a silicon: $\varepsilon_r = 11.7$

$\epsilon_0 = 8.854 \times 10^{-14}$ F/m

- The total charge on the n-side must be equal to that on the p-side side for overall charge neutrality, so

$$N_A W_p = N_D W_n$$

$N_A \gg N_D$, the depletion region is almost entirely on the n-side, due to the need to balance the charge and the resulting electric field that promotes electron movement from the n-sideand vice-versa.

heavily doped regions, p^+, n^+

p-n junction biasing

- Biasing a p-n junction means applying an external voltage to control electrical behaviour.
- Biasing changes the depletion region width.
- A diode is a device that allows current to flow in one direction while blocking it in the opposite direction.

Zero bias: No external voltage is applied

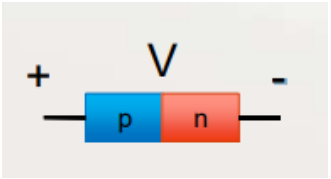
Forward bias: Positive Terminal ↔ p-type and Negative Terminal ↔ n-type (depletion region gets smaller)

Reverse bias: Positive Terminal ↔ n-type and Negative Terminal ↔ p-type (depletion region gets bigger)

p-n junction biasing

During biasing, almost all of that voltage falls across the depletion region.

$$W = \sqrt{\frac{2\epsilon_0\epsilon_r\,(V_{bi}-V)}{q}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)}$$



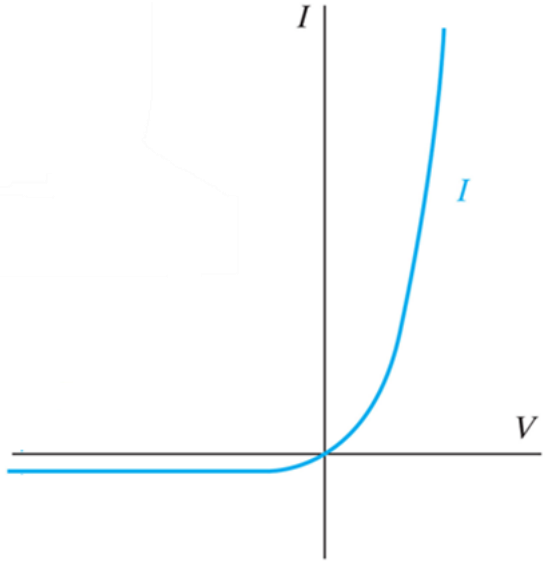
The applied voltage either increases or decreases the built-in voltage, resulting in a junction voltage of $V_{bi}-V$.

Small depletion width → increases diffusion current due to lower electric field/potential barrier

Large depletion width → decreases diffusion current due to higher electric field/potential barrier

Ideal diode (Shockley) equation

$$I = I_0\left(e^{qV/kT} - 1\right)$$



I-V characteristics of a diode in ideal conditions.

- In forward bias (positive voltage), the current increases exponentially with voltage.
- In reverse bias (negative voltage), the current approaches the small reverse saturation current I_S .

ED Class Task:
Real-World Application Case Study

Teams of 4-5: 15-20 minutes

Task:

- Research the **real-world applications** of p-n junctions (for example: transistors). (5-7 minutes)
- Analyze how **built-in potential** and **depletion region width** affect the performance of the device. (3-4 minutes)
- **Present** your findings, focusing on: (5-6 minutes)
  - The **importance** of p-n junctions in your assigned application.
  - The **implications** of these concepts for device functionality.
- Participate in a class discussion about: (2-3 minutes)
  - The **impact** of understanding these principles on future innovations in electronics.

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Design Example

Design a silicon-based PN junction diode for a specific application. The desired characteristics of the diode are: the p-type region should have an acceptor concentration $N_a = 1 \times 10^{18}$ cm^{-3} and the n-type region should have a donor concentration $N_d = 1 \times 10^{15}$ cm^{-3}. The diode will operate at room temperature (300 K). The relative permittivity of silicon is 11.7. The intrinsic carrier concentration of silicon $n_i = 1.5 \times 10^{10}$ cm^{-3}. Assume no external voltage is applied. Determine the width of the depletion region. Calculate the built-in potential of the diode.

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Design Example: Solution

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In next Lecture

- Junction Capacitance
- Carrier Action


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Thank you
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