晶体管的分类:

$$\text{BJT:(双极晶体管)}\begin{cases}\text{PNP}\\ \text{NPN}\end{cases} \tag{1}$$

$$\text{FET:(场效应晶体管)}\begin{cases}\text{JFET}\\ \text{MOSFET}\end{cases} \tag{2}$$

BJT

BJT 在 1948 年于贝尔实验室发明, 主要作用是放大和当作开关.
BJT 可以视为由两个共有一个区域的 PN 结构成, 两边分别是 Emiiter(发射极),Collector(集电极)和基级(Base).

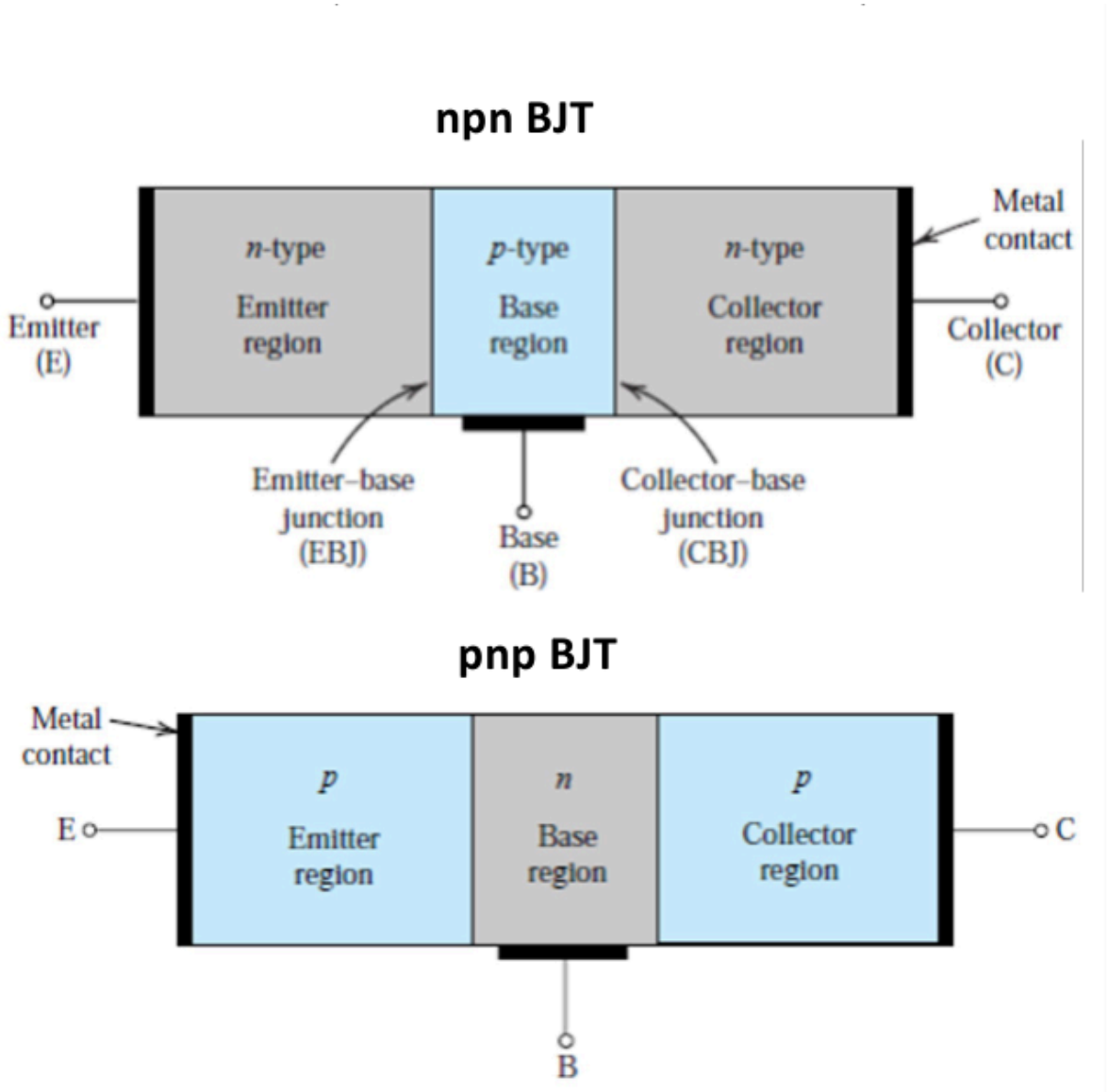


Figure 1: BJT 的结构

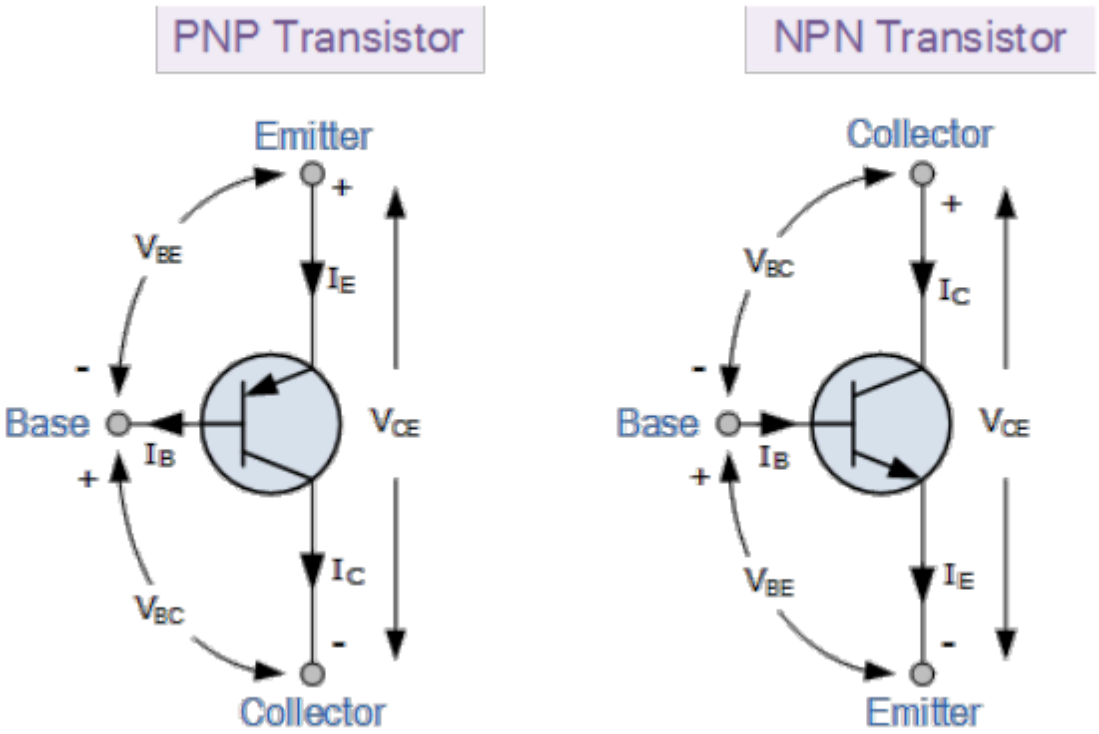


Figure 2: NPN:从 C 到 E,PNP:从 E 到 C;箭头的一端始终是 E 极

BJT 的工作模式

由V_{BC}和V_{BE}决定,组合起来是有四种?

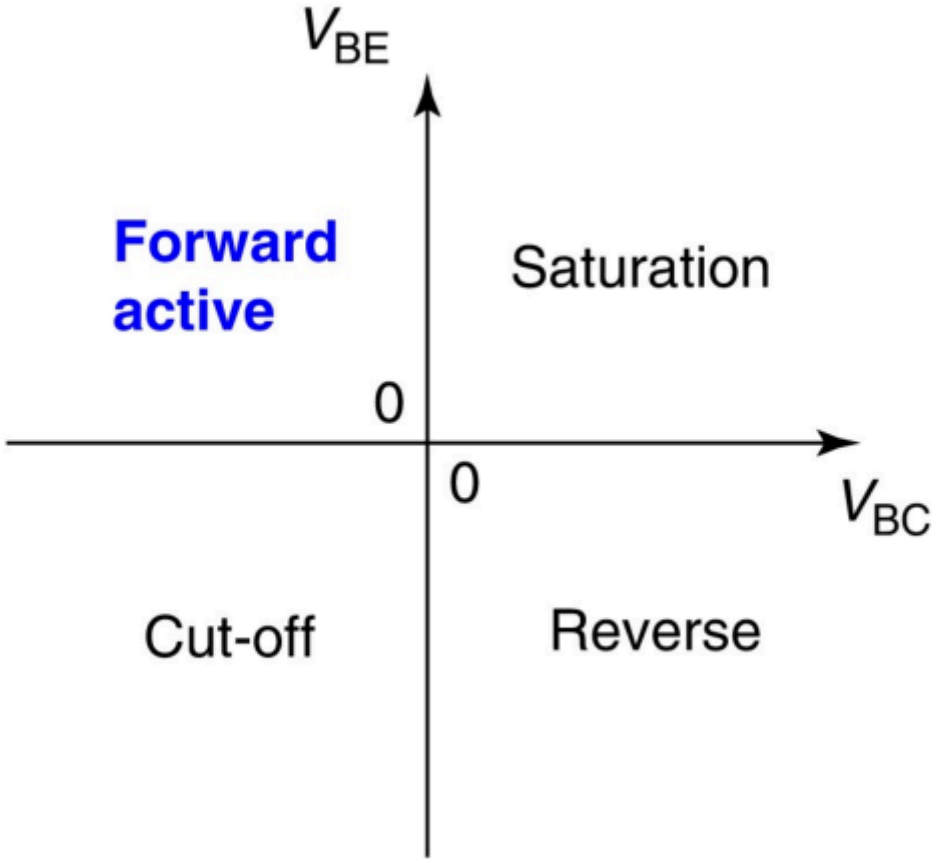


Figure 3: 四种工作模式

放大区(Forward active)

- 条件:$V_{\mathrm{BE}} > V_t \approx 0.7V$,$V_{\mathrm{CB}} > 0$
- 电流放大:$I_C = \beta I_B = I_S\left(e^{\frac{V_{\mathrm{BE}}}{V_T}} - 1\right)$
  - $I_S = A_E q \frac{D_B}{W_B} \frac{n_{\mathrm{ib}}^2}{N_B}$
  - D_B:中间 P 区少子(电子)的 diffusion 常数
  - A_E:发射极面积
  - W_B:基极的宽度
  - n_{ib}:基级的本征浓度
- 对于 NPN 管,Base 和 Collector 是反向偏置的, I_C基本不受到这个电压的影响

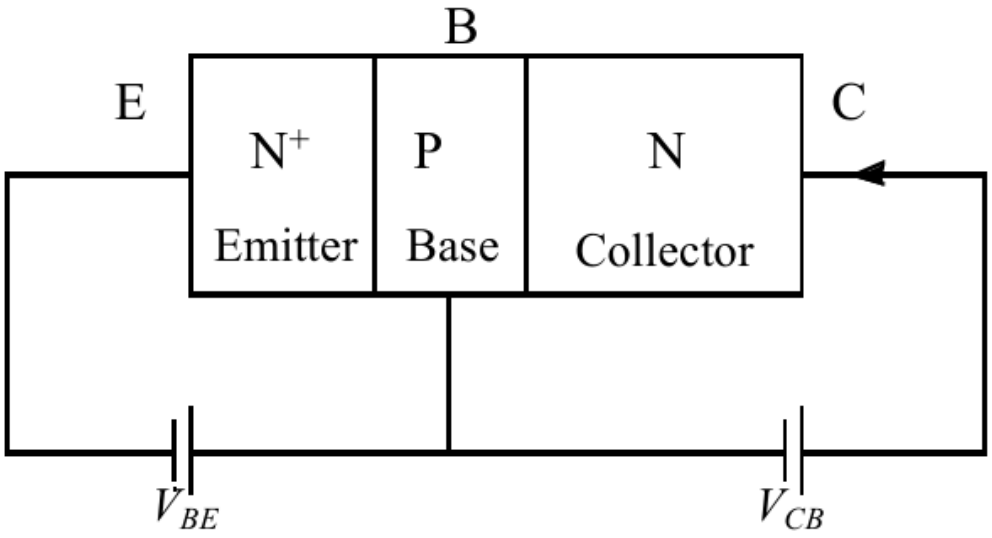


Figure 4: 放大 qu

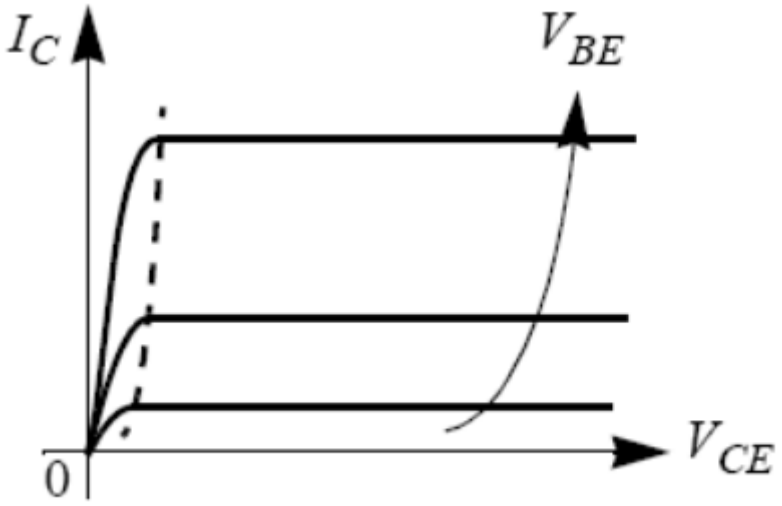


Figure 5: 以V_{CE}为轴

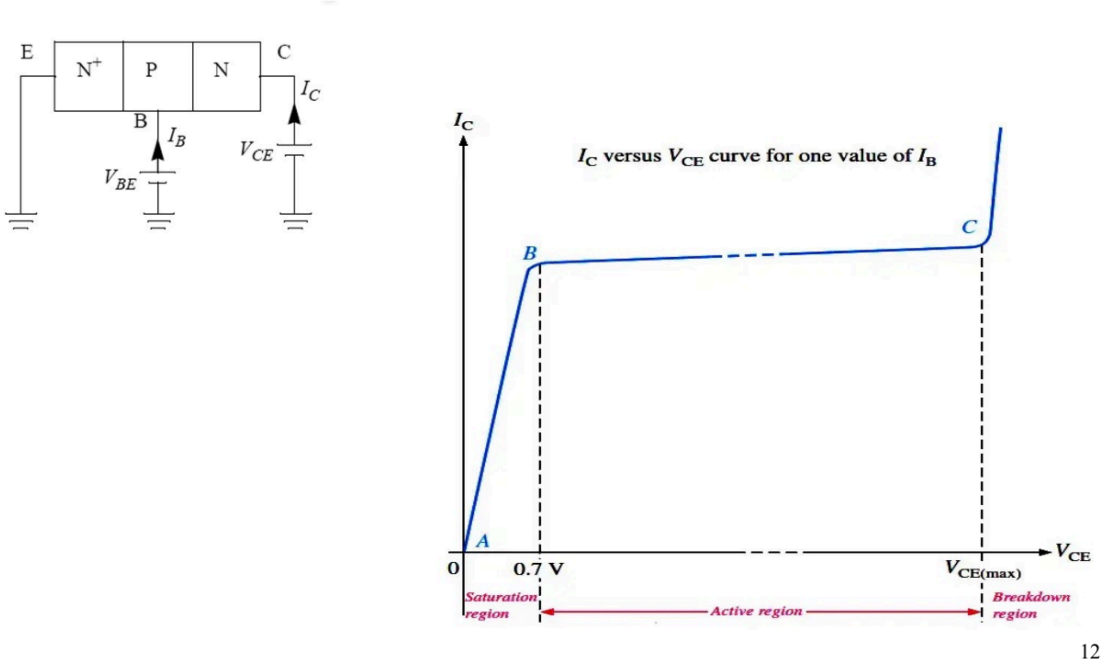


Figure 6: 对于 Common Emiiter, 随着V_{CE}增加从饱和区到放大区再到击穿区

关于电流增益(以 **npn** 为例子)

$$I_C = \beta I_B \tag{3}$$

$$I_E = I_B + I_C \tag{4}$$

$$\frac{I_C}{I_E} = \alpha = \frac{\beta}{\beta + 1} \text{ base transport factor} \tag{5}$$

$$\beta_F = \frac{G_E}{G_B} = \frac{D_B W_E N_E n_{iB}^2}{D_E W_B N_B n_{iE}^2}$$

Figure 7: 用物理公式计算

BJT 的耗能

$$P = V_{\mathrm{BE}} I_B + V_{\mathrm{CE}} I_C \tag{6}$$

基级宽度调制效应(Base-Width Modulation)

会导致在放大区, 随着V_{CE}的增大, I_C也增大的效应

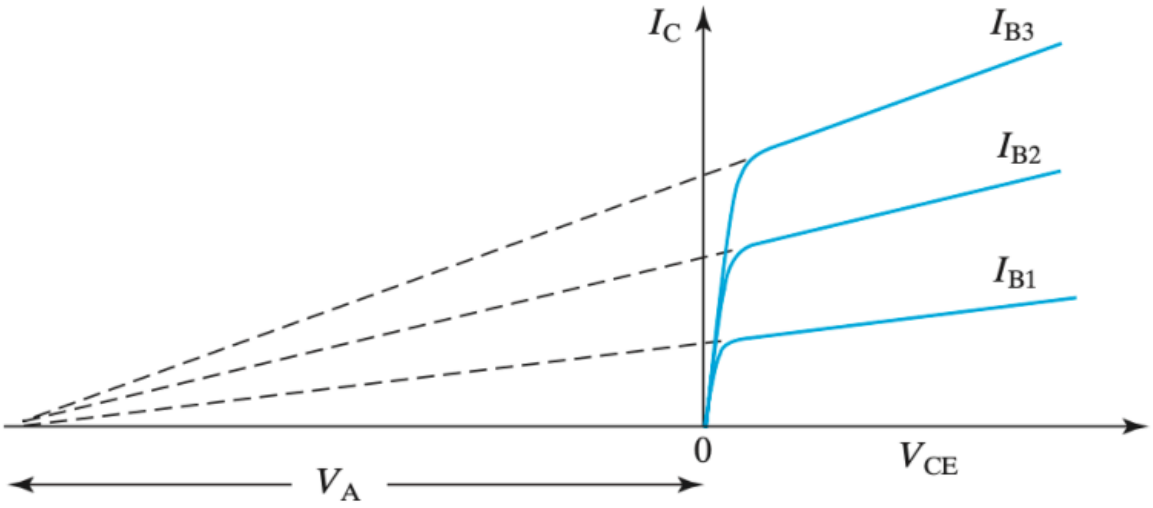


Figure 8: 基极宽度调制效应

$$I_C = \beta I_B \left(1 + \frac{V_{\text{CE}}}{V_A}\right) \tag{7}$$

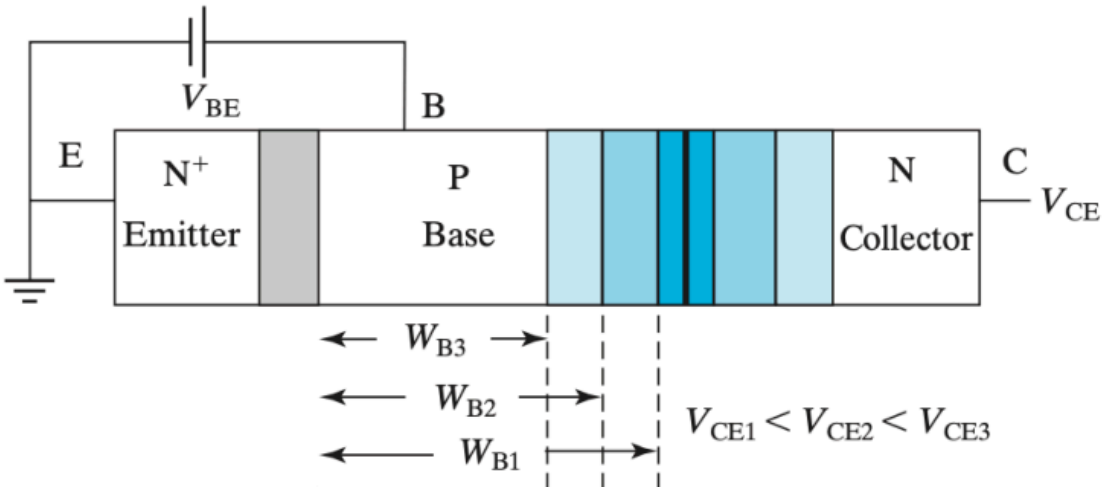


Figure 9: 随着V_{CE}增加,集电极和基极之间的耗尽层会增大

如何减小这种效应?

- 增加基极宽度
- 增加基极的参杂浓度(concentration)
- 减少集电极参杂浓度

这种效应又叫做:Early effect(Early 是人名)

BJT 的发射效率(emiiter efficiency)

$$\gamma = \frac{I_E - I_B}{I_E} = \frac{I_C}{I_C + I_B} \tag{8}$$

JFET(Junction field transistor,场效应晶体管)

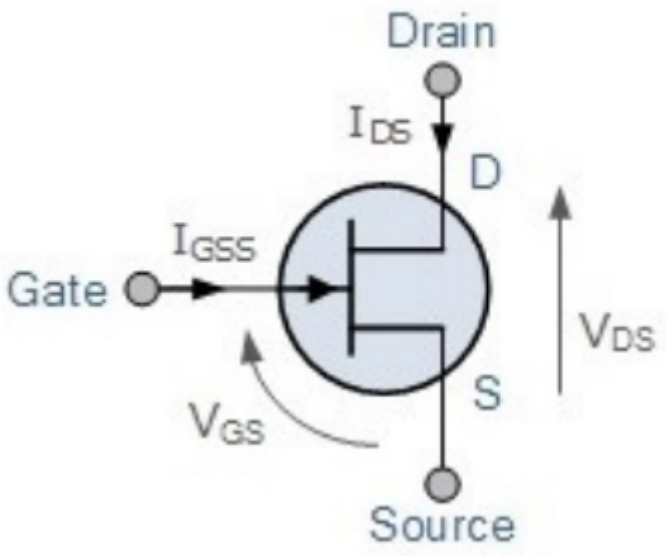


Figure 10: JFET 也有三个极(漏级,源极还有栅极)

是一种控制电压的器件(BJT 用于控制电流)

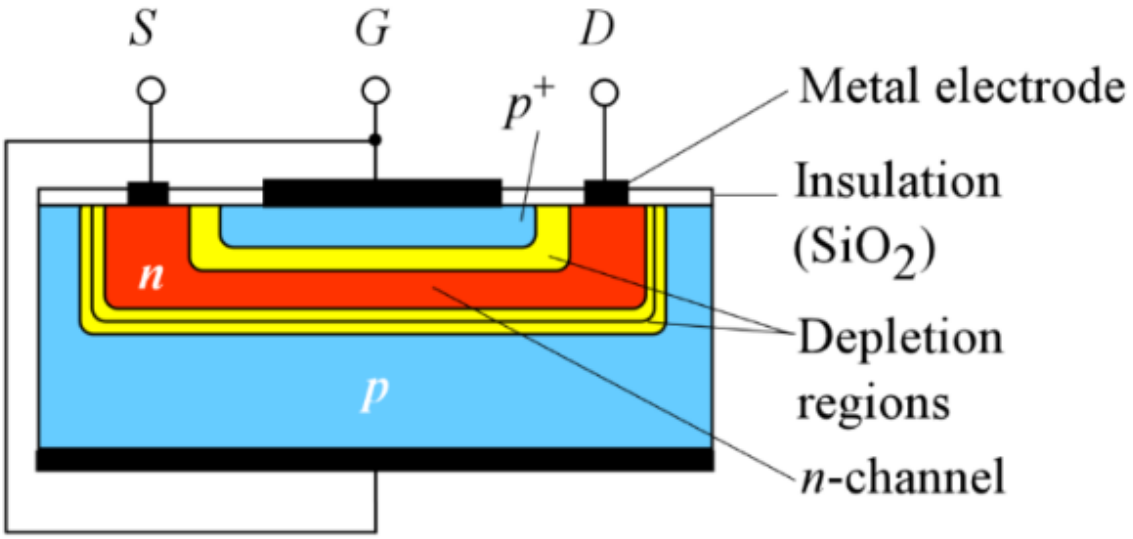


Figure 11: n 沟道 JFET 的结构

pinch-off voltage(夹断电压)

随着V_{DS}的增加,Drain 极的两个耗尽区会逐渐接近, 直到挨到一起,这个节点的电压 是夹断电压, 夹断了之后, I_D不随着V_{DS}而增加

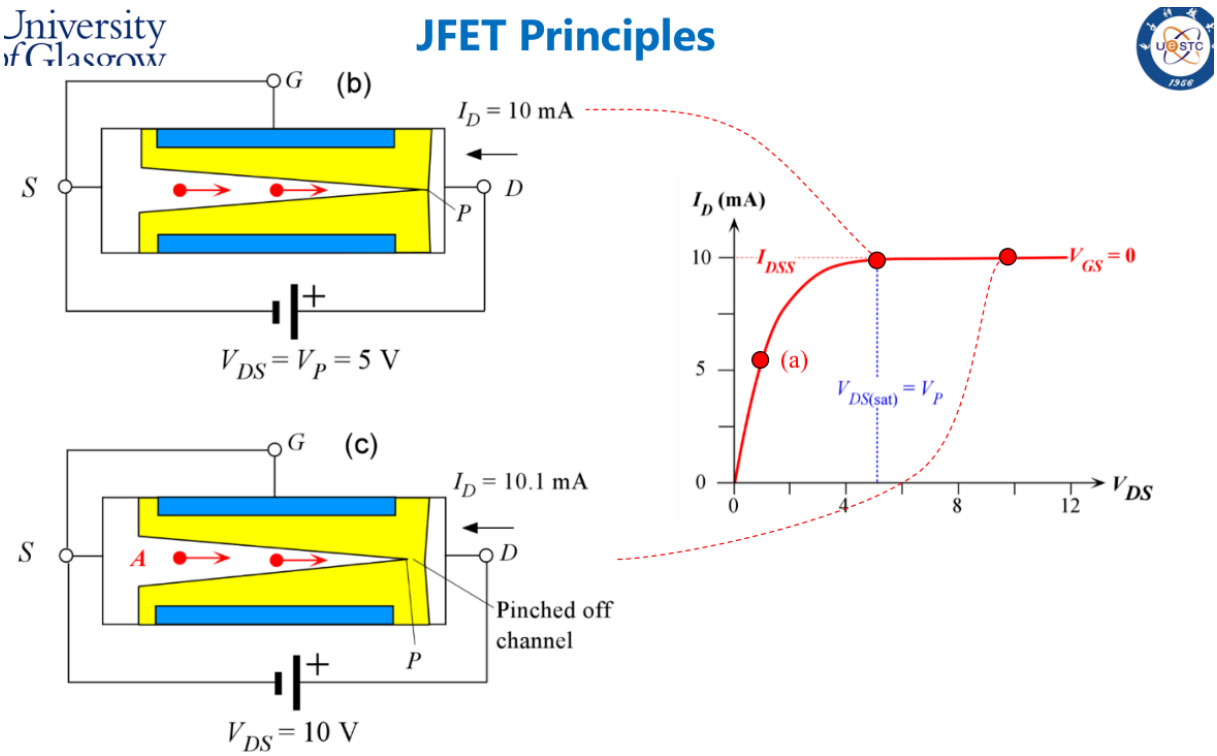


Figure 12: JFET 的原理

比如沟道是 n 型的,那么其中的电子会被迅速拉入 D, 这个过程收到V_{DS}和v_{GS}的限制
在饱和区,I_D满足$I_D = \frac{V_p}{R_{\mathrm{AP}}}$, 和从 A 到 P 的沟道电阻有关(S 接地)

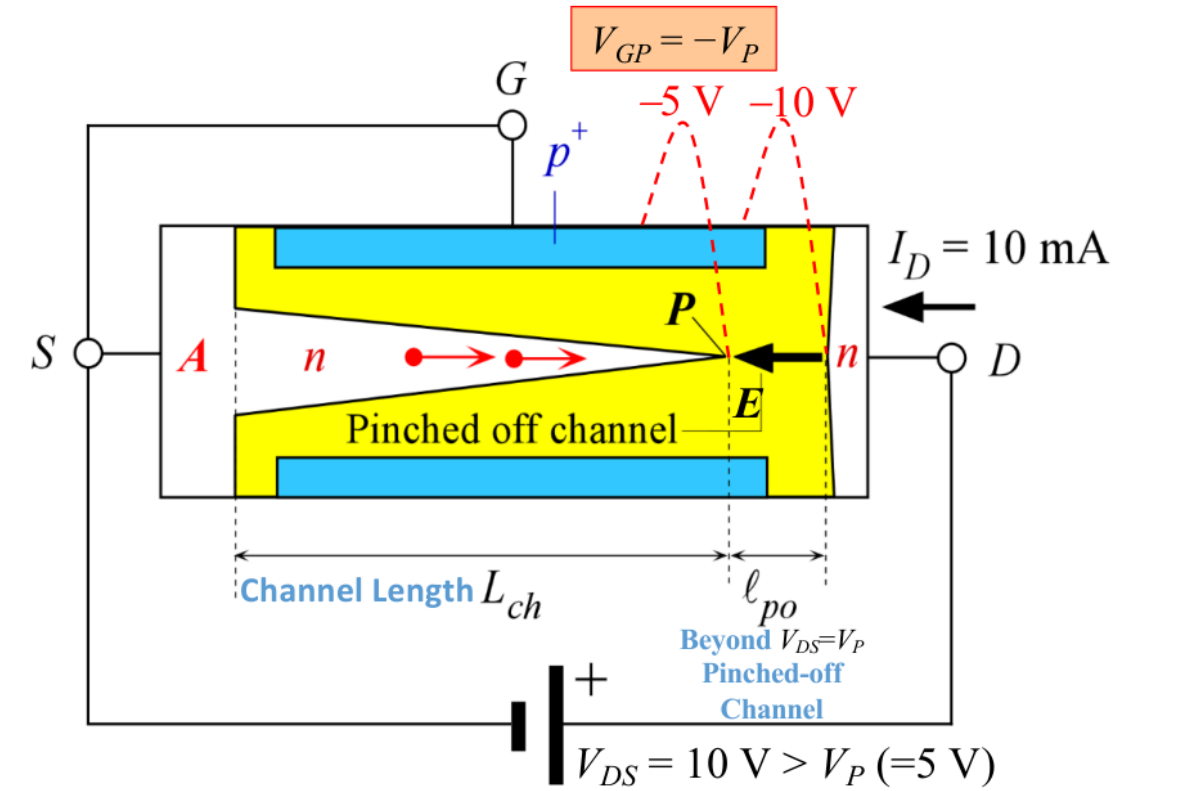


Figure 13: 决定 p 的位置的重要关系$V_{\mathrm{GP}} = -V_p$

$I_D = \frac{V_{\mathrm{DS}}}{R_{\mathrm{AB}}}$,在饱和区,增加$V_{\mathrm{DS}}$由于 PN-结的效应, R_{AB}也增加了, 最终电流不会随着V_{DS}线性增加了

V_{GS}的影响(之前的都是 G 和 S 一起接地的情况)

加了正的V_{GS},一开始就扩展了耗尽区的厚度, 达到饱和区跟容易了

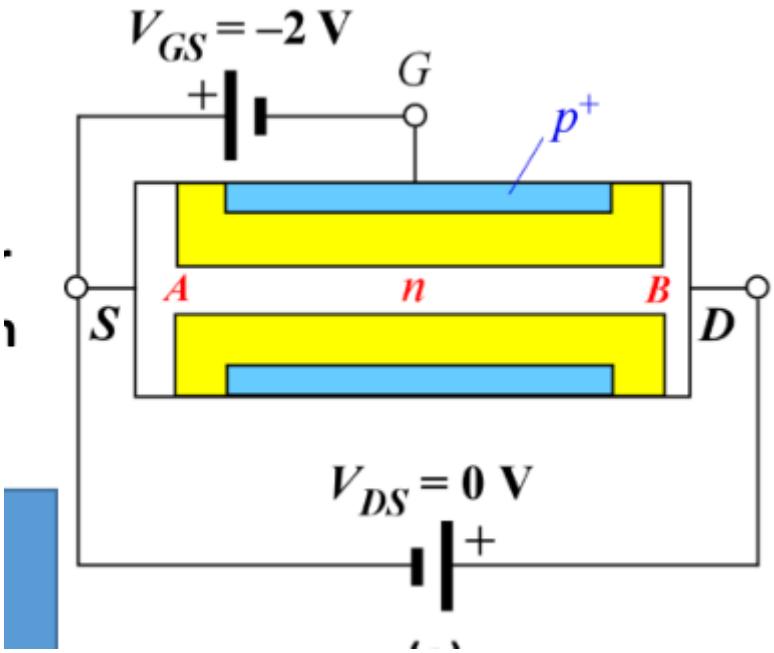


Figure 14: 加了V_{GS}

新的饱和区条件:$V_{\mathrm{DS}} = V_{\mathrm{GS}} + V_p$
还是满足:$V_{\mathrm{GP}} = -V_p$

V_{GS}Turn-off 的情况

$$V_{\mathrm{GS}} = -V_p \tag{9}$$

$V_{\mathrm{DS}} = 0$就完全夹断了, 完全成了耗尽层,加上V_{DS}也只能由热激发的电子导电,这个电流非常小

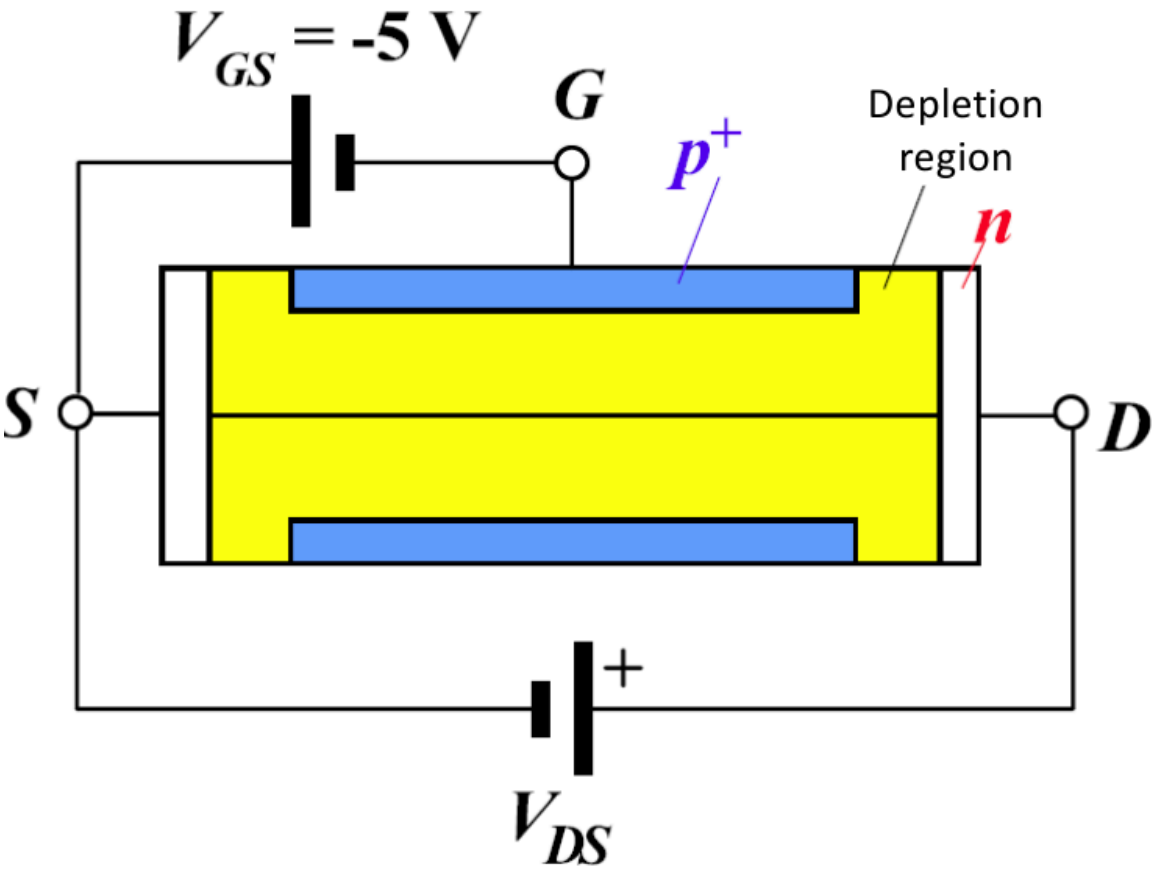


Figure 15: Turn off

JFET 的电流电压特征

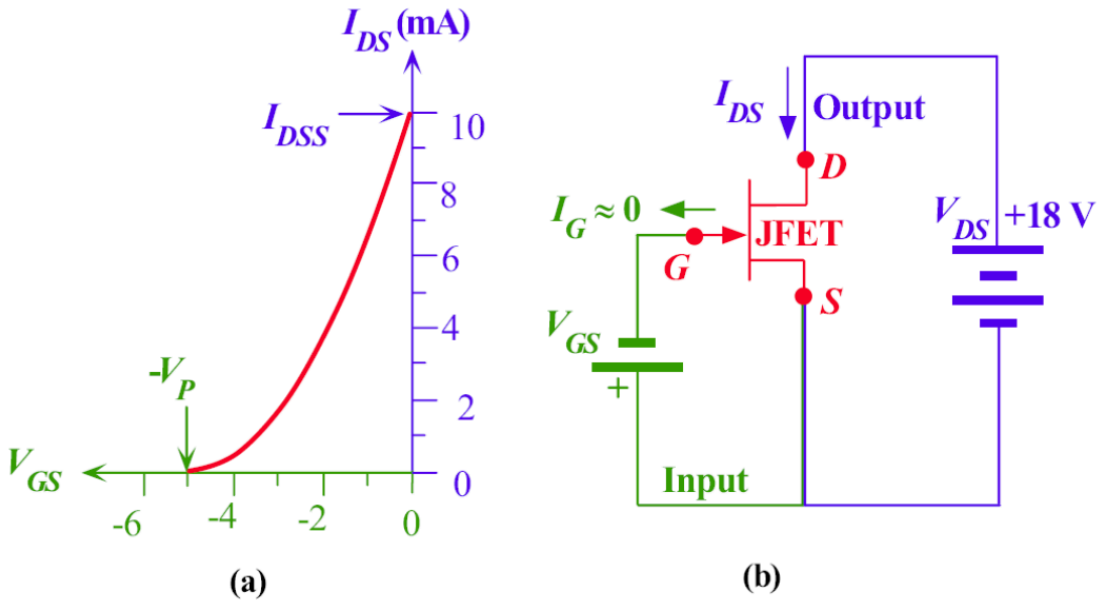


Figure 16: V_{DS}是常数,由V_{GS}控制I_{DS}

饱和区

$$I_D = I_{\text{DSS}}\left(1 + \frac{V_{\text{GS}}}{V_P}\right)^2 \tag{10}$$

I_{DSS}指的是$V_{\text{GS}} = 0$的时候的I_D

线性区(欧姆区)

$$I_D = k \cdot V_{\text{DS}} \tag{11}$$

k 由V_{GS}和沟道常数等因素决定

JFET Commons Source Amplifier—用 JFET 构造放大器

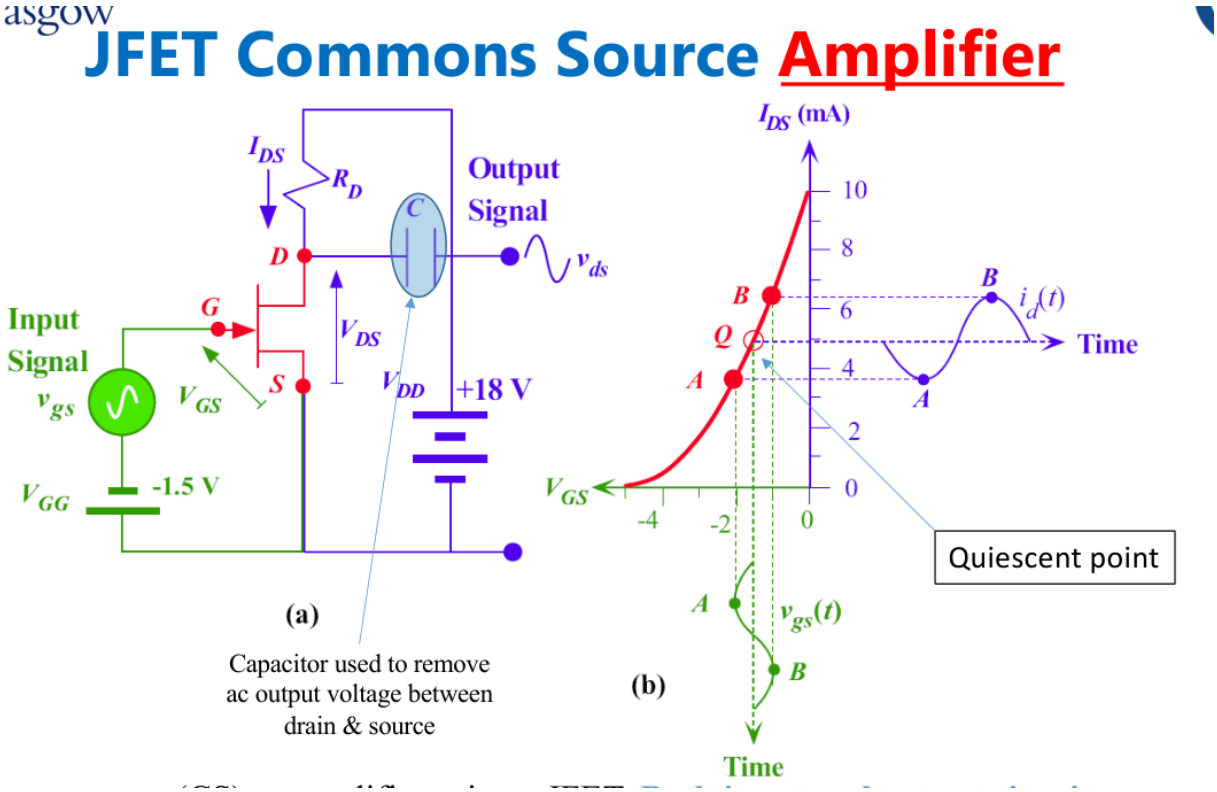


Figure 17: 共源放大器

直流偏置$V_{\text{GG}} < 0$,上面加一个交流小信号,

$$g_m = \frac{i_d(i_d\text{的微小变化})}{v_{\text{gs}}(v_{\text{gs}}\text{的微小变化})} \tag{12}$$

对 Equation 10 求$\frac{\partial I_D}{\partial V_p} = \frac{2I_{\text{DSS}}}{V_p}\left(1 + \frac{V_{\text{GS}}}{V_p}\right) = \left(2\frac{\sqrt{I_{\text{DSS}} I_{\text{DS}}}}{V_p}\right)$

$$A_v = -g_m R_D \tag{13}$$

, 由于非线性性质, 放大较大的信号的时候增益会比较低

MOSFET

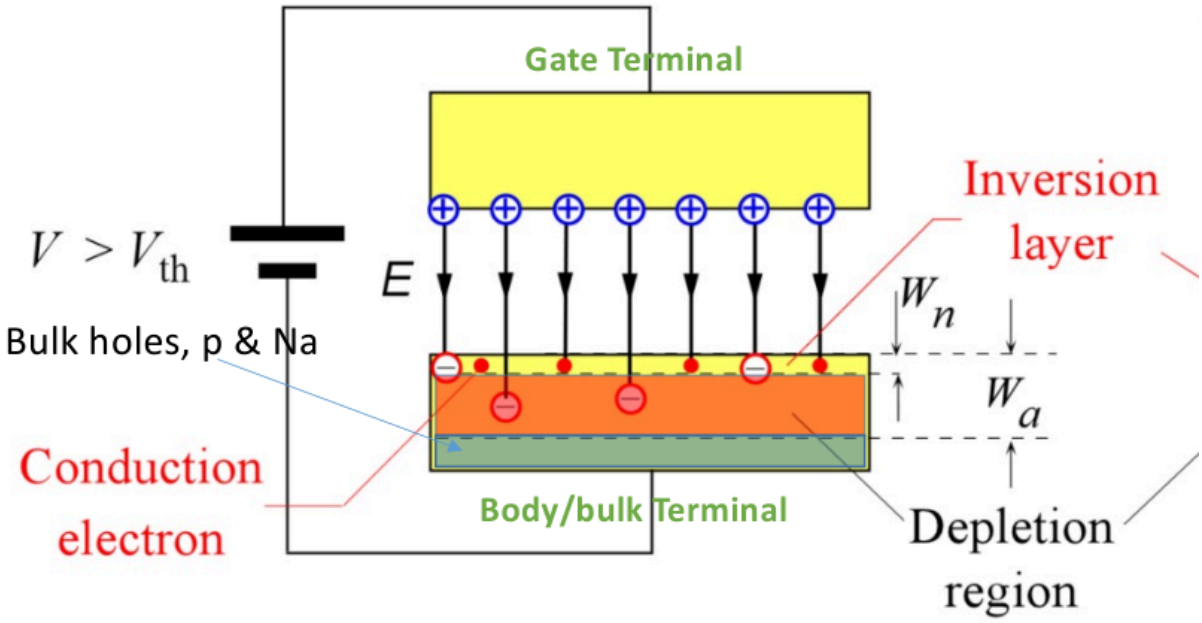


Figure 18: 电容器连接负极的换成了 p 型半导体

会在 p 型半导体表面形成一个反转层,然后是耗尽区, 使得反转层电子浓度和 p 型本体空穴浓度相等的电压就是V_t.

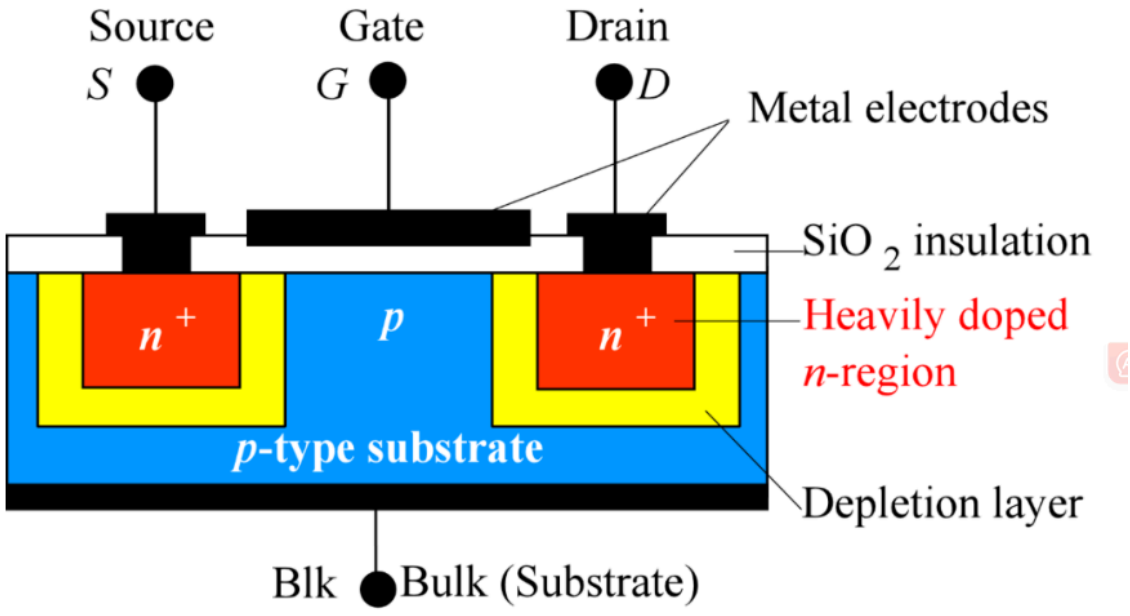


Figure 19: n 沟道 MOSFET,S 和 D 极是高浓度参杂的

$V_{\mathrm{GS}} > V_t$的话, 会形成反转层使得 S 和 D 之前能够导通,再加上一个V_{DS}就能形成电流 $I_D = \frac{v_{\mathrm{DS}}}{R_n}$

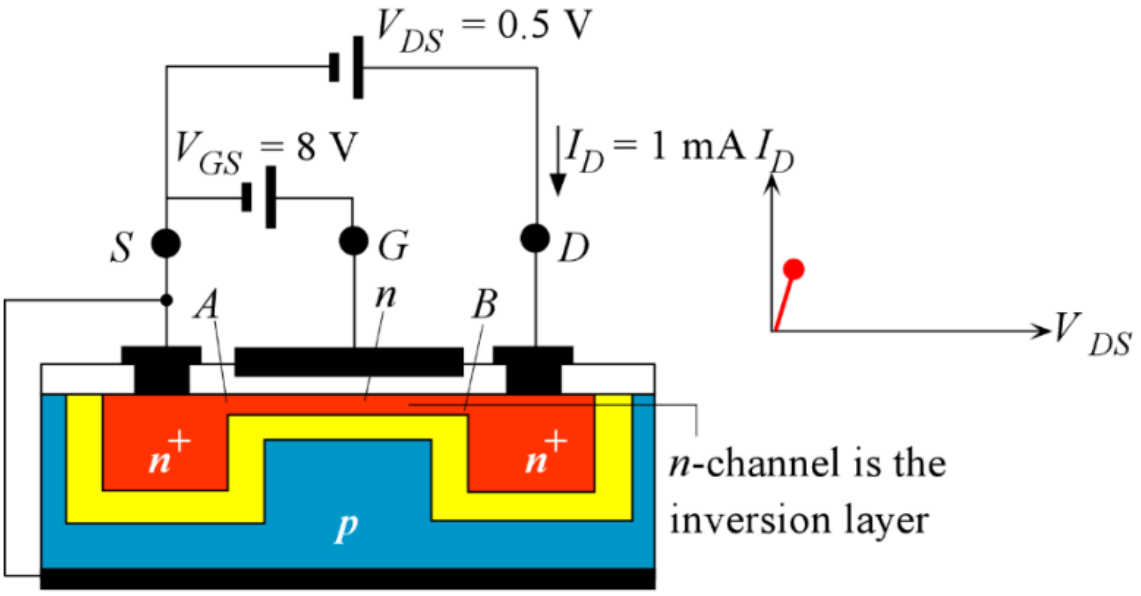


Figure 20: $V_{\mathrm{GS}} > V_t$

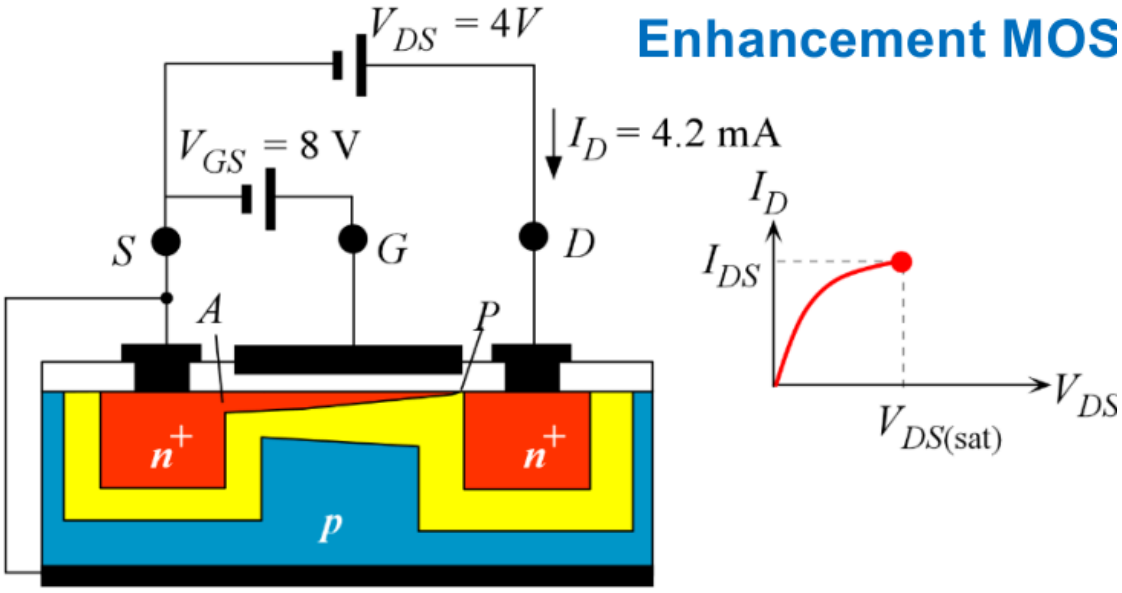


Figure 21: 增加V_{DS},沟道又会出现缩小直到饱和的效应

饱和条件:$V_{\mathrm{DS}} \geq V_{\mathrm{GS}} - V_{\mathrm{th}}$

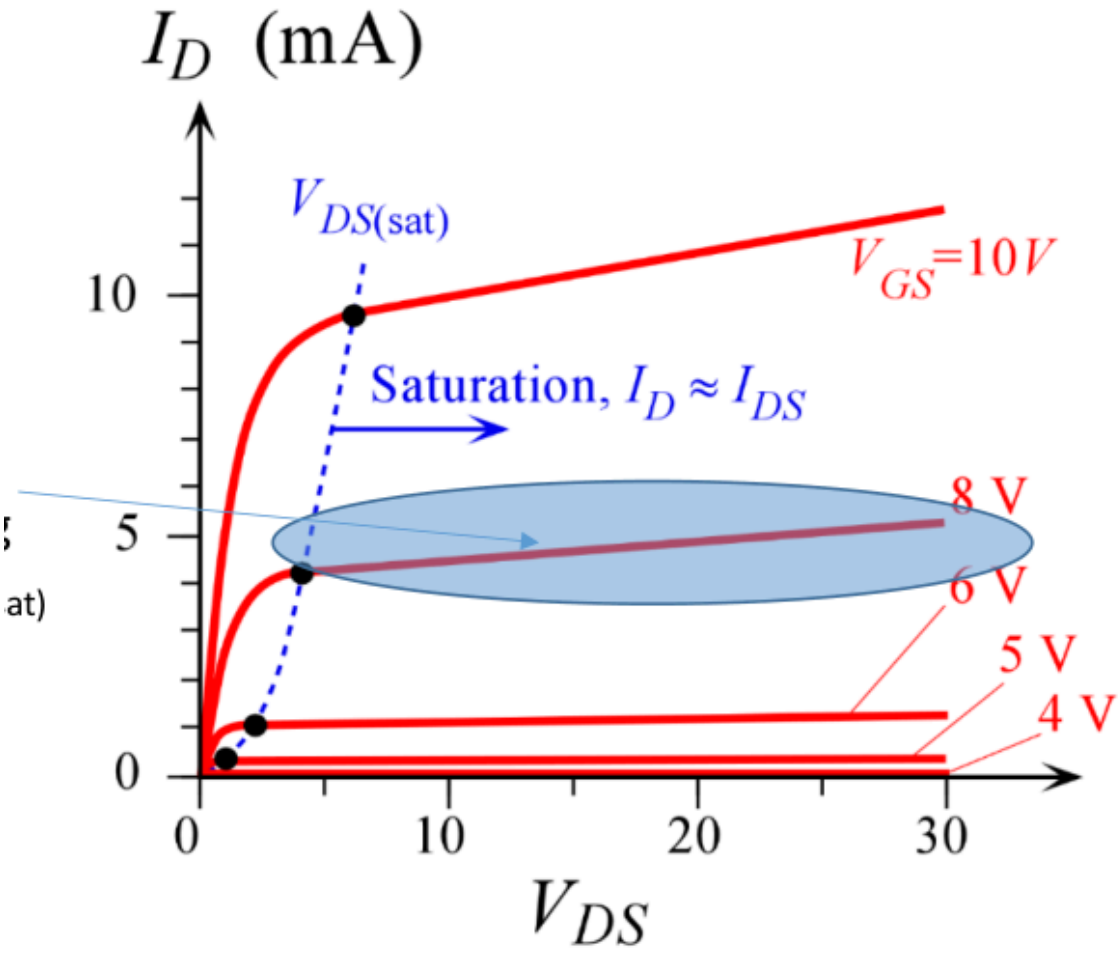


Figure 22: 饱和区电流主要由V_{GS}决定

传输公式

线性区($V_{\mathrm{GS}} > V_{\mathrm{th}}$,$V_{\mathrm{DS}} < V_{\mathrm{GS}} - V_t$)

$$I_D = k'(V_{\mathrm{GS}} - V_{\mathrm{th}})V_{\mathrm{DS}} - \frac{1}{2}k'V_{\mathrm{DS}}^2 \tag{14}$$

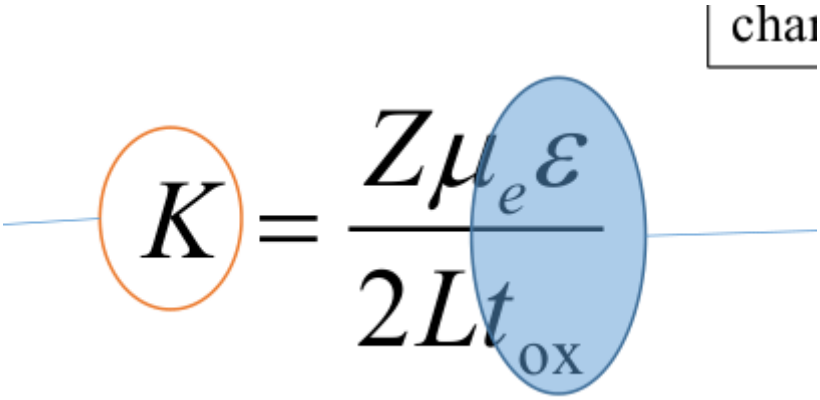


Figure 23: $k' = \frac{1}{2}k$. Z 是 MOSFET 的宽度,L 是沟道长度,μ_e是电子迁移率,$\frac{\varepsilon}{t_{ox}}$是氧化层电容

饱和区

$$I_D = \frac{1}{2}k'(V_{GS} - V_{th})(1 + \lambda V_{DS}) \quad 15$$

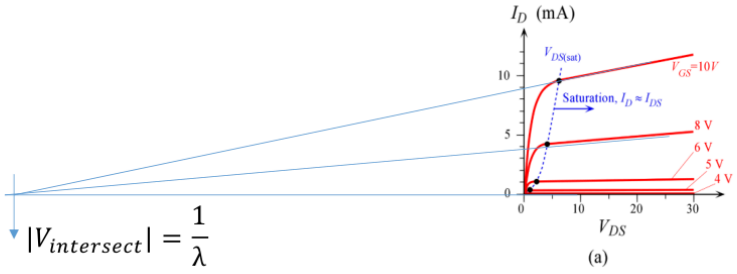
PMOS

- 线性区:$V_{SG} > |V_{th}|, V_{SD} < V_{SG} - |V_{th}|$,$I_D = k'\left[(V_{SG} - |V_{th}|V_{SD}) - \frac{1}{2}V_{SD}^2\right]$
- 饱和区:$I_D = \frac{1}{2}k'(V_{SG} - |V_{th}|)^2$

Enhancement MOSFET in SATURATION REGION

$$I_{DS} = K(V_{GS} - V_{th})^2(1 + \lambda V_{DS})$$

Where λ is the channel-length modulation parameter, which is a constant that is typically 0.01 V^{-1}. It can be determined by extending I_D vs V_{DS} lines and finding the intersect at - V_{DS}



$$V_{ov} = V_{GS} - V_{th}(\text{override voltage}) \quad 16$$

$$g_m = k' V_{\text{ov}} = 2\frac{I_D}{V_{\text{ov}}} \tag{17}$$

真空介电常数:$\varepsilon_0 = 8.85 \times 10^{-12} F/m$

Depletion MOSFET(一种和增强型 MOSFET 不一样的设备)

$V_{\text{GS}} = 0$的时候,就已经形成了沟道, 不需要大于V_t,

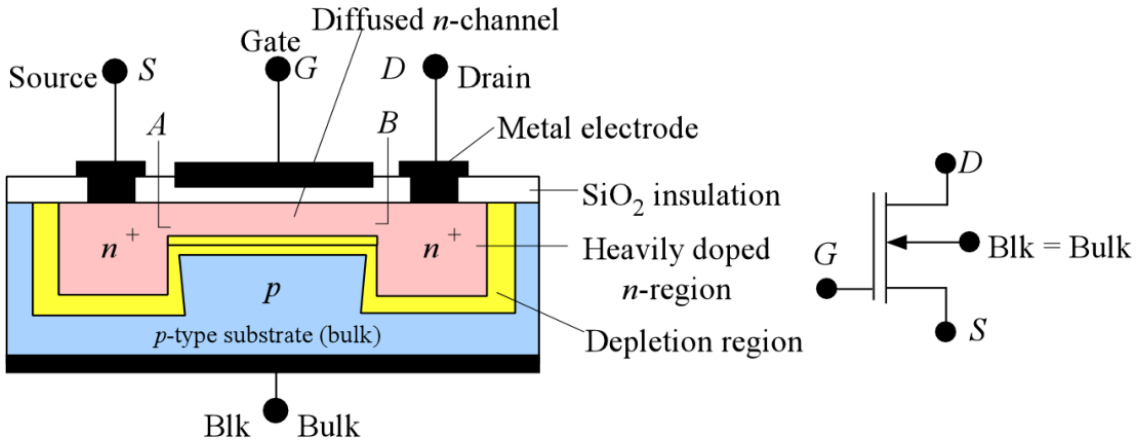


Figure 24: 耗尽型 MOSFET

它有两种模式

- 耗尽模式 $V_{\text{GS}} < 0$, 只需要更小的V_{DS}就可以达到饱和
- 增强模式 $V_{\text{GS}} > 0$, 需要更大的V_{DS}才能达到饱和

MOSFET 反向器

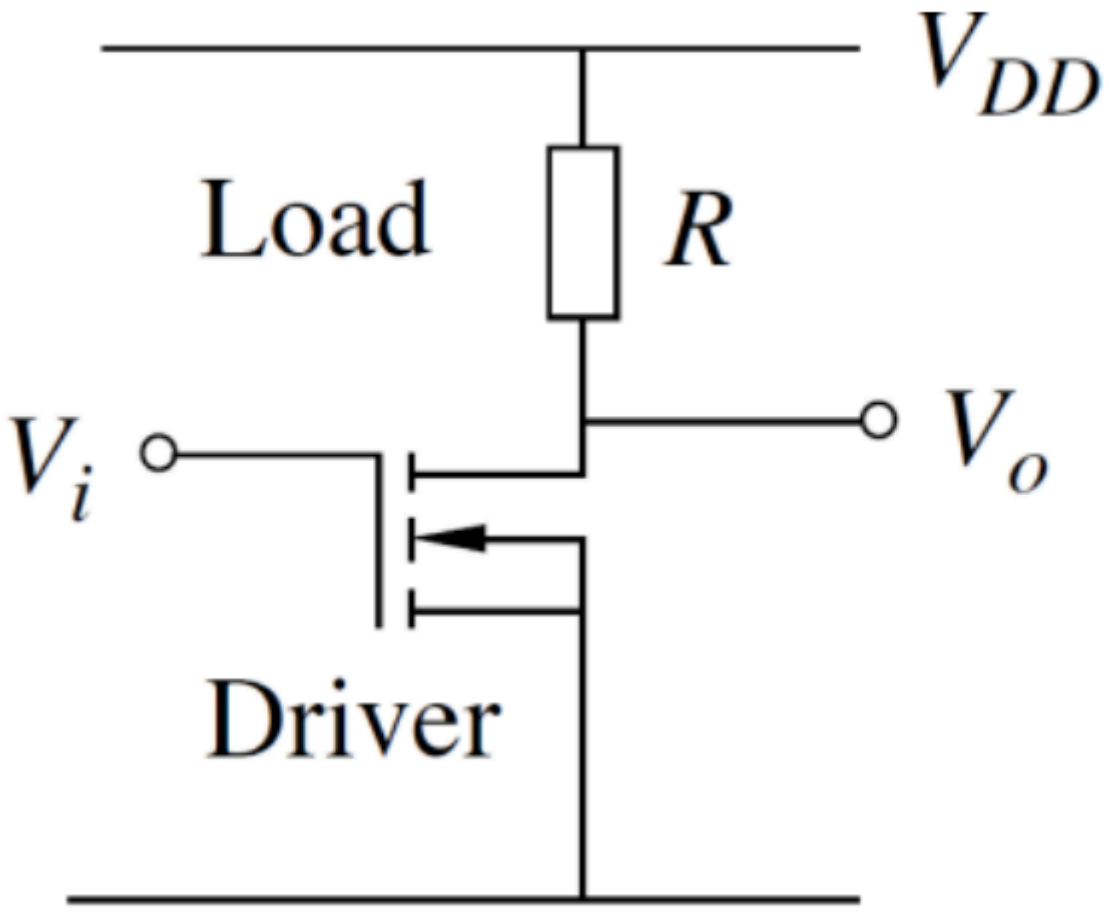


Figure 25: 简单 MOSFET 反向器

, 再输出为低电平的时候有直流电流,所以这种门耗能大

COMS(Complementary MOS, 互补 MOS)

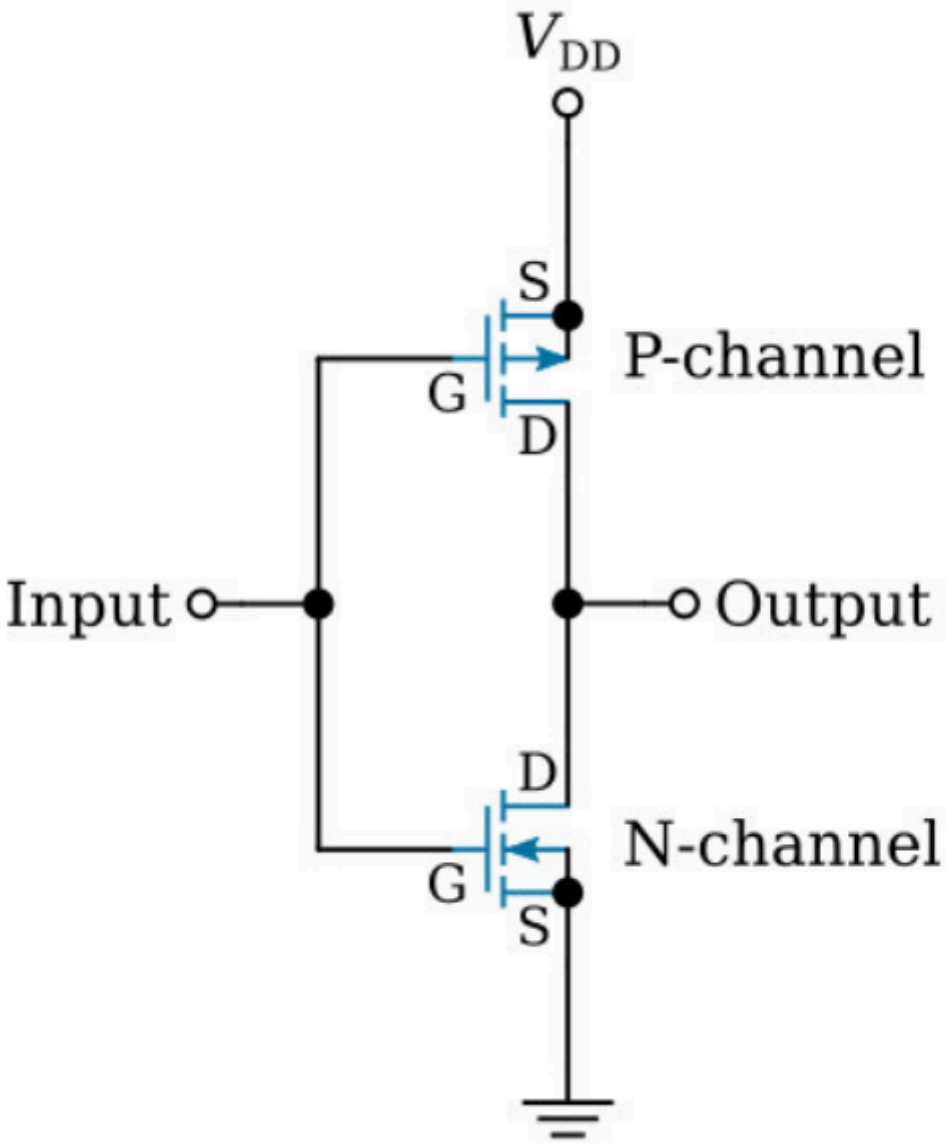


Figure 26: CMOS 的反向器的结构,没有什么电流通过

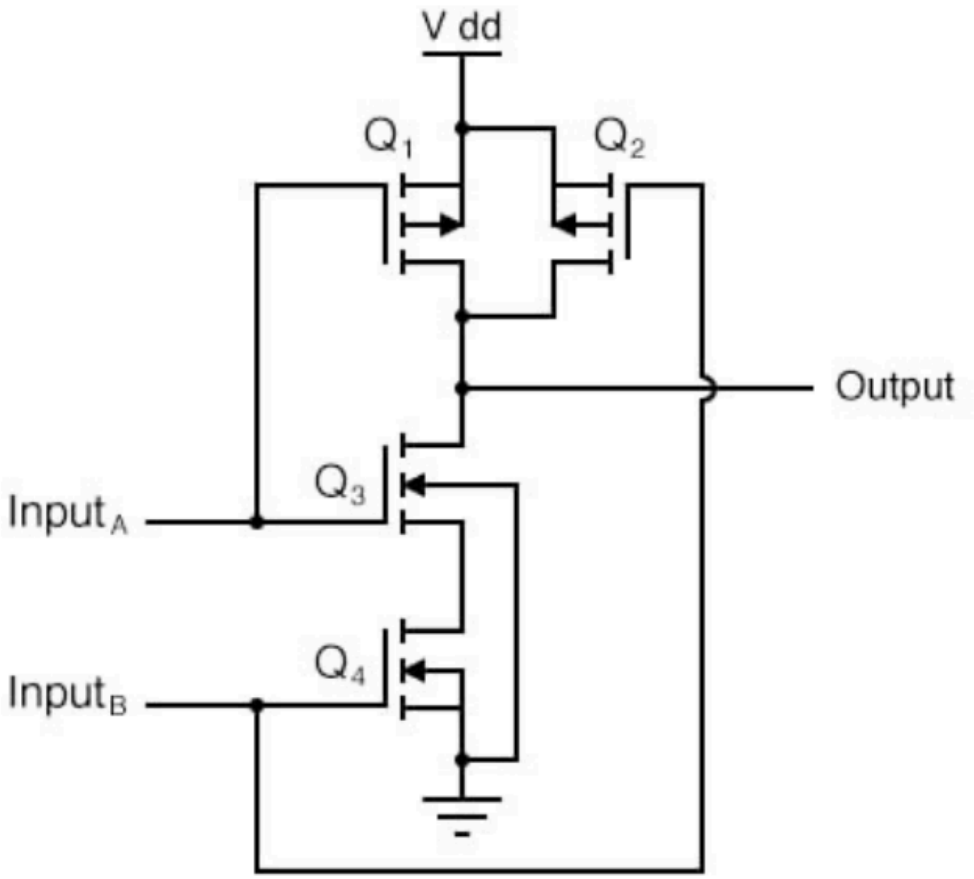


Figure 27: CMOS NAND 门

Appendix

****Given Data:****

- Gate width: $Z = 150\,\mu m = 150 \times 10^{-6} \,m$
- Channel length: $L = 10\,\mu m = 10 \times 10^{-6} \,m$
- Oxide thickness: $t_{ox} = 500\,\text{Å} = 500 \times 10^{-10} \,m = 5 \times 10^{-8}\,m$
- Electron mobility: $\mu_e = 700\,\text{cm}^2/\text{V·s} = 700 \times 10^{-4} \,m^2/\text{V·s} = 0.07\,m^2/\text{V·s}$
- Threshold voltage: $V_{th} = 2\,V$
- Gate-source voltage: $V_{GS} = 5\,V$
- Drain-source voltage: $V_{DS} = 5\,V$
- Channel-length modulation parameter: $\lambda = 0.01$

The relative permittivity of SiO_2: $\varepsilon_r = 3.9$

Permittivity of free space: $\varepsilon_0 = 8.85 \times 10^{-12}\,F/m$

Step-by-step Solution:

(a) Calculate the drain current I_D

1. Compute the oxide capacitance per unit area C_{ox}:

$$
C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}, \quad \text{where } \varepsilon_{ox} = \varepsilon_0 \varepsilon_r.
$$

$$
\varepsilon_{ox} = 8.85 \times 10^{-12} \times 3.9 = 3.4515 \times 10^{-11}\,F/m.
$$

$$
C_{ox} = \frac{3.4515 \times 10^{-11}}{5 \times 10^{-8}} = \frac{3.4515 \times 10^{-11}}{5 \times 10^{-8}} = 6.9 \times 10^{-4} \,F/m^2.
$$

2. Aspect ratio Z/L:

$$
\frac{Z}{L} = \frac{150 \times 10^{-6}}{10 \times 10^{-6}} = 15.
$$

3. Overdrive voltage $V_{OV} = V_{GS} - V_{th}$:

$$
V_{OV} = 5\,V - 2\,V = 3\,V.
$$

4. MOSFET saturation current without channel-length modulation:

In saturation (assuming $ V_{DS} > V_{OV} $, which is true since 5 V > 3 V):

$$
```
```

$$
I_{D0} = \frac{1}{2}\mu_e C_{ox} \frac{Z}{L} (V_{OV})^2.
$$

Plugging in numbers:
$$
I_{D0} = \frac{1}{2}(0.07)(6.9 \times 10^{-4})(15)(3^2).
$$

First, calculate the product $\mu_e C_{ox} \frac{Z}{L}$:
$$
\mu_e C_{ox} \frac{Z}{L} = 0.07 \times 6.9 \times 10^{-4} \times 15.
$$

$$
6.9 \times 10^{-4} \times 15 = 1.035 \times 10^{-2}.
$$

$$
0.07 \times 1.035 \times 10^{-2} = 7.245 \times 10^{-4}.
$$

Now multiply by $(V_{OV})^2 = 9$:
$$
7.245 \times 10^{-4} \times 9 = 6.5205 \times 10^{-3}.
$$

Then multiply by $1/2$:
$$
I_{D0} = \frac{6.5205 \times 10^{-3}}{2} = 3.26025 \times 10^{-3} A = 3.26\,mA.
$$

5. Include channel-length modulation:
The current with channel-length modulation:
$$
I_D = I_{D0}(1 + \lambda V_{DS}) = 3.26025 \times 10^{-3}(1 + 0.01 \times 5).
$$

$$
\[

$$
1 + 0.01 \times 5 = 1 + 0.05 = 1.05.
$$

$$
I_D = 3.26025 \times 10^{-3} \times 1.05 \approx 3.423 \times 10^{-3} A = 3.42\,mA.
$$

Answer for (a):
$$
I_D \approx 3.42\,mA.
$$

(b) Small-signal voltage gain with a 2.2 kΩ load

When the NMOS is used as a common-source amplifier with a resistor R_D in the drain, the small-signal voltage gain is approximately:
$$
A_v \approx -g_m R_D.
$$

1. Compute g_m:
For a MOSFET in saturation,
$$
g_m = \frac{2 I_D}{V_{OV}}.
$$

We have $I_D = 3.42\,mA$ and $V_{OV} = 3\,V$:
$$
g_m = \frac{2 \times 3.42 \times 10^{-3}}{3} = \frac{6.84 \times 10^{-3}}{3} = 2.28 \times 10^{-3}\,S = 2.28\,mS.
$$

2. Voltage gain:
$$
A_v = -g_m R_D = -(2.28 \times 10^{-3})(2200) = -5.016 \approx -5.
$$

So the small-signal voltage gain is about -5.

Determining V_{DD}:
We know at the operating point $V_{DS} = 5\,V$. The drain current is $3.42\,mA$, and the drain resistor is $2.2\,k\Omega$.

$$
I_D R_D = 3.42 \times 10^{-3} A \times 2200\,\Omega = 7.524\,V \approx 7.53\,V.
$$

The drain voltage at Q-point is:
$$
V_D = V_{DS} + V_S = 5\,V + 0\,V = 5\,V.
$$

Since $V_D = V_{DD} - I_D R_D$:
$$
5\,V = V_{DD} - 7.53\,V \implies V_{DD} = 12.53\,V.
$$

If the drain supply V_{DD} is smaller than 12.5 V, the transistor cannot maintain $V_{DS}=5\,V$ at the chosen operating point. The transistor might move out of saturation or the Q-point will shift, resulting in a lower gain or a distorted output swing.

Answer for (b):
Small-signal gain ≈ -5.
To achieve $V_{DS}=5\,V$ at the given bias current and resistor, $V_{DD}\approx 12.5\,V.$
If the drain supply is smaller, the transistor may leave saturation and the gain would drop.

(c) Maximum input signal swings

We have a quiescent point at $V_D = 5\,V$ and $V_{DD} =$

12.5\,V\). The MOSFET remains in saturation as long as:
\[
V_{DS} \ge V_{OV} = 3\,V.
\]

The drain quiescent voltage is 5 V. The minimum drain voltage to stay in saturation is 3 V. Thus, the output can swing down from 5 V to about 3 V, a 2 V downward swing.

On the positive side, the drain can go up toward \(V_{DD}\). The maximum upwards swing is from 5 V to about 12.5 V, which is ~7.5 V. Thus, the negative swing is the limiting factor for symmetrical linear operation.

Since the voltage gain is about -5, a 2 V output swing corresponds to about 0.4 V input swing (because \(\Delta v_{out} = A_v \Delta v_{in} \implies \Delta v_{in} = \Delta v_{out}/|A_v| = 2/5 = 0.4\,V\)).

Answer for (c):
- Maximum negative input swing to stay in saturation is about ±0.4 V (around the Q-point) to avoid pushing the output below 3 V.
- On the positive side, there is more headroom, but the limiting factor is the lower saturation boundary. Thus, about ±0.4 V input signal can be cleanly amplified if a symmetrical swing is desired.

(d) Factors leading to higher voltage amplification

The voltage gain of a common-source stage is approximately:
\[
A_v \approx -g_m R_{load}.
\]

To increase the gain:
1. **Increase \(g_m\):**
   - Increase the bias current \(I_D\).
   - Increase the device transconductance by using a larger W/

L ratio.
   - Use a higher mobility transistor or reduce threshold to increase V_{OV} for given bias.

2. **Increase load resistance R_D:**
   - Use a larger resistor.
   - Replace the resistor with an active load (current mirror load), increasing the effective load impedance.

3. **Increase supply voltage V_{DD}:**
   - Allows for larger R_D while maintaining the transistor in saturation, thus increasing gain.

4. **Reduce channel-length modulation (λ):**
   - Using longer channel devices or cascoding increases the output impedance, effectively boosting gain.

Answer for (d):
Higher voltage amplification can be achieved by increasing transconductance (larger I_D, larger W/L, higher μ_e), increasing load resistance (or using active loads), increasing V_{DD} to allow higher load resistance while keeping the transistor in saturation, and reducing λ through device geometry or cascoding.

Final Answers:
- (a) $ I_D \approx 3.42\,mA $
- (b) Gain ≈ -5, $V_{DD} \approx 12.5\,V$. If V_{DD} is smaller, the transistor may leave saturation, reducing gain.
- (c) About ±0.4 V input swing for symmetrical undistorted output swing given the determined Q-point and gain.
- (d) Higher gain is achieved by increasing g_m, increasing R_D or using active loads, increasing V_{DD}, and reducing $\lambda.$

为什么基极很窄?

- 避免载流子被复合,提高从发射极到集电极的传输效率,增大电流增益