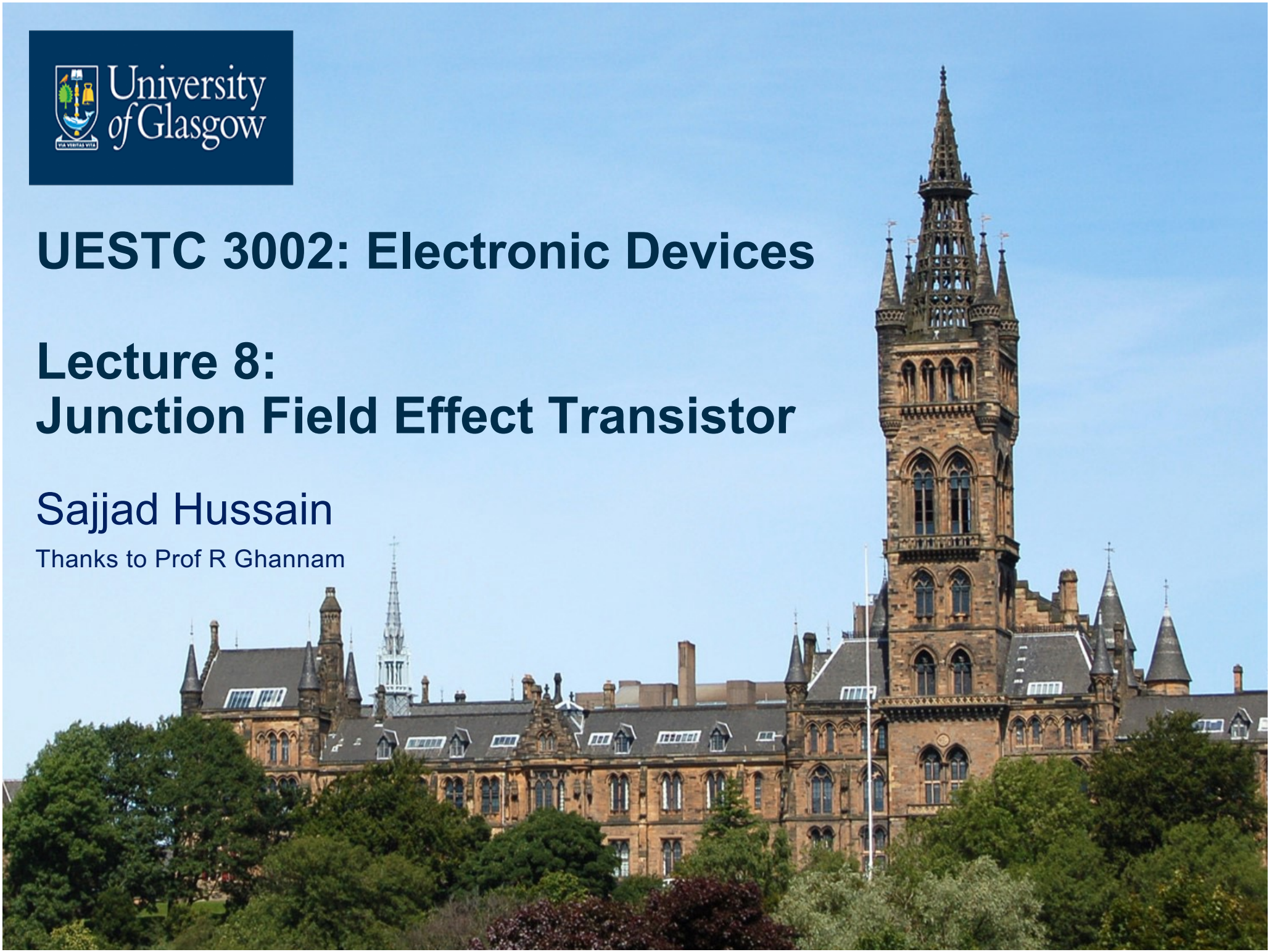


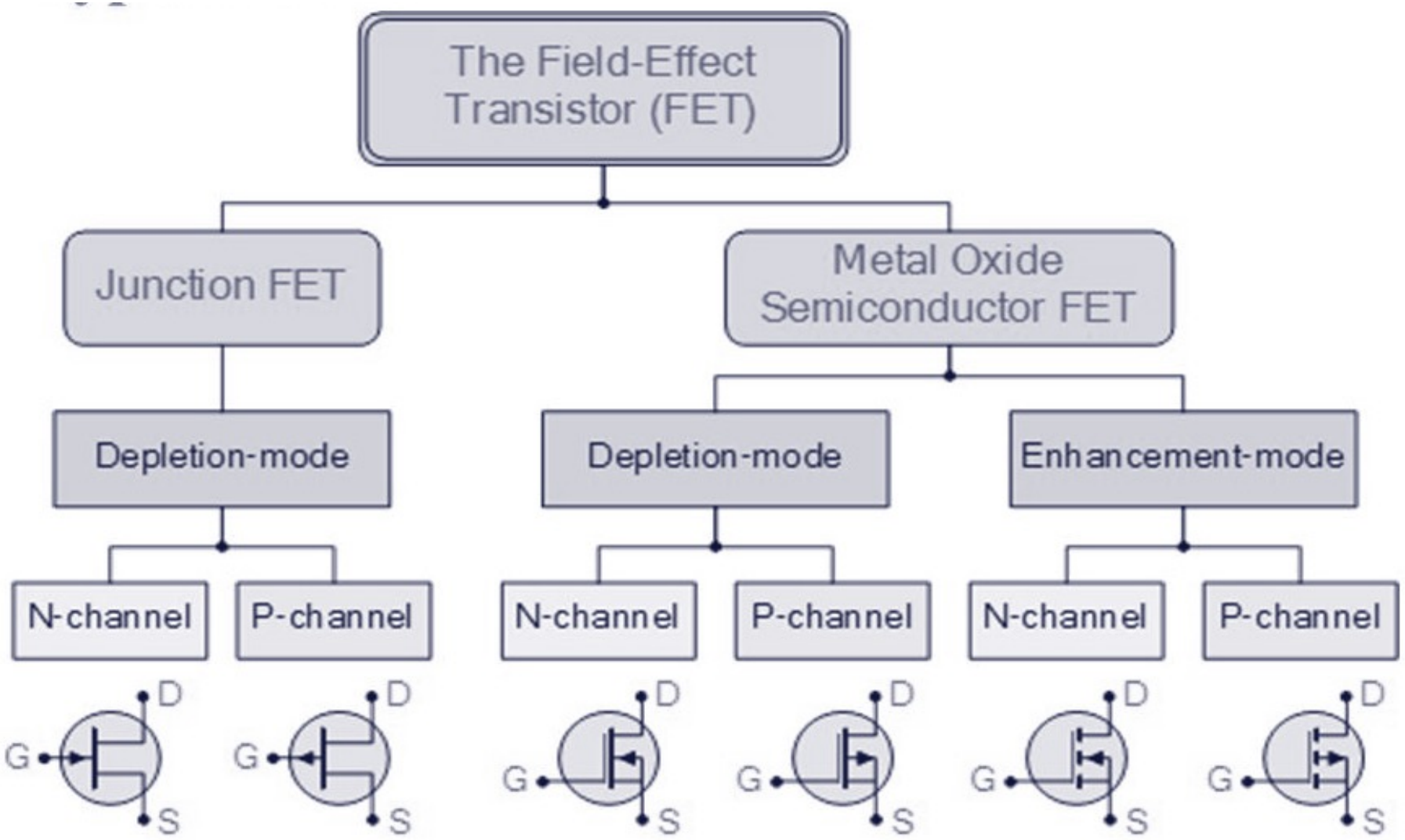
UESTC 3002: Electronic Devices

Lecture 8:
Junction Field Effect Transistor

Sajjad Hussain

Thanks to Prof R Ghannam

Types of Field Effect Transistors

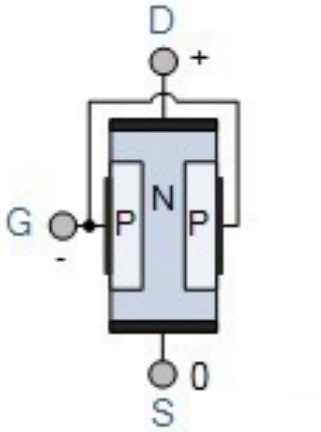


Junction Field Effect Transistor (JFET)

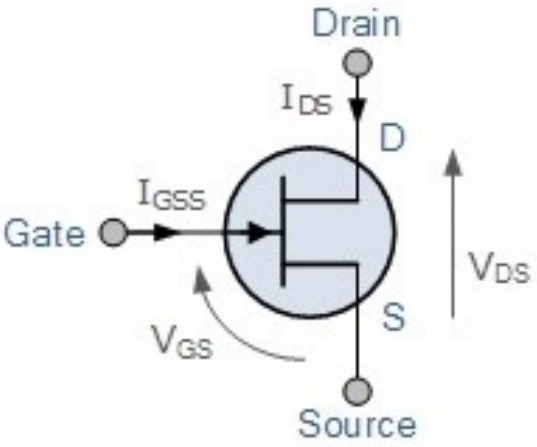
JFETs are three-terminal voltage-controlled semiconductor devices that can be used to control switches or amplifiers.

There are two JFET types:

- n-channel and p-channel.
- Similar in physical structure to a BJT.
  - It is also a 3-terminal device
  - There are two pn-junctions



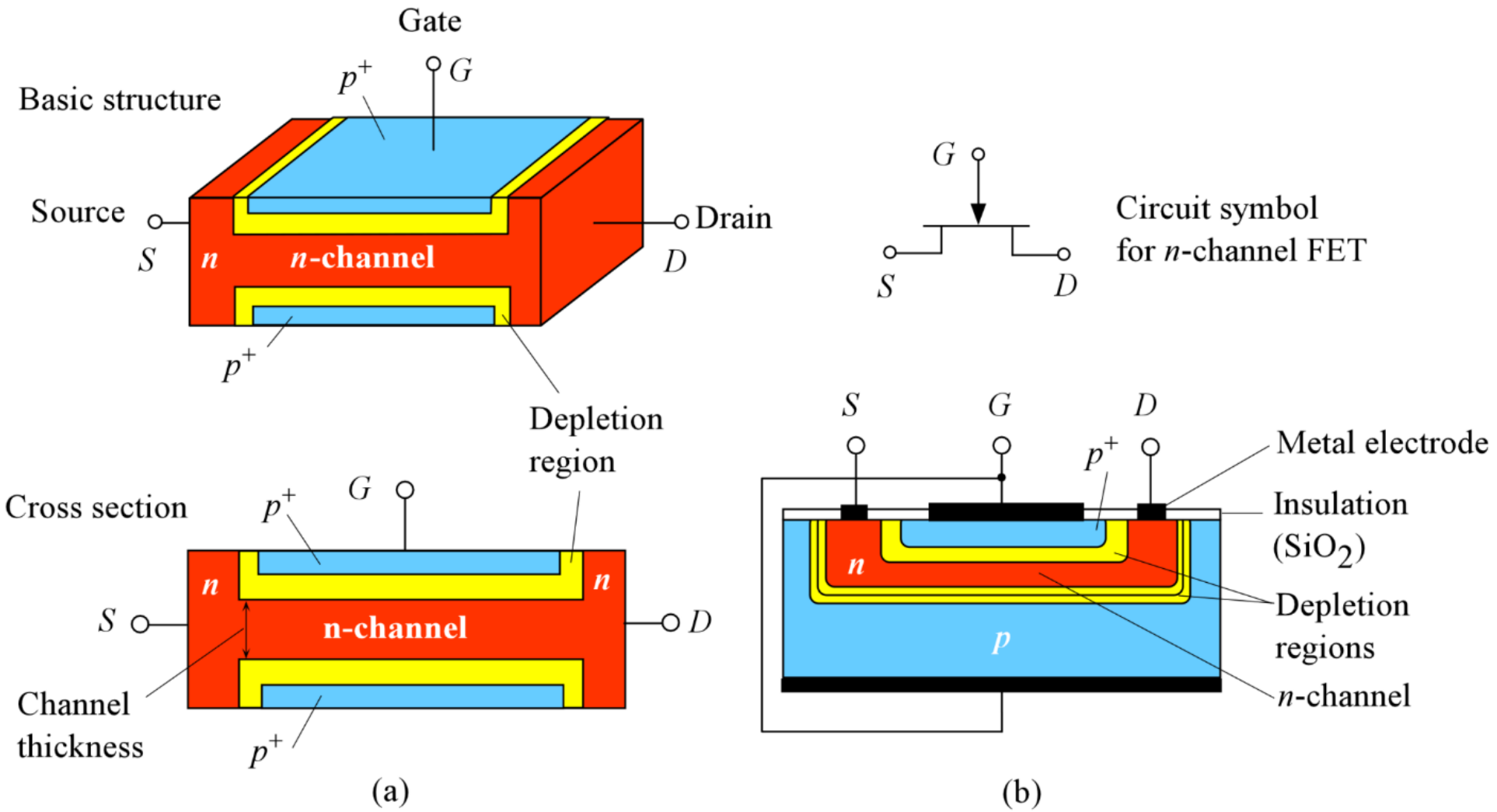
Construction



N-channel JFET

- However, JFET is a **Voltage Controlled Device**, as opposed to a Current Controlled Device in the case of the BJT.

Junction Field Effect Transistor (JFET)



(a) The basic structure of the junction field effect transistor (JFET) with an n-channel. The two p^+ regions are electrically connected and form the gate.

(b) A simplified sketch of the cross section of a more practical *n*-channel JFET

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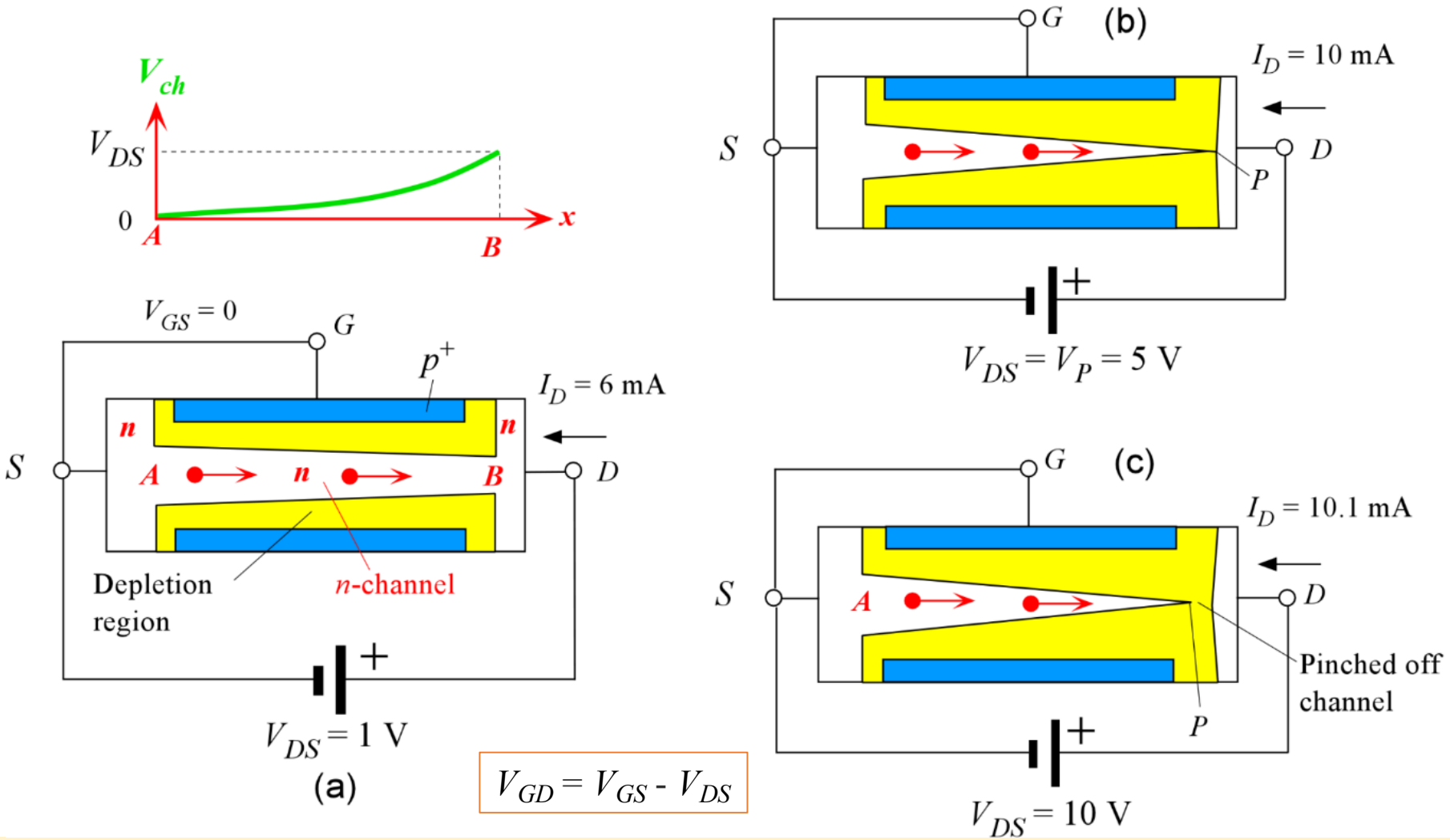
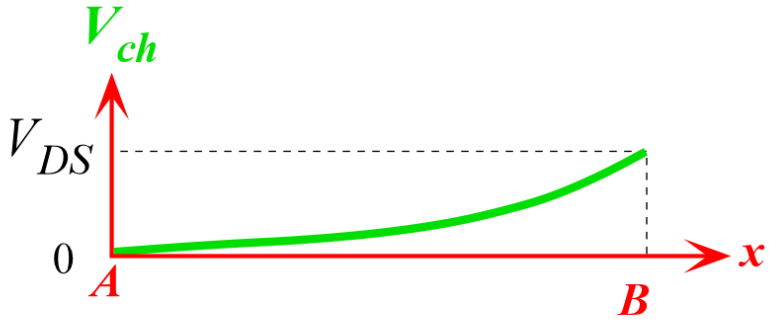
JFET Principles

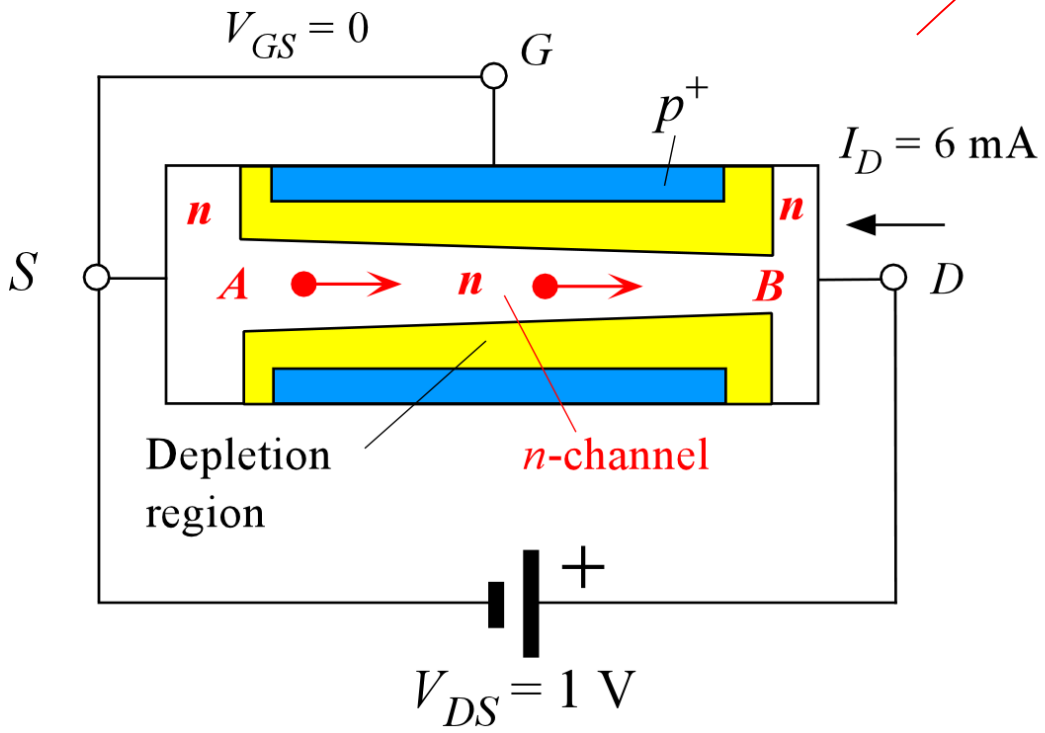


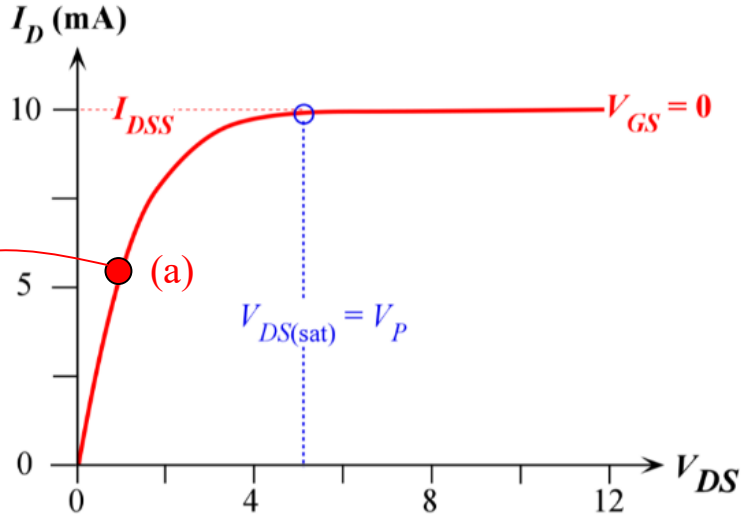
$V_{GD} = V_{GS} - V_{DS}$

(a) The gate and source are shorted ($V_{GS} = 0$) and V_{DS} is small,
(b) V_{DS} has increased to a value that allows the two depletion layers to just touch. This is called pinch-off voltage, $V_{DS} = V_P (= 5$ V). Since gate to source is short, $V_{GS} = 0$, $V_{GD} = -V_{DS} = -V_P = -5$ V.
(c) V_{DS} is large ($V_{DS} > V_P$) so that a short length of the channel is pinched off.

JFET Principles







The gate and source are shorted ($V_{GS} = 0$) and V_{DS} is small

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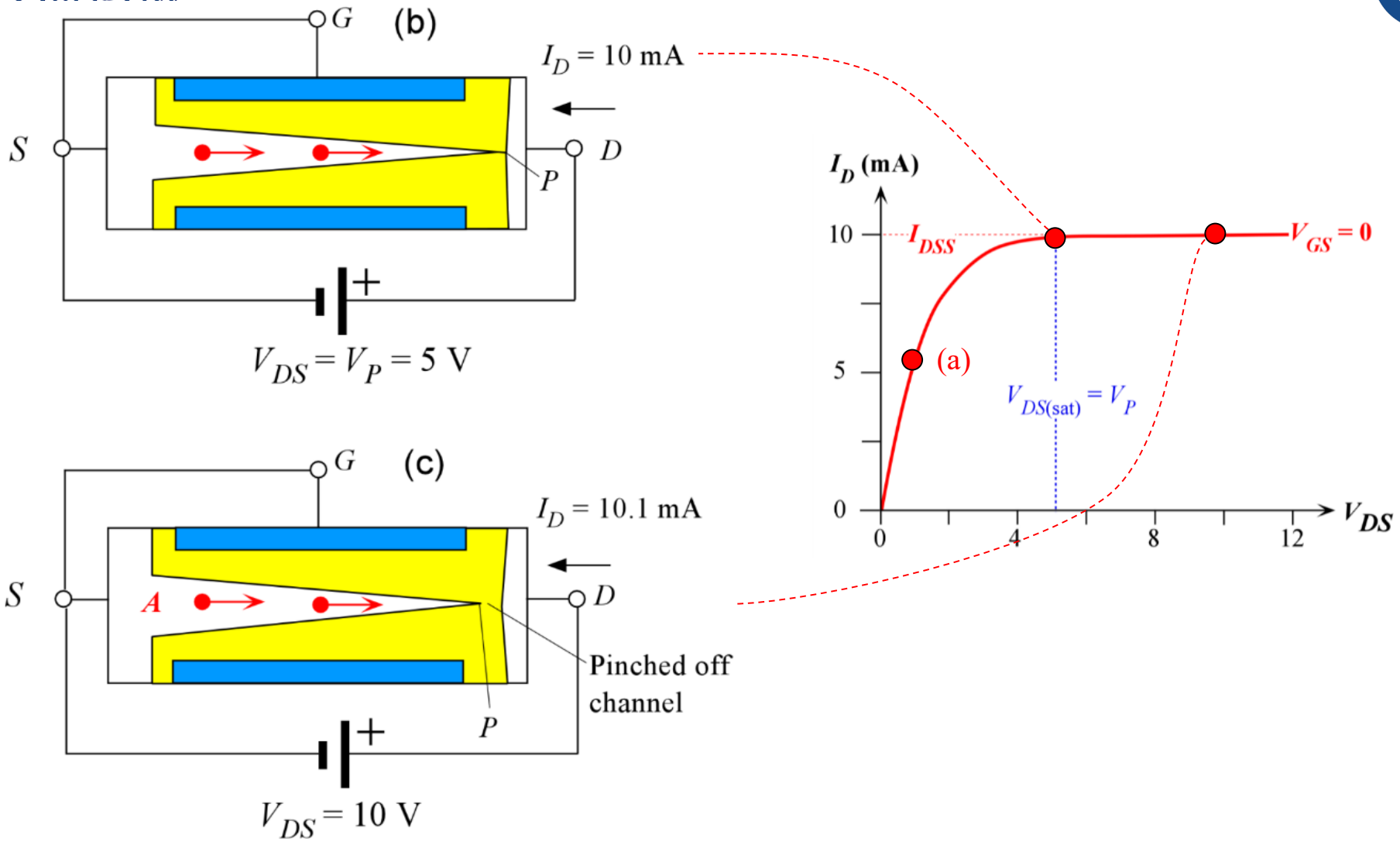
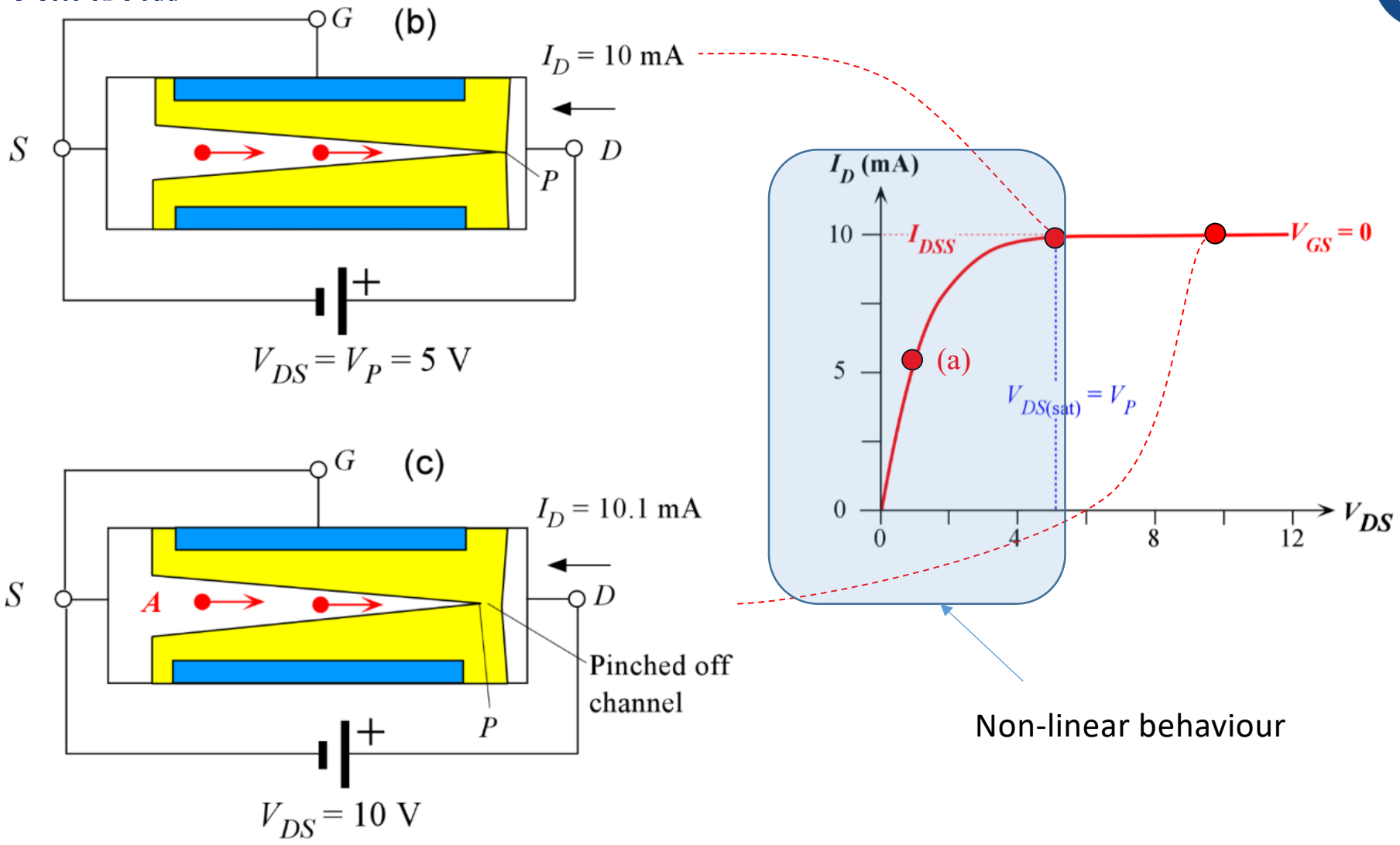
JFET Principles



(b) V_{DS} has increased to a value that allows the two depletion layers to just touch, when $V_{DS} = V_P (= 5\text{ V})$ when the p^+n junction voltage at the drain end, $V_{GD} = -V_{DS} = -V_P = -5$ V.
(c) V_{DS} is large ($V_{DS} > V_P$) so that a short length of the channel is pinched off.

JFET Principles



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(c) V_{DS} is large ($V_{DS} > V_P$) so that a short length of the channel is pinched off.

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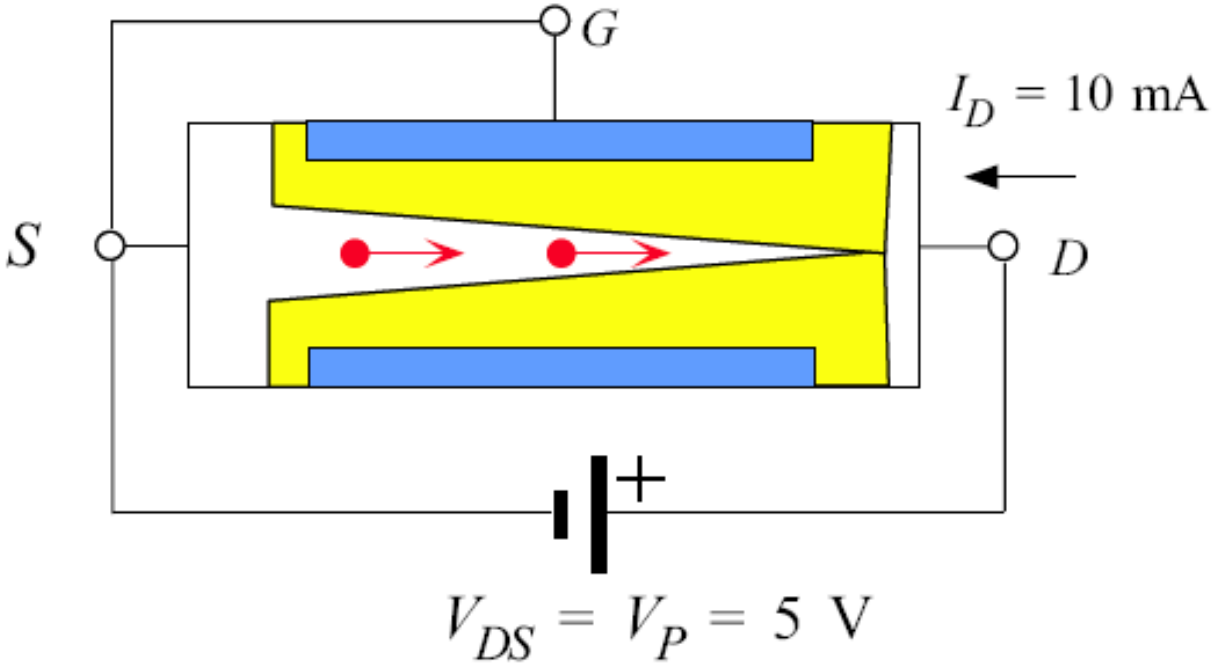
JFET Principles: Channel Pinch-off



Pinch-off Condition with $V_{GS} = 0$

$$V_{GD}(\text{pinch-off}) = -V_P$$

V_{DS} has increased to a value that allows the two depletion layers to just touch, when $V_{DS} = V_P (= 5\text{ V})$ when the p^+n junction voltage at the drain end, $V_{GD} = -V_{DS} = -V_P = -5$ V.

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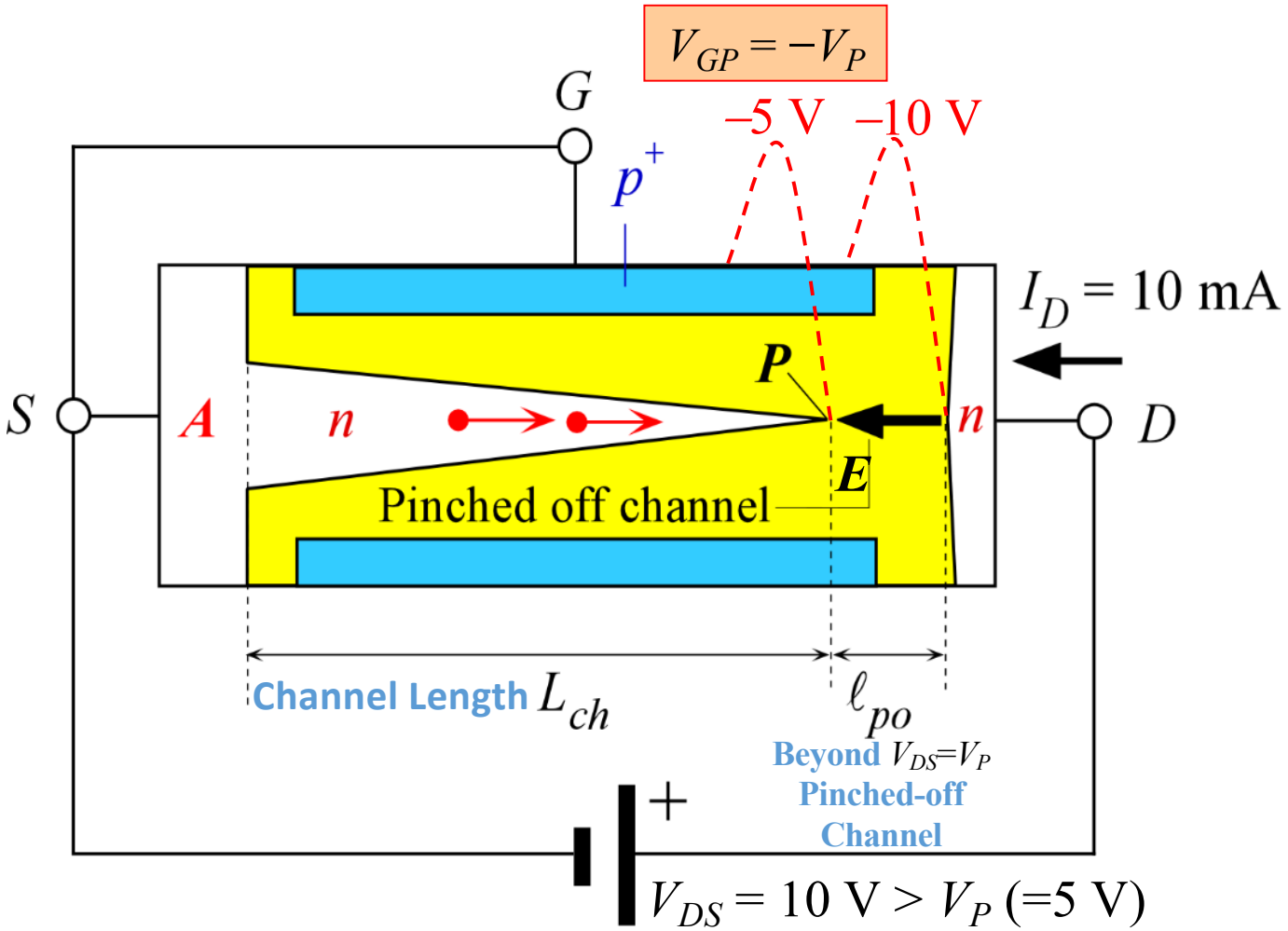
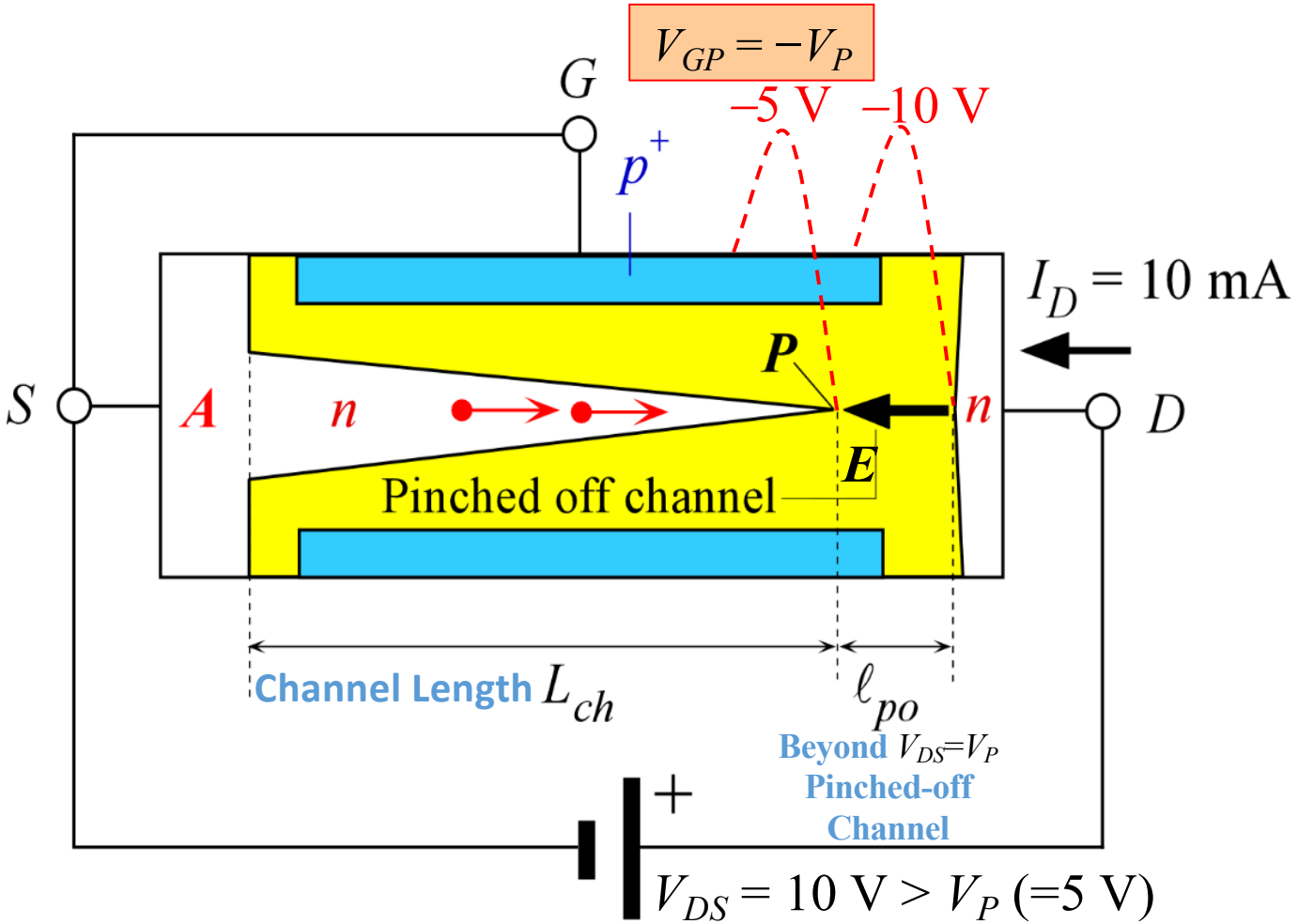
JFET Principles: Beyond Channel Pinch-off



Electrons in the n-channel drift toward P. When they arrive at P, they are swept across the pinched-off channel by E-field. This process is similar to minority carriers in the base of a BJT.

JFET Principles: Beyond Channel Pinch-off



Drain current, I_D, is actually determined by the resistance of the conducting n-channel over L_{ch} from A to P.

Thus $$I_D = \frac{V_P}{R_{AP}} \qquad (V_{DS} > V_P)$$

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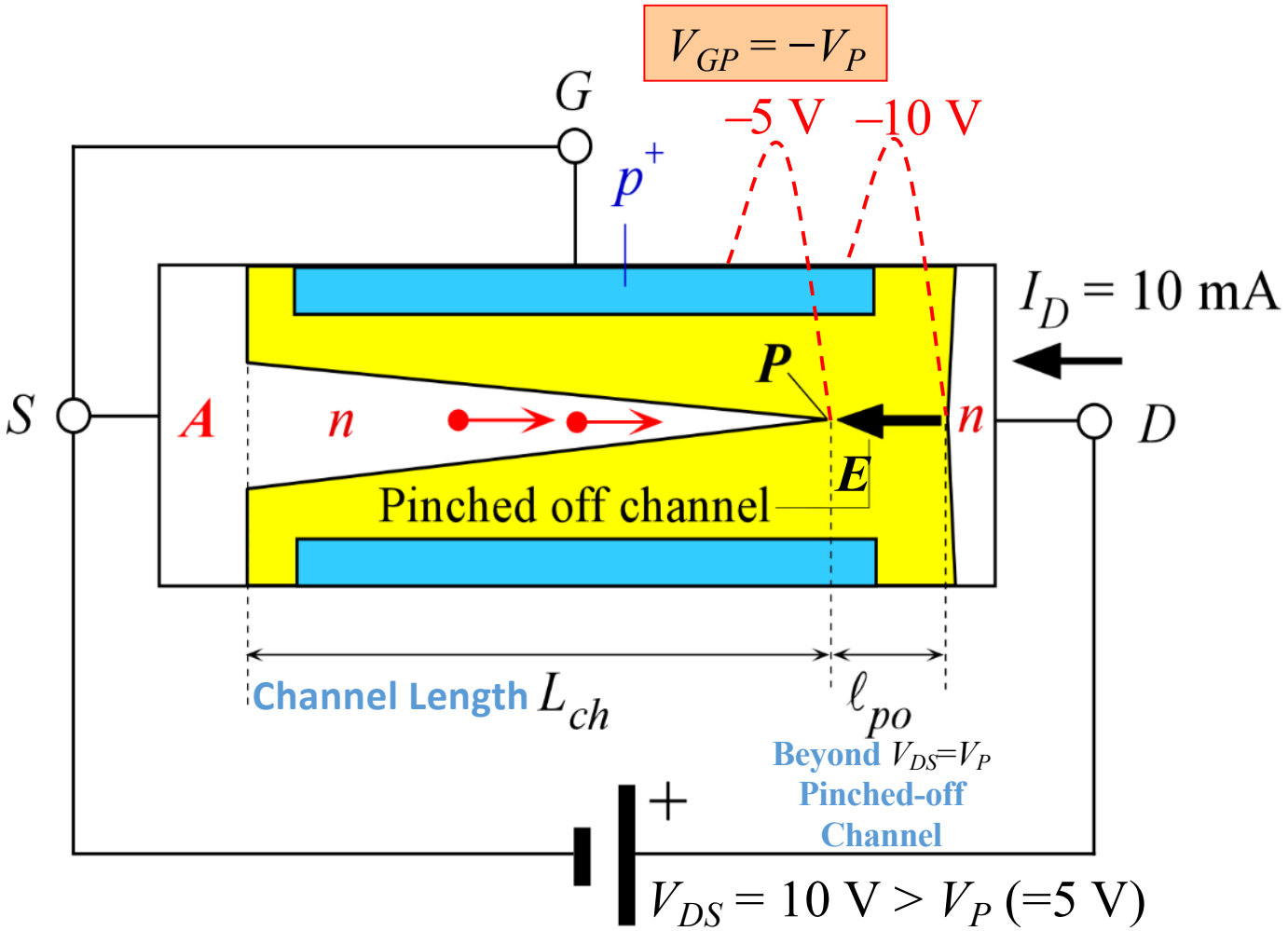
JFET Principles: Beyond Channel Pinch-off



As V_{DS} increases, most of the additional voltage simply drops across l_{po} as this region is depleted of carriers and hence highly resistive.

Junction Field Effect Transistor (JFET)

- We first considered the behavior of the JFET with the gate and source shorted ($V_{GS} = 0$). The resistance between S and D is the resistance of the conducting n-channel between A and B, R_{AB}.

- When a positive voltage is applied to D with respect to S ($V_{DS} > 0$), then a current flows from D to S which is called the drain current I_D.

- There is a voltage drop along the channel, between A and B. The voltage in the n-channel is zero at A and V_{DS} at B.

- As the voltage along the n-channel is positive, the pn junctions between the gates and the n-channel become progressively more reverse-biased from A to B. Consequently, the depletion layers extend more into the channel and thereby decrease the thickness of the conducting channel from A to B.

- Increasing V_{DS} increases the widths of the depletion layers, which penetrate more into the channel and hence result in more channel narrowing toward the drain.

- The resistance of the n-channel R_{AB} therefore increases with V_{DS}. The drain current therefore does not increase linearly with V_{DS}.

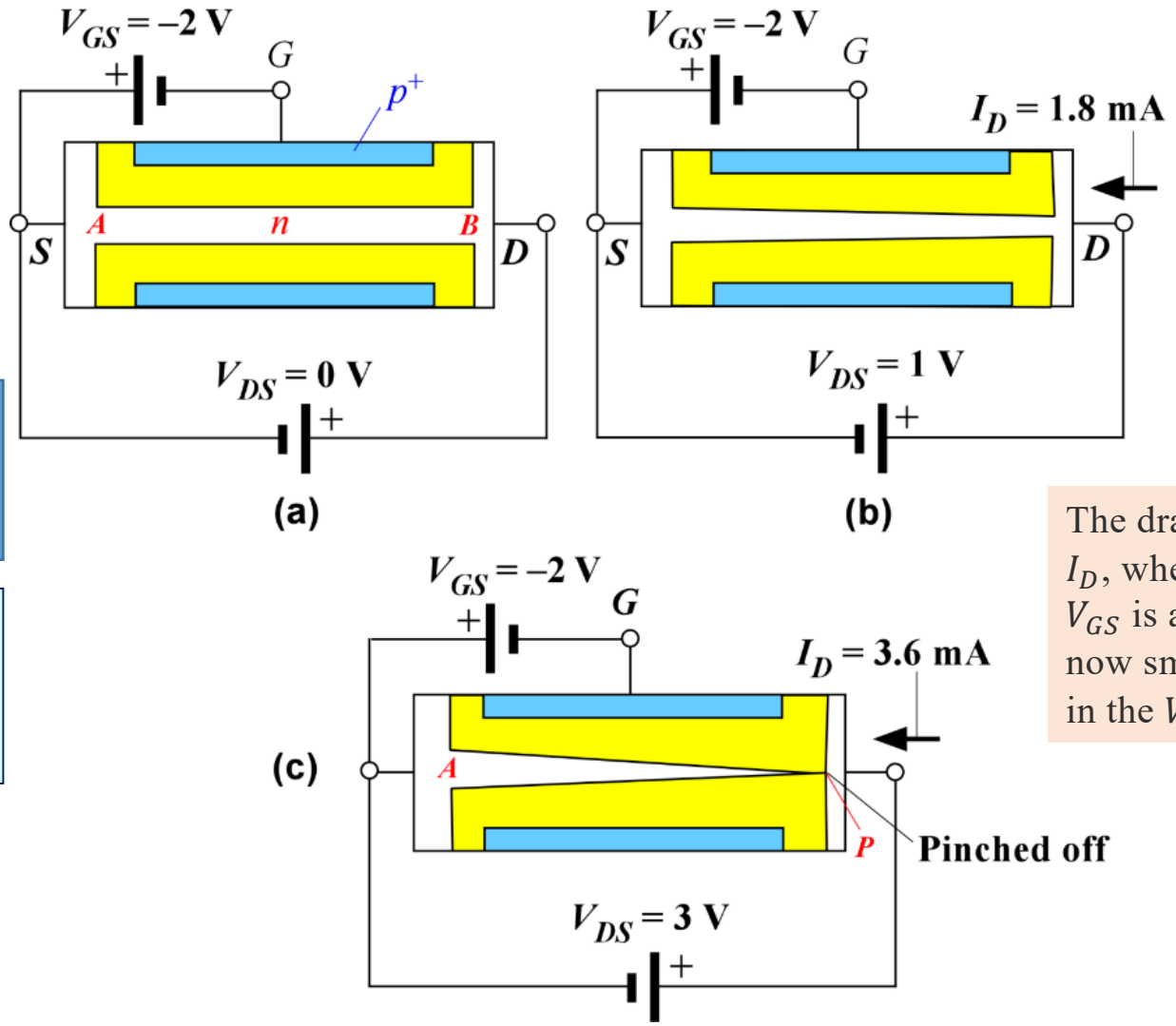
$$I_D = \frac{V_{DS}}{R_{AB}}$$

JFET Principles: Effect of V_{GS}

Note the thicker depletion region

$$V_{DS(sat)} = V_{GS} + V_p$$

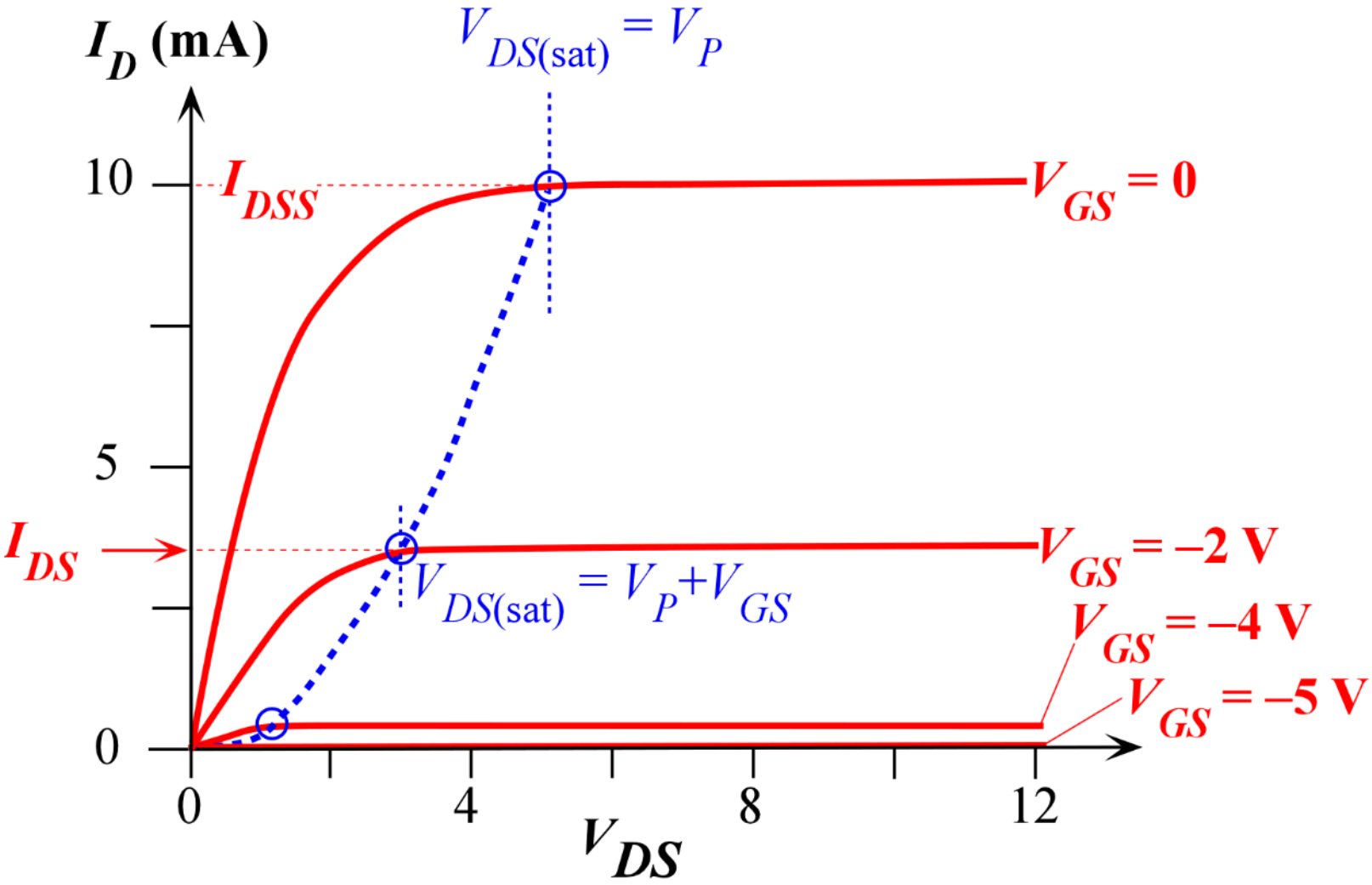
Thus, a smaller V_{DS} is needed to pinch off channel (say V_{DS}=3V)



The drain current, I_D, when a small V_{GS} is applied is now smaller than in the $V_{GS} = 0$ case.

(a) The JFET with a negative V_{GS} bias has a **narrower** n-channel at the start. (b) Compared to the $V_{GS} = 0$ case, the same V_{DS} gives less I_D as the channel is narrower. (c) A smaller voltage is required for pinch-off. The channel is pinched off at $V_{DS} = 3$V sooner than the $V_{GS} = 0$ case where it was $V_{DS} = 5$ V.

JFET Characteristics



Typical I_D vs. V_{DS} characteristics of a JFET for various fixed gate voltages V_{GS}.

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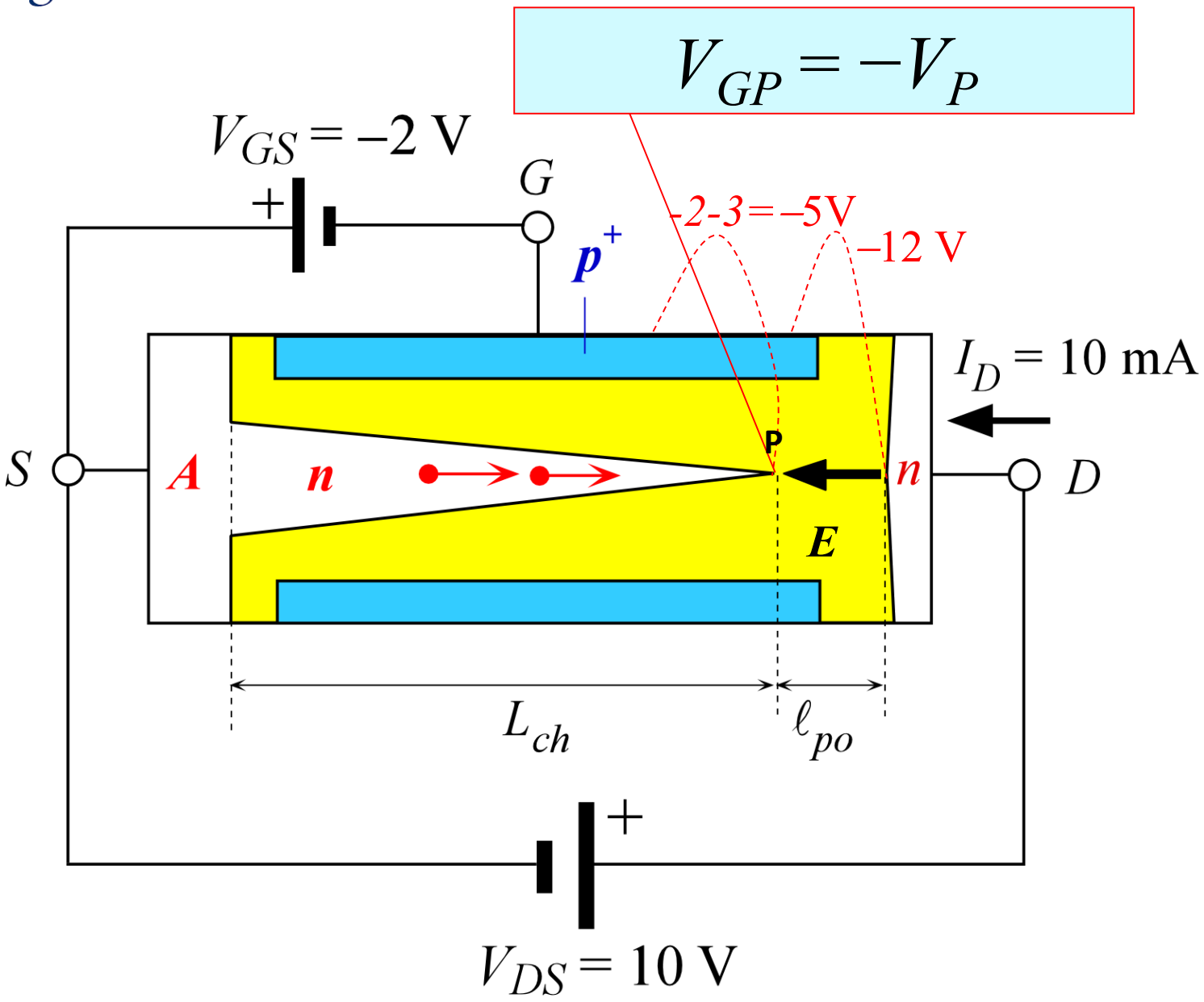
JFET Principles: Beyond Channel Pinch-off



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Junction Field Effect Transistor (JFET)

Pinch-off condition

$$V_{DS(\text{sat})} = V_P + V_{GS}$$

$$I_D \approx I_{DS} \approx \frac{V_{DS(sat)}}{R_{AP}(V_{GS})} = \frac{V_P + V_{GS}}{R_{AP}(V_{GS})}$$

where V_{GS} is a negative voltage (reducing $V_{DS\ (sat)}$) and R_{AP} is the effective resistance of the n-channel from A to P.

Beyond pinch-off when $V_{DS} > V_{DS(\text{sat})}$, the point P where the channel is just pinched still remains at potential V_P, thus V_{AP} remains at $V_{DS(\text{sat})}$, given by the above equation.

Junction Field Effect Transistor (JFET)

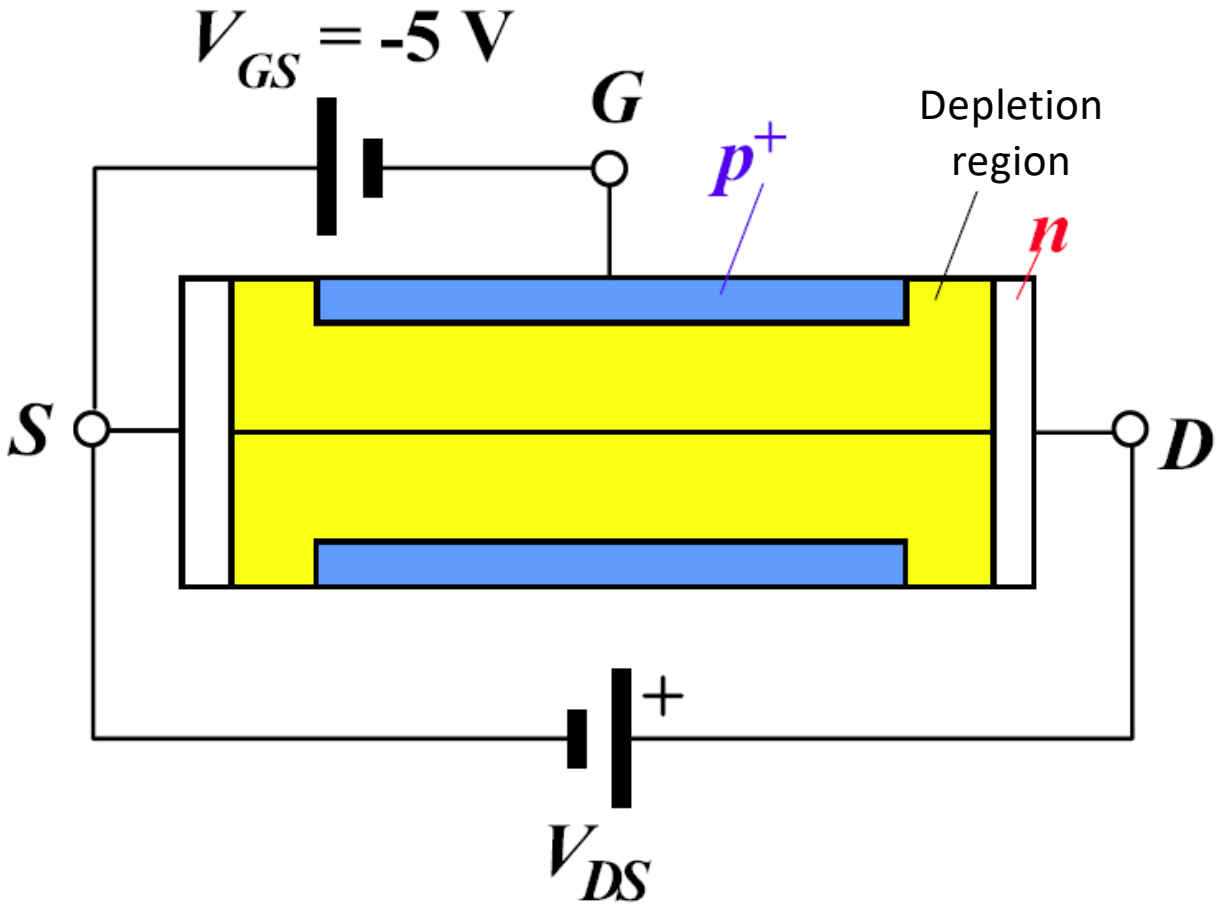
- The resistance increases with more negative gate voltage as this increases the reverse bias across the p^+n junction, which leads to the narrowing of the channel.
    - e.g. when V_{GS} = -4 V, the channel thickness at A becomes narrower than in the case with V_{GS} = -2 V, thereby increasing the resistance (R_{AP}) of the conducting channel and therefore decreasing I_{DS}.

- Further, there is a reduction in the drain current by virtue of $V_{DS(\text{sat})}$ decreasing with negative V_{GS}.

- These two effects (i.e. from $V_{DS(\text{sat})}$ and that from R_{AP}) lead to I_{DS} almost decreasing parabolically with $-V_{GS}$.

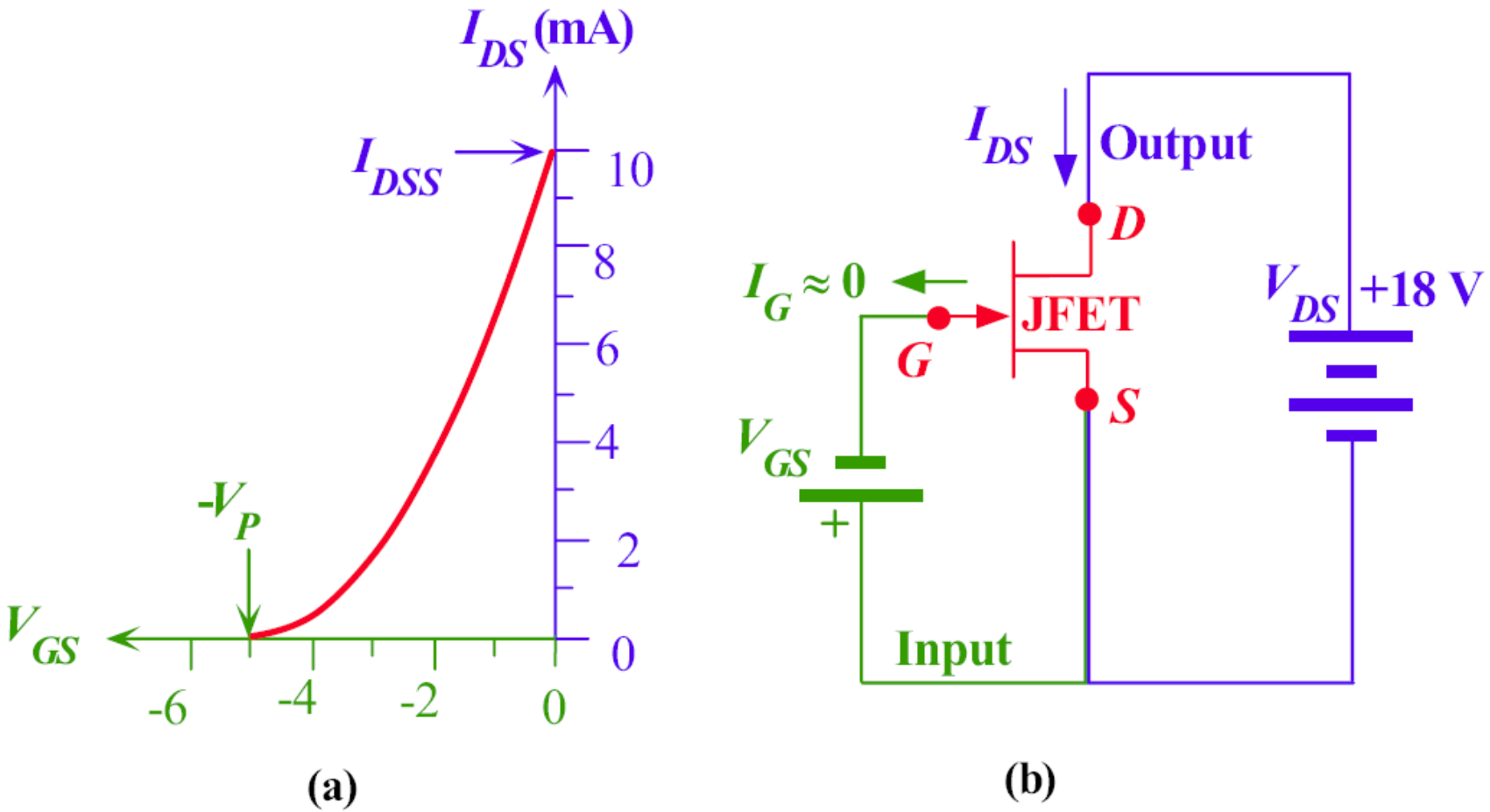
JFET with Turn-off V_{GS}

When the gate voltage is such that $V_{GS} = -V_p$ (= -5 V) with the source and drain shorted (V_{DS} = 0), then the two depletion layers touch over the entire channel length and the whole channel is closed. **The channel is said to be off.** The only drain current that flows when a V_{DS} is applied is due to the thermally generated carriers in the depletion layers. This current is very small.



When V_{GS} = – 5 V the depletion layers close the whole channel from the start, at V_{DS} = 0. As V_{DS} is increased there is a very small drain current which is the small reverse leakage current due to thermal generation of carriers in the depletion layers.

JFET Transfer Characteristics



(a) Typical I_{DS} versus V_{GS} characteristics of a JFET. (b) The dc circuit where V_{GS} in the gate–source circuit (input) controls the drain current I_{DS} in the drain–source (output) circuit in which V_{DS} is kept constant and large ($V_{DS} > V_P$).

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Junction Field Effect Transistor (JFET)

Beyond pinch-off

A simple way to express the relationship between I_{DS} and V_{GS} is:

$$I_{DS} = I_{DSS}\left[1 - \left(\frac{V_{GS}}{V_{GS(\text{off})}}\right)\right]^2$$

where,

I_{DSS} is the drain current when $V_{GS} = 0$

$V_{GS(\text{off})} = -V_p$; the gate-source voltage that just pinches off the channel

JFET SUMMARY

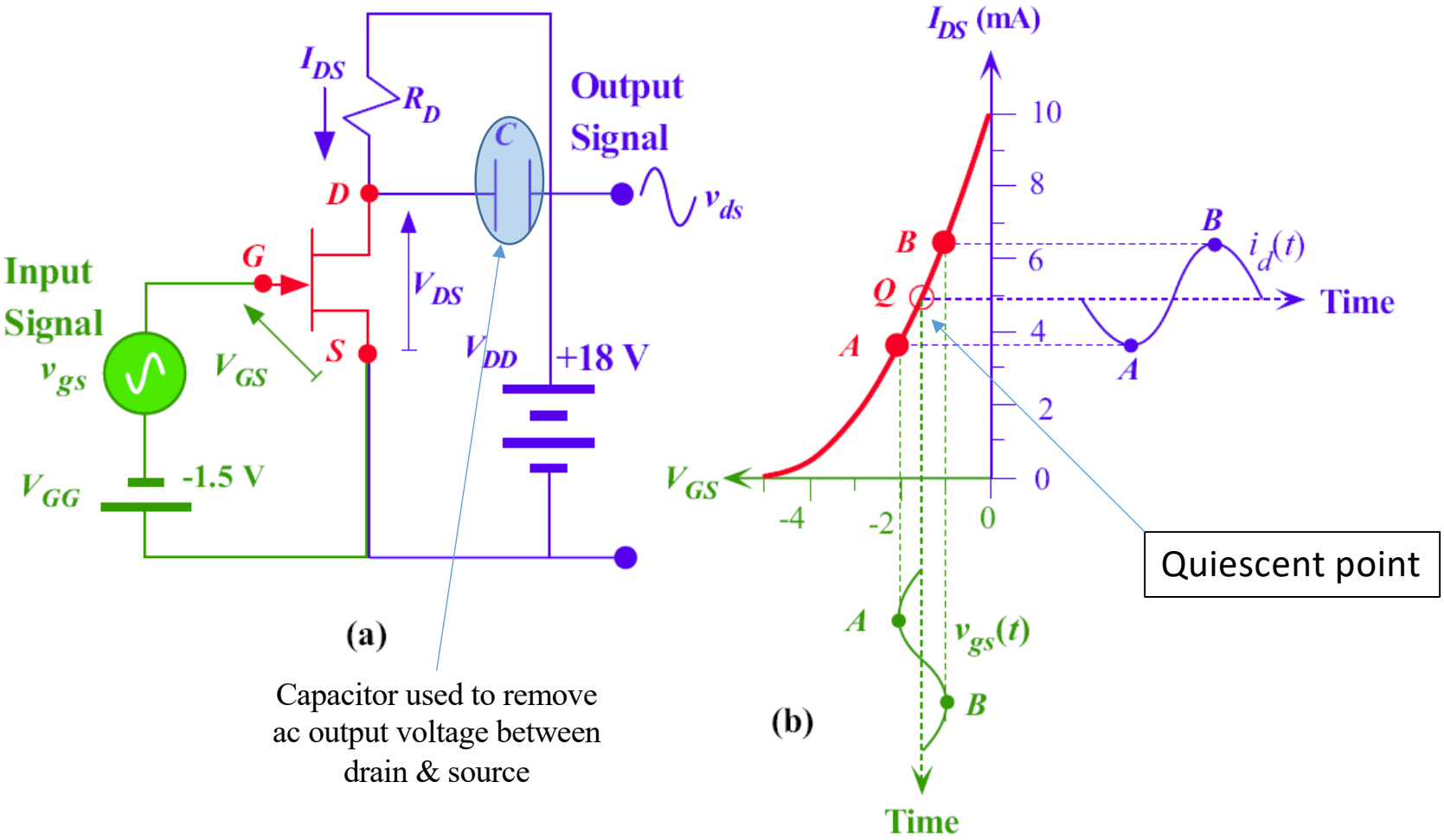
Two important facts about the JFET:

- Modulating the electric field in the reverse-biased depletion layers (by changing V_{GS}) varies the depletion layer penetration into the channel and hence the resistance of the channel. **The transistor action hence can be thought of as being based on a field effect**. Since there is a pn junction between the gate and the channel, the name has become **JFET**. This junction in reverse bias provides the isolation between the gate and channel.
- Secondly, the region beyond pinch-off is commonly called the current saturation region, as well as constant current region and pentode region. The term **saturation** should not be confused with similar terms used for **saturation effects in bipolar transistors**. A saturated BJT cannot be used as an amplifier, but ***JFETs are invariably used as amplifiers in the saturated current region***.

JFET Commons Source Amplifier

- The transistor action in the JFET is the control of I_{DS} by V_{GS} . The input circuit is the gate-source circuit containing V_{GS} and the output circuit is the drain-source circuit in which the drain current I_{DS} flows.
- The JFET is almost never used with the pn junction between the gate and channel forward-biased ($V_{GS} > 0$).
- With V_{GS} limited to negative voltages, the maximum current in the output circuit can only be I_{DSS}. The maximum input voltage V_{GS} should therefore give an I_{DS} less than I_{DSS}.

JFET Commons Source Amplifier



(a) Common source (CS) ac amplifier using a JFET. **Both input and output circuits are connected to the same source.**

(b) Explanation of how I_D is modulated by the signal v_{gs} in series with the dc bias voltage V_{GG}, supposing that v_{gs} varies sinusoidally between -0.5 V and +0.5 V.

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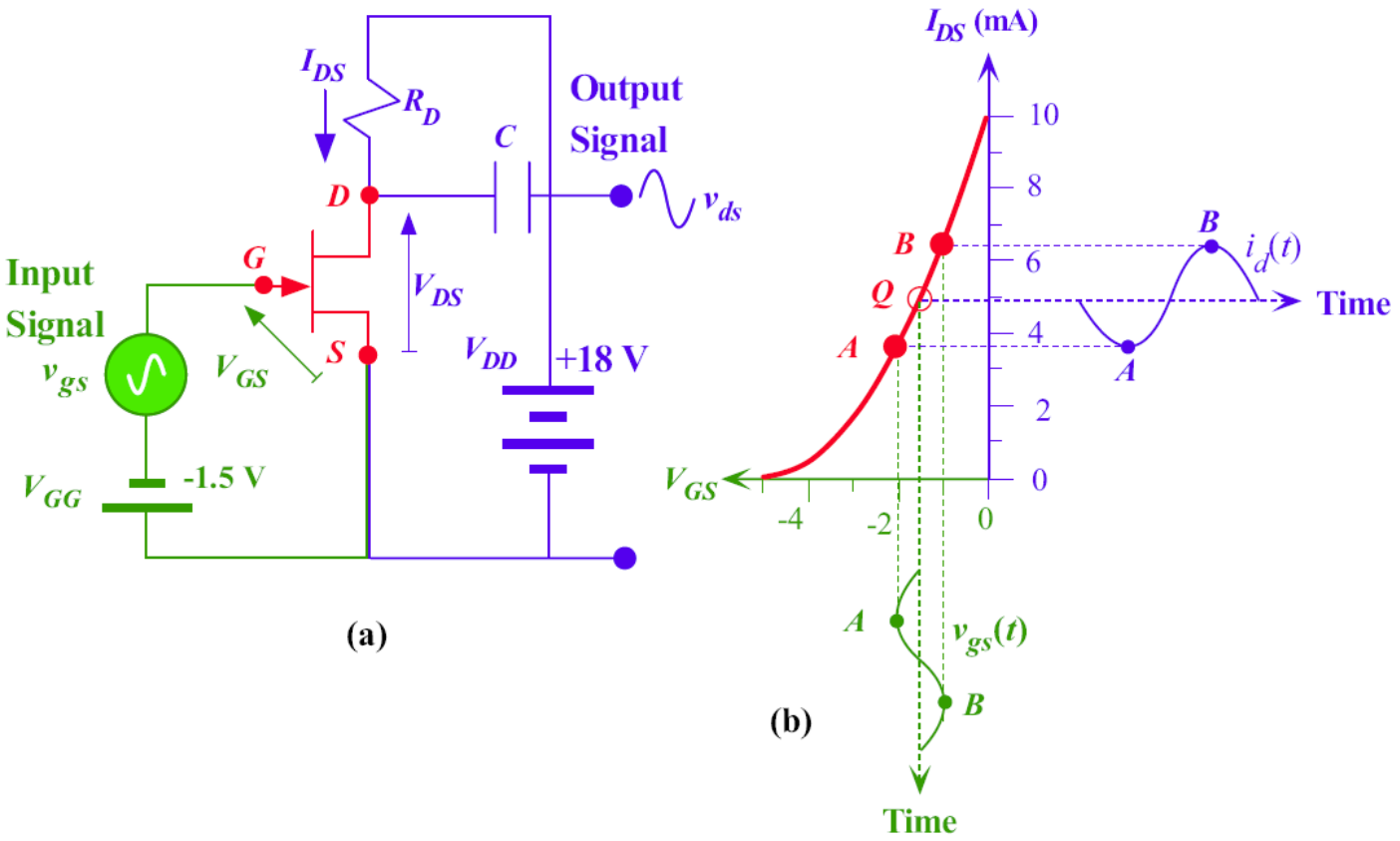
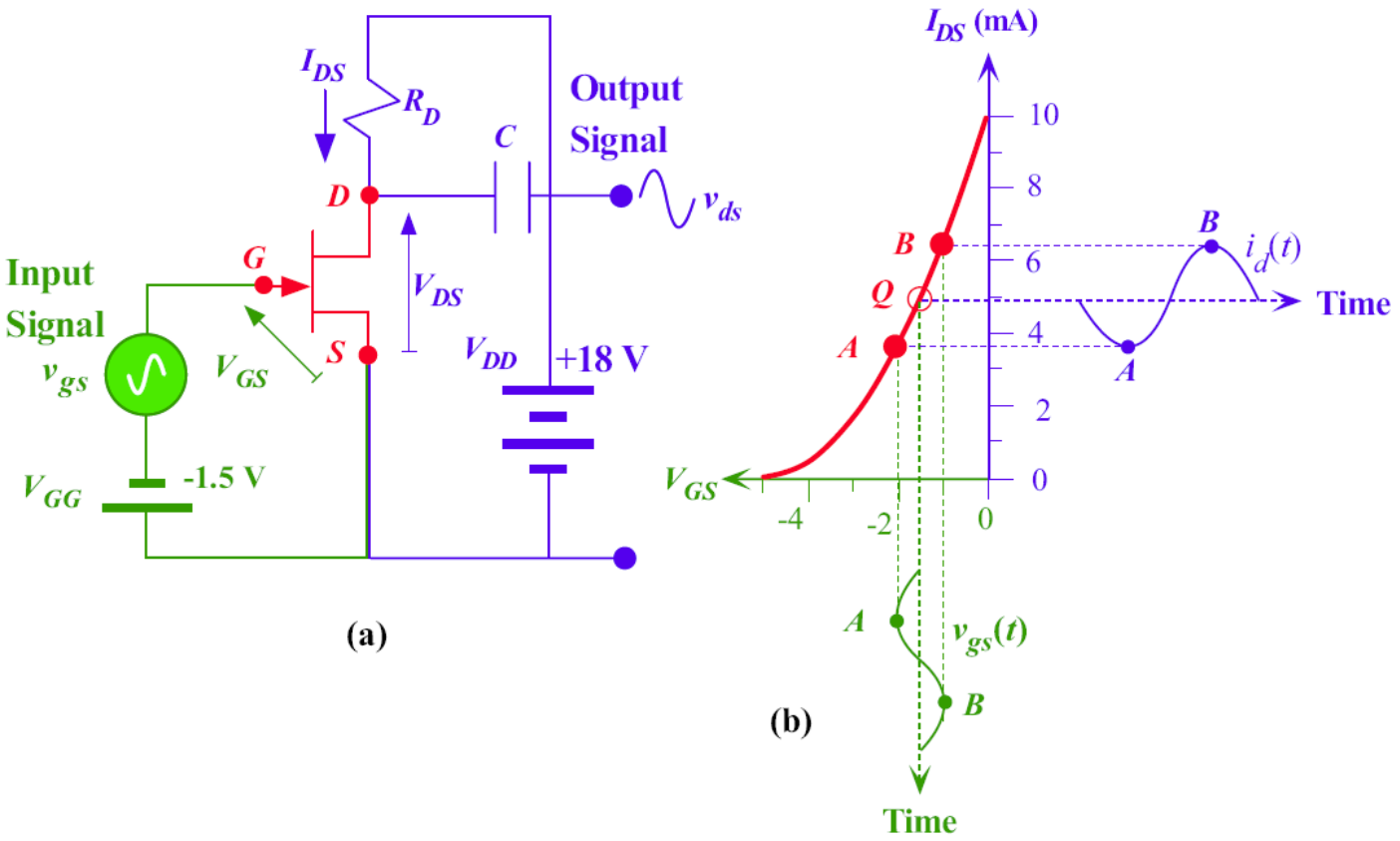


v_{gs} (V)	V_{GS} (V)	I_{DS} (mA)	$i_d = \delta I_{DS}$ (mA)	$V_{DS} = V_{DD} - I_{DS}R_D$	v_{ds} (V)	Voltage Gain	Comment
0	−1.5	4.9	0	8.2	0		dc conditions, point *Q*
−0.5	−2.0	3.6	−1.3	10.8	+2.6	−5.2	Point *A*
+0.5	−1.0	6.4	+1.5	5.2	−3.0	−6	Point *B*

NOTE: $V_{DD} = 18$ V and $R_D = 2000\ \Omega$.



v_{gs} (V)	V_{GS} (V)	I_{DS} (mA)	i_d (mA)	$V_{DS} = V_{DD} - I_{DS}R_D$	v_{ds} (V)	Voltage Gain	Comment
0	−1.5	4.9	0	8.2	0		dc conditions, point *Q*
−0.5	−2.0	3.6	−1.3	10.8	+2.6	−5.2	Point *A*
+0.5	−1.0	6.4	+1.5	5.2	−3.0	−6	Point *B*

NOTE: $V_{DD} = 18$ V and $R_D = 2000\ \Omega$.

Asymetric due to "$I_{DS} - V_{GS}$" relationship

$$I_{DS} = I_{DSS}\left[1 - \left(\frac{V_{GS}}{V_{GS(\text{off})}}\right)\right]^2$$

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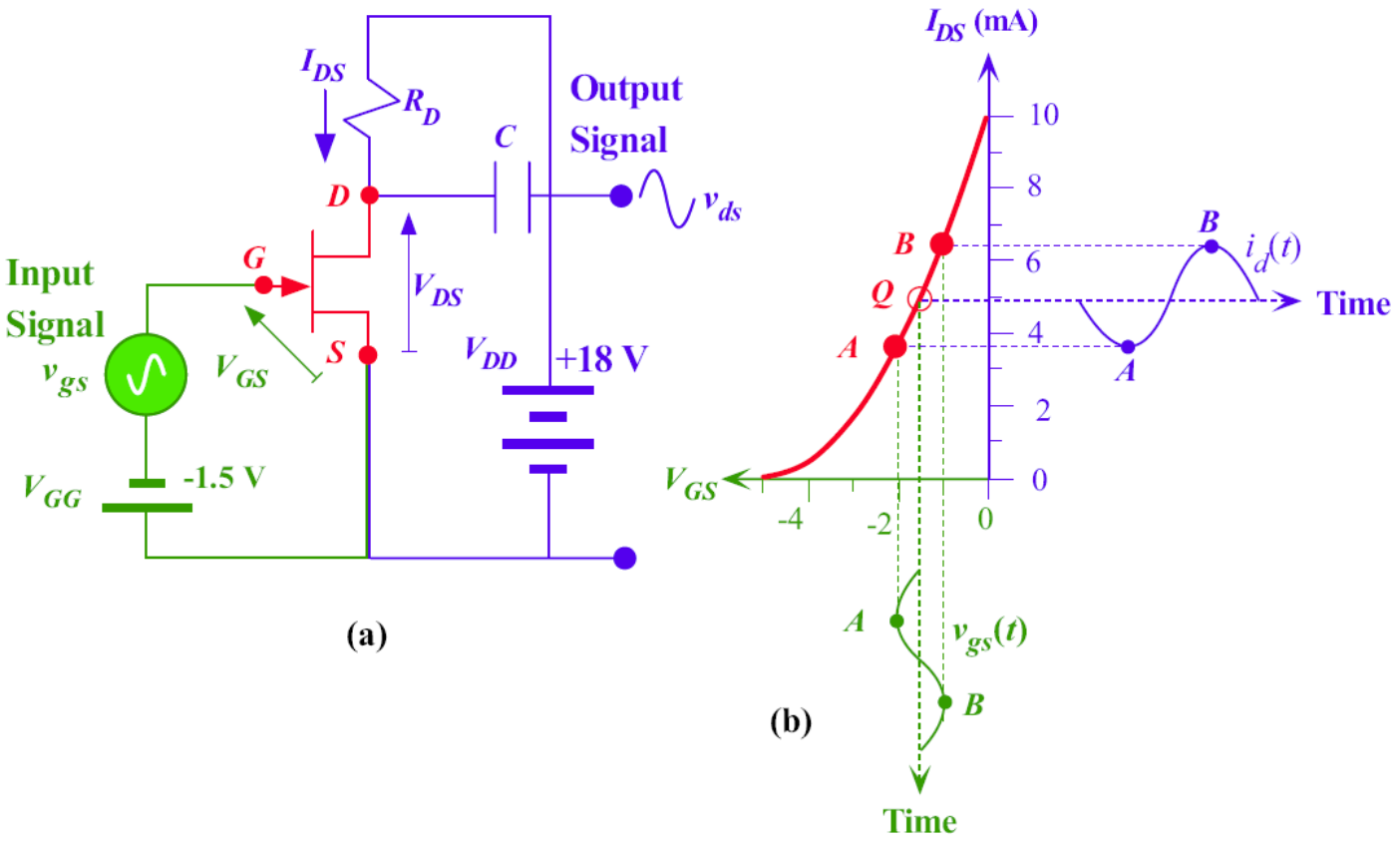


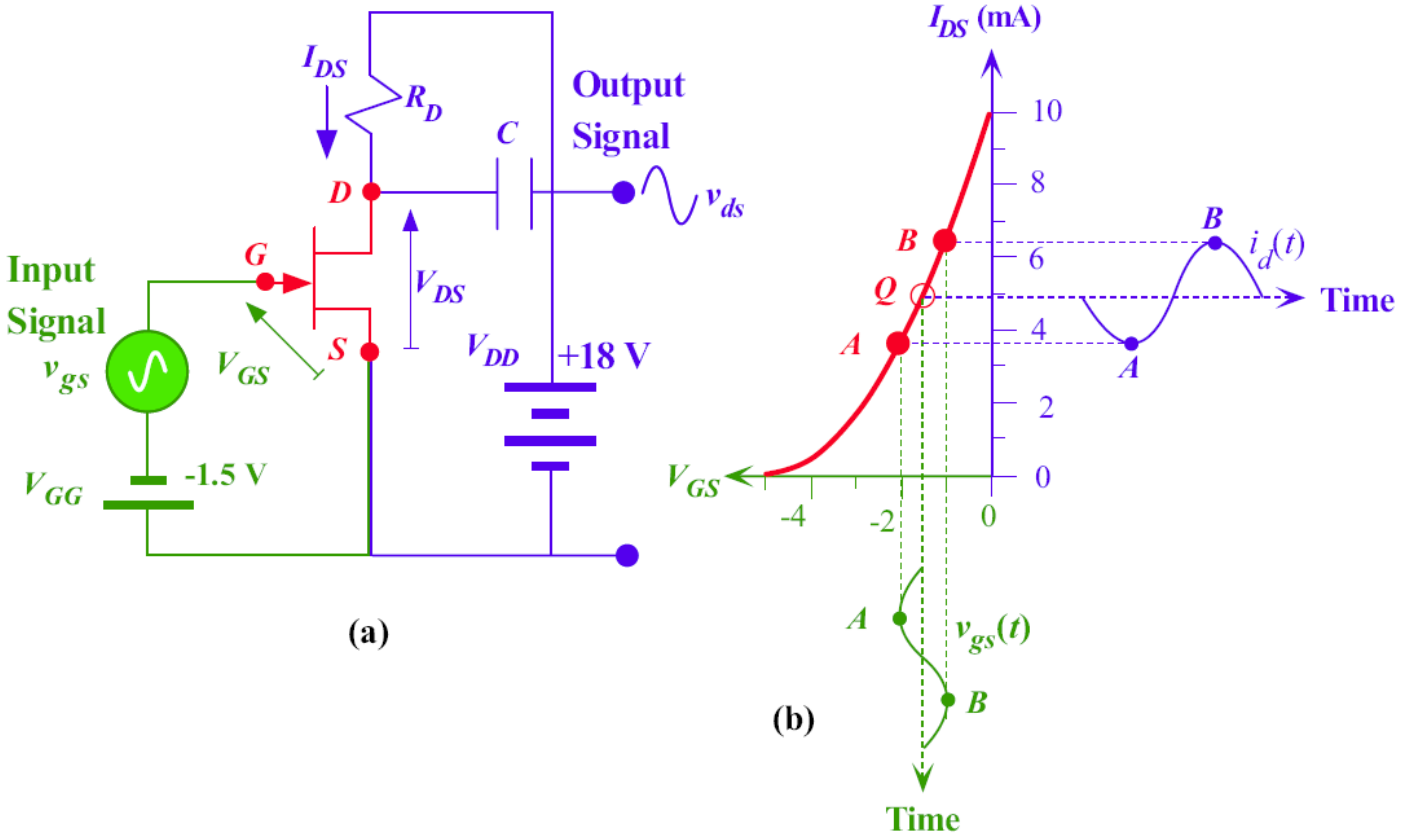
v_{gs} (V)	V_{GS} (V)	I_{DS} (mA)	i_d (mA)	$V_{DS} = V_{DD} - I_{DS}R_D$	v_{ds} (V)	Voltage Gain	Comment
0	−1.5	4.9	0	8.2	0		dc conditions, point Q
−0.5	−2.0	3.6	−1.3	10.8	+2.6	−5.2	Point A
+0.5	−1.0	6.4	+1.5	5.2	−3.0	−6	Point B

NOTE: $V_{DD} = 18$ V and $R_D = 2000\ \Omega$.

$$v_{ds} = -R_D i_d$$

Asymetric due to "$I_{DS} - V_{GS}$" relationship

$$I_{DS} = I_{DSS}\left[1 - \left(\frac{V_{GS}}{V_{GS(\text{off})}}\right)\right]^2$$



Thus the output, v_{ds}, changes from −3.0 V to 2.6 V. The peak-to-peak voltage amplification is

$$A_{V(\text{pk-pk})} = \frac{\Delta V_{DS}}{\Delta V_{GS}} = \frac{v_{ds(\text{pk-pk})}}{v_{gs(\text{pk-pk})}} = \frac{-3\text{ V} - (2.6\text{ V})}{0.5\text{ V} - (-0.5\text{ V})} = -5.6$$

The negative sign represents the fact that the output and input voltages are out of phase by 180º

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JFET Amplifier

- The amplification can be increased by **increasing** $\boldsymbol{R_D}$, but we must maintain V_{DS} at all times above $V_{DS(sat)}$ (i.e. beyond pinch-off) to ensure that the drain current $\boldsymbol{I_{DS}}$ in the output circuit is only controlled by $\boldsymbol{V_{GS}}$ in the input circuit.
- When the signals are small about dc values, we can use differentials to represent small signals. For example, $\boldsymbol{v_{gs} = \delta V_{GS}}$, $\boldsymbol{i_d = \delta I_{DS}}$, $\boldsymbol{v_{ds} = \delta V_{DS}}$ and so on. The variation δI_{DS} due to δV_{GS} about the dc value may be used to define a **mutual transconductance g_m for the JFET**.

JFET Common Source Amplifier

Definition of the JFET transconductance (small signal)

$$g_m = \frac{dI_{DS}}{dV_{GS}} \approx \frac{\delta I_{DS}}{\delta V_{GS}} = \frac{i_d}{v_{gs}}$$

JFET transconductance (small signal)

$$g_m = \frac{dI_{DS}}{dV_{GS}} = -\frac{2I_{DSS}}{V_{GS(\text{off})}}\left[1-\left(\frac{V_{GS}}{V_{GS(\text{off})}}\right)\right] = \frac{-2\left[I_{DSS}I_{DS}\right]^{1/2}}{V_{GS(\text{off})}}$$

JFET Common Source Amplifier

Small-signal voltage gain

$$A_V = \frac{v_{ds}}{v_{gs}} = \frac{-R_D i_d}{v_{gs}}$$

$$\therefore \quad A_V = \frac{-R_D(g_m v_{gs})}{v_{gs}} = -g_m R_D$$

$$\therefore \quad A_V = -g_m R_D$$

The negative sign indicates that the output and input voltages are out of phase by 180º

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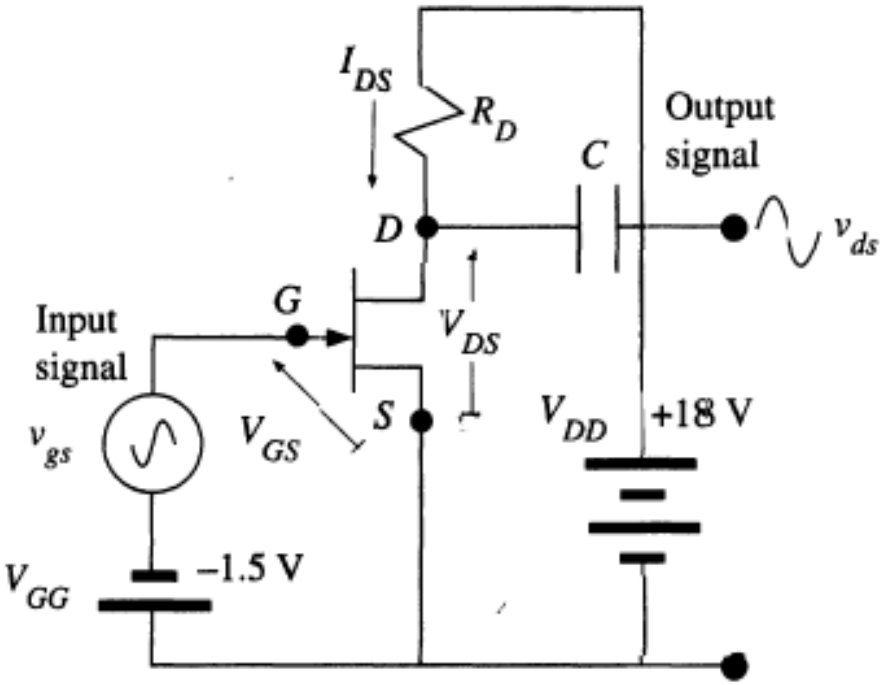
JFET – Example 1

THE JFET AMPLIFIER Consider the *n*-channel JFET common source amplifier shown in Figure 6.34a. The JFET has an I_{DSS} of 10 mA and a pinch-off voltage V_P of 5 V as in Figure 6.34b. Suppose that the gate dc bias voltage supply $V_{GG} = -1.5$ V, the drain circuit supply $V_{DD} = 18$ V, and $R_D = 2000\ \Omega$. What is the voltage amplification for small signals? How does this compare with the peak-to-peak amplification of −5.6 found for an input signal that had a peak-to-peak value of 1 V ?

We have already solved this problem; however, the previous solution can be simplified by using the below equations

$$A_V = -g_m R_D$$

$$g_m = \frac{dI_{DS}}{dV_{GS}} = -\frac{2I_{DSS}}{V_{GS(\text{off})}}\left[1-\left(\frac{V_{GS}}{V_{GS(\text{off})}}\right)\right] = \frac{-2\left[I_{DSS}I_{DS}\right]^{1/2}}{V_{GS(\text{off})}}$$



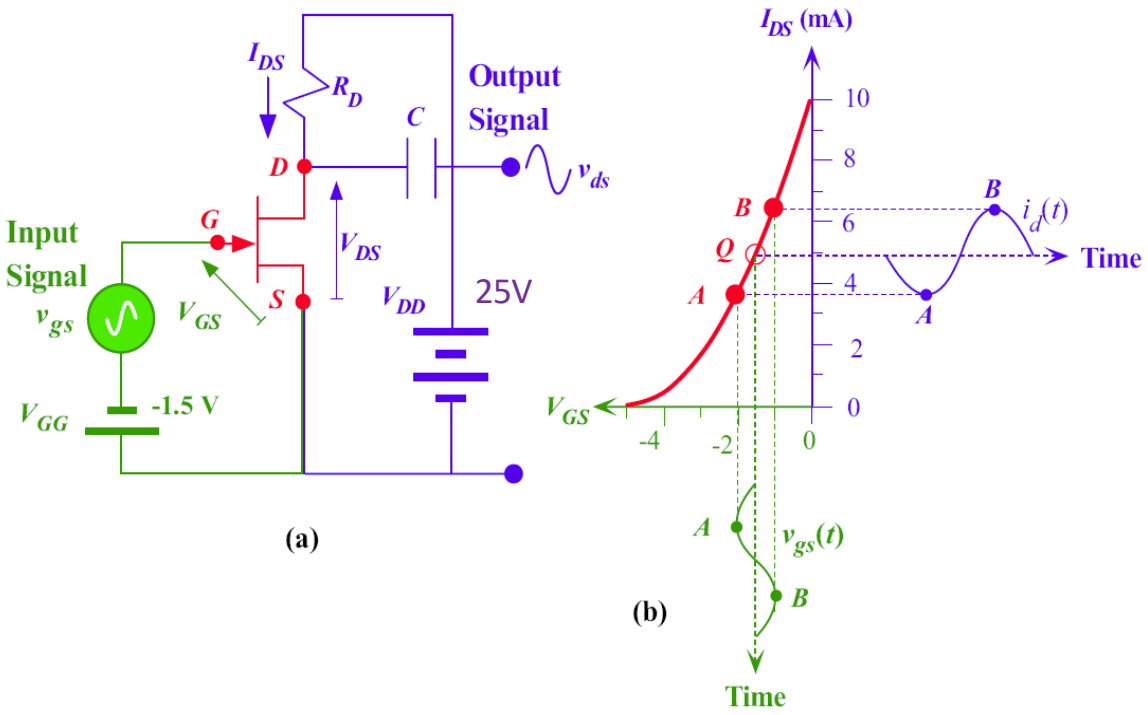
From *Principles of Electronic Materials and Devices, Fourth Edition*, S.O. Kasap (© McGraw-Hill Education, 2018)

JFET – Example 2

The JFET amplifier Consider an *n*-channel JFET that has a pinch-off voltage (V_P) of 5 V and I_{DSS} = 10 mA. It is used in a common source configuration as shown, in which the gate to source bias voltage (V_{GS}) is −1.5 V. Suppose that V_{DD} = 25 V.

a. If a small signal voltage gain of −10 is needed, what should be the drain resistance (R_D)? What is V_{DS}?

b. If an ac signal of 1 V peak-to-peak is applied to the gate in series with the dc bias voltage, what will be the ac output voltage peak-to peak? What is the voltage gain for positive and negative input signals? What is your conclusion?



Task - BJTs and FETs Differences

- What are the main differences between BJTs and FETs? Think in terms of device control, power consumption, applications, etc.