GLASGOW COLLEGE UESTC

Main Exam Paper

Electronic System Design 3 (UESTC 3003)

Date: Dec.22th, 2021
Time: 9:30-11:30am

Attempt all PARTS. Total 100 marks

Use one answer sheet for each of the questions in this exam.

Make sure that your University of Glasgow and UESTC Student Identification Numbers are on all answer sheets.

An electronic calculator may be used provided that it does not allow text storage or display, or graphical display.

All graphs should be clearly labelled and sufficiently large so that all elements are easy to read.

The numbers in square brackets in the right-hand margin indicate the marks allotted to the part of the question against which the mark is shown. These marks are for guidance only.

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Q1 You have been asked to help design a system with a primary role of improving the level of a typical talking voice. The input is a microphone that must connect to a pre-amplifier, and then to an ARM Cortex processor, through an analogue to digital converter (ADC), to provide a digital display and for signal processing. The microphone has an rms noise voltage of 0.25 μV, a typical output voltage of 1.8 mV and a maximum output voltage of 200 mVrms. The ARM processor has a DC supply of +3.5V which is used to power the system. There is a 16 bit (ADC) connected to the input of the ARM processor.

(a) Draw a block diagram of your system which must include the microphone, an amplifier, the ARM processor with the ADC, and show the interconnects between the devices. [4]

(b) Explain fully how your design is limited due to the microphone and ARM Cortex processor being fixed components (i.e., you are not able to change them). You should also comment on design limitations that may exist due to customer requirements. [8]

(c) Redraw the block diagram drawn for part (a) showing how you would interface to the ADC. You should explain fully your design decisions and include any relevant calculations. [8]

(d) The customer wants to make full use of the microphone's dynamic range. How would you make this possible? [5]

Note: To get full marks for part (d) all working must be shown in your answer.

Q2

a) You have designed an inverting amplifier using a LM358 Op-Amp. You put the schematic shown in Figure Q2a into a SPICE simulator to test your design before building a prototype. When you run the simulation you obtain the output voltage waveform shown in Figure Q2b

i. Given that Vs is a sine wave, with a 1V peak and a frequency of 10 kHz, draw the expected waveform for Vout. [4]

ii. Considering the requirement for bias current to each input of the op-amp, what modification would you make to the layout in Figure Q2a? [8]

iii. Re-draw the schematic to illustrate the change, or changes, you propose to make. [4]

Note: Parts (ii) and (iii) maybe answered together, but full marks will only be given for a re-drawn schematic and a full explanation.

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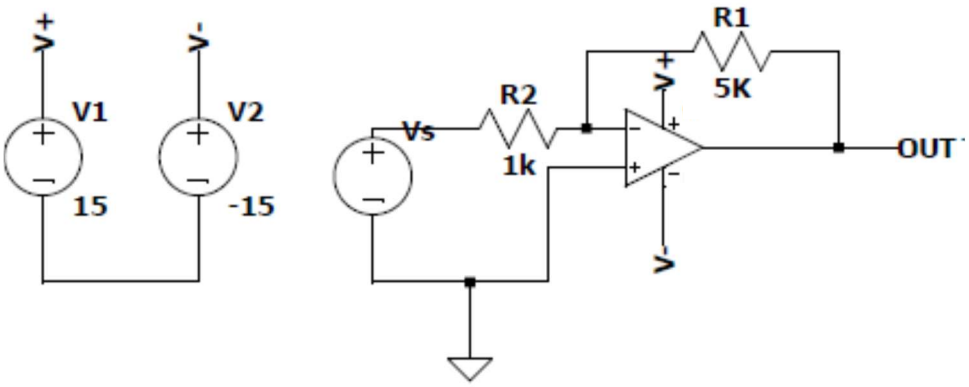

Figure Q2a

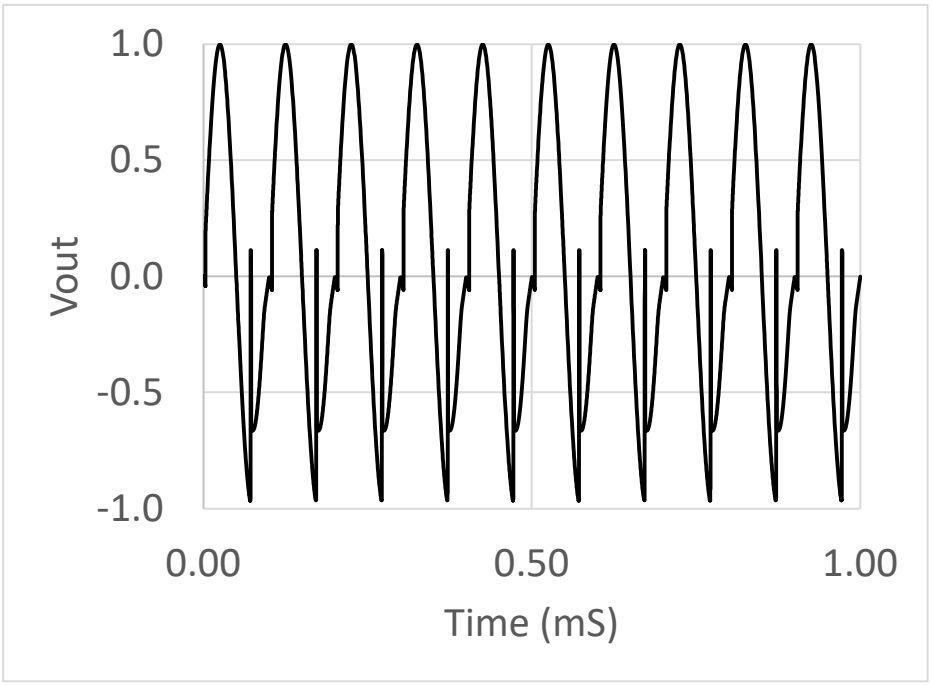

Figure Q2b

b) Consider Figure Q2c, where a thermocouple generates a small voltage proportional to the difference in temperature between the measurement junction and the "reference" junction, which is near the input to device "X".

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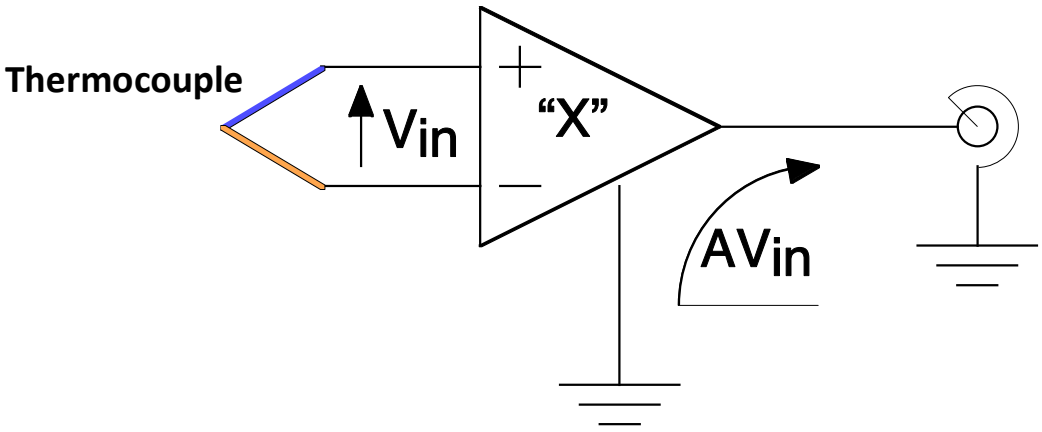

Figure Q2c

i. Discuss why this circuit may not work when "X" is an instrumentation amplifier with bipolar transistor input stages. [6]

ii. Redraw Figure Q2c so that the circuit will work. [3]

Q3

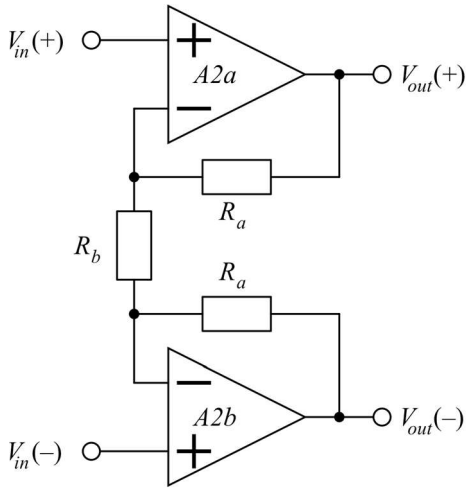

Figure Q3a

a) Figure Q3a shows the circuit schematic of part of an instrumentation amplifier. Show that the expressions for the differential and common mode gains of the circuit in Figure Q3a are given by:

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$$A_{Vdiff} = \frac{2.Ra+Rb}{Rb} \quad \text{and} \quad A_{CM} = 1 \qquad [5]$$

b) Including the circuit fragment shown in Figure Q3a, draw the diagram of a traditional three-opamp instrumentation amplifier. Write down expressions for the differential and common–mode gains of the complete circuit. [5]

The next generation of 'mild-hybrid' motor cars will be based on a battery voltage of 48V DC (instead of 12V) that provides power to many of the vehicle's electrical systems and traction assistance to the engine during acceleration. Figure Q3b shows the circuit for controlling the interior heater motor for the vehicle. The motor is rated at 100W and is connected to a speed controller that can apply a varying voltage of 0 -> +40V to the motor and thus change the speed. The controller can also monitor the motor current to control the speed or detect motor faults. The current flowing through the motor is monitored using a series resistor '*RCM*' and an Instrumentation amplifier, *A1*. The voltage at *'Vout'* is proportional to the motor current and is used by the speed controller to control the drive power to the motor.

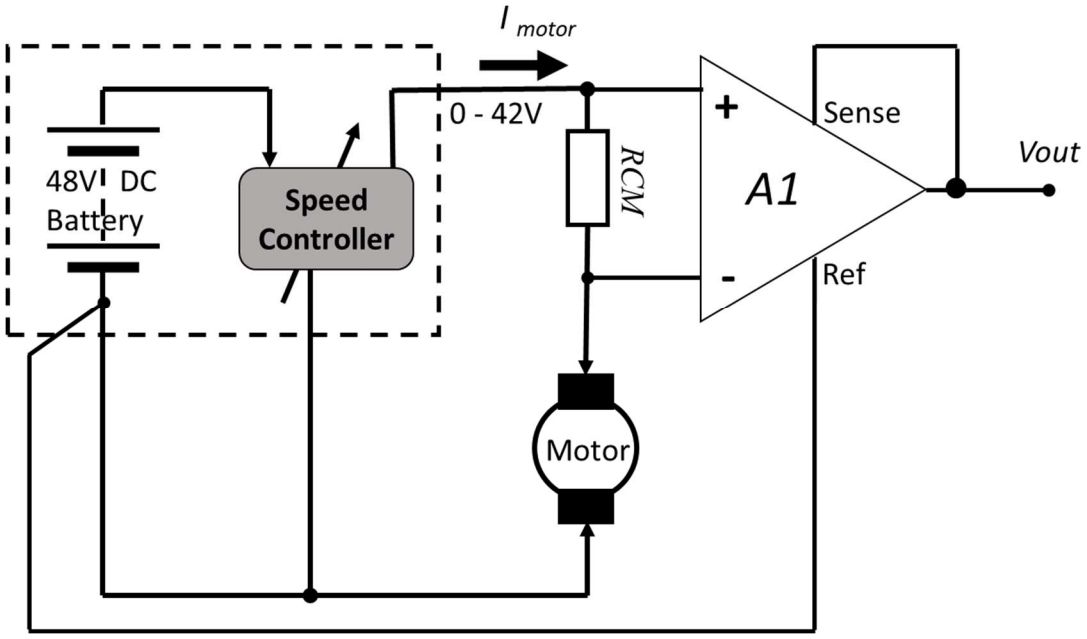

Figure Q3b: Simplified heater motor speed control

c) If the voltage applied across the motor is 40V DC to produce an output power of 100W, and the maximum differential voltage applied to the instrumentation amplifier *'A1'*

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should be 375mV, demonstrates how you would calculate the correct value for *RCM* and determine that value. Show all your working and assumptions. [3]

d) The drive voltage for the motor can be from '0V' (off) to +40V (full power) as the motor power varies from 0 – >100W. If *RCM* = 150mΩ, calculate the CMRR required for *A1* if the motor drive current measurement error across the speed range due to a common-mode signal must be less than 1%. [4]

e) Hence design *A1* demonstrating the calculation of all resistance values and tolerances for an overall gain of x150. You can assume there are no restrictions on the power supplies for the amplifier. [5]

f) If the required tolerance for the motor current measurement was relaxed to +/- 5%, does this change the tolerance on any of the resistors? Justify your argument. [3]

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Q4 In modern instrumentation, Digital-to-Analog Converters (DACs) are critical in defining the performance of test equipment for converting digitally generated signals into analog waveforms. Figure Q4 shows the circuit schematic of a R-2R DAC used to convert a digital input word (b_0 – b_n) into an analog signal (V_{out}). The circuit comprises a precision DC voltage reference (V_{ref}) and a number of transistor switches, each controlled by a digital 'bit' ($b_0 \rightarrow b_n$) that connect the R-2R resistor ladder network to either V_{ref} or zero volts. The advantage of the R-2R circuit configuration is it may be extended to any number of bits (shown by the dotted lines between bit *'b_2'* ----- *'b_n'*) using only 2 matched resistor values. Another feature of this configuration is it can be simplified to a variable voltage source (V_{dac}) in series with a resistor 'R' for circuit analysis (shown in dotted inset box). The output of the resistor ladder network is applied to a buffer amplifier(A1) to produce the final output level (V_{out}) with a low source resistance.

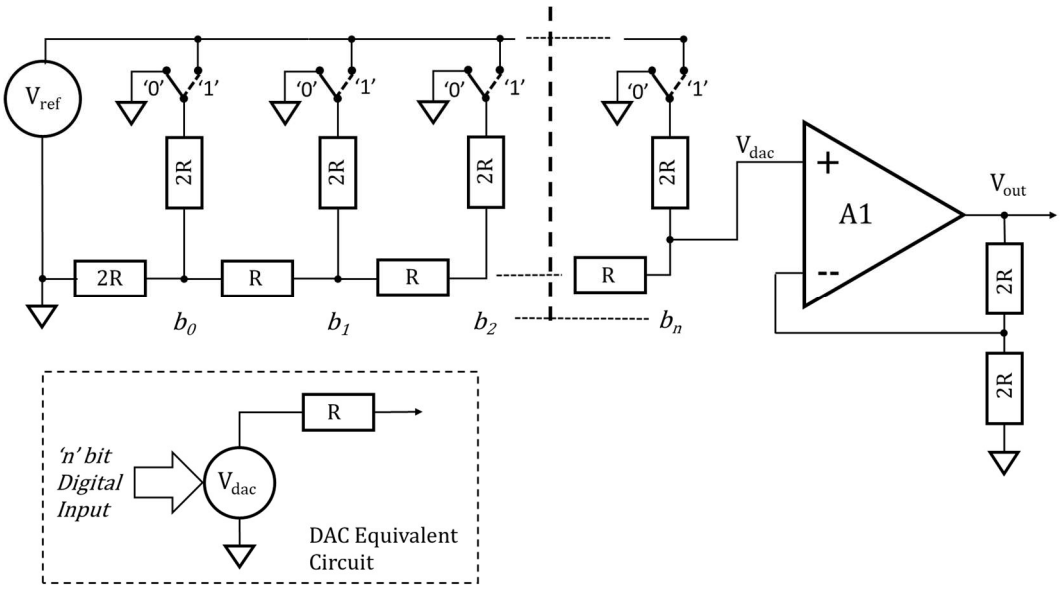

Figure Q4: R-2R DAC converter schematic

a) Using the above information and assuming a reference voltage (V_{ref}) =2.048V, and a digital word width of 10 bits ($b_0 \rightarrow b_9$), calculate the maximum output voltage that can appear at both the ladder output (V_{dac}) and the amplifier output(V_{out}). Also, calculate the minimum voltage step that can be programmed at V_{dac}. Show all your calculations and state all assumptions made in your answer. [3]

b) Including any noise produced by V_{ref}, re-draw the circuit diagram showing <u>all</u> sources of noise when the 10 bit digital word ($b_0 \rightarrow b_9$) is 11111 11111. [5]

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c) Hence derive an expression for the voltage noise spectral density present at the output (Vout) of the amplifier at a room temperature of 25 °C. Clearly identify each source of noise in your calculations and state any assumptions you make. [5]

d) The operational amplifier '*A1*' is one of the three shown in Table Q4:

OpAmp	v_n **(nV /√Hz)**	i_n **(fA/√Hz)**
Amplifier 1	4.8	4600
Amplifier 2	7.0	25
Amplifier 3	3.8	200

Table Q4

If the unit resistance 'R' for this circuit is 1000Ω, draw a table comparing the performance of each amplifier and identify which would to be most suitable for this application. Explain your reasoning using a suitable diagram. [6]

e) Using your amplifier choice from part (d), and assuming the temperature of the circuit = 25 °C, 'R' = 1000Ω, and the ladder output (V_{dac}) is a DC level of Vref/2, calculate what level of noise generated by V_{ref} could be tolerated that would limit the overall noise increase appearing at the output (V_{out}) to +3dB? [5]

PHYSICAL CONSTANTS Boltzmann Constant = 1.38×10^{-23} $J.K^{-1}$

End of question paper