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UESTC 3003: Electronic System Design

Static Errors
Lecture 2.6: Input Offset Voltage

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Thanks to Prof. Duncan Bremner

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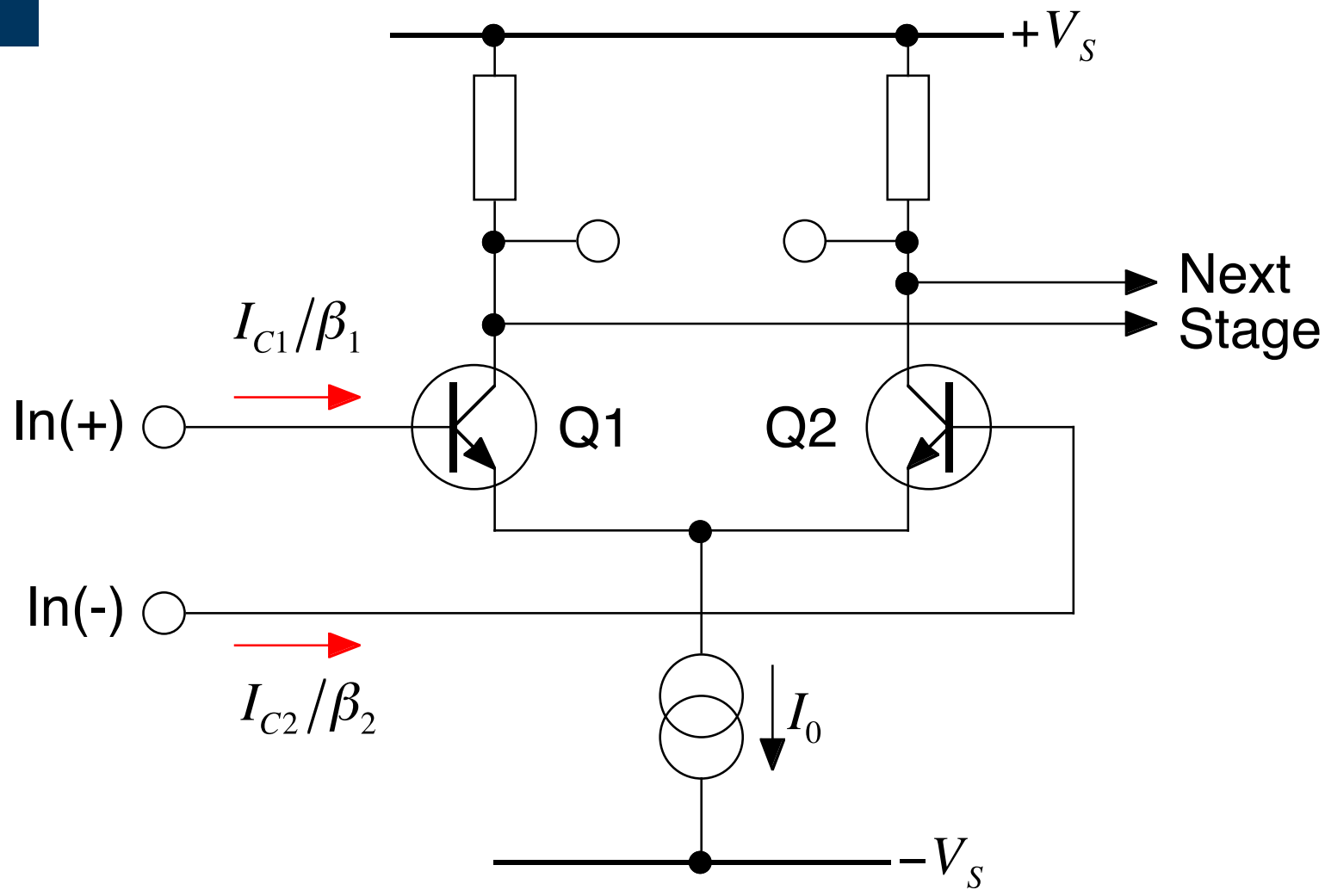
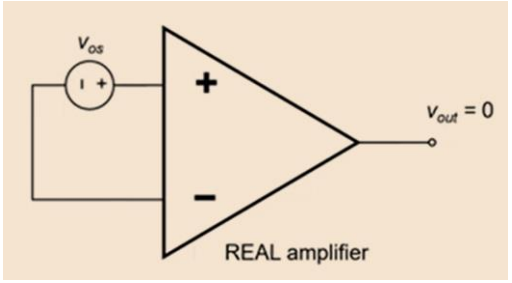
Imperfect opamps (revision)



Transistors are closely matched, but... β is up to $\approx 5\%$ out

Input Offset Voltage (Vos)

V_{OS} is defined as the voltage that must be applied between the two input terminals of the op amp to obtain zero volts at the output.



V_{os} is the input voltage required to make $V_{out} = 0$.

Symbolically represented by a voltage source that is in series with either the positive or negative input terminal.

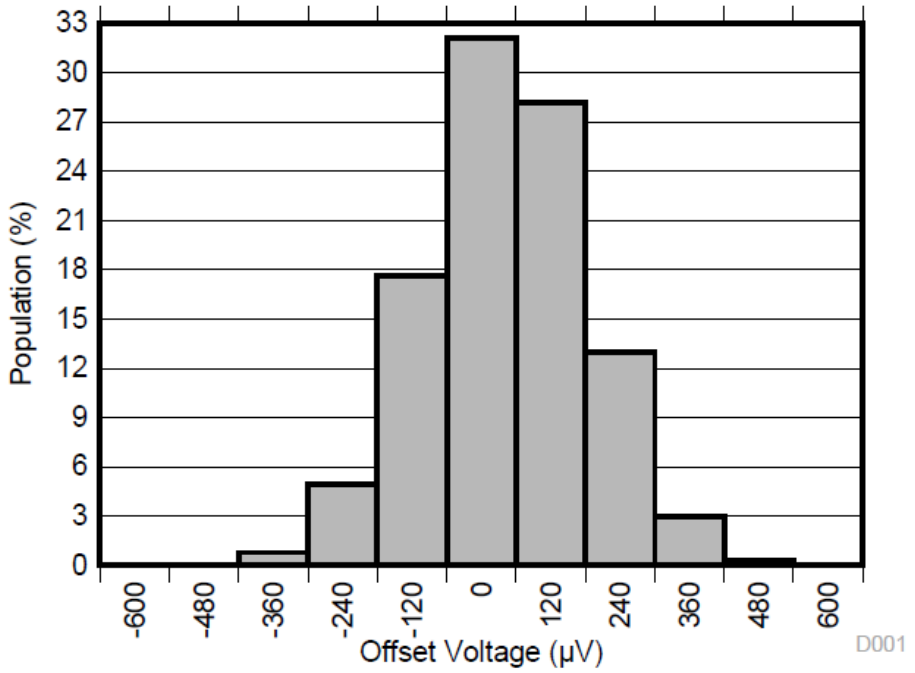
Is considered to be a DC error and is present from the moment that power is applied until it is turned off, with or without an input signal.

Occurs during the biasing of the op amp and its effect can only be reduced, not eliminated.

Input Offset Voltage (1)

Can be either negative or positive in polarity and can vary from device to device (die to die) of the same wafer lot.

Typically in the range of 10µV to 10mV.



Distribution of V_{OS} for the OPA2991

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Cause of V_{OS}

Mostly due to the inherent mismatch of the input transistors and components during fabrication of the silicon die.

Stresses placed on the die during the packaging process have a minor contribution.

These effects collectively produce a mismatch of the bias currents that flow through the input circuit, and primarily the input devices, resulting in a voltage differential at the input terminals of the opamp.

V_{OS} has been reduced with modern manufacturing processes through increased matching and improved package materials and assembly.

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Vos

Three general manufacturing processes : CMOS, JFET, and bipolar.

CMOS devices typically have the lowest V_{OS} of the three, and they have the least drift.

JFET devices have the worst V_{OS} and temperature drift.

Bipolar devices have a V_{OS} that is close to that of CMOS devices, and a low temperature drift.

Process	Device Type	Year	V_{OS} †at 25 °C (µV)	$\Delta V_{OS}/\Delta T$† (µV/°C)
Bipolar	LM2904B	2019	300	3.5
	LM2902B	2022	300	7
	TLV6003	2019	390	2
JFET	OPA462	2018	200	4
	OPA828*	2018	50	0.45
CMOS	OPA2991	2019	125	0.3
	TLV9041	2021	600	0.8
	OPA2310	2022	250	0.5
	TLV9162	2021	210	0.25

Range of Input Offset Voltage and Drift Per Device Process

Effect of Input offset voltage

Reduce/minimize V_{OS} - can only be reduced, not eliminated.

Mismatch mainly due to:

- Doping variations,
- Lithographic errors
- Packaging and local stress

Effect of Input offset voltage - Example (2)

V_{OUT} when V_{IN} = 10 mV. Assume op-amp has no offset voltage (V_{OS} = 0)

$$I_1 = I_2$$

$$\frac{10mv - 0}{1k\Omega} = \frac{0 - Vout}{100K\Omega}$$

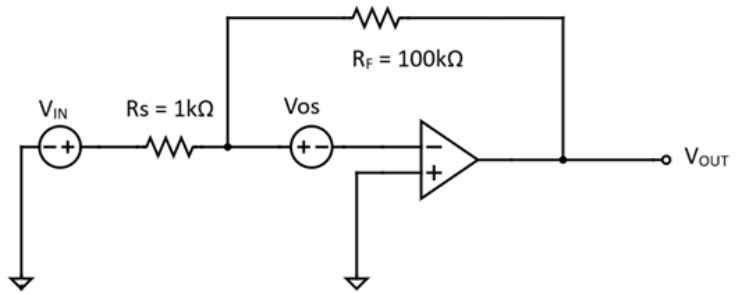
Vout = -1V (Gain of -100)

V_{OUT} when V_{IN} = 10 mV. Assume op-amp has offset voltage (V_{OS} = 5mV)

$$I_1 = I_2$$

$$V_{out} = -495mV$$

Gain = -49.5



Slew rate

Maximum rate of change of an opamp output voltage.

How fast the op-amp is capable of changing its output voltage in response to a change in input.

Usually measured in units of a volt per unit of time, (V/μs).

Primarily caused by the internal compensation capacitor, which is used to stabilize the op-amp and prevent oscillations.

High slew rate is essential for applications requiring fast response times, i.e. high-speed data acquisition, audio amplifiers, and video signal processing.

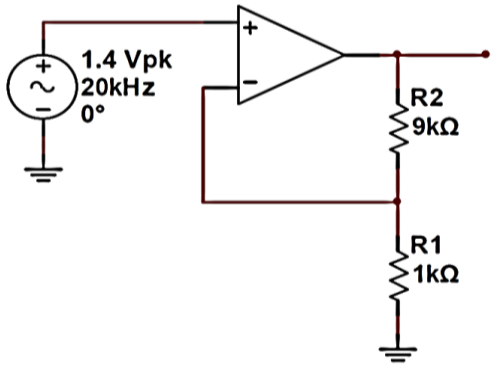
Slew rate effect - Example

The Opamp circuit is used to amplify a 1.4 Vpk line-level audio signal with a f = 20 kHz.

slew rate of 1 V/µsec. Output is slew rate limited?

non-inverting amplifier.

Voltage gain $A_v = 1 + \frac{R_2}{R_1} = 10$



Peak output voltage $V_{out} = A_v \times V_{in} = 10 \times 1.4 = 14V$

Maximum slope $= 2\pi f V_{out} = 2\pi \times 20 \times 10^3 \times 14 = 1759291.89\ V/s$

Opamp has a slew rate of 1V/µs = 1×10^6V/s

Opamp is slew-rate limited.

To avoid slew-rate limiting, slew rate = 1.76V/µs or more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Thank you
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