

# 1DT301, Computer Technology

- Programming in Assembly and C
- STK500 or STK600
- Lectures
- Laboratory work (6 labs)
- Laboratory work is mandatory
- Written exam,  
Monday, October 23, 2017, 8.00-13.00  
(2nd exam: Saturday, December 2, 12.00-17.00)

# Course syllabus

## Objectives

After the course the student should have knowledge about:

- computer hardware
- microprocessors
- assembler programming
- computer communication with units outside the computer
- interrupts
- write, test and troubleshoot computer programs in assembler on the actual microprocessor
- develop simple programs in assembler

# Course syllabus

## Content

The AVR ATMEGA16, PIC16F877 or a similar microprocessor and a specific development card are used in the course.

Practical work and lectures are based on the actual microprocessor.

The course consists of the following topics:

- programming in assembler
- computer hardware
- computer architecture
- address-, data- and control buses
- input and output units
- timers
- interrupts
- microprocessor, memory and memory handling
- higher level programs and assembler

# Course syllabus

## Type of Instruction

Lectures and practical work. Practical work is mandatory.

## Examination

The course is assessed with the grades A, B, C, D, E, Fx or F.

The grade A constitutes the highest grade on the scale and the remaining grades follow in descending order where the grade E is the lowest grade on the scale that will result in a pass. The grade F means that the student's performance is assessed as fail (i.e. received the grade F).

Written reports of laboratory experiments and/or written examination. The assessment method is decided at the start of the course.

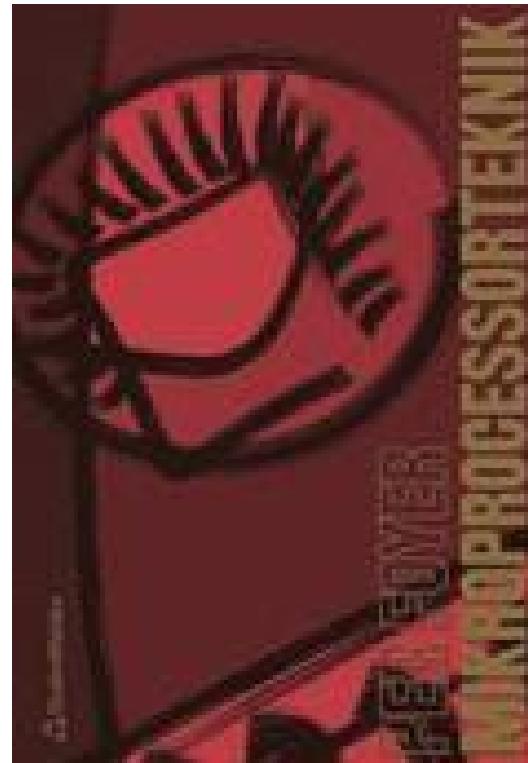
Students who do not pass the regular examination are given the opportunity to do a *resit* examination shortly after the regular examination.

# Course syllabus

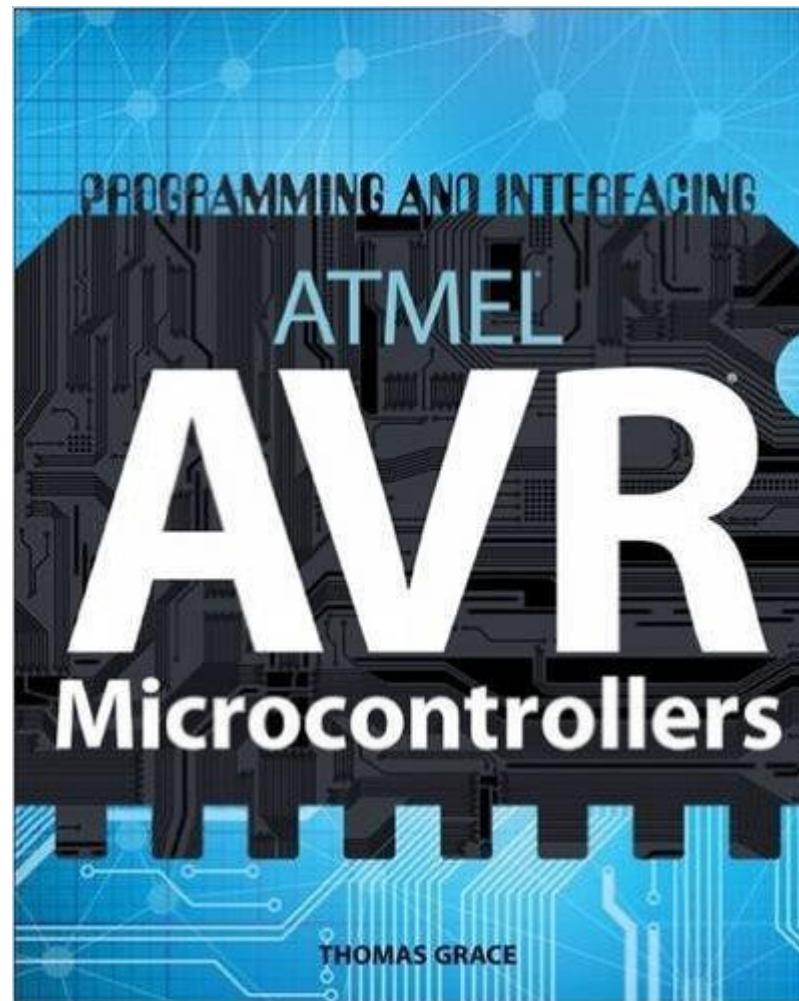
Required Reading and Additional Study Material

**Required reading**

Foyer Per, *Mikroprocessorteknik*, Studentlitteratur, 2005. Pages 275. (275)



New book:

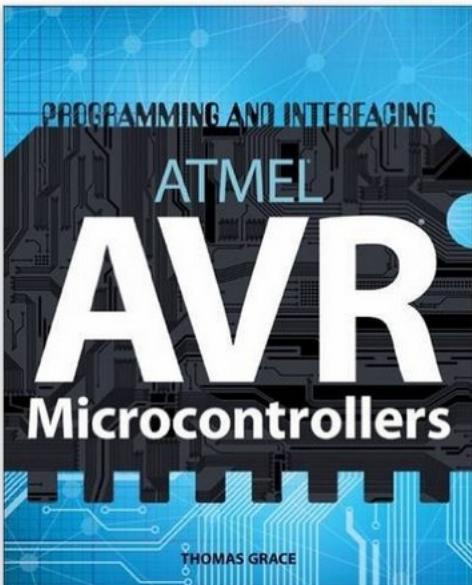


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# Programming and Interfacing ATMEL's AVR's 1st Edition

by Thomas Grace (Author)

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TimeEdit Linnéuniversitetet > Schema och visning av bokningar av lokaler, personal mm

Idag < Feb > 2015-02-02 - 2016-02-07 Ändra sökning 1DT301, Datorteknik I, HT15

Välj vad du vill söka

Kurs ▼ 1dt301 Sök Visa kategorier

Sökresultat 1dt301, Starttermin: HT15, VT15

1DT301, Datorteknik I, HT15  
1DT301, Datorteknik I, HT15  
1DT301, Datorteknik I, HT15  
1DT301, Datorteknik I, HT15

Mina val

1DT301, Datorteknik I, HT15 Rensa allt

Visa schema

Historik

1DT301, Datorteknik I, HT15  
1DT301, Datorteknik I, HT15, 1DT301, Datorteknik I, HT15, 1DT301, Datorteknik I, HT15, 1DT301, Datorteknik I, HT15  
1MA131, Grundläggande matematik för ingenjörer, HT15, 1MA131, Grundläggande matematik för ingenjörer, HT15, 1DT100, Datortek...  
1DT100, Datorteknik - introduktion med projektarbete Datorteknik – introduktion med projektarbete, HT15, 1DT100, Datorteknik - introd...

Schema

# Weekly layout in general

TimeEdit® LINNÉUNIVERSITETET > ÖPPEN SCHEMAVISNING > SCHEMA (VÄXJÖ)

IDAG < V 36 > 2017-09-04 - 2017-09-10 ÄNDRA SÖKNING 1DT301, Datorteknik I, HT17, 1DT301, Datorteknik I, HT17, +2 Kurs (4)

KONTO ▾

PRENUMERERA SKRIV UT ANPASSA

Schema				
MÅNDAG 4/9	TISDAG 5/9	ONSDAG 6/9	TORSDAG 7/9	FREDAG 8/9
8 Lab group 1 8:15-12	10 Lecture 10:15 -12		10 Lab group 3 8:15-12	10 Lab group 4 13:15-17
13 Lab group 2 13:15-17	13 Lecture 13:15-15		15 <del>15 1DT301, NGDNS, NGDPV, TGIID-E, HT17-67006, HT17-6004, HT17-F6516, HT17-U6M02, HT16-61000, HT16-61001, HT16-F6100-6101, HT16-61002, HT16-61003, HT16-61021, HT16-61022, D1166V. Amanuens: 3. Laboration, Växjö</del>	15 Lab group 5 8:15-12
16			17	
17				

1DT301 Datorteknik I, HT17-67006  
1DT301 Datorteknik I, HT17-68004  
1DT301 Datorteknik I, HT17-F6516

■ Föreläsning ■ Laboration

DÖJJ BOKNINGAR LÄNK TILL DETTA SCHEMA TEXTSCHEMA

# MyMoodle

Dashboard > 16HT-1DT301

Turn editing on

## NAVIGATION

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  - My courses

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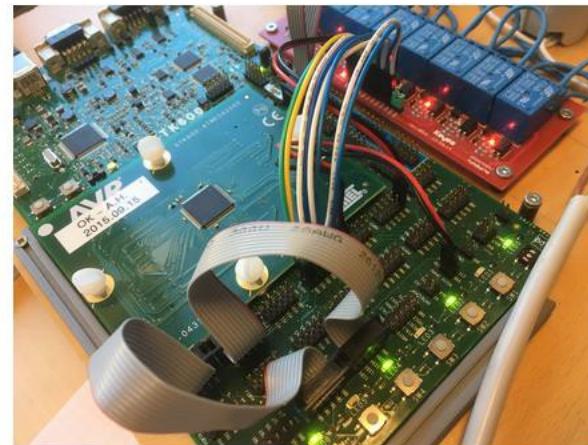
- Course administration
  - Turn editing on
  - Edit settings
  - Users
    - Unenrol me from 16HT-1DT301
  - Filters
  - Reports
  - Grades
  - Gradebook setup
  - Backup
  - Restore
  - Import
  - Question bank
  - Repositories
  - Legacy course files
- Switch role to...

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## 16HT - 1DT301 - Computer Technology 1 - 7,5hp - Växjö



## Computer Technology 1, 2016

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- [Private conversation with your teacher](#)
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- [Some important internet links for students](#)

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(No news has been posted yet)

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 Anders Haggren

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## Planning, lab groups etc.

## 2016 Lectures, Slides etc.

# MyMoodle

Repositories  
Legacy course files  
Switch role to...

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### GUIDES

- [Datavetenskap](#)
- [Computer Science](#)



Café  
Some important internet links for students

### Planning, lab groups etc.

### 2016 Lectures, Slides etc.

### 2016 Lab instructions

### Manuals and data books.

- doc2549 ATmega2560
- Instruction set
- m2560def
- doc1022 AVR Assembler user guide
- doc2466 ATmega16
- m16def
- STK600 User Guide
- Using Arduino boards with Atmel Studio
- JHD202C display 2x20
- GDM1602A display 2x16
- CyberTech Display
- C compiler settings 2014 11 07

# MyMoodle

MyMoodle

 My latest courses ▾

 This course ▾



3



Anders ▾

## Old exams.

-  Exam Task 4 2014 10 29
-  Exam 2014 12 05
-  Exam 2014 10 29
-  Exam 13 02 16
-  Exam 2013 10 28
-  Exam 13 01 18
-  Exam 12 01 13
-  Tenta 11 01 14
-  Solutions Exam 2014 12 05
-  Solutions Exam 2014 10 29
-  Solutions Exam 2013 12 13
-  Exam 2013 12 13
-  Laborationer 2013
-  Answers Exam 2013 10 28
-  Answers Exam 13 02 16
-  Answers Exam 13 01 18
-  Answers Exam 12 01 13
-  Losning Tenta 11 01 14
-  Answers Exam 2015 10 26
-  Answers Exam 2015 11 28
-  Exam 2015 10 26
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## Other Categories

## Beginners Introduction to the Assembly Language of ATMEL-AVR-Microprocessors

Thinking to start career in video **Game Programming**? click [here](#).

- **Title:** Beginners Introduction to the Assembly Language of ATMEL-AVR-Microprocessors
- **Author(s):** Gerhard Schmidt (2011)
- **Publisher:** Unknown
- **Paperback:** N/A
- **eBook:** PDF (81 pages, 3.2 MB)
- **Language:** English
- **ISBN-10:** N/A
- **ISBN-13:** N/A
- **Share This:**



## Book Description

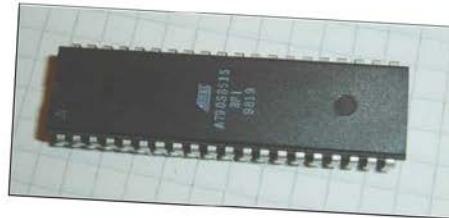
This book features a step-by-step approach in covering Assembly language programming of Atmel AVR microcontrollers. It offers a systematic approach in programming and interfacing of the Atmel AVR with LCD, keyboard, ADC, DAC, Sensors, Serial Ports, Timers, DC and Stepper Motors, Opto-isolators, and RTC. Assembly languages are used in all the peripherals programming.

## About the Authors

- N/A

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[www.avr-asm-download.de/beginner\\_en.pdf](http://www.avr-asm-download.de/beginner_en.pdf)



**Beginners Introduction to the  
Assembly Language of  
ATMEL-AVR-Microprocessors**

*by*

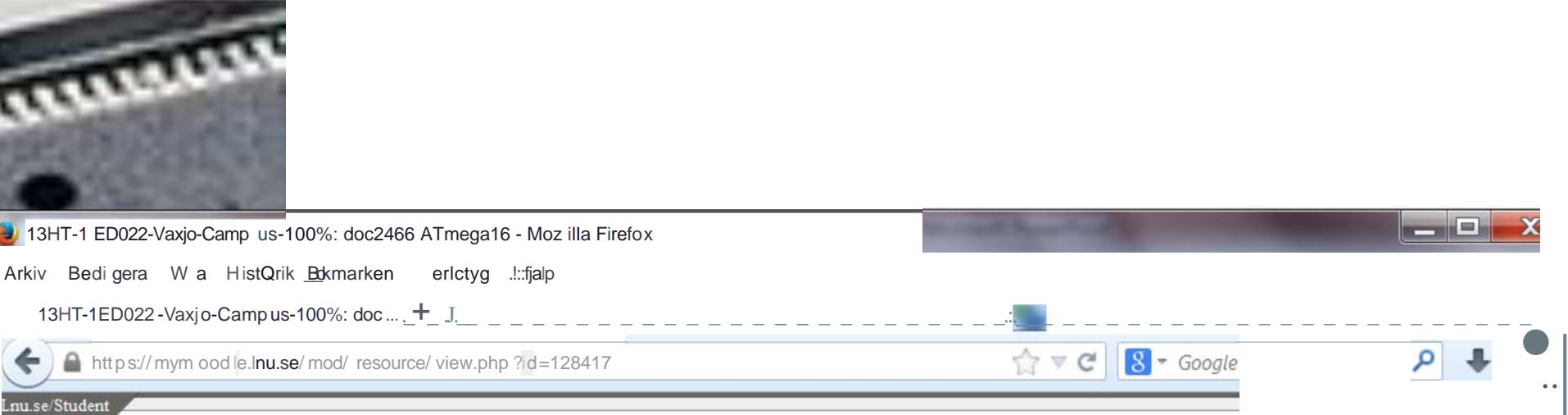
*Gerhard Schmidt*

<http://www.avr-asm-tutorial.net>

*May 2016*

**History:**

Corrected a calculation error in May 2016  
Added page on assembler concept in February 2011  
Added chapter on code structures in April 2009  
Additional corrections and updates as of January 2008  
Corrected version as of July 2006  
Original version as of December 2003



# doc2466\_ATmega16

doc2466\_ATmega16.pdf (SKYDDAD) - Adobe Acrobat Pro

Arkiv Redigera Visa Fönster Hjälp

Skapa | 1 / 354 | Verktyg Kommentar Dela

Bokmärken

Features

- High-performance, Low-power AVR® 8-bit Microcontroller
- Advanced RISC Architecture
  - 131 Powerful Instructions – Most Single-clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 16 MIPS Throughput at 16 MHz
  - On-chip 2-cycle Multiplier
- High Endurance Non-volatile Memory segments
  - 16K Bytes of In-system Self-programmable Flash program memory
  - 512 Bytes EEPROM
  - 4 Kbytes Internal SRAM
- Write/Erase Cycles: 10,000 Flash/100,000 EEPROM
- Data retention: 20 years at 85°C/100 years at 25°C
- Optional Boot Code Section with Independent Lock Bits
- In-System Programming by On-chip Boot Program
- True Read-While-Write Operation
- Programming Lock for Software Security
- JTAG (IEEE std. 1149.1 Compliant) Interface
  - Boundary-scan Capabilities According to the JTAG Standard
  - Extensive On-chip Debug Support
  - Programming of Flash, EEPROM, Fuses, and Lock Bits through the JTAG Interface
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescalers and Compare Modes
  - One 16-bit Timer/COUNTER with Separate Prescaler, Compare Mode, and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Four PWM Channels
  - One 10-bit ADC
  - 8 Single-ended Channels
  - 7 Differential Channels in TQFP Package Only
  - 2 Differential Channels with Programmable Gain at 1x, 10x, or 200x
  - Byte-oriented Two-wire Serial Interface
  - Programmable Serial USART
  - Master/Slave SPI Serial Interface
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated RC Oscillator
  - External and Internal Interrupt Sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby and Extended Standby
  - I/O and Packages
    - 32 Programmable I/O Lines
    - 40-pin TDF, 44-pin TQFP, and 44-pin QFNMLF
- Operating Voltages
  - 2.7...5V for ATmega16L
  - 4.5...5.5V for ATmega16
- Speed Grades
  - 0...8 MHz for ATmega16L
  - 0...16 MHz for ATmega16
- Power Consumption @ 1 MHz, 3V, and 25°C for ATmega16L
  - Active: 1.1 mA
  - Idle Mode: 0.35 mA
  - Power-down Mode: < 1 µA



# Lars Karlsson

Business Sector : industry, medical,  
military.

1991.

Software Engineer.

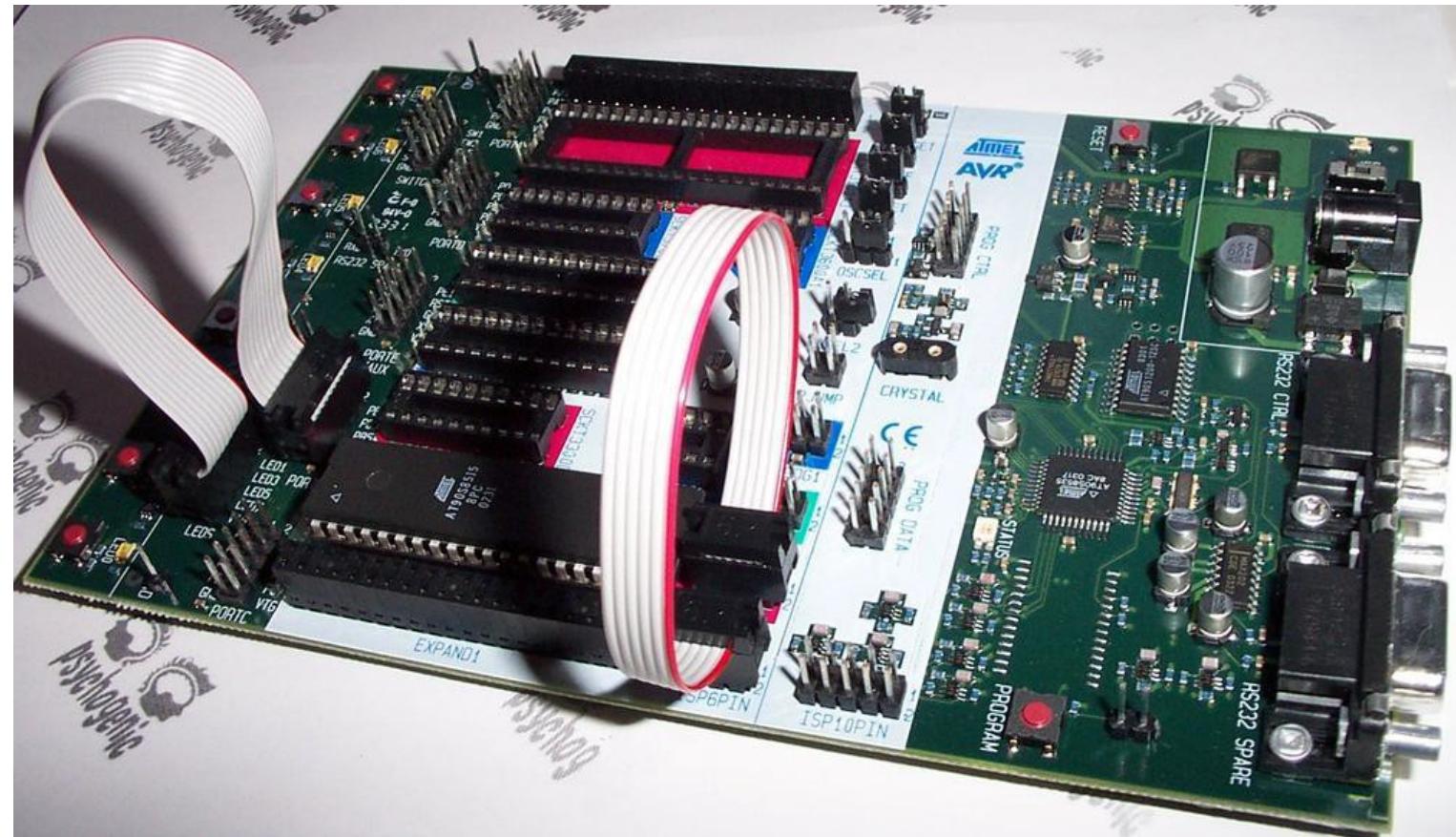
(And sometimes teaching at LNU,  
BTH)

Register!

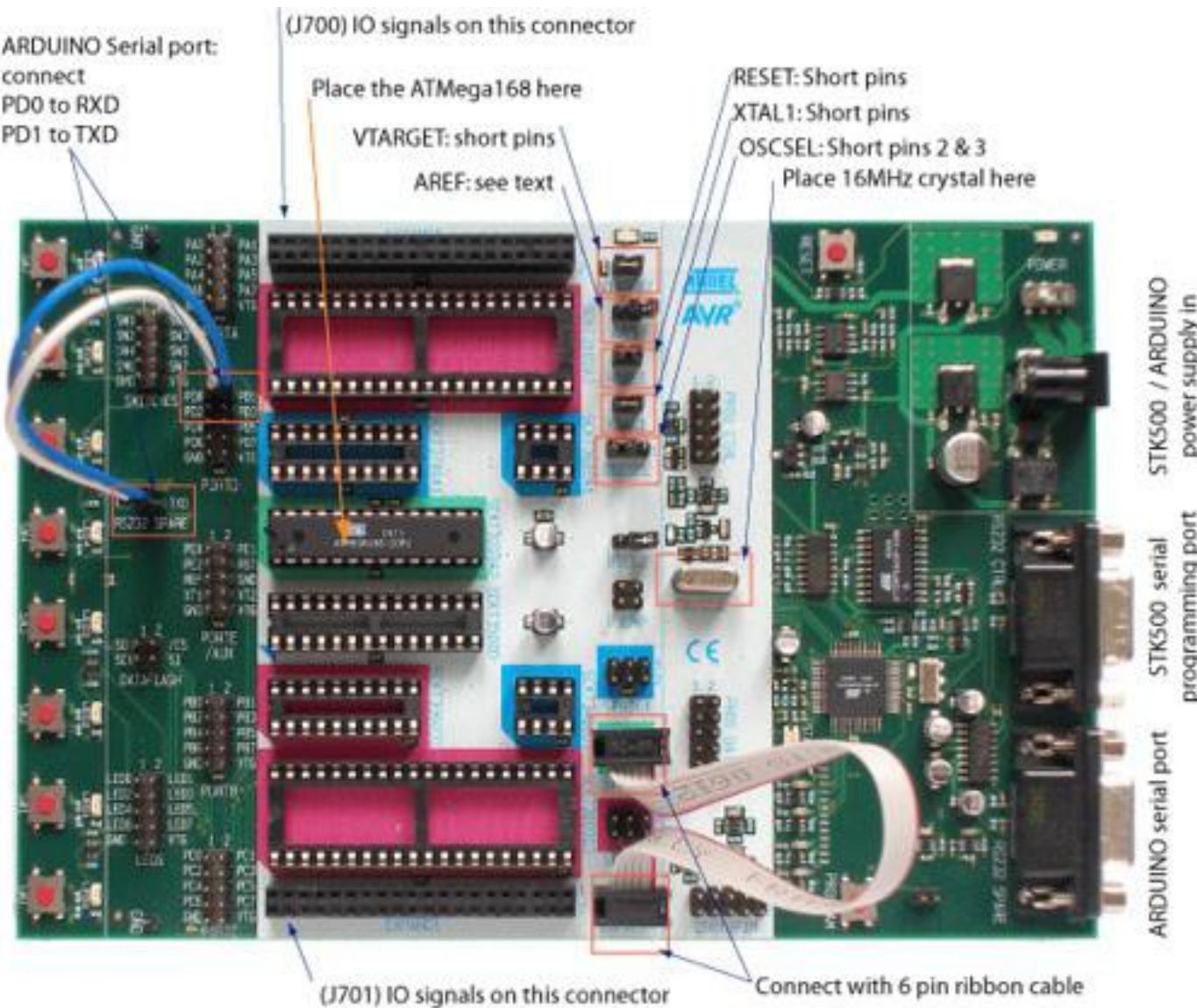


Register.

# STK500



# STK 500



# STK 600



# Examples of systems with digital inputs and outputs



# Examples of systems with digital inputs and outputs





# Examples of systems with digital inputs and outputs

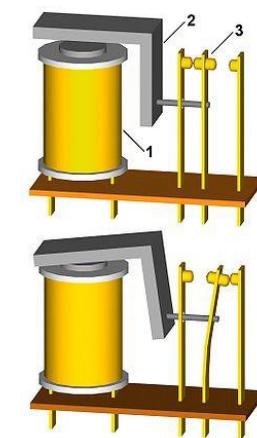


# Examples of systems with digital inputs and outputs



# Lecture, November 6, 2012

## Digital Input/Output

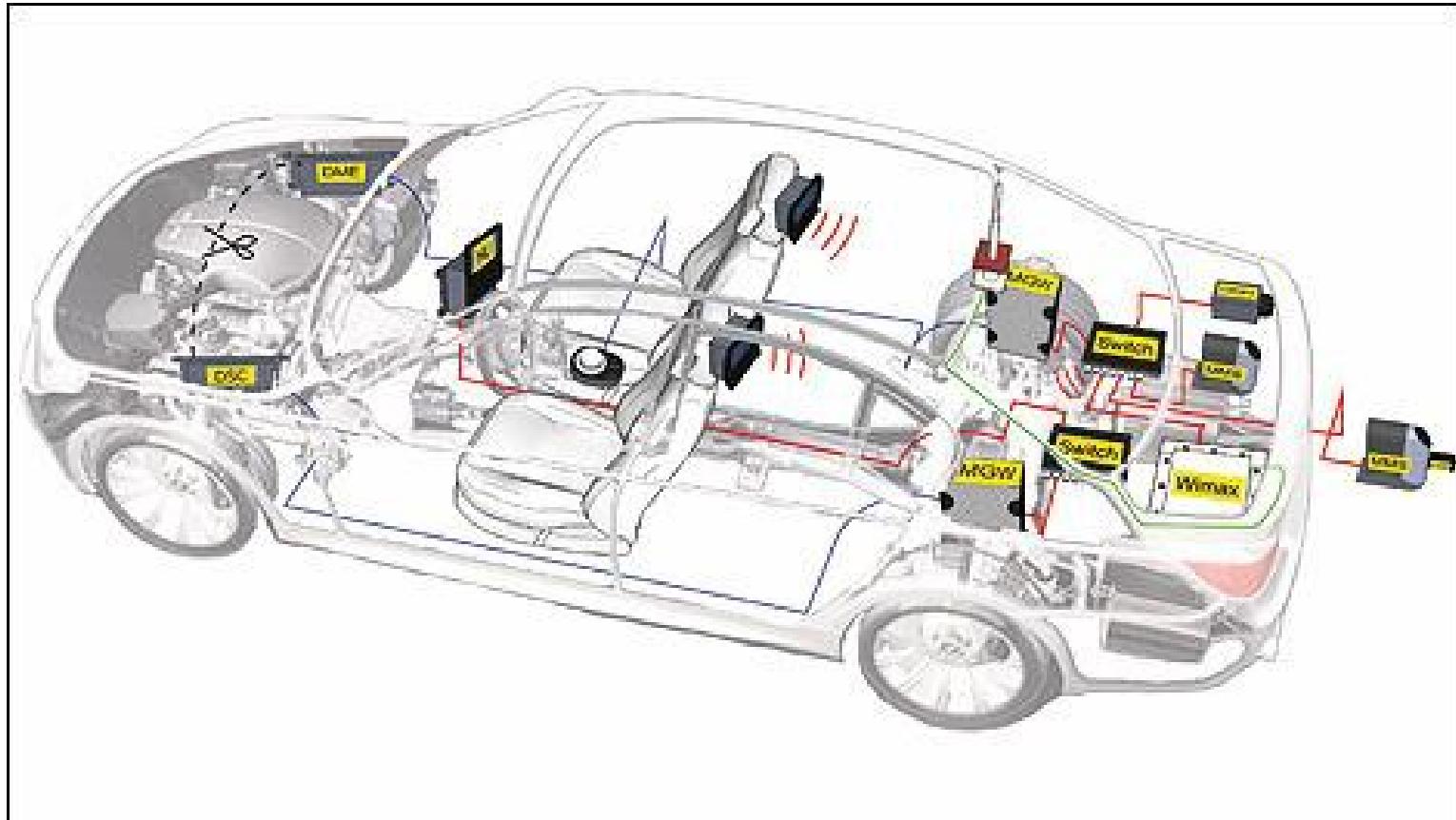


## **Comfort & Convenience**

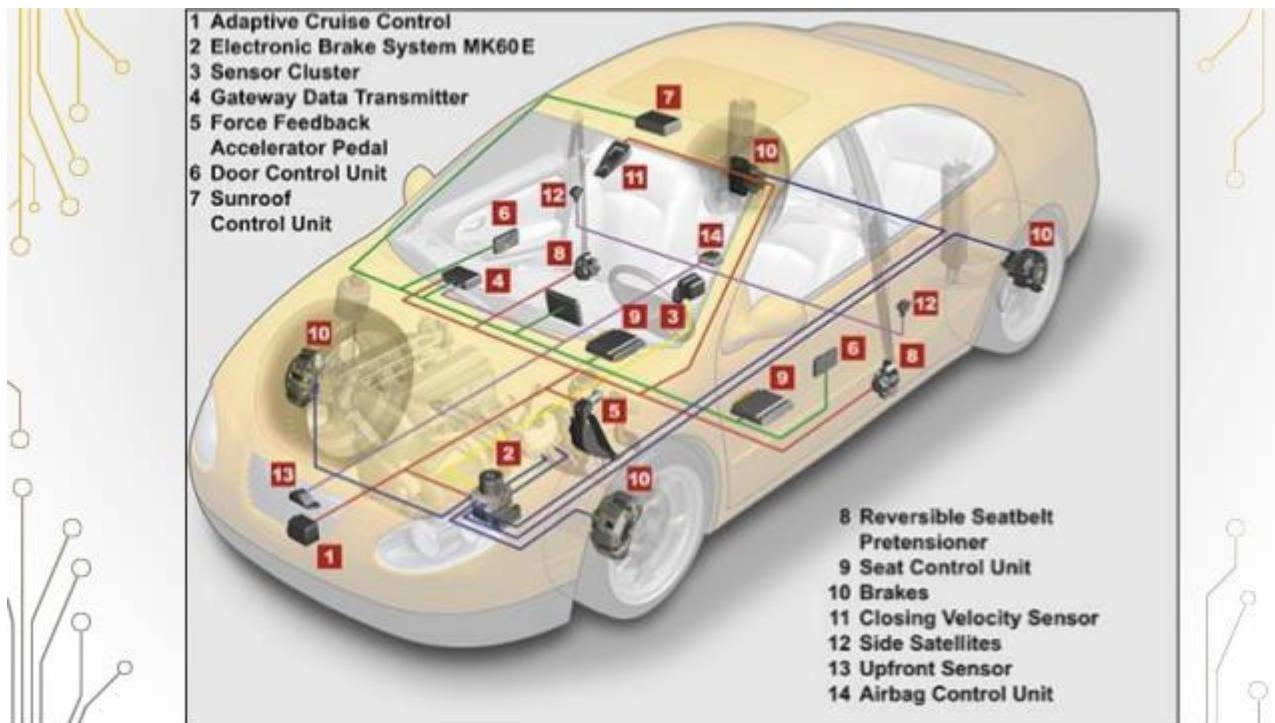


## **Driver Assistance System**

# Cars



# Cars





# Documentation:

- ATMega 16, 8-bit Microcontroller
- 8 –bit AVR Instruction Set
- AVR An Introductory Course, John Morton
- Mikroprocessorteknik, Per Foyer

# ATMega 16, 8-bit Microcontroller

---

## Features

- High-performance, Low-power Atmel® AVR® 8-bit Microcontroller
- Advanced RISC Architecture
  - 131 Powerful Instructions – Most Single-clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 16 MIPS Throughput at 16 MHz
  - On-chip 2-cycle Multiplier
- High Endurance Non-volatile Memory segments
  - 16 Kbytes of In-System Self-programmable Flash program memory
  - 512 Bytes EEPROM
  - 1 Kbyte Internal SRAM
  - Write/Erase Cycles: 10,000 Flash/100,000 EEPROM
  - Data retention: 20 years at 85°C/100 years at 25°C<sup>(1)</sup>
  - Optional Boot Code Section with Independent Lock Bits
  - In-System Programming by On-chip Boot Program
  - True Read-While-Write Operation
  - Programming Lock for Software Security
- JTAG (IEEE std. 1149.1 Compliant) Interface
  - Boundary-scan Capabilities According to the JTAG Standard
  - Extensive On-chip Debug Support
  - Programming of Flash, EEPROM, Fuses, and Lock Bits through the JTAG Interface
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescalers and Compare Modes
  - One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Four PWM Channels
  - 8-channel, 10-bit ADC
    - 8 Single-ended Channels
    - 7 Differential Channels in TQFP Package Only
    - 2 Differential Channels with Programmable Gain at 1x, 10x, or 200x
  - Byte-oriented Two-wire Serial Interface
  - Programmable Serial USART
  - Master/Slave SPI Serial Interface
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
- Special Microcontroller Features



---

8-bit **AVR®**  
Microcontroller  
with 16K Bytes  
In-System  
Programmable  
Flash

---

**ATmega16**  
**ATmega16L**

# 8-bit AVR Instruction Set

---

## Instruction Set Nomenclature

### **Status Register (SREG)**

- SREG: Status Register  
C: Carry Flag  
Z: Zero Flag  
N: Negative Flag  
V: Two's complement overflow indicator  
S:  $N \oplus V$ , For signed tests  
H: Half Carry Flag  
T: Transfer bit used by BLD and BST instructions  
I: Global Interrupt Enable/Disable Flag

### **Registers and Operands**

- Rd: Destination (and source) register in the Register File  
Rr: Source register in the Register File  
R: Result after instruction is executed  
K: Constant data  
k: Constant address  
b: Bit in the Register File or I/O Register (3-bit)  
s: Bit in the Status Register (3-bit)  
X,Y,Z: Indirect Address Register  
(X=R27:R26, Y=R29:R28 and Z=R31:R30)  
A: I/O location address

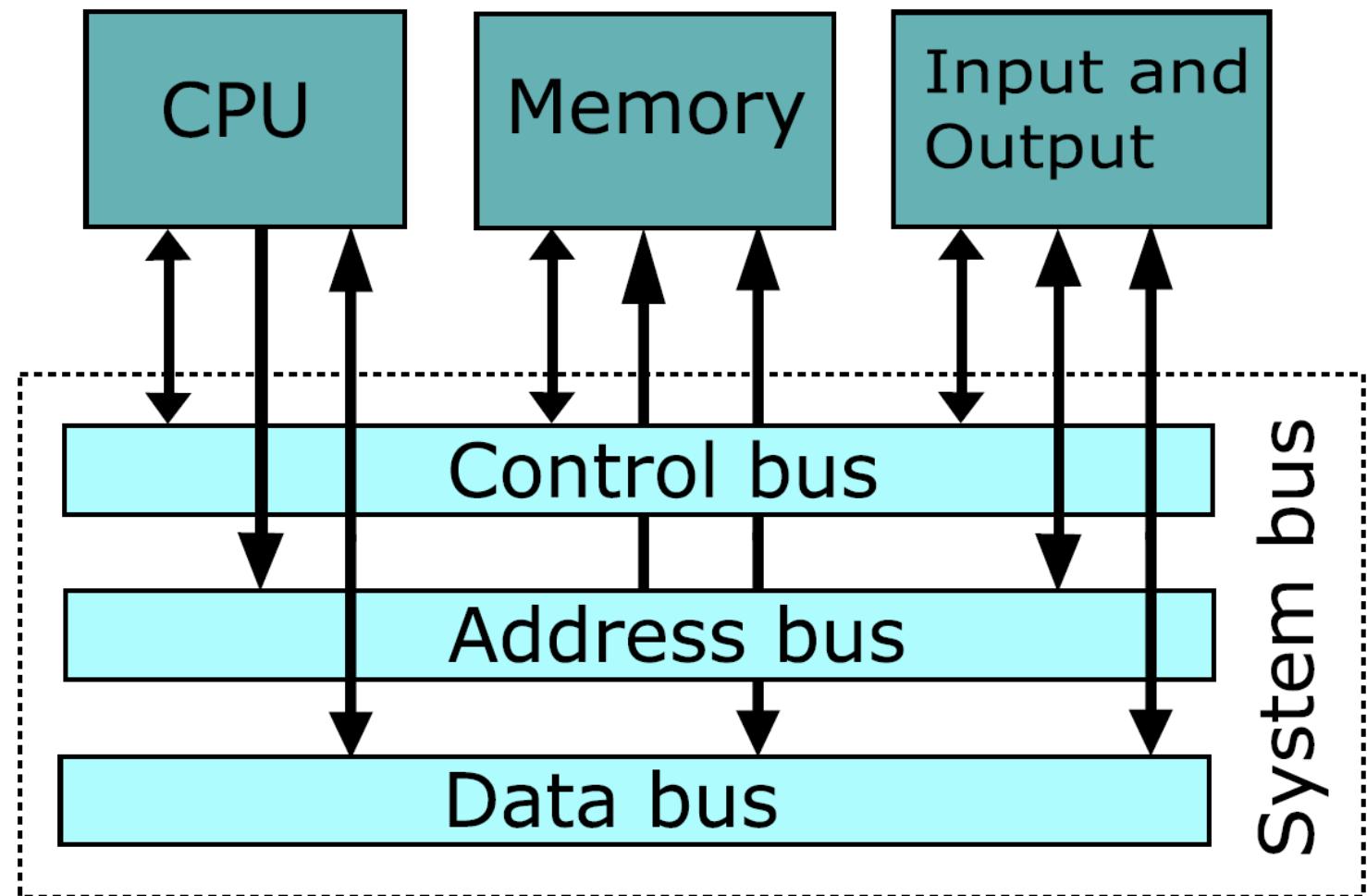


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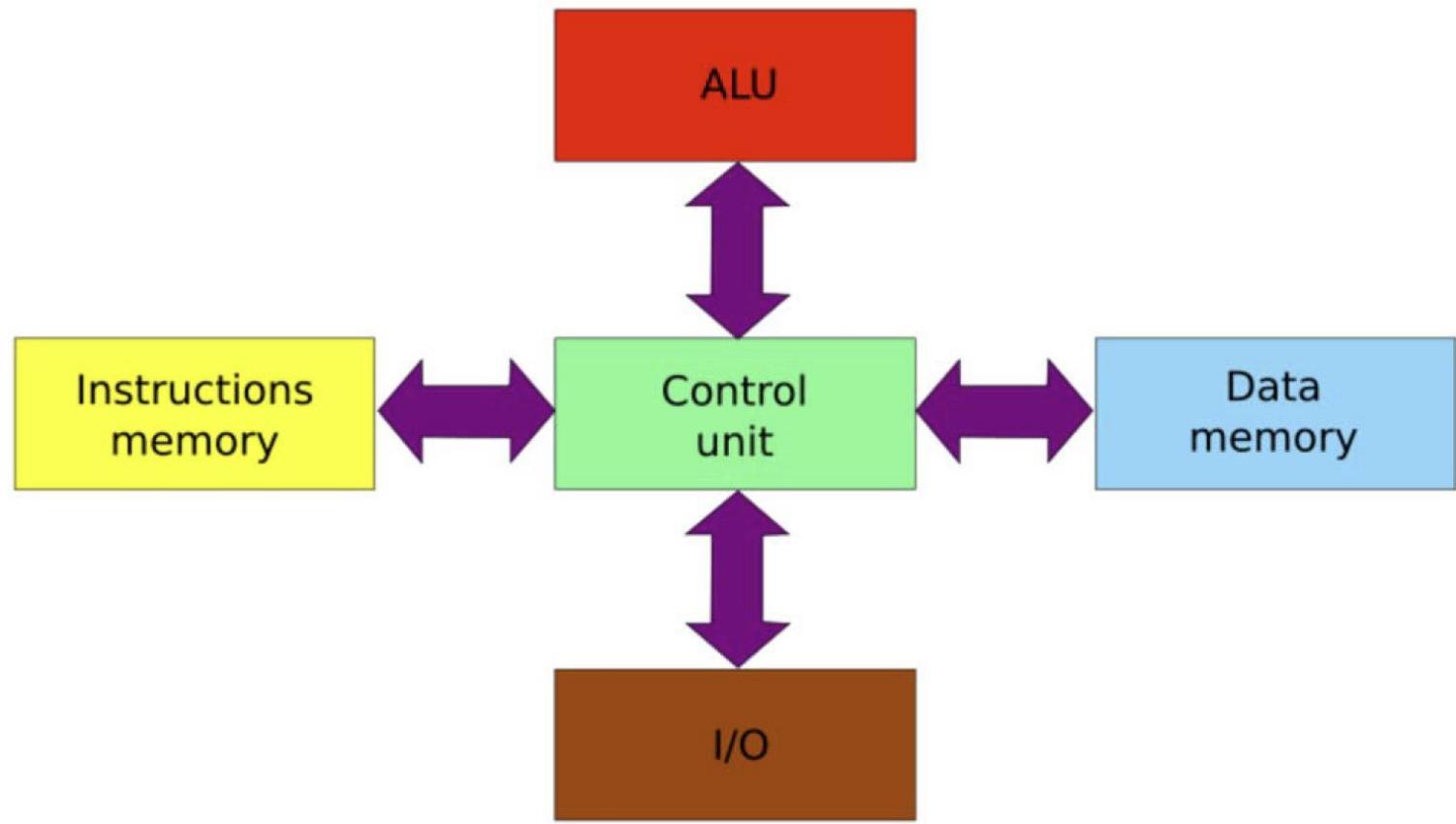
**8-bit AVR®  
Instruction Set**

---

# Von Neumann architecture:



# Harvard architecture:



# Binary and hexadecimal numbers.

0001 1110 1101 0000 0010 0001

$$0 * 2^{23} + 0 * 2^{22} + 0 * 2^{21} + 1 * 2^{20} + 1 * 2^{19} + 1 * 2^{18} + 1 * 2^{17} + 0 * 2^{16} + \dots$$

1 E D 0 2 1

$$* 16^5 + 14 * 16^4 + 13 * 16^3 + 0 * 16^2 + 2 * 16^1 + 1 * 16^0 =$$

$$1 * 1048576 + 14 * 65536 + 13 * 4096 + 0 * 256 + 2 * 16 + 1 * 1 = \\ 2\ 019\ 361_{10}$$

# Hexadecimal numbers.

<http://en.wikipedia.org/wiki/Hexadecimal>

The screenshot shows a web browser window with the URL <http://en.wikipedia.org/wiki/Hexadecimal> in the address bar. The page content is the Wikipedia article on Hexadecimal numbers. The sidebar on the left includes links to Main page, Contents, Featured content, Current events, Random article, Donate to Wikipedia, and Wikimedia Shop. The right sidebar contains sections for Numerical systems by culture, Hindu-Arabic origins, East Asian, Alphabetic, and Former. The main article text explains the hexadecimal system, its conversion to decimal, and its use in computing.

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Hexadecimal

From Wikipedia, the free encyclopedia

In mathematics and computing, **hexadecimal** (also **base 16**, or **hex**) is a positional numeral system with a radix, or base, of 16. It uses sixteen distinct symbols, most often the symbols 0–9 to represent values zero to nine, and A, B, C, D, E, F (or alternatively a–f) to represent values ten to fifteen. Hexadecimal numerals are widely used by computer systems designers and programmers. In computing, hexadecimal numerals are usually written with a prefix, "0x" (in reference to the abbreviated pronunciation of "hexadecimal"). Alternately, some authors denote hexadecimal values using a suffix or subscript. For example, one could write 0x2AF3 or 2AF3<sub>16</sub>, depending on the choice of notation.

As an example, the hexadecimal number 2AF3<sub>16</sub> can be converted to an equivalent decimal representation. Observe that 2AF3<sub>16</sub> is equal to a sum of (2000<sub>16</sub> + A00<sub>16</sub> + F0<sub>16</sub> + 3<sub>16</sub>), by decomposing the numeral into a series of place value terms. Converting each term to decimal, one can further write: (2<sub>16</sub> × 16<sup>3</sup>) + (A<sub>16</sub> × 16<sup>2</sup>) + (F<sub>16</sub> × 16<sup>1</sup>) + (3<sub>16</sub> × 16<sup>0</sup>), (2 × 4096) + (10 × 256) + (15 × 16) + (3 × 1), or 10995.

Each hexadecimal digit represents four binary digits (**bits**), and the primary use of hexadecimal notation is a human-friendly representation of **binary-coded** values in computing and digital electronics. One hexadecimal digit represents a **nibble**, which is half of an **octet** or byte (8 bits). For example, **byte** values can range from 0 to 255 (decimal), but may be more conveniently represented as two hexadecimal digits in the range 00 to FF. Hexadecimal is also commonly used to represent computer **memory addresses**.

Contents [hide]

1 Representation

1.1 Written representation

Numerical systems by culture

Hindu–Arabic origins

Indian (Bengali · Tamil · Telugu)  
Eastern Arabic · Western Arabic  
Burmese · Khmer · Lao · Mongolian · Sinhala · Thai

East Asian

Chinese (Suzhou) · Japanese · Korean · Vietnamese  
Counting rods

Alphabetic

Abjad · Armenian · Āryabhaṭa · Cyrillic · Ge'ez · Georgian · Greek · Hebrew · Roman

Former

Aegean · Attic · Babylonian · Brahmi · Egyptian · Etruscan · Inuit · Kharosthi · Mayan · Quipu · Prehistoric

# Two's complement.

[http://en.wikipedia.org/wiki/Two%27s\\_complement](http://en.wikipedia.org/wiki/Two%27s_complement)

Arkiv Redigera Visa Histgrik Bokmärken Verktyg Hjälp

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**Two's complement**

From Wikipedia, the free encyclopedia

**Two's complement** is a mathematical operation on binary numbers, as well as a binary signed number representation based on this operation. Its wide use in computing makes it the most important example of a radix complement.

The two's complement of an  $N$ -bit number is defined as the complement with respect to  $2^N$ ; in other words, it is the result of subtracting the number from  $2^N$ , which in binary is one followed by  $N$  zeroes. This is also equivalent to taking the ones' complement and then adding one, since the sum of a number and its ones' complement is all 1 bits. The two's complement of a number behaves like the negative of the original number in most arithmetic, and positive and negative numbers can coexist in a natural way.

In two's-complement representation, positive numbers are simply represented as themselves, and negative numbers are represented by the two's complement of their absolute value;<sup>[1]</sup> the table on the right provides an example for  $N = 8$ . In general, negation (reversing the sign) is performed by taking the two's complement. This system is the most common method of representing signed integers on computers.<sup>[2]</sup> An  $N$ -bit two's-complement numeral system can represent every integer in the range  $-(2^{N-1})$  to  $+(2^{N-1} - 1)$  while ones' complement can only represent integers in the range  $-(2^{N-1} - 1)$  to  $+(2^{N-1} - 1)$ .

The two's-complement system has the advantage that the fundamental arithmetic operations of addition, subtraction, and multiplication are identical to those for unsigned binary numbers (as long as the inputs are represented in the same number of bits and any overflow beyond those bits is discarded from the result). This property makes the system both simpler to implement and capable of easily handling higher precision arithmetic. Also, zero has only a single representation, obviating the subtleties associated with negative zero, which exists in ones'-complement systems.

**8-bit two's-complement integers**

Bits	Unsigned value	2's complement value
0111 1111	127	127
0111 1110	126	126
0000 0010	2	2
0000 0001	1	1
0000 0000	0	0
1111 1111	255	-1
1111 1110	254	-2
1000 0010	130	-126
1000 0001	129	-127
1000 0000	128	-128

Contents [hide]

1 Potential ambiguities of terminology

# doc2549\_ATmega2560

## ATMega2560, 8-bit Microcontroller

### Features

- High Performance, Low Power Atmel® AVR® 8-Bit Microcontroller
- Advanced RISC Architecture
  - 135 Powerful Instructions – Most Single Clock Cycle Execution
  - 32 × 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 16 MIPS Throughput at 16MHz
  - On-Chip 2-cycle Multiplier
- High Endurance Non-volatile Memory Segments
  - 64K/128K/256KBytes of In-System Self-Programmable Flash
  - 4Kbytes EEPROM
  - 8Kbytes Internal SRAM
  - Write/Erase Cycles: 10,000 Flash/100,000 EEPROM
  - Data retention: 20 years at 85°C/ 100 years at 25°C
  - Optional Boot Code Section with Independent Lock Bits
    - In-System Programming by On-chip Boot Program
    - True Read-While-Write Operation
  - Programming Lock for Software Security
    - Endurance: Up to 64Kbytes Optional External Memory Space
- Atmel® QTouch® library support
  - Capacitive touch buttons, sliders and wheels
  - QTouch and QMatrix acquisition
  - Up to 64 sense channels
- JTAG (IEEE std. 1149.1 compliant) Interface
  - Boundary-scan Capabilities According to the JTAG Standard
  - Extensive On-chip Debug Support
  - Programming of Flash, EEPROM, Fuses, and Lock Bits through the JTAG Interface
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescaler and Compare Mode
  - Four 16-bit Timer/Counter with Separate Prescaler, Compare- and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Four 8-bit PWM Channels
  - Six/Twelve PWM Channels with Programmable Resolution from 2 to 16 Bits (ATmega1281/2561, ATmega640/1280/2560)
  - Output Compare Modulator
  - 8/16-channel, 10-bit ADC (ATmega1281/2561, ATmega640/1280/2560)
  - Two/Four Programmable Serial USART (ATmega1281/2561, ATmega640/1280/2560)
  - Master/Slave SPI Serial Interface
  - Byte Oriented 2-wire Serial Interface
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
  - Interrupt and Wake-up on Pin Change
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated Oscillator
  - External and Internal Interrupt Sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby, and Extended Standby
- I/O and Packages
  - 54/86 Programmable I/O Lines (ATmega1281/2561, ATmega640/1280/2560)
  - 64-pad QFN/MLF, 64-lead TQFP (ATmega1281/2561)
  - 100-lead TQFP, 100-ball CBGA (ATmega640/1280/2560)
  - RoHS/Fully Green



8-bit Atmel  
Microcontroller  
with  
64K/128K/256K  
Bytes In-System  
Programmable  
Flash

ATmega640/V  
ATmega1280/V  
ATmega1281/V  
**ATmega2560/V**  
ATmega2561/V

Preliminary

# 8-bit AVR Instruction Set

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## Instruction Set Nomenclature

### **Status Register (SREG)**

- SREG: Status Register  
C: Carry Flag  
Z: Zero Flag  
N: Negative Flag  
V: Two's complement overflow indicator  
S:  $N \oplus V$ , For signed tests  
H: Half Carry Flag  
T: Transfer bit used by BLD and BST instructions  
I: Global Interrupt Enable/Disable Flag

### **Registers and Operands**

- Rd: Destination (and source) register in the Register File  
Rr: Source register in the Register File  
R: Result after instruction is executed  
K: Constant data  
k: Constant address  
b: Bit in the Register File or I/O Register (3-bit)  
s: Bit in the Status Register (3-bit)  
X,Y,Z: Indirect Address Register  
(X=R27:R26, Y=R29:R28 and Z=R31:R30)  
A: I/O location address



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**8-bit AVR®  
Instruction Set**

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# Architecture

Figure 2. Block Diagram

