REPORT

COURSE: CSE - 206
EXPERIMENT NO: 4
TOPIC: Flip-Flops and Registers

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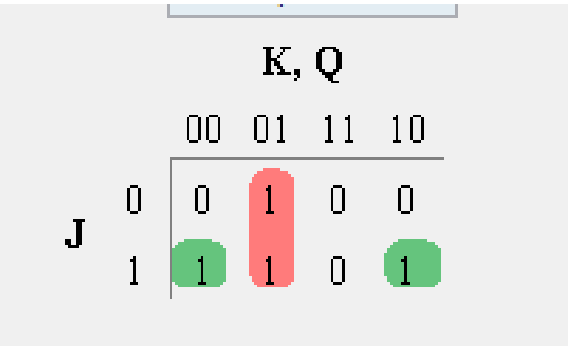
Problem - 1

Problem Specification:
Design and implement a master-slave JK flip-flop using only NAND gates.

Excitation Table:

J	K	Q_n	C	Q_{n+1}	Comment
0	0	0	⊓	0	Hold
0	0	1	⊓	1	
0	1	0	⊓	0	Reset
0	1	1	⊓	0	
1	0	0	⊓	1	Set
1	0	1	⊓	1	
1	1	0	⊓	1	Toggle
1	1	1	⊓	0	

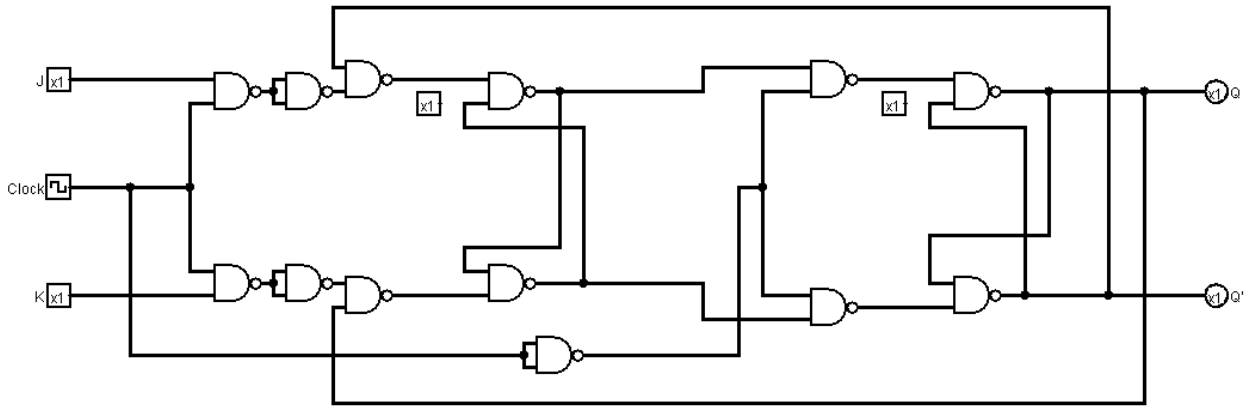
Truth Table and Function minimization:



So, the function is K'Q + JQ'

Required instruments:
(1) 3 input pins, (2) 2 output pins, (3) 1 IC7410 gate, (4) 2 IC7400 gates, (5) 1 clock, (6) 1 Power, (7) 3 Grounds, (8) Wires.

Circuit diagram:



Observations:

Here we see that two JK flip flops are used. It is to account for the continuous toggle of the output for 1 1 condition. Here the first flip flop is called master and the second one is called slave.
The circuit requires an initial value in some inputs of the slave part to work. So, we need to provide an initial value at first to achieve the expected circuit.

Problem - 2

Problem Specification:
Design and implement a 4-bit universal shift register.

Excitation Table:

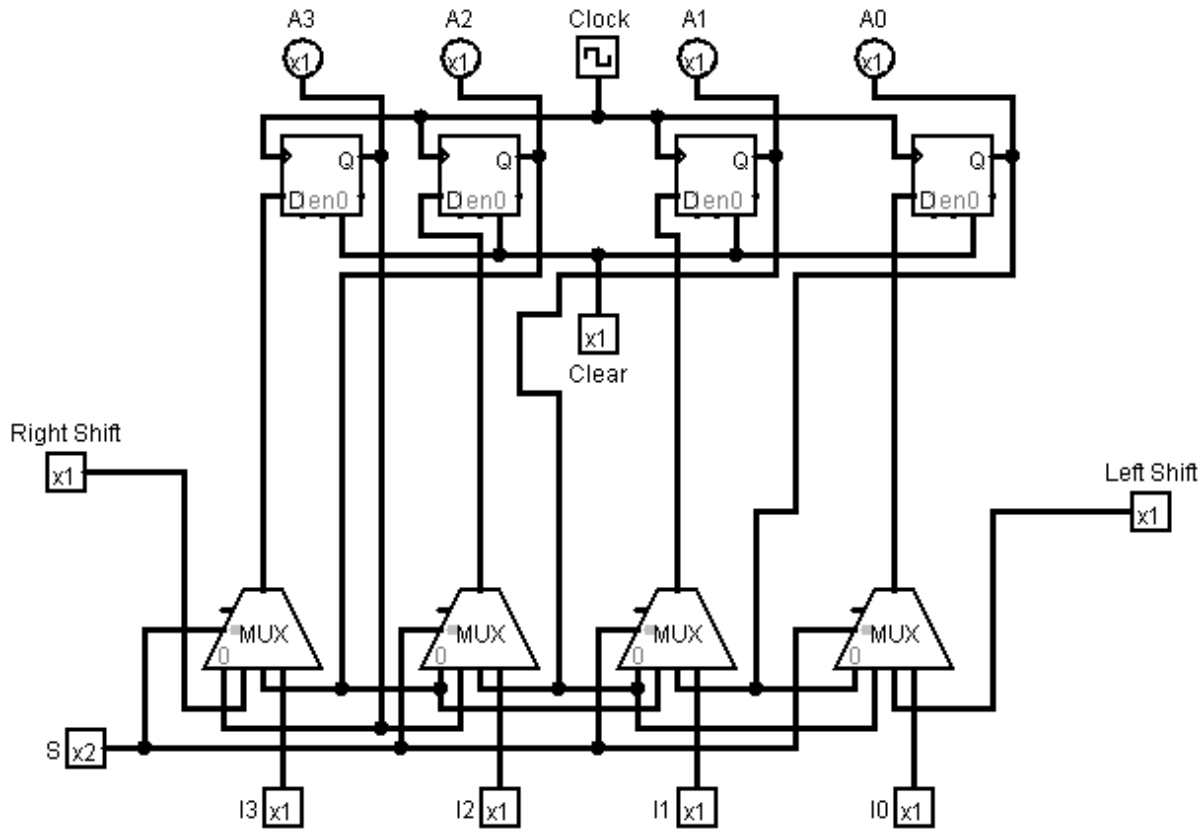
The following table explains the mode of operation of the universal shift register depending on the select bit inputs on every clock pulse:

Clear	Clock	S1	S0	A3	A2	A1	A0	Mode of Operation
1	X	X	X	0	0	0	0	Clear
0	X	0	0	A3	A2	A1	A0	No change
0	⊓	0	1	SR	A3	A2	A1	Right Shift
0	⊓	1	0	A2	A1	A0	SL	Left Shift
0	⊓	1	1	I3	I2	I1	I0	Parallel Loading

Required instruments:

(1) 9 input pins, (2) 4 output pins, (3) 2 IC7474 gates, (4) 1 IC7404 gate, (5) 2 IC 7408 gates, (6) 1 IC 7432 gate, (7) 1 clock input, (8) 1 Power, (9) 1 Ground, (10)Wires.

Circuit diagram:



Observations:

From the truth table, we see that whenever the input of select pins S1S0 is *00*, there is no change in the mode of operation. For *01* input combination, it indicates that the register will complete the right shift. Similarly, for the input combination *10*, the left shift operation will be performed. It is because a universal shift register does both the shift operations. For the input combination *11*, the provided bits will be loaded to the output pins parallely. It is to be noted that whenever the clear pins are ON/1, the output pins will be cleared. Moreover, whenever the clock pulse is absent, the output will be retained.