Batch-14th Class Test: 01 Department: CSE

Course Code: CSE-2215 Course Title: Digital Electronics and Pulse Technique

Full Marks: 15 Time: 30 minutes

Q. No.:		Marks	CO	PO	BL
1.	(a) How are the rise time and fall time of a pulse measured?	3	1	1	C1
	(b) Draw the truth table for a 2- input AND gate and show the output assuming two arbitrary input pulse trains.	5			C1
	(c) Convert J-K flip-flop to S-R flip-flop with necessary diagram.	7	2		C3

Class Test: 02 Department: CSE Batch: 14th

Course Code: CSE-2215 Course Title: Digital Electronics and Pulse Technique

Full Mark: 15 Time: 40 minutes

Q. No.:		Marks	CO	PO	BL
1.	(a). What are the advantages and disadvantages of a synchronous counter over an asynchronous counter?	3	2	2	C1
	(b). How many flip-flops are required for a counter that will count 0 to 511_{10} ? What is the MOD number of this counter?	2			C2
	(c). Design a synchronous counter that has the following sequence: 0,3,5,7	6			C3
	(d) Explain how the hour's section of a digital clock is implemented.	4			C2
	OR				
	Design a 3 bit asynchronous up-counter				C3

Class Test: 03 Department: CSE Batch: 14th

Course Code: CSE-2215 Course Title: Digital Electronics and Pulse Technique

Full Mark: 15 Time: 40 minutes

Q. No.:		Marks	CO	PO	BL
1.	(a).Explain how data are stored on a magnetic tape.	2	2	2	C2
	(b). What are advantages and disadvantages of magnetic tape?	2			C1
	(c). How many address inputs,data inputs are required for a 16Kx12 memory?	3			C3
	(d) Implement the following Boolean functions using PROM $F_0(x,y,z) = \sum m(1,2,4,6)$ $F_0(x,y,z) = \sum m(0,1,6,7)$ $F_0(x,y,z) = \sum m(2,6)$	8			C3

Class Test: 04 Department: CSE Batch: 14th

Course Code: CSE-2215 Course Title: Digital Electronics and Pulse Technique

Full Mark: 15 Time: 40 minutes

Q. No.:		Marks	CO	PO	BL
1	(a) Discuss the basic characteristics of ADCs in brief.	2	3	3	1
	(b) Explain how a flash ADC works.	4	3	3	2
	(c) For an R-2R ladder DAC, Calculate the analog output voltage for the digital input 0111.	6	3	3	3
	(d) Discuss the function of a sample- and- hold circuit .	3	3	3	2