LITERATURE REVIEW

SL. NO	TITLE	YEAR	TECHNOLOGY	DRAWBACKS	LINK
01	Advancing cryptographic security: a novel hybrid AES-RSA model with byte-level tokenization	Apr 16, 2024	• byte-level Byte-Pair Encoding (BPE) tokenizer. • RSA algorithm • Advanced Encryption Standard (AES).	• Increased Computational Overhead • Complexity in Key Management • Potential Vulnerabilities in Tokenization	[A]
02	Design and Implementation of Memory Controller for Byte Access from Data Memory for SoC's Devices	July, 2024	• System-on-Chip (SoC) Architecture. • Advanced eXtensible Interface (AXI). • Verilog and SystemVerilog UVM (Universal Verification Methodology).	• Limited Scalability in Multi-Processor Environments. • Limited Flexibility in Dynamic Environments • Verification and Validation Challenges	[B]
03	Optimizing Systems for Byte-Addressable NVM by Reducing Bit Flipping	Februar y, 2019	• Phase Change Memory (PCM). • XOR Linked Lists. • XOR Hash Tables. • XOR Red-Black Tree.	• PCM Write Endurance Power Consumption • Memory Allocation Overhead. • XOR Hash Tables, Complexity	[C]

04	**20nm High-density single-port and dual-port SRAMa with worldline-voltage-adjustments system for read/write assists**	**06 March 2014**	• **Wordline-Voltage-Adjustment System** • **On-Chip Voltage Regulator** • **Temperature Monitoring and Control** • **Temperature and Process Variation-Based Adjustmen**	• **Increased Complexity** • **Write/Read Disturb Issues in DP-SRAM** • **Timing Considerations**	**[D]**
05	**A 45-nm Single-port and Dual-port SRAM family with Robust Read/Write Stabilizing Circuitry under DVFS Environment.**	**01 August 2008**	• **Improved Wordline Suppression Circuitry** • **Negative Bitline Technique.** • **45nm CMOS Technology**	• **Process Variation Sensitivity** • **Complexity in Negative Bitline Implementation**	**[E]**