DRV2605L 2 to 5.2 V Haptic Driver for LRA and ERM With Effect Library and Smart-Loop Architecture

1 Features

- Flexible Haptic and Vibration Driver
  - LRA (Linear Resonance Actuator)
  - ERM (Eccentric Rotating Mass)
- I^2C-Controlled Digital Playback Engine
  - Waveform Sequencer and Trigger
  - Real-Time Playback Mode through I^2C
  - I^2C Dual-Mode Drive (Open and Closed Loop)
- Smart-Loop Architecture(1)
  - Automatic Overdrive and Braking
  - Automatic Resonance Tracking and Reporting (LRA Only)
  - Automatic Actuator Diagnostic
  - Automatic Level Calibration
  - Wide Support for Actuator Models
- Licensed Immersion TouchSense® 2200 features:
  - Integrated Immersion Effect Library
  - Audio-to-Vibe
- Drive Compensation Over Battery Discharge
- Wide Voltage Operation (2 V to 5.2 V)
- Efficient Differential Switching Output Drive
- PWM Input With 0% to 100% Duty-Cycle Control Range
- Hardware Trigger Input
- Fast Start-up Time
- 1.8 V Compatible, V_{DD}-Tolerant Digital Interface

(1) Patent pending control algorithm

2 Applications

- Mobile Phones and Tablets
- Watches and Wearable Technology
- Remote Controls, Mice, and Peripheral Devices
- Touch-Enabled Devices
- Industrial Human-Machine Interfaces
- Electronic Point of Sale (ePOS)

3 Description

The DRV2605L device is a low-voltage haptic driver which includes a haptic-effect library and provides a closed-loop actuator-control system for high-quality haptic feedback for ERM and LRA. This schema helps improve actuator performance in terms of acceleration consistency, start time, and brake time and is accessible through a shared I^2C compatible bus or PWM input signal.

The DRV2605L device offers a licensed version of TouchSense 2200 software from Immersion which eliminates the need to design haptic waveforms because the software includes over 100 licensed effects (6 ERM libraries and 1 LRA library) and audio-to-vibe features.

Additionally, the real-time playback mode allows the host processor to bypass the library playback engine and play waveforms directly from the host through I^2C.

The smart-loop architecture inside the DRV2605L device allows simple auto-resonant drive for the LRA as well as feedback-optimized ERM drive allowing for automatic overdrive and braking. This architecture creates a simplified input waveform interface as well as reliable motor control and consistent motor performance. The DRV2605L device also features automatic transition to an open-loop system in the event that an LRA actuator is not generating a valid back-EMF voltage. When the LRA generates a valid back-EMF voltage, the DRV2605L device automatically synchronizes with the LRA. The DRV2605L also allows for open-loop driving through the use of internally-generated PWM. Additionally, the audio-to-vibe mode automatically converts an audio input signal to meaningful tactile effects.

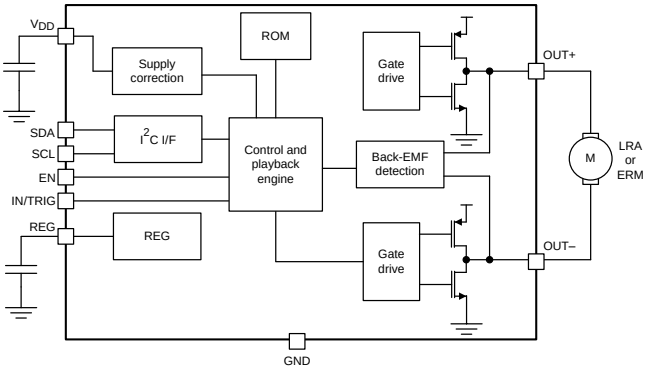
For an important notice regarding Immersion software, see the *Legal Notice* section.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (MAX)
DRV2605L	DSBGA (9)	1.50 mm × 1.50 mm
DRV2605L	VSSOP (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range, T_A = 25°C (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	V_{DD}	–0.3	5.5	V
	EN	–0.3	V_{DD} + 0.3	V
	SDA	–0.3	V_{DD} + 0.3	V
	SCL	–0.3	V_{DD} + 0.3	V
	IN/TRIG	–0.3	V_{DD} + 0.3	V
Operating free-air temperature range, T_A		–40	85	°C
Operating junction temperature range, T_J		–40	150	°C

6.2 Handling Ratings

					MIN	MAX	UNIT
T_{stg}	Storage temperature range				–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	DSBGA package, all pins		–1000	1000	V
			VSSOP package	OUT+, OUT–	–500	500	
				Other pins	–1000	1000	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins			–250	250	

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Supply voltage	V_{DD}	2	5.2	V
$f_{(PWM)}$	PWM input frequency	IN/TRIG Pin	10	250	kHz
Z_L	Load impedance	V_{DD} = 5.2 V	8		Ω
V_{IL}	Digital low-level input voltage	EN, IN/TRIG, SDA, SCL		0.5	V
V_{IH}	Digital high-level input voltage	EN, IN/TRIG, SDA, SCL	1.3		V
$V_{I(ANA)}$	Input voltage (analog mode)	IN/TRIG	0	1.8	V
$f_{(LRA)}$	LRA Frequency Range		125	300	Hz

6.4 Thermal Information

THERMAL METRIC(1)		DSBGA (9-PINS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	145.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	105	
ψ_{JT}	Junction-to-top characterization parameter	5.1	
ψ_{JB}	Junction-to-board characterization parameter	103.3	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics

T_A = 25°C, V_{DD} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(REG)}$	Voltage at the REG pin			1.83		V
I_{IL}	Digital low-level input current	EN, IN/TRIG, SDA, SCL V_{DD} = 5.2 V , V_I = 0 V			1	µA
I_{IH}	Digital high-level input current	IN/TRIG, SDA, SCL V_{DD} = 5.2 V, V_I = V_{DD}			1	µA
		EN V_{DD} = 5.2 V, V_I = V_{DD}			3.5	
V_{OL}	Digital low-level output voltage	$SDAI_{OL}$= 4 mA			0.4	V
$R_{(EN-GND)}$	Digital pull-down resistance	EN V_{DD} = 5.2 V , V_I = V_{DD}		2		MΩ
$I_{(SD)}$	Shutdown current	$V_{(EN)}$ = 0 V		4	7	µA
$I_{I(standby)}$	Standby current	$V_{(EN)}$ = 1.8 V, STANDBY = 1		4.1	7	µA
I_Q	Quiescent current	$V_{(EN)}$ = 1.8 V, STANDBY = 0, no signal		0.5	0.65	mA
Z_I	Input impedance	IN/TRIG to $V_{(CM\_ANA)}$		100		kΩ
$V_{(CM\_ANA)}$	IN/TRIG common-mode voltage (AC-coupled)	AC_COUPLE = 1		0.9		V
$Z_{O(SD)}$	Output impedance in shutdown	OUT+ to GND, OUT– to GND		15		kΩ
$Z_{L(th)}$	Load impedance threshold for over-current detection	OUT+ to GND, OUT– to GND		4		Ω
$I_{(BAT\_AV)}$	Average battery current during operation	Duty cycle = 90%, LRA mode, no load		2.4	3.5	mA
		Duty cycle = 90%, ERM mode, no load		2.3	3.5	

6.6 Timing Requirements

T_A = 25°C, V_{DD} = 3.6 V (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$f_{(SCL)}$	Frequency at the SCL pin with no wait states				400	kHz
$t_{w(H)}$	Pulse duration, SCL high	See Figure 1.	0.6			µs
$t_{w(L)}$	Pulse duration, SCL low		1.3			µs
$t_{su(1)}$	Setup time, SDA to SCL		100			ns
$t_{h(1)}$	Hold time, SCL to SDA		10			ns
$t_{(BUF)}$	Bus free time between stop and start condition	See Figure 2.	1.3			µs
$t_{su(2)}$	Setup time, SCL to start condition		0.6			µs
$t_{h(2)}$	Hold time, start condition to SCL		0.6			µs
$t_{su(3)}$	Setup time, SCL to stop condition		0.6			µs

6.7 Switching Characteristics

T_A = 25°C, V_{DD} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(start)}$	Start-up time	Time from the GO bit or external trigger command to output signal		0.7		ms
		Time from EN high to output signal (PWM/Analog Modes)		1.5		
$f_{O(PWM)}$	PWM Output Frequency		19.5	20.5	21.5	kHz

Programming (continued)

8.5.2.2 Overdrive Voltage-Clamp Programming

During closed-loop operation, the actuator feedback allows the output voltage go above the rated voltage during the automatic overdrive and automatic braking periods. The OD_CLAMP[7:0] bit (in Register 0x17) sets a clamp so that the automatic overdrive is bounded. The OD_CLAMP[7:0] bit also serves as the full-scale reference voltage for open-loop operation. The OD_CLAMP[7:0] bit always represents the maximum *peak voltage* that is allowed, regardless of the mode.

NOTE

If the supply voltage (V_{DD}) is less than the overdrive clamp voltage, the output driver is unable to reach the clamp voltage value because the output voltage cannot exceed the supply voltage. If the rated voltage exceeds the overdrive clamp voltage, the overdrive clamp voltage has priority over the rated voltage.

In ERM mode, use Equation 8 to calculate the allowed maximum voltage. In LRA mode, use Equation 9 to calculate the maximum peak voltage.

$$V_{(ERM\_clamp)} = \frac{21.64 \times 10^{-3} \times OD\_CLAMP[7:0] \times (t_{(DRIVE\_TIME)} - 300 \times 10^{-6})}{t_{(DRIVE\_TIME)} + t_{(IDISS\_TIME)} + t_{(BLANKING\_TIME)}} \quad (8)$$

$$V_{(LRA\_clamp)} = 21.22 \times 10^{-3} \times OD\_CLAMP[7:0] \quad (9)$$

8.5.3 I²C Interface

8.5.3.1 General I²C Operation

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. The bus transfers data serially, one bit at a time. The 8-bit address and data bytes are transferred with the most-significant bit (MSB) first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data pin (SDA) while the clock is at logic high to indicate start and stop conditions. A high-to-low transition on the SDA signal indicates a start, and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. Figure 20 shows a typical sequence. The master device generates the 7-bit slave address and the read-write (R/W) bit to start communication with a slave device. The master device then waits for an acknowledge condition. The slave device holds the SDA signal low during the acknowledge clock period to indicate acknowledgment. When this acknowledgment occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus a R/W bit (1 byte). All compatible devices share the same signals through a bidirectional bus using a wired-AND connection.

The number of bytes that can be transmitted between start and stop conditions is not limited. When the last word transfers, the master generates a stop condition to release the bus. Figure 20 shows a generic data-transfer sequence.

Use external pullup resistors for the SDA and SCL signals to set the logic-high level for the bus. Pullup resistors with values between 660 Ω and 4.7 kΩ are recommended. Do not allow the SDA and SCL voltages to exceed the DRV2605L supply voltage, V_{DD}.

NOTE

The DRV2605L slave address is 0x5A (7-bit), or 1011010 in binary.

12 Device and Documentation Support

12.1 Device Support

12.1.1 Legal Notice

In order to assist purchasers and users of TI's DRV2605L product, TI has paid a royalty on your behalf to Immersion Corporation to secure your rights to use certain Immersion Corporation software embedded (or designed specifically to be embedded) in TI's DRV2605L product solely as incorporated in TI's DRV2605L product, subject to the terms, conditions and restrictions of TI's license with Immersion Corporation. Subject to the terms, conditions and restrictions of TI's license with Immersion Corporation, you shall not (1) use or distribute any Immersion Corporation software incorporated in TI's DRV2605L product except as incorporated in TI's DRV2605L product in accordance with TI's applicable published specifications and data sheets for the DRV2605L product, (2) modify any Immersion software, (3) change or delete any Immersion proprietary notices, (4) reverse engineer or disassemble any Immersion software or otherwise attempt to discover the internal workings or design of any Immersion software, or (5) distribute Immersion software as a stand-alone basis.

12.1.2 Waveform Library Effects List

EFFECT ID NO.	WAVEFORM NAME	EFFECT ID NO>	WAVEFORM NAME	EFFECT ID NO.	WAVEFORM NAME
1	Strong Click - 100%	42	Long Double Sharp Click Medium 2 – 80%	83	Transition Ramp Up Long Smooth 2 – 0 to 100%
2	Strong Click - 60%	43	Long Double Sharp Click Medium 3 – 60%	84	Transition Ramp Up Medium Smooth 1 – 0 to 100%
3	Strong Click - 30%	44	Long Double Sharp Tick 1 – 100%	85	Transition Ramp Up Medium Smooth 2 – 0 to 100%
4	Sharp Click - 100%	45	Long Double Sharp Tick 2 – 80%	86	Transition Ramp Up Short Smooth 1 – 0 to 100%
5	Sharp Click - 60%	46	Long Double Sharp Tick 3 – 60%	87	Transition Ramp Up Short Smooth 2 – 0 to 100%
6	Sharp Click - 30%	47	Buzz 1 – 100%	88	Transition Ramp Up Long Sharp 1 – 0 to 100%
7	Soft Bump - 100%	48	Buzz 2 – 80%	89	Transition Ramp Up Long Sharp 2 – 0 to 100%
8	Soft Bump - 60%	49	Buzz 3 – 60%	90	Transition Ramp Up Medium Sharp 1 – 0 to 100%
9	Soft Bump - 30%	50	Buzz 4 – 40%	91	Transition Ramp Up Medium Sharp 2 – 0 to 100%
10	Double Click - 100%	51	Buzz 5 – 20%	92	Transition Ramp Up Short Sharp 1 – 0 to 100%
11	Double Click - 60%	52	Pulsing Strong 1 – 100%	93	Transition Ramp Up Short Sharp 2 – 0 to 100%
12	Triple Click - 100%	53	Pulsing Strong 2 – 60%	94	Transition Ramp Down Long Smooth 1 – 50 to 0%
13	Soft Fuzz - 60%	54	Pulsing Medium 1 – 100%	95	Transition Ramp Down Long Smooth 2 – 50 to 0%
14	Strong Buzz - 100%	55	Pulsing Medium 2 – 60%	96	Transition Ramp Down Medium Smooth 1 – 50 to 0%
15	750 ms Alert 100%	56	Pulsing Sharp 1 – 100%	97	Transition Ramp Down Medium Smooth 2 – 50 to 0%
16	1000 ms Alert 100%	57	Pulsing Sharp 2 – 60%	98	Transition Ramp Down Short Smooth 1 – 50 to 0%
17	Strong Click 1 - 100%	58	Transition Click 1 – 100%	99	Transition Ramp Down Short Smooth 2 – 50 to 0%
18	Strong Click 2 - 80%	59	Transition Click 2 – 80%	100	Transition Ramp Down Long Sharp 1 – 50 to 0%
19	Strong Click 3 - 60%	60	Transition Click 3 – 60%	101	Transition Ramp Down Long Sharp 2 – 50 to 0%
20	Strong Click 4 - 30%	61	Transition Click 4 – 40%	102	Transition Ramp Down Medium Sharp 1 – 50 to 0%
21	Medium Click 1 - 100%	62	Transition Click 5 – 20%	103	Transition Ramp Down Medium Sharp 2 – 50 to 0%
22	Medium Click 2 - 80%	63	Transition Click 6 – 10%	104	Transition Ramp Down Short Sharp 1 – 50 to 0%
23	Medium Click 3 - 60%	64	Transition Hum 1 – 100%	105	Transition Ramp Down Short Sharp 2 – 50 to 0%
24	Sharp Tick 1 - 100%	65	Transition Hum 2 – 80%	106	Transition Ramp Up Long Smooth 1 – 0 to 50%
25	Sharp Tick 2 - 80%	66	Transition Hum 3 – 60%	107	Transition Ramp Up Long Smooth 2 – 0 to 50%
26	Sharp Tick 3 – 60%	67	Transition Hum 4 – 40%	108	Transition Ramp Up Medium Smooth 1 – 0 to 50%
27	Short Double Click Strong 1 – 100%	68	Transition Hum 5 – 20%	109	Transition Ramp Up Medium Smooth 2 – 0 to 50%
28	Short Double Click Strong 2 – 80%	69	Transition Hum 6 – 10%	110	Transition Ramp Up Short Smooth 1 – 0 to 50%
29	Short Double Click Strong 3 – 60%	70	Transition Ramp Down Long Smooth 1 – 100 to 0%	111	Transition Ramp Up Short Smooth 2 – 0 to 50%
30	Short Double Click Strong 4 – 30%	71	Transition Ramp Down Long Smooth 2 – 100 to 0%	112	Transition Ramp Up Long Sharp 1 – 0 to 50%
31	Short Double Click Medium 1 – 100%	72	Transition Ramp Down Medium Smooth 1 – 100 to 0%	113	Transition Ramp Up Long Sharp 2 – 0 to 50%
32	Short Double Click Medium 2 – 80%	73	Transition Ramp Down Medium Smooth 2 – 100 to 0%	114	Transition Ramp Up Medium Sharp 1 – 0 to 50%
33	Short Double Click Medium 3 – 60%	74	Transition Ramp Down Short Smooth 1 – 100 to 0%	115	Transition Ramp Up Medium Sharp 2 – 0 to 50%

Device Support (continued)

EFFECT ID NO.	WAVEFORM NAME	EFFECT ID NO>	WAVEFORM NAME	EFFECT ID NO.	WAVEFORM NAME
34	Short Double Sharp Tick 1 – 100%	75	Transition Ramp Down Short Smooth 2 – 100 to 0%	116	Transition Ramp Up Short Sharp 1 – 0 to 50%
35	Short Double Sharp Tick 2 – 80%	76	Transition Ramp Down Long Sharp 1 – 100 to 0%	117	Transition Ramp Up Short Sharp 2 – 0 to 50%
36	Short Double Sharp Tick 3 – 60%	77	Transition Ramp Down Long Sharp 2 – 100 to 0%	118	Long buzz for programmatic stopping – 100%
37	Long Double Sharp Click Strong 1 – 100%	78	Transition Ramp Down Medium Sharp 1 – 100 to 0%	119	Smooth Hum 1 (No kick or brake pulse) – 50%
38	Long Double Sharp Click Strong 2 – 80%	79	Transition Ramp Down Medium Sharp 2 – 100 to 0%	120	Smooth Hum 2 (No kick or brake pulse) – 40%
39	Long Double Sharp Click Strong 3 – 60%	80	Transition Ramp Down Short Sharp 1 – 100 to 0%	121	Smooth Hum 3 (No kick or brake pulse) – 30%
40	Long Double Sharp Click Strong 4 – 30%	81	Transition Ramp Down Short Sharp 2 – 100 to 0%	122	Smooth Hum 4 (No kick or brake pulse) – 20%
41	Long Double Sharp Click Medium 1 – 100%	82	Transition Ramp Up Long Smooth 1 – 0 to 100%	123	Smooth Hum 5 (No kick or brake pulse) – 10%

12.2 Trademarks

TouchSense is a registered trademark of Immersion Corporation.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.