Features

- Single 2.5V - 3.6V or 2.7V - 3.6V Supply
- Atmel RapidS Serial Interface: 66MHz Maximum Clock Frequency
  - SPI Compatible Modes 0 and 3
- User Configurable Page Size
  - 512-Bytes per Page
  - 528-Bytes per Page
  - Page Size Can Be Factory Pre-configured for 512-Bytes
- Page Program Operation
  - Intelligent Programming Operation
  - 4,096 Pages (512-/528-Bytes/Page) Main Memory
- Flexible Erase Options
  - Page Erase (512-Bytes)
  - Block Erase (4-Kbytes)
  - Sector Erase (128-Kbytes)
  - Chip Erase (16-Mbits)
- Two SRAM Data Buffers (512-/528-Bytes)
  - Allows Receiving of Data while Reprogramming the Flash Array
- Continuous Read Capability through Entire Array
  - Ideal for Code Shadowing Applications
- Low-power Dissipation
  - 7mA Active Read Current Typical
  - 25µA Standby Current Typical
  - 15µA Deep Power Down Typical
- Hardware and Software Data Protection Features
  - Individual Sector
- Sector Lockdown for Secure Code and Data Storage
  - Individual Sector
- Security: 128-byte Security Register
  - 64-byte User Programmable Space
  - Unique 64-byte Device Identifier
- JEDEC Standard Manufacturer and Device ID Read
- 100,000 Program/Erase Cycles Per Page Minimum
- Data Retention – 20 Years
- Industrial Temperature Range
- Green (Pb/Halide-free/RoHS Compliant) Packaging Options

1. Description

The Atmel® AT45DB161D is a 2.5V or 2.7V, serial-interface sequential access Flash memory ideally suited for a wide variety of digital voice-, image-, program code- and data-storage applications. The AT45DB161D supports Atmel RapidS™ serial interface for applications requiring very high speed operations. RapidS serial interface is SPI compatible for frequencies up to 66MHz. Its 17,301,504-bits of memory are organized as 4,096 pages of 512-bytes or 528-bytes each. In addition to the main memory, the AT45DB161D also contains two SRAM buffers of 512-/528-bytes each. The buffers allow the receiving of data while a page in the main Memory is being reprogrammed, as well as writing a continuous data stream. EEPROM emulation (bit or byte alterability) is easily handled with a self-contained three step read-modify-write

16-megabit 2.5V or 2.7V DataFlash

Atmel AT45DB161D

3500N–DFLASH–05/10

operation. Unlike conventional Flash memories that are accessed randomly with multiple address lines and a parallel interface, the Atmel® DataFlash® uses a Atmel RapidS™ serial interface to sequentially access its data. The simple sequential access dramatically reduces active pin count, facilitates hardware layout, increases system reliability, minimizes switching noise, and reduces package size. The device is optimized for use in many commercial and industrial applications where high-density, low-pin count, low-voltage and low-power are essential.

To allow for simple in-system reprogrammability, the Atmel AT45DB161D does not require high input voltages for programming. The device operates from a single power supply, 2.5V to 3.6V or 2.7V to 3.6V, for both the program and read operations. The AT45DB161D is enabled through the chip select pin ($\overline{CS}$) and accessed via a three-wire interface consisting of the Serial Input (SI), Serial Output (SO), and the Serial Clock (SCK).

All programming and erase cycles are self-timed.

2. Pin Configurations and Pinouts

Figure 2-1. TSOP Top View: Type 1

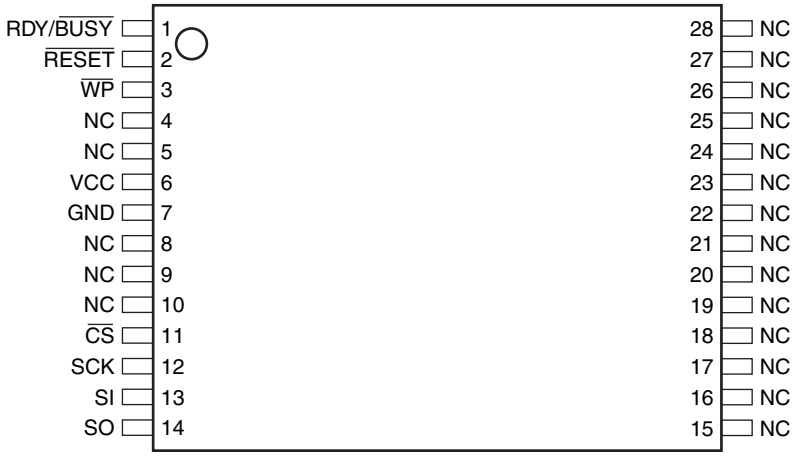


Figure 2-2. BGA Package Ball-out (Top View)

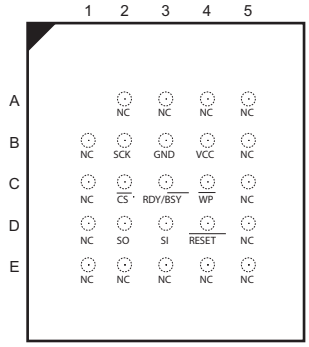


Figure 2-3. MLF (VDFN) Top View

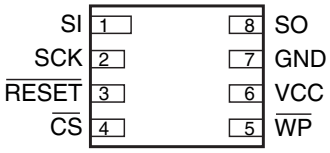
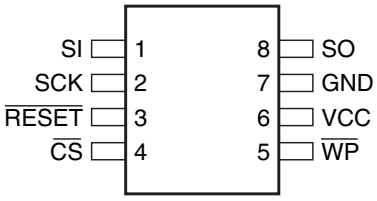


Figure 2-4. SOIC Top View



Note: 1. The metal pad on the bottom of the MLF package is floating. This pad can be a “No Connect” or connected to GND

Table 2-1. Pin Configurations

Symbol	Name and Function	Asserted State	Type
$\overline{CS}$	**Chip Select:** Asserting the $\overline{CS}$ pin selects the device. When the $\overline{CS}$ pin is deasserted, the device will be deselected and normally be placed in the standby mode (not Deep Power-Down mode), and the output pin (SO) will be in a high-impedance state. When the device is deselected, data will not be accepted on the input pin (SI). A high-to-low transition on the $\overline{CS}$ pin is required to start an operation, and a low-to-high transition is required to end an operation. When ending an internally self-timed operation such as a program or erase cycle, the device will not enter the standby mode until the completion of the operation.	Low	Input
SCK	**Serial Clock:** This pin is used to provide a clock to the device and is used to control the flow of data to and from the device. Command, address, and input data present on the SI pin is always latched on the rising edge of SCK, while output data on the SO pin is always clocked out on the falling edge of SCK.	–	Input
SI	**Serial Input:** The SI pin is used to shift data into the device. The SI pin is used for all data input including command and address sequences. Data on the SI pin is always latched on the rising edge of SCK.	–	Input
SO	**Serial Output:** The SO pin is used to shift data out from the device. Data on the SO pin is always clocked out on the falling edge of SCK.	–	Output
$\overline{WP}$	**Write Protect:** When the $\overline{WP}$ pin is asserted, all sectors specified for protection by the Sector Protection Register will be protected against program and erase operations regardless of whether the Enable Sector Protection command has been issued or not. The $\overline{WP}$ pin functions independently of the software controlled protection method. After the $\overline{WP}$ pin goes low, the content of the Sector Protection Register cannot be modified. If a program or erase command is issued to the device while the $\overline{WP}$ pin is asserted, the device will simply ignore the command and perform no operation. The device will return to the idle state once the $\overline{CS}$ pin has been deasserted. The Enable Sector Protection command and Sector Lockdown command, however, will be recognized by the device when the $\overline{WP}$ pin is asserted. The $\overline{WP}$ pin is internally pulled-high and may be left floating if hardware controlled protection will not be used. However, it is recommended that the $\overline{WP}$ pin also be externally connected to V_{CC} whenever possible.	Low	Input
RESET	**Reset:** A low state on the reset pin ($\overline{RESET}$) will terminate the operation in progress and reset the internal state machine to an idle state. The device will remain in the reset condition as long as a low level is present on the $\overline{RESET}$ pin. Normal operation can resume once the $\overline{RESET}$ pin is brought back to a high level. The device incorporates an internal power-on reset circuit, so there are no restrictions on the $\overline{RESET}$ pin during power-on sequences. If this pin and feature are not utilized it is recommended that the $\overline{RESET}$ pin be driven high externally.	Low	Input
RDY/$\overline{BUSY}$	**Ready/Busy:** This open drain output pin will be driven low when the device is busy in an internally self-timed operation. This pin, which is normally in a high state (through an external pull-up resistor), will be pulled low during programming/erase operations, compare operations, and page-to-buffer transfers. The busy status indicates that the Flash memory array and one of the buffers cannot be accessed; read and write operations to the other buffer can still be performed.	–	Output
V_{CC}	**Device Power Supply:** The V_{CC} pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.	–	Power
GND	**Ground:** The ground reference for the power supply. GND should be connected to the system ground.	–	Ground

18. Electrical Specifications

Table 18-1. Absolute Maximum Ratings*

Temperature under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (except V_{CC} but including NC pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. The "Absolute Maximum Ratings" are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Voltage Extremes referenced in the "Absolute Maximum Ratings" are intended to accommodate short duration undershoot/overshoot conditions and does not imply or guarantee functional device operation at these levels for any extended period of time

Table 18-2. DC and AC Operating Range

		Atmel AT45DB161D (2.5V Version)	Atmel AT45DB161D
Operating Temperature (Case)	Ind.	-40·C to 85·C	-40·C to 85·C
V_{CC} Power Supply		2.5V to 3.6V	2.7V to 3.6V

Table 18-3. DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DP}	Deep Power-down Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{IH}, all inputs at CMOS levels		15	25	µA
I_{SB}	Standby Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{IH}, all inputs at CMOS levels		25	50	µA
I_{CC1} (1)	Active Current, Read Operation	f = 20MHz; I_{OUT} = 0mA; V_{CC} = 3.6V		7	10	mA
		f = 33MHz; I_{OUT} = 0mA; V_{CC} = 3.6V		8	12	mA
		f = 50MHz; I_{OUT} = 0mA; V_{CC} = 3.6V		10	14	mA
		f = 66MHz; I_{OUT} = 0mA; V_{CC} = 3.6V		11	15	mA
I_{CC2}	Active Current, Program/Erase Operation	V_{CC} = 3.6V		12	17	mA
I_{LI}	Input Load Current	V_{IN} = CMOS levels			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = CMOS levels			1	µA
V_{IL}	Input Low Voltage				V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7			V
V_{OL}	Output Low Voltage	I_{OL} = 1.6mA; V_{CC} = 2.7V			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100µA	V_{CC} - 0.2V			V

Notes: 1. I_{CC1} during a buffer read is 20mA maximum @ 20MHz
2. All inputs (SI, SCK, CS#, WP#, and RESET#) are guaranteed by design to be 5V tolerant

Table 18-4. AC Characteristics – Atmel RapidS/Serial Interface

Symbol	Parameter	Atmel AT45DB161D (2.5V Version)			Atmel AT45DB161D			Units
		Min	Typ	Max	Min	Typ	Max	
f_{SCK}	SCK Frequency			50			66	MHz
f_{CAR1}	SCK Frequency for Continuous Array Read			50			66	MHz
f_{CAR2}	SCK Frequency for Continuous Array Read (Low Frequency)			33			33	MHz
t_{WH}	SCK High Time	6.8			6.8			ns
t_{WL}	SCK Low Time	6.8			6.8			ns
t_{SCKR}[1]	SCK Rise Time, Peak-to-Peak (Slew Rate)	0.1			0.1			V/ns
t_{SCKF}[1]	SCK Fall Time, Peak-to-Peak (Slew Rate)	0.1			0.1			V/ns
t_{CS}	Minimum $\overline{CS}$ High Time	50			50			ns
t_{CSS}	$\overline{CS}$ Setup Time	5			5			ns
t_{CSH}	$\overline{CS}$ Hold Time	5			5			ns
t_{CSB}	$\overline{CS}$ High to RDY/$\overline{BUSY}$ Low			100			100	ns
t_{SU}	Data In Setup Time	2			2			ns
t_{H}	Data In Hold Time	3			3			ns
t_{HO}	Output Hold Time	0			0			ns
t_{DIS}	Output Disable Time		27	35		27	35	ns
t_{V}	Output Valid			8			6	ns
t_{WPE}	$\overline{WP}$ Low to Protection Enabled			1			1	µs
t_{WPD}	$\overline{WP}$ High to Protection Disabled			1			1	µs
t_{EDPD}	$\overline{CS}$ High to Deep Power-down Mode			3			3	µs
t_{RDPD}	$\overline{CS}$ High to Standby Mode			35			35	µs
t_{XFR}	Page to Buffer Transfer Time			200			200	µs
t_{COMP}	Page to Buffer Compare Time			200			200	µs
t_{EP}	Page Erase and Programming Time (512-/528-bytes)		17	40		17	40	ms
t_{P}	Page Programming Time (512-/528-bytes)		3	6		3	6	ms
t_{PE}	Page Erase Time (512-/528-bytes)		15	35		15	35	ms
t_{BE}	Block Erase Time (4096-/4224-bytes)		45	100		45	100	ms
t_{SE}	Sector Erase Time (131,072/135,168-bytes)		0.7	1.3		0.7	1.3	s
t_{CE}	Chip Erase Time		12	25		12	25	s
t_{RST}	$\overline{RESET}$ Pulse Width	10			10			µs
t_{REC}	$\overline{RESET}$ Recovery Time			1			1	µs

Note: 1. Values are based on device characterization, not 100% tested in production