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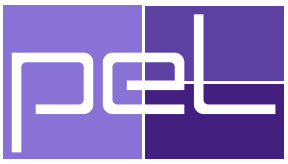	*Author(s) Name(s)* Camille Coppieters de Gibson 394956 Silvia Camenzind 339712	*Function* Exchange Student Bsc Student
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Title

R1: FLYBACK CONVERTER — BASIC DESIGN AND SIMULATIONS

Course Name

EE-365 Power Electronics

Keywords

Flyback Converter, PLECS, Device selection

TABLE OF CONTENTS

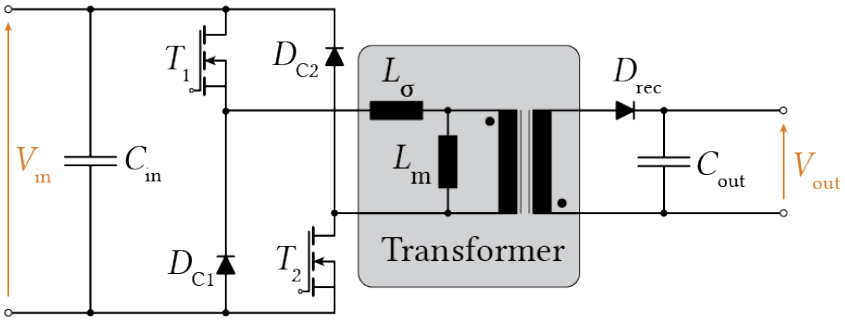
FLYBACK CONVERTER SIZING

The first part of the project deals with sizing of the main elements of a Flyback converter, according to given converter specifications and design requirements. Throughout the whole project continuous conduction mode (CCM) of the converter will be assumed. Fill out Table 1 with the parameters assigned to your group. Regarding the results, please provide them with two digits after the decimal point in the unit provided in the solution box and use the framed boxes below each question to insert your answers and explanations.

Table 1 Given parameters and design requirements for the Flyback converter.

Property	Value	Unit
$P_{out,nom}$	50	W
$P_{out,min,CCM}$	10	W
$U_{in,nom}$	50	V
$U_{in,min}$	30	V
$U_{in,max}$	60	V
U_{out}	24	V
$\Delta U_{out,pp}/U_{out}$	2	%
f_{sw}	360	kHz

Figure 1 Schematic of the double switch Flyback.



Q1: VOLTAGE TRANSFER FUNCTION

Derive the input-output voltage transfer function $\frac{U_{out}}{U_{in}} = f(D)$ of a Flyback converter and solve it for the duty cycle $D = f(U_{in}, U_{out})$.

The given Flyback converter operates in six stages. To derive the transfer function in terms of the duty cycle, we apply the volt-second balance to the magnetizing inductance L_m across the transformer:

$$0 = U_{in} \cdot (\Delta t_2 - \Delta t_3 - \Delta t_4) - n \cdot U_{out} \cdot (\Delta t_1 + \Delta t_5 + \Delta t_6)$$

In CCM, the most significant time intervals are $\Delta t_2 \gg \Delta t_3, \Delta t_4$ and $\Delta t_6 \gg \Delta t_1, \Delta t_5$, simplifying the equation to:

$$U_{in} \cdot \Delta t_2 = n \cdot U_{out} \cdot \Delta t_6$$

During stage 2, the input voltage is directly applied to the primary winding (active phase), while in stage 6, the stored energy is transferred to the secondary side (passive phase). The duty cycle is then given by:

$$D = \frac{t_{active}}{t_{complete}} \approx \frac{\Delta t_2}{\Delta t_2 + \Delta t_6}$$

Using: $\Delta t_2 = D \cdot (\Delta t_2 + \Delta t_6)$ and $\Delta t_6 = (1 - D)(\Delta t_2 + \Delta t_6)$ we find:

$$U_{in} \cdot \Delta t_2 = n \cdot U_{out} \cdot \Delta t_6$$

$$U_{in} \cdot D \cdot (\Delta t_2 + \Delta t_6) = n \cdot U_{out} \cdot (1 - D)(\Delta t_2 + \Delta t_6)$$

$$U_{in} \cdot D \cdot = n \cdot U_{out} \cdot (1 - D)$$

$$\frac{U_{out}}{U_{in}}(D) = \frac{D}{n(1 - D)}$$

Using this formula, we can then solve for D.

$\frac{U_{out}}{U_{in}}(D) = \frac{D}{n(1-D)}$

$D = \frac{U_0 N}{U_0 N + U_{in}}$

/ 4 pt.

Q2: WINDING RATIO

To determine the winding ratio, the following steps should be followed::

a) Define a maximum duty ratio D_{max} for your further calculations (please note that the datasheet of the UCC38C44 limits the duty cycle to 0.50)
b) Calculate the winding ratio $N = \frac{N_P}{N_S}$ to match the requested voltages with your selection of D_{max}.

From the datasheet, we know that $D_{max} = 48\%$. This means that the PWM Controller cannot supply a higher duty cycle.
We then modify the formula for the duty ratio to find the winding ratio N. We use $V_{in,min}$ to calculate the worst case scenario.

$$D = 0.48 = \frac{V_0 N}{V_0 N + V_{in,min}} \longrightarrow N = \frac{D U_{in,min}}{U_O(1-D)} = \frac{0.48 \cdot 30}{24(1-0.48)} = 1.15$$

a) D_{max} = 0.48	b) N = 1.15	/ 3 pt.

Q3: DUTY CYCLE

Calculate the duty cycle under the following operating conditions:

a) Nominal operation $D|_{U_{in,nom}}$;
b) Minimum input voltage $D|_{U_{in,min}}$;
c) Maximum input voltage $D|_{U_{in,max}}$.

$$D|_{U_{in,nom}} = \frac{U_0 n}{U_0 n + U_{in,nom}} = \frac{24 \cdot 1.15}{24 \cdot 1.15 + 50} = 0.356$$
$$D|_{U_{in,min}} = \frac{U_0 n}{U_0 n + U_{in,min}} = \frac{24 \cdot 1.15}{24 \cdot 1.15 + 30} = 0.479$$
$$D|_{U_{in,max}} = \frac{U_0 n}{U_0 n + U_{in,max}} = \frac{24 \cdot 1.15}{24 \cdot 1.15 + 60} = 0.315$$

a) $D\|_{U_{in,nom}}$ = 0.356	b) $D\|_{U_{in,min}}$ = 0.479	c) $D\|_{U_{in,max}}$ = 0.315	/ 2 pt.

Q4: MAGNETIZING INDUCTANCE AND STRAY INDUCTANCE

Derive an expression and calculate the required magnetizing inductance L_m of your transformer, considering that the Flyback converter should operate down to $P_{out,min,CCM}$ in continuous conduction mode.
A specific stray inductance cannot be calculated easily, therefore an estimation is needed. To design this converter, use the assumption $L_\sigma \approx 0.05 \cdot L_m$.

From stage 2 (when T_1, T_2 act like switches 'on' and all diodes are off) we have that:

$$\Delta i_{L_m} = \frac{U_l \cdot D}{f_{sw} \cdot (L_m + L_l)} \approx \frac{U_l \cdot D}{f_{sw} \cdot (L_m)} \;\&\; I_{L_m,avg} = n \cdot I_{out,min} = n \cdot \frac{P_{out,min}}{U_{out}}$$

For Continuous Conduction Mode, we require: $\Delta I_{Lm} \leq 2 I_{Lm,avg}$ and we then substitute $\Delta I_{Lm} = \frac{U_l D}{f_s L_m}$:

$$\frac{U_l \cdot D}{f_s \cdot L_m} \leq 2n \frac{P_{out,min}}{U_O}$$

Rearranging for L_m:

$$L_m \geq \frac{U_l \cdot D \cdot U_O}{2 \cdot n \cdot f_s \cdot P_{out,min}}$$

$$L_\sigma \approx 0.05 L_m$$

L_m = 51.59 µH	L_σ = 2.58 µH	/ 6 pt.

Q5: OUTPUT CAPACITANCE

Derive an expression and calculate the required output capacitance C_{out} to fulfill the output voltage ripple requirements under all operating conditions.

The basic formula of a capacitor is: $C = \frac{\Delta Q}{\Delta U}$, which expresses the stored charge over the voltage drop across the capacitor.

- From the charge variation we derived the maximum charge stored during Δt_{up}:

$$\Delta Q_{out} = I_{out} \cdot \Delta t_{up} = \frac{U_{out}}{R_L} \cdot \frac{D}{f_s} \longrightarrow Q_{max} = \frac{U_{out}}{R_{L,min}} \cdot \frac{D_{max}}{f_s}$$

- The output voltage ripple observed across the capacitor is:

$$\Delta U_{out} = U_{out} \cdot 2\% = 0.48V$$

So we obtain the final value: $C_{out} = \frac{D_{max}}{f_s \cdot R_{L,min} \cdot 2\%}$ with $R_{L,min} = \frac{U_{out}^2}{P_{out,nom}} = 57.6\,[\Omega]$

C_{out} = 1.16 µF	/ 4 pt.

Q6: INPUT CAPACITANCE

Similar to the output capacitance, the input capacitance has to be calculated. The constraint is that the converter should survive the loss of a half-period of the supplying 50 Hz-grid, i.e. 10 ms. During this so called 'Hold-up time', the voltage should not drop below $U_{in,min}$ when starting from $U_{in,nom}$.

The energy stored in a capacitor is $E = \frac{C \cdot U^2}{2}$ and the energy required to sustain the output power during the hold-up time is: $\Delta E = P_{out} \cdot t_{UP}$. (where $t_{UP} = \Delta t_2 = 10ms$.)
Using the energy loss equation: $E_{loss} = \Delta E = E_{initial} - E_{final} = \frac{C_{in}}{2} \cdot (U_{in,nom}^2 - U_{in,min}^2)$, we can solve for C_{in}:

$$C_{in} = \frac{2 \cdot P_{out} \cdot t_{UP}}{U_{in,\text{nom}}^2 - U_{in,\text{min}}^2}$$

C_{in} = 625.00 µF	/ 4 pt.

Q7: PLECS VALIDATION AT NOMINAL OPERATION

Using the provided PLECS model, verify your calculations during steady state at nominal operation by presenting the following waveforms over five switching periods:

a) Output voltage, also provide the measured voltage ripple $\Delta U_{out,pp}|_{nom}$;
b) Inductor current, also provide the minimum measured inductor current $I_{m,min}|_{nom}$;
c) Voltage and current of the transistors;
d) Voltage and current of the rectifying diode.

Start with configuring the Plecs model by clicking on the configuration block in the model. The stray inductance can be neglected here and should be put to 0.

We observe that our calculations correspond to the simulation.

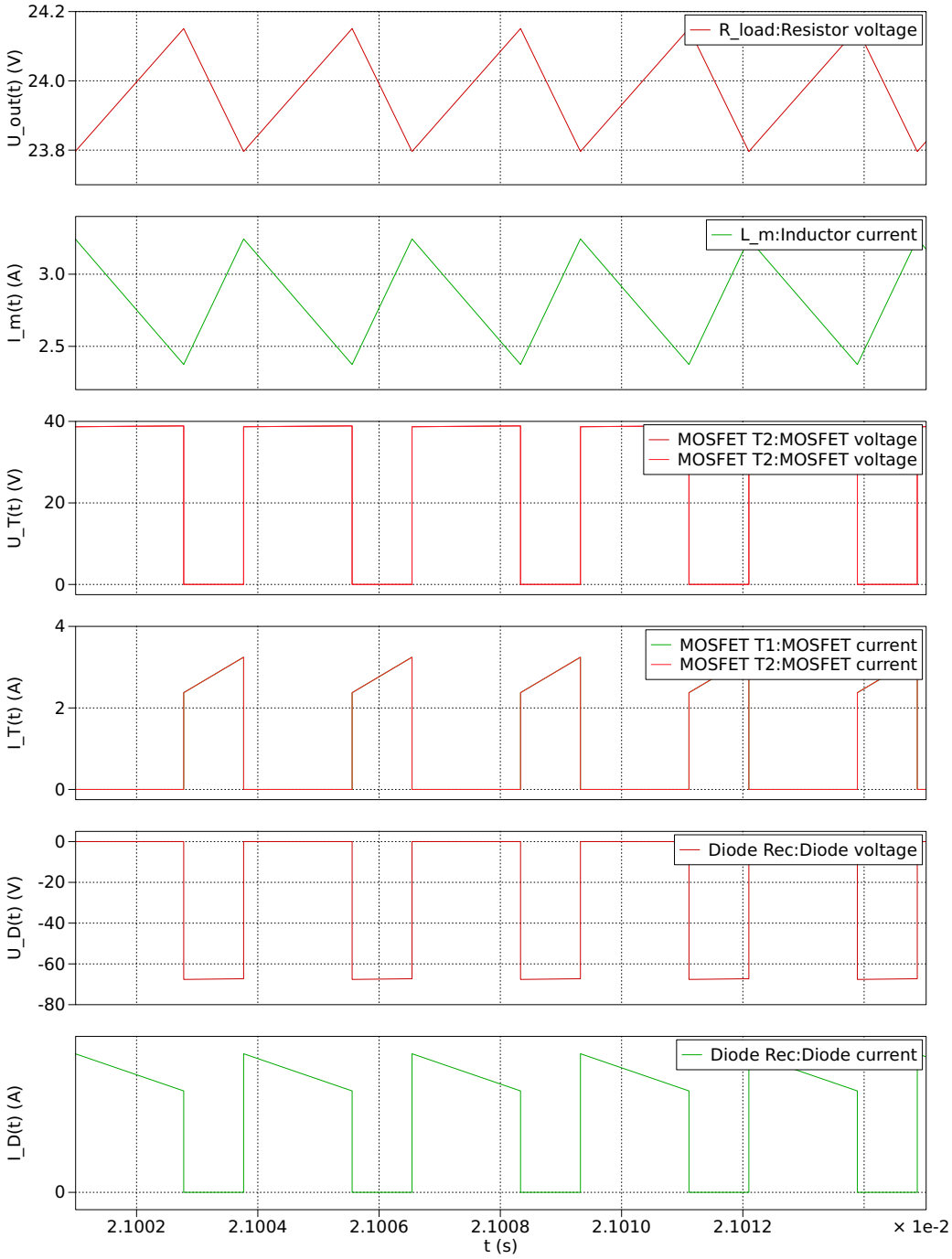


Figure 2 Voltage and current waveforms of interest. From top to bottom: output voltage $U_{out}\,(t)$, magnetizing current $I_m\,(t)$, transistor voltage $U_T\,(t)$, diode voltage $U_D\,(t)$, diode current $I_D\,(t)$; all as a function of time.

a) $U_{out,pp}\big\vert_{nom}$ = 355 mV	b) $I_{m,min}\big\vert_{nom}$ = 2.37 A	/ 2 pt.

Q8: PLECS VALIDATION FOR CCM

Using the provided PLECS model, verify that your design stays in continuous conduction in steady state mode under worst case operating conditions (`OP: Limit CCM`) by presenting the following waveforms over five switching periods:

a) Output voltage, also provide the measured voltage ripple $\Delta U_{out,pp}\big|_{P_{out,min,CCM}}$;
b) Inductor current, also provide the measured minimum inductor current $I_{m,min}\big|_{P_{out,min,CCM}}$;
c) Voltage and current of the transistors;
d) Voltage and current of the rectifying diode.

PS: If the output voltage U_{out} does not exactly correspond to the desired value, check the inductor current i_m carefully. It may be that i_m drops to zero for a very short time. This does not mean that your calculation from Q4 are wrong, but is rather due to numerical reasons. Slightly increase your magnetizing inductance L_m and try it again.

Looking at the magnetizing current I_m, we observe that it never falls to zero and always stays in CCM mode.

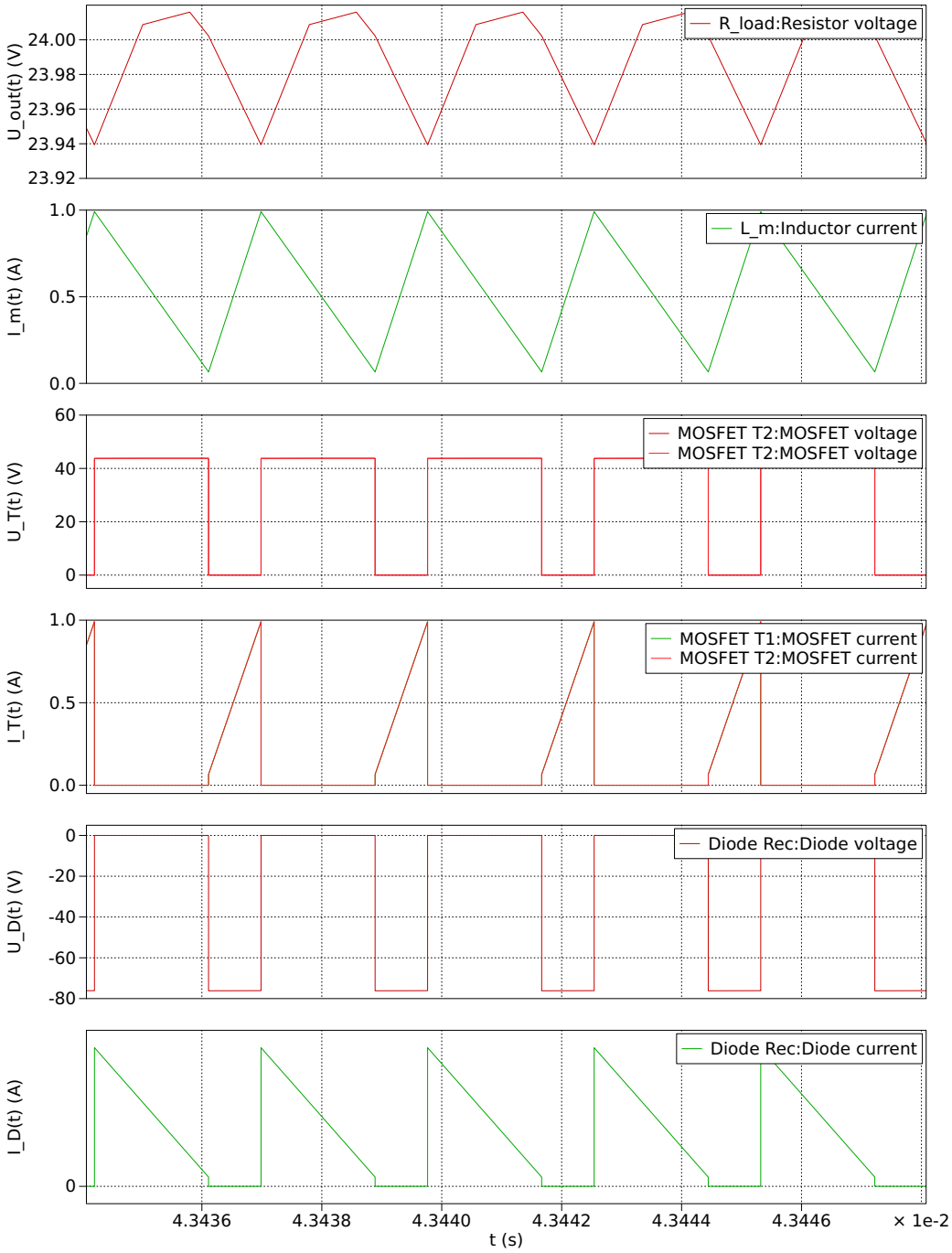


Figure 3 Voltage and current waveforms of interest. From top to bottom: output voltage $U_{out}\,(t)$, magnetizing current $I_m\,(t)$, transistor voltage $U_T\,(t)$, diode voltage $U_D\,(t)$, diode current $I_D\,(t)$; all as a function of time.

a) $U_{out,pp}\big\vert_{P_{out,min,CCM}}$ = 76.61 mV	b) $I_{m,min}\big\vert_{P_{out,min,CCM}}$ = 66.01 mA	/ 2 pt.

Q9: PLECS VALIDATION FOR MAXIMUM DUTY RATIO

Using the provided PLECS model, verify that your design does not exceed your selection of neither D_{max} nor $\Delta U_{out,pp}$ (`OP: Limit ripple and duty cycle;`) by presenting the following waveforms with $U_{in,min}$ and $P_{out,nom}$ in steady state (again five switching periods):

a) Output voltage, also provide the measured voltage ripple $\Delta U_{out,pp}\big|_{D_{max}}$;
b) Inductor current, also provide the measured minimum inductor current $I_{m,min}\big|_{D_{max}}$;
c) Voltage and current of the transistors;
d) Voltage and current of the rectifying diode.

The maximal duty cycle observed in the simulation is $D_{sim,max} = 0.479$ which is below $D_{max} = 0.48$ from Q2.
The simulated peak-to-peak output voltage ripple is: $U_{out,pp,sim} = 0.4785$ which is smaller than the maximum voltage ripple $\Delta U_{out,pp} = 2\% \cdot 24/100 = 0.48$.

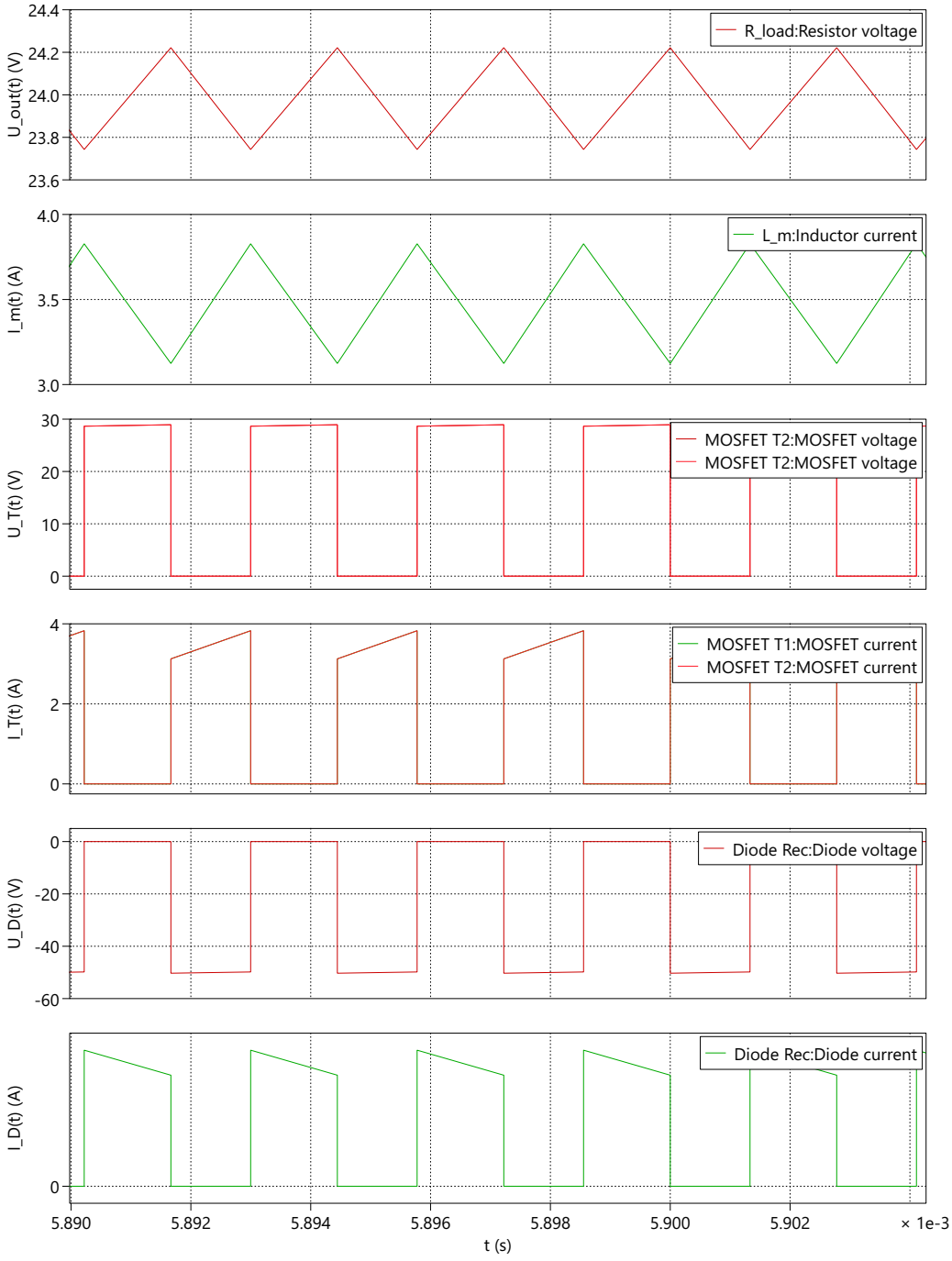


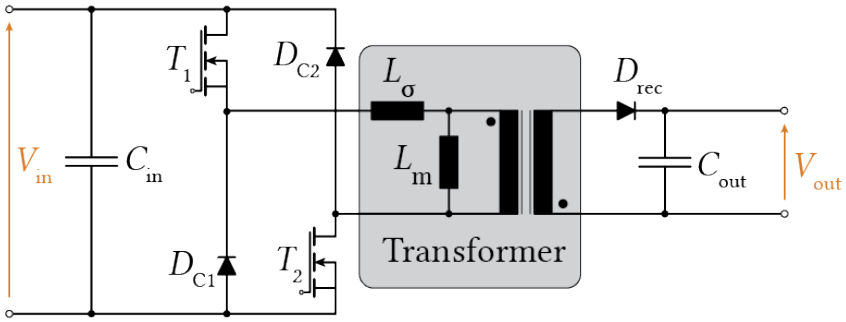
Figure 4 Voltage and current waveforms of interest. From top to bottom: output voltage $U_{out}\,(t)$, magnetizing current $I_m\,(t)$, transistor voltage $U_T\,(t)$, diode voltage $U_D\,(t)$, diode current $I_D\,(t)$; all as a function of time.

a) $U_{out,pp}\big\vert_{D_{max}}$ = 478.55 mV	b) $I_{m,min}\big\vert_{D_{max}}$ = 3.12 A	/ 2 pt.

SEMICONDUCTOR COMPONENTS

The second part of this report focuses on the semiconductors. You will have to derive equations for your design, eventually leading to the selection of proper semiconductors that you will use in your design. To achieve this, the highest occurring voltage and biggest current needs to determined for every device. As in the first set of questions, provide numeric answers with a precision of two digits after the decimal point in the provided unit. From now on, you can use the assumption for L_σ you made in .

Figure 5 Schematic of the double switch Flyback.



Q10: TRANSISTOR STRESSES

To select an appropriate transistors for your design, you need to determine maximum voltage and current stress that it has to handle in the Flyback converter. For this purpose, derive analytically. Also provide the results for your converter in normal operation mode in table 2:

a) The maximum voltage over each transistor $u_{T1,max}$ and $u_{T2,max}$;
b) The maximum current flowing through each transistor $i_{T1,max}$ and $i_{T2,max}$.

The maximum voltage across the transistors is the same as the maximum current that flows through the transistors (due to some symmetry in the circuit).
The voltage across T_1 is given by $U_{T1} = U_{in} - U_{D2}$. The maximum value would be $U_{T1,max} = U_{T2,max} = U_{in}$.
The current through T_1 is given by: $I_{T1} = I_{L_m} + \frac{I_{out}}{n\cdot(1-D)} - I_{D2}$. The maximum value is:
$I_{T1,max} = I_{T2,max} = \frac{I_{out}}{n\cdot(1-D)} + \frac{\Delta i_{L_m,max}}{2} = \frac{P_{out,nom}}{n\cdot(1-D)\cdot U_{out}} + \frac{U_{in}\cdot D}{2\cdot f_{sw}\cdot(L_m+L_\sigma)}$

/ 6 pt.

Q11: RECTIFYING DIODE STRESSES

Identical to the transistors, the maximum values of the rectifying diode have to be identified. Thus, derive analytically. Provide the results for your converter in normal operation mode in table 2:

a) The maximum voltage over the diode $u_{D,rec,max}$;
b) The maximum current flowing through the diode $i_{D,rec,max}$.

When $U_{T1} = U_{T2} = U_{T1,max} = U_{in,max}$ and the diodes are blocked, $U_{D1} = U_{D2} = 0[V]$, we obtain $U_{L_m} = -U_{in}$. Using Kirchhoff's Law and the induced voltage of the transformer, we find: $U_{D,rec,max} = \frac{U_{in}}{n} + U_{out} = 67.33V$
$i_{D,rec,max} = N \cdot i_{Lm(max)} = N \cdot \frac{P_{out,nom}}{U_0} = 1.15 \cdot \frac{50W}{24V} = 2.40A$
(*In this case the normal and the worst case are the same because* $P_{out,nom} = P_{out,max}$)

/ 6 pt.

Q12: CLAMPING DIODES STRESSES

Furthermore the maximum values of the clamping diodes on the primary side have to be considered. Derive analytically. Provide the results for your converter in normal operation mode in table 2:

a) The maximum voltage over the diode $u_{D,c,max}$;

	Normal conditions				Worst conditions			
Semiconductors	u_{max}		i_{max}		u_{max}		i_{max}	
T_1	50	V	3.26	A	60	V	3.36	A
T_2	50	V	3.26	A	60	V	3.36	A
D_{rec}	67.48	V	2.40	A	76.0	V	2.40	A
$D_{c,1}$	50	V	3.26	A	60	V	3.36	A
$D_{c,2}$	50	V	3.26	A	60	V	3.36	A

Table 2 Currents and voltages for all semiconductor devices in normal and (respective) worst case condition,

b) The maximum current flowing through the diode $i_{D,c,max}$.

The maximum voltage across the diodes occurs when the transistors on the primary side let the current pass. In this case there's a small voltage drop across the transistors: ($\approx 0.7[V]$):

$$U_{D_{C1},max} = U_{D_{C2},max} = U_{in} - U_{T_1,min} \approx U_{in}$$

For the maximum current, we calculate the maximum current that would flow in the secondary part because almost no current enters the source of a transistor at $0[V]$. So we obtain:

$$I_{D_{C1},max} = I_{D_{C2},max} = \frac{\Delta I_{Lm,max}}{2} + I_{secundary} = \frac{U_{in} \cdot D}{2 \cdot f_{sw} \cdot (L_m + L_\sigma)} + \frac{I_{out}}{N \cdot (1 - D)}$$

with $I_{out} = \frac{P_{out,nom}}{U_{out}}$

/ 4 pt.

Q13: WORST CASE CONDITIONS

Consider the equations you derived in the three previous questions. Identify and explain briefly when the highest voltage and current stress occur for every component. Also calculate the values under their respective worst case condition (that means $U_{in,min} \leq U_{in} \leq U_{in,max}$ and $P_{out,min,CCM} \leq P_{out} \leq P_{out,nom}$). Please note that the worst case may be different for the different values:

- The **maximum voltage across the transistors** occurs when both transistors (switches) are blocked. At this point, all the current through the transformer passes through the diodes, and no current flows through the transistors. (Stage 4)
- The **maximum current through the transistors** happens when the clamping diodes are blocked. In this condition, all the current passing through the transformer flows through the transistors. The current through the transistors increases linearly until the switch-mode is turned off. (End of Stage 2)
- The **maximum voltage across the rectifying diode** occurs when the inductor current satisfies the condition $I_{L_m} = -U_{L_m,\max}$. This begins when the clamping diodes are conducting and have a boundary voltage of $U_{D_1,\max} = U_{in}$. At this moment, Kirchhoff's voltage law states that the sum of the voltages across the transformer and the output resistance results in the maximum voltage across the rectifying diode. (Stage 4) The voltage across the rectifying diode decreases when the transistors switch on. (Stage 1)
- The **maximum current through the rectifying diode** occurs at the end of Stage 4, when both clamping diodes are also conducting. During this stage, the current through the rectifying diode increases linearly. Once the current starts flowing through the capacitor of the transistor instead of through the primary-side diodes, the current through the rectifying diode decreases.
- The **maximum voltage across the clamping diodes** occurs when the clamping diodes are conducting. This situation is similar to the condition for the maximum voltage across the rectifying diode, which happens in Stage 4.
- The **maximum current through the clamping diodes** occurs at the beginning of Stage 4. When the clamping diodes turn on, they experience a peak current at the start of this stage.

/ 4 pt.

Q14: SEMICONDUCTOR SELECTION

Based on the obtained values from Q12, select from the offered lists in Tables 3 and 4 MOSFET (Metal Oxide Semiconductor Field-Effect Transistor) devices and diodes for your design. For all five, the blocking voltage of the device should be at least 1.5-times your result to provide sufficient safety margin during operation (e.g. overvoltages due to parasitic effects). Elaborate briefly why you chose exactly these models and highlight them in the tables, as it is exemplary done for the first device. Note that due to the low operating voltage, Schottky diodes are offered, and thus reverse recovery is not of concern for the design. All devices are built in a TO-220 case as shown in Fig. 6.

To choose the right elements for the circuit, we need to take a margin factor of 1.5-times the maximum values. To be safe, it is better to take the worst-case scenario values than the nominal values, even though we know that most of the time the flyback will be used under normal conditions.

- For both transistors, we have $U_{T1,max,worstcase} = U_{T2,max,worstcase} = 60[V]$, so we have to take $U_{ds} \geq 1.5 \cdot 60[V] = 90[V]$ and $I_{T1,max,worstcase} = I_{T2,max,worstcase} = 3.36[A]$ so we have to take $I_{cont} \geq 1.5 \cdot 3.36[A] = 5.03[A]$.
- The maximum values of the clamping diodes are the same.
- For the rectifying diode we have $U_{D_3,max,worstcase} = 76[V]$ so we have to take $U_{ds} \geq 1.5 \cdot 76[V] = 114[V]$ and $I_{D_3,max,worstcase} = 2.40[A]$ so we have to take $U_{ds} \geq 1.5 \cdot 2.40[A] = 3.60[A]$

Upper transistor model No. : 7

Lower transistor model No. : 7

Rectifying diode model No. : 2

Upper clamping diode model No. : 3

Lower clamping diode model No. : 3

/ 2 pt.

Table 3 The list of offered MOSFET devices. The parameter U_{ds} is the rated drain-source voltage, whereas the I_{cont} stands for continuous drain-source current. All devices are in the TO-220 package (see Fig. 6).

No.	Manufacturer	Product	U_{ds} (V)	I_{cont} (A)	$R_{ds,on}$ @ 25 °C (mΩ)
1	Infineon	IRFB5620PbF	200	18	60
2	Rohm	RCX300N20	200	16.3	60
3	Onsemi	FDPF18N20FT-G	200	10.8	120
4	Rohm	RCX200N20	200	10.8	100
5	Onsemi	FQPF630	200	6.3	340
6	Nexperia	PHP18NQ11T	110	13	80
7	Vishay	SiHF530	100	10	160
8	ST	STP16NF06	60	11	80

Table 4 The list of offered Schottky diode devices. The parameter U_{dc} refers to the maximum dc blocking voltage, whereas I_{cont} is the continuous forward current. All devices are in the TO-220 package (see Fig. 6).

No.	Manufacturer	Product	U_{dc} (V)	I_{cont} (A)	U_f @ 25 °C (V)
1	Taiwan	MBR16150	150	16	0.95
2	Taiwan	SRAF10150	150	10	0.95
3	Onsemi	MBR10100G	100	10	0.70
4	ST	STPS20SM60	60	20	0.57
5	Onsemi	MBR1660	60	16	0.75
6	Vishay	VT3045BP	45	30	0.58
7	Vishay	VFT2045BP	45	20	0.57
8	Vishay	VS-12TQ045-M3	45	15	0.56

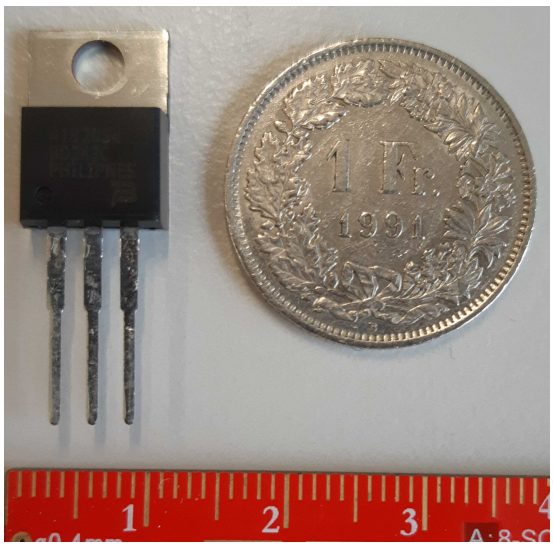


Figure 6 A semiconductor in a TO-220 case.

CALCULATION OF CURRENT AVERAGE AND RMS VALUES

To serve as a basis for the loss calculation using simplified models, expressions for the average and rms currents must be derived and calculated. In addition, this also reveals the current condition in a given operating point. The results have to be given with two digits after the decimal point using the given unit.

Q15: TRANSISTOR CURRENT

Consider the current passing through the transistors in the steady state operation of the Flyback converter. Derive an analytical expression for the average current $I_{T,avg}$ and for the rms current $I_{T,rms}$. To make the calculations easier, you can assume pulse-shaped waveforms (e.g. neglecting the output voltage ripple). Provide the results for your converter in table 5.

We integrate from t_0 to t_2 because outside of this interval there is no current through the transistors.

$$I_{T,rms} = \sqrt{\frac{1}{T_s}\int_{t_0}^{t_2} i_T^2 dt}$$

We approximate the current in the second stage with $I_T = \frac{I_{out}}{N(1-D)}$. We then substitute this in the above equation:

$$I_{T,rms} = \sqrt{\frac{1}{T_s}\int_{t_0}^{t_2}(\frac{I_{out}}{N(1-D)})^2 dt} = \sqrt{\frac{1}{T_s}\left[(\frac{I_{out}}{N(1-D)})^2 \cdot t\right]_{t_0}^{t_2}} = \sqrt{\frac{1}{T_s}\left[(\frac{I_{out}}{N(1-D)})^2 \cdot \Delta t_2\right]}$$

We further have $\frac{\Delta t_2}{T_s} = \frac{\Delta t_2}{\Delta t_2 + \Delta t_6} = D$

$$I_{T,rms} = \sqrt{\frac{\Delta t_2}{T_s}\left[(\frac{I_{out}}{N(1-D)})^2\right]} = (\frac{I_{out}}{N(1-D)})\sqrt{D} = \frac{I_{out}\sqrt{D}}{N(1-D)}$$

where $I_{out,nom} = \frac{P_{out,nom}}{U_{in}}$.
To find the average value, we use

$$I_{T,avg} = \frac{1}{T_s}\int_0^{T_s} i(t)dt = \frac{1}{T_s}\int_{t_0}^{t_2}\left(\frac{I_{out}}{N(1-D)}\right)dt = \frac{I_{out}\cdot D}{N\cdot(1-D)}$$

/ 6 pt.

Q16: RECTIFYING DIODE CURRENT

Consider now the current passing through the rectifying diode in the steady state operation of the Flyback converter. Derive an analytical expression for the average current $I_{D,rec,avg}$ for the rms current $I_{D,rec,rms}$. Also here, the simplifications can be used.

The average current through the rectifying diode $I_{D,rec,avg} = I_{out}$. To calculate the rms current value, we use

$$I_{rec} = \sqrt{\frac{1}{T_s}\int_{t_2}^{t_6} i_{D_{rect}^2(t)dt}}$$

We use the approximation that the current in the time interval $\Delta t_6 \approx t_6 - t_2$ is equal to its maximal value $I_{D,rect,max} = \frac{I_{out}}{1-D}$.
Furthermore we use the simplification $T_s = \Delta t_2 + \Delta t_6$ and $(1-D) = \frac{\Delta t_6}{\Delta t_2 + \Delta t_6}$.
By substituing we obtain:

$$I_{D,rec} = \sqrt{\frac{1}{T_s}\int_{t_2}^{t_6}(\frac{I_{out}}{1-D})^2 dt} = \sqrt{\frac{1}{T_s}\left[(\frac{I_{out}}{1-D})^2 \cdot t\right]_{t2}^{t6}} = \sqrt{\frac{1}{T_s}\left[(\frac{I_{out}}{1-D})^2 \cdot \Delta t_6\right]} = \sqrt{\frac{1}{\Delta t_2 + \Delta t_6}\left[(\frac{I_{out}}{1-D})^2 \cdot \Delta t_6\right]}$$

$$= \sqrt{\frac{\Delta t_6}{\Delta t_2 + \Delta t_6}(\frac{I_{out}}{1-D})^2} = \sqrt{\frac{\Delta t_6}{\Delta t_2 + \Delta t_6}(\frac{I_{out}}{1-D})^2} = \sqrt{(1-D)(\frac{I_{out}}{1-D})^2} = \sqrt{\frac{(I_{out})^2}{1-D}} = \frac{I_{out}}{\sqrt{1-D}}$$

$I_{out} = \frac{P_{out,nom}}{U_o ut} = 2.083A$

/ 6 pt.

Q17: CLAMPING DIODE CURRENT

Consider again the current passing through the diode. Derive an analytical expression for the rms current during steady state $I_{D,c1,rms}$ with the simplified assumptions.

The average values of the clamping currents are

$$I_{D,c1,avg} = \frac{1}{T_s}\int_{t_3}^{t_4} i_D dt$$

We then use the approximation for the fourth stage

$$I_{c1,max} = \frac{I_{out}}{N(1-D)}$$

We then substitute:

$$I_{D,c1,avg} = \frac{1}{T_s}\int_{t_3}^{t_4} \frac{I_{out}}{N(1-D)} dt = \frac{1}{T_s}\frac{I_{out}}{N(1-D)}\Delta t_4 = \frac{I_{out}\cdot \Delta t_4}{N(1-D)T_s}$$

We can then assume that $\Delta t_4 = 10\% T_s$. This gives

$$I_{D,c1,avg} = \frac{I_{out}\cdot 0.1}{N(1-D)}$$

.

Using the same approximations as for the average value, we find the rms value

$$I_{D,c1,rms} = \sqrt{\frac{1}{T_s}\int_{t_3}^{t_4} I_{c1,max}^2 dt} = \sqrt{\frac{1}{T_s}\int_{t_3}^{t_4} (\frac{I_{out}}{N(1-D)})^2}$$

$$= \sqrt{\frac{1}{T_s}\left[(\frac{I_{out}}{N(1-D)})^2 \cdot t\right]_{t_3}^{t_4}} = \sqrt{\frac{1}{T_s}(\frac{I_{out}}{N(1-D)})^2 \cdot \Delta t_4} = \sqrt{\frac{\Delta t_4}{T_s}(\frac{I_{out}}{N(1-D)})^2} = \frac{I_{out}}{N(1-D)}\sqrt{\frac{\Delta t_4}{T_s}} = \frac{I_{out}}{N(1-D)}\sqrt{\frac{0.1T_s}{T_s}} = \frac{I_{out}}{N(1-D)}\sqrt{0.1}$$

/ 4 pt.

Q18: PLECS VERIFICATION FOR THE CURRENT CALCULATIONS

Using the provided PLECS model, verify your formulas by calculating the values during nominal operation and comparing them with the model output (for nominal operation, in the model `OP = 1;` has to be selected):

a) The transistor rms current $I_{T,rms}|_{nom}$;
b) The transistor average current $I_{T,avg}|_{nom}$;
c) The diode rms current $I_{D,rms}|_{nom}$;
d) The diode average current $I_{D,avg}|_{nom}$.

In the model we added another probe to also get the current in the clamping diode. We have 2 possibilities:

- **using the approximation** $L_\sigma = 0$: For the transistor and the rectifying diode, our calculated values are equal to the simulated results. However, the simulated clamping values differ from the calculated clamping values.
- **using** $L_\sigma = 2.58\mu H$: The simulated currents are slightly smaller than the calculated values. This is due to additional losses in the stray inductance.

A possible reason for this discrepancy is that the values for $R_{DS,ON}$ and $U_{D,f}$ used in the program may differ from those specified in the datasheet.
(i.e. From the datasheet we have: $U_{df} = 0.95[V]; R_{ds,ON} = 95[m\Omega]$ in the code was used $U_{df} = 0.4[V]; R_{ds,ON} = 33[m\omega]$)

	Calculated				Plecs Model $L_{sigma} = 0$				Plecs Model $L_{\sigma} = 2.58\mu H$			
Semiconductors	I_{avg}		I_{rms}		I_{avg}		I_{rms}		I_{avg}		I_{rms}	
T_1	1.00	A	1.68	A	1.00	A	1.68	A	0.87	A	1.48	A
T_2	1.00	A	1.68	A	1.00	A	1.68	A	0.87	A	1.48	A
D_{rec}	2.08	A	2.60	A	2.08	A	2.60	A	1.76	A	2.23	A
$D_{c,1}$	0.28	A	0.89	A	0	A	0	A	0.15	A	0.54	A
$D_{c,2}$	0.28	A	0.89	A	0	A	0	A	0.15	A	0.54	A

Table 5 Currents and voltages for all semiconductor devices in normal and (respective) worst case condition,

/ 2 pt.

THERMAL DESIGN BASED ON THE EXPECTED SEMICONDUCTOR LOSSES

Based on your previously calculated results, losses in the semiconductors for normal operation condition will be calculated. These results will be compared with the results of the provided Loss Tool in MATLAB. Results from the Loss Tool will also be used to select appropriate heatsinks for your design. As in the other questions, results should be given with two digits after the decimal point in the unit indicated by the answer.

Q19: RECTIFYING DIODE CONDUCTION LOSSES

Using the datasheet of your selected diode as well as the results from your calculations, calculate the conduction losses of your diode at steady state operation with nominal data $P_{D,cond}|_{nom}$. Note that the datasheet values may not be at the temperature your diode will operate, which is assumed to be 125 °C. The provided Application Notes of INFINEON may serve you as a guideline for this calculation.

From the datasheet of the rectifying diode we have $U_{D,f} = 0.95[V]$ and $I_{D,f} = 10\,[A]$, we calculated $R_{D,on} \approx \frac{U_{D,f}}{I_{D,f}} = 95[m\Omega]$.
The diode has an operating temperature between -55 and 150 °C.
The power loss in the rectifying diode due to conduction is given by:

$$P_{D,rec,cond} = U_{D,f} \cdot I_{D,avg} + R_{D,on} \cdot I_{D,rms}^2$$

For $I_{D,rms}$ we used the value with $L_\sigma = 0$ because it's preferred to have a slightly overdimensioned heatsink than destroying the system because it gets too hot.

$P_{D,rec,cond}|_{nom}$ = 2.62 W

/ 4 pt.

Q20: TRANSISTOR CONDUCTION LOSSES

Using the datasheet of your selected transistor as well as the results from your calculations, calculate the conduction losses for one of your transistors at steady state operation with nominal data $P_{T,cond}|_{nom}$. Identical to the diode, the transistor operates at a temperature of 125 °C (for temperature scaling, follow the instructions of the provided INFINEON Application Note and/or the figures provided in the datasheet).

From the datasheet of the transistor we found the correlation of the equivalent resistance at different temperatures (e.g Fig 4 : Normalized On-Ressistance vs Temperature.):

$$R_{T,on}(125C) = 2 \cdot R_{T,on}(25C) = 0.32[\Omega]$$

The power loss due to conduction in the transistors (same for both) is given by:

$$P_{rDS} = R_{T,on} \cdot I_{T,rms}^2 + U_{D,0} \cdot I_{avg} = 0.32 \cdot 1.68^2[W] + 0 = 903.18[mW]$$

$U_{D,0} = 0$ because we calculate the loss in a MOSFET.

$P_{T,cond}|_{nom}$ =0.90 W

/ 4 pt.

Q21: TRANSISTOR SWITCHING LOSSES

Calculate the switching losses for one of your transistors at steady state operation with nominal data $P_{T,sw}|_{nom}$. Here not the temperature, but the proper scaling of the switching times and electrical values is crucial, for which the procedure can be found again in the provided INFINEON Application Notes.

The switching frequency and the energy storage capacity of the different possibilities (on and off) can determine the power loss due to switching in the transistors. The transistor can be on and off and both cases are studied for calculating the switching power loss.
From the datasheet and extra documents given in class we have:

- Reverse recovery charge $Q_{rr} = 0.85\,[\mu C]$

- Driver output voltage $U_{D,rr} = 15\,[V]$
- Converter supply (DC bus) voltage: $U_{DD} \approx 37[V]$
- Current fall time $t_{fi} = 24[ns]$
- Zero gate voltage drain current: $I_{D,off} = 250[\mu A]$
- Gate resistor: $R_G = 12\,[\Omega]$
- Reverse transfer capacitance: $C_{rss} = 60[pF]$
- Plateau voltage: $U_{plateau} = 6.8\,[V]$

Putting all this information together based on the answer block's first sentences. We can write:

$$E_{on} = \frac{Q_{rr} \cdot U_{D,rr}}{4} = \frac{0.85[\mu C] \cdot 15[V]}{4} = 3.19\,[\mu J] \qquad E_{off} = U_{DD} \cdot I_{Doff} \cdot \frac{t_{ru} + t_{fi}}{2} = 126.93\,[nJ]$$

$$t_{ru} = (U_{DD} - R_{DS,on} \cdot I_{D,on}) \cdot R_G \cdot \frac{C_{rss}}{U_{plateau}}$$

$$P_{sw} = f_{sw} \cdot (E_{on} + E_{off}) = 1.19\,[W]$$

$P_{T,sw}\|_{nom}$ = 1.19 W	/ 6 pt.

Q22: COMPARISON WITH THE LOSS TOOL

Use the Loss Tool to calculate the semiconductor losses in detail for the nominal operation point and compare them to your results. Comment deviations in case they appear. Read the comments in the code carefully to obtain valid results!

In these graphs, efficiency reaches its maximum at the highest U_{in}, following a curve $\propto \sqrt{x}$. At lower output power (10 W) the efficiency values stay around 96% whereas at 50 W output power the efficiency values vary between 88% and 94%. Thus, the variance of the efficiency values increases as the output power goes up.
In this particular case, efficiency is indeed maximized at the highest input voltage. However, the $\eta - U$ curve would more likely take on a parabolic shape over a broader range of input voltages.

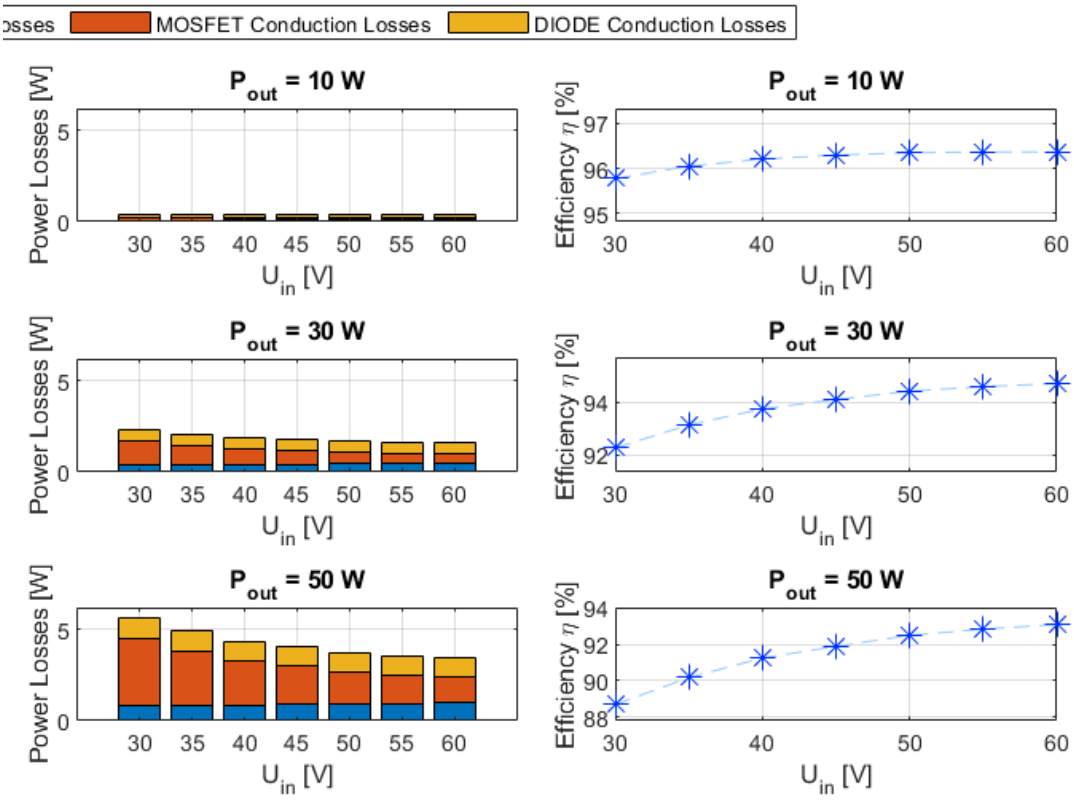


Figure 7 Semiconductor power losses and efficiencies achieved for different operating points.

/ 3 pt.

Q23: EFFICIENCY

Calculate the efficiency of your Flyback converter in nominal operation $\eta|_{nom}$, when only semiconductor losses are considered. Please note that there will be other losses in your converter that will appear during the design. Nevertheless, semiconductor losses are a good indication of the overall converter performance.

The efficiency represents the useful output energy relative to the total energy input

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{LS} + P_{out}} = \frac{1}{1 + \frac{P_{LS}}{P_{out}}} \Leftrightarrow \eta|_{nom} = \frac{1}{1 + \frac{P_{LS}}{P_{out,nom}}}$$

with P_{LS} all the power losses in the circuit. The main sources of power loss are introduced by the MOSFETs and diodes, e.g. conduction losses P_{cond}, switching losses P_{sw}, and blocking (leakage) losses P_b, although the last one is usually negligible. The transformer also introduces magnetizing losses P_{rL}, which are relatively small.
In the previous questions, we calculated the power losses under nominal conditions, with $P_{out,nom} = 50\,[W]$. So we have:

$$P_{LS} \approx P_{D,rec,cond} + 2 \cdot (P_{T,cond}) + P_{T,sw}$$

Substituting this value in the efficiency formula we obtain $\eta|_{nom} = 91.39\%$

We observe that the values obtained in the loss tool and our calculations are close but not identical. A possible reason for this discrepancy is that the values for $R_{DS,ON}$ and $U_{D,f}$ used in the program may differ from those specified in the datasheet.
(i.e. From the datasheet we have: $U_{df} = 0.95[V]$; $R_{ds,ON} = 95[m\Omega]$ in the code was used $U_{df} = 0.4[V]$; $R_{ds,ON} = 33[m\omega]$)

$\eta|_{nom}$ = 0.91

/ 3 pt.

Q24: LOSS TOOL

Use the provided Loss Tool to investigate the semiconductor losses for a set of different values of U_{in} and P_{out}. Comment on how the efficiency changes for the different operating points.

The range values of U_{in}; P_{out} where changed from $U_{in} \in [30, 60] \rightarrow U_{in} \in [30, 90]$ and $P_{out} \in [10, 50] \rightarrow P_{out} \in [10, 60]$.
In the graph for $P_{out} = 10[W]$ we observe a clear peak in the efficiency curve. In contrast, the two other curves with higher P_{out}, efficiency tends to stabilize to a plateau at higher values of U_{in}.

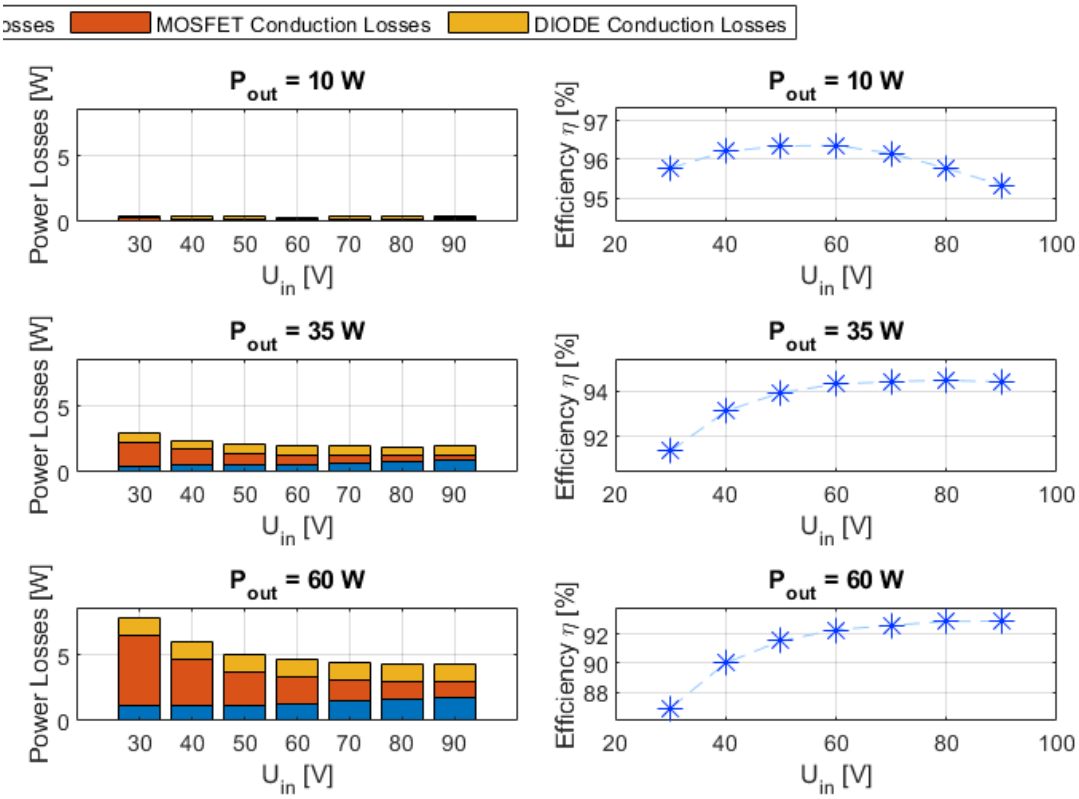


Figure 8 Semiconductor power losses and efficiencies achieved for different operating points.

/ 2 pt.

Q25: TRANSISTOR HEATSINK

To choose a proper heatsink, answer the following questions. For the calculations, assume a maximum ambient temperature of $\vartheta_a = 40\,^{\circ}\mathrm{C}$, whereas the semiconductor junction temperature should not exceed $\vartheta_j = 125\,^{\circ}\mathrm{C}$. Please note that there is already a thermal resistance from the junction to the case of the semiconductor.:

a) Considering the output of the previous question, determine the worst case operation condition for the transistor in terms of power losses $P_T|_{wc}$.
b) Calculate the maximum allowed thermal resistance $R_{th,T,j-a}$ (where $_{j-a}$ indicates junction to ambient).
c) Based on b), choose a heatsink from the selection provided in Table 6, they are also presented graphically in Fig. 9 (all images from the manufacturer websites). Elaborate briefly on your choice. Don't forget to highlight your selection in blue.

The largest (and thus worst case)power losses in the transistors observed with the loss tool are 6.45$[W]$ (= conduction and switching loss).
From the assignment we know the maximum desired temperature difference (between the maximum temperature under which the transistor should work and the ambient temperature is: $\Delta T = \theta_j - \theta_a = 85\,[K]$
Putting all that information together we obtain (with $R_{T,th,j-c} = 1.7\,[K/W]$ from the datasheet):

$$R_{th,T,j-a} = \frac{\Delta T}{P_T|_{wc}} - R_{th,j-c} = 11.47[K/W]$$

remark: due to the symmetry of the circuit, most values for the transistors are identical.

So, for this problem, we chose heatsink No. 4 as it has the highest $R_{th,j-a}$ while still meeting the requirements. A lower $R_{th,j-a}$ would require more engineering and be more expensive.

$P_{T1}\|_{wc}$ =	6.45 W	$R_{th,T1,j-a}$ =	11.47 K W^{-1}	T1 heatsink model No. :	4
$P_{T2}\|_{wc}$ =	6.45 W	$R_{th,T2,j-a}$ =	11.47 K W^{-1}	T2 heatsink model No. :	4

/ 3 pt.

Q26: RECTIFYING DIODE HEATSINK

Similar to the transistor, a diode heatsink has to be selected. Assuming the same thermal constraints, answer the following questions:

a) Considering the output of the Loss Tool, determine the worst case operation condition for the diode in terms of losses $P_D|_{wc}$.
b) Calculate the maximum allowed thermal resistance $R_{th,D,rec,j-a}$.
c) Select a suitable heatsink from the selection provided in Table 6 (highlight in green) Elaborate briefly on your choice..

The largest (and thus worst case) power losses observed in the Rectifying Diode with the loss tool are 1.39$[W]$ (= conduction and switching loss).
From the assignment we know the maximum desired temperature difference (between the maximum temperature under which the transistor should work and the ambient temperature is: $\Delta T = \theta_j - \theta_a = 85\,[K]$
Putting all that information together we obtain (with $R_{th,j-c} = 4\,[K/W]$ from the datasheet):

$$R_{th,T,j-a} = \frac{\Delta T}{P_D|_{wc}} - R_{th,j-c} = 57.15[K/W]$$

So, for this problem, we chose heatsink No. 7 as it has the highest $R_{th,j-a}$ while still meeting the requirements. A lower $R_{th,j-a}$ would require more engineering and be more expensive.

$P_D\|_{wc}$ = 1.39	$R_{th,D,rec,j-a}$ = 57.15 K W^{-1}	Diode heatsink model No. : 7	/ 3 pt.

Q27: CLAMPING DIODE HEATSINK

Also the cooling for the clamping diode needs to be assessed. Assuming the same thermal constraints, answer the following questions:

a) Considering the output of the Loss Tool, determine the worst case operation condition for the diode in terms of losses $P_D|_{wc}$.
b) Calculate the maximum allowed thermal resistance $R_{th,D,C,j-a}$.
c) Select a suitable cooling option. Provide an explanation for your choice.

The loss tool doesn't provide loss values for the clamping diodes. So we based our calculations on the power loss derived in *question 19*:

From the datasheet of the clamping diodes we have:

- $U_{D,f} = 0.7\,[V]$
- Operating point of the diode is between -65 and 175 °C)
- derived from the datasheet: $R_{D,on} \approx \frac{U_{D,f}}{I_{D,f}} = 70[m\Omega]$

Thus, the conduction losses for the clamping diode are:

$$P_{D,\text{clamp, cond}} = U_{D,f} \cdot I_{D,\text{avg}} + R_{D,on} \cdot I^2_{D,\text{rms}} = 0.251\,[W]$$

Using the same formulas as above to determine the heatsink resistance, we obtain:

$$R_{th,T,j-a} = \frac{\Delta T}{P_D|_{\text{wc}}} - R_{th,j-c} = 336.65\,[K/W]$$

where $R_{th,j-c} = 2\,[K/W]$
Given that the power loss is relatively small, a large PCB copper area should be used to cool the clamping diode.

$P_D\|_{wc}$ = 0.25	$R_{th,D,C1,j-a}$ = 336.65 K W^{-1}	Diode D_{C1} heatsink model No. : N/A	
$P_D\|_{wc}$ = 0.25	$R_{th,D,C1,j-a}$ = 336.65 K W^{-1}	Diode D_{C2} heatsink model No. : N/A	/ 3 pt.

Table 6 List of the offered heatsinks.

No.	Manufacturer	Product	R_{th} (K W^{-1})	Figure
1	Ohmite	FA-T220-64E	3.00	9a
2	Ohmite	FA-T220-25E	4.70	9a
3	Ohmite	EA-T220-51E	7.50	9b
4	Ohmite	EA-T220-38E	10.40	9b
5	Wakefield-Vette	265-118ABHE-22	14.00	9c
6	Ohmite	E2A-T220-25E	16.40	9d
7	Wakefield-Vette	OMNI-220-18-25-1C	24	9e
8	Wakefield-Vette	OMNI-220-18-50-2C	12	9f
9	Wakefield-Vette	OMNI-220-18-75-3C	8	9g

(a) Ohmite FA-T220-xxE

(b) Ohmite EA-T220-xxE

(c) Wakefield 265-118ABHE-xx

(d) Ohmite E2A-T220-xxE

(e) Wakefield OMNI 220 18 25 1C

(f) Wakefield OMNI 220 18 50 2C

(g) Wakefield OMNI 220 18 75 3C

Figure 9 The available heatsinks.

REPORT 1 SUMMARY

Fill out the table below with your results as well as your chosen devices:

Table 7 Calculated parameter values, selected components and efficiency.

Property	Value	Unit
N	1.15	–
$D\|_{U_{in,nom}}$	0.356	–
L_m	51.59	µH
C_{out}	1.16	µF
C_{in}	625.00	µF
Switch no.	7	–
Diode no.	2	–
$\eta\|_{U_{in,nom}}$	0.91	–
Switch heatsink no.	4	–
Diode heatsink no.	7	–

Total:	/ 100 pt.