MONASH University
MALAYSIA

SCHOOL OF ENGINEERING

ELECTRICAL AND COMPUTER SYSTEMS ENGINEERING

LABORATORY REPORT MARKING RUBRIC

ECE3051: ELECTRICAL ENERGY SYSTEMS

Experiment Number: 4

Title of Lab Sheet: _____

Group Number: _____

No.	Student ID	Name of Group Members	Total Marks
1	30720230	Loh Jia Quan	97/100
2	31106889	Agill Kumar Saravanan	97/100
3	30719305	Huan Meng Hui	97/100
4	32194471	Tan Jin Chun	97/100
5	32259417	Chong Yen juin	97/100

MARKS BREAKDOWN

Section	*Total Score*	*Actual Marks*	*Scoring Band*	*Criteria*	*Comment*
Results	*40*		*30-40*	*Clear and completely labelled figures of the experiment/simulation results with justifications and tables. A detailed caption is provided for each figure with an in-text figure reference. The x-axis and y-axis are labelled with the unit in the bracket. The legend is provided whenever it is deemed to be required. If there is more than one line, the lines should be clearly distinguishable with the visible difference such as dotted line, dashed line and solid line, even in black and white.*	40
			20-30	*Some of the figures of the experiment/simulation setup are not clear, do not have any labelling/ caption/ in-text caption reference/ distinguishable multiple lines and are blurry. The table and justification have mistakes or errors.*	
			0-20	*Insufficient amounts of figures and labelling of the experiment/simulation layout setup, which is not correct and/or unclear. The table is not filled.*	
Discussion	*40*		*30-40*	*Complete data collection and presentation using tables/figures/ graphs with appropriate labels. Discussion of the results with prudent judgment. Have a comparison of the measured results with theoretical values and in-text citations from the peer-reviewed references. The comprehensive comparison, evaluation and justification of the results are given with clear explanation to demonstrate the understanding of the laboratory.*	40
			20-30	*The discussion shows little understanding of what the experiment/simulation is all about. Brief comparison, evaluation and justification of the results, with unclear/ incorrect explanation on the theoretical and experimental/ simulation results.*	
			0-20	*Only restatement of the results without commenting on the expected key points. Incorrect judgment/ arguments were used. No comparison, evaluation and justification of the results, with an unsatisfactory explanation on the theoretical and experimental/ simulation results.*	
Conclusion, References and Appendix	*20*		*15-20*	*Explained how the aims of the experiment have been achieved. The key features of the methods used, the most important results and the findings of the laboratory have been summarized. Complete references list to any book, articles and websites is provided with proper in-text citations in correct formatting. The appendix is provided in detail.*	17

			10-15	*A conclusion is drawn but is not supported by the experimental/ simulation evidence and a clear understanding of the findings. Incomplete references to the books or any other sources used in the report and the in-text citations are inappropriate or incorrect. The appendix is partially provided.*	
			0-10	*No sensible conclusion. The referencing is presented in the wrong format. No evidence, attachments, appendices are attached. Irrelevant referencing was used. Unclear understanding of the experiment without a summarized conclusion and the evidence of results. No appendix is provided.*	
Total	*100*				97

Examiner/ Assessor of ECE3051: Electrical Energy Systems
Date: 5/5/2023

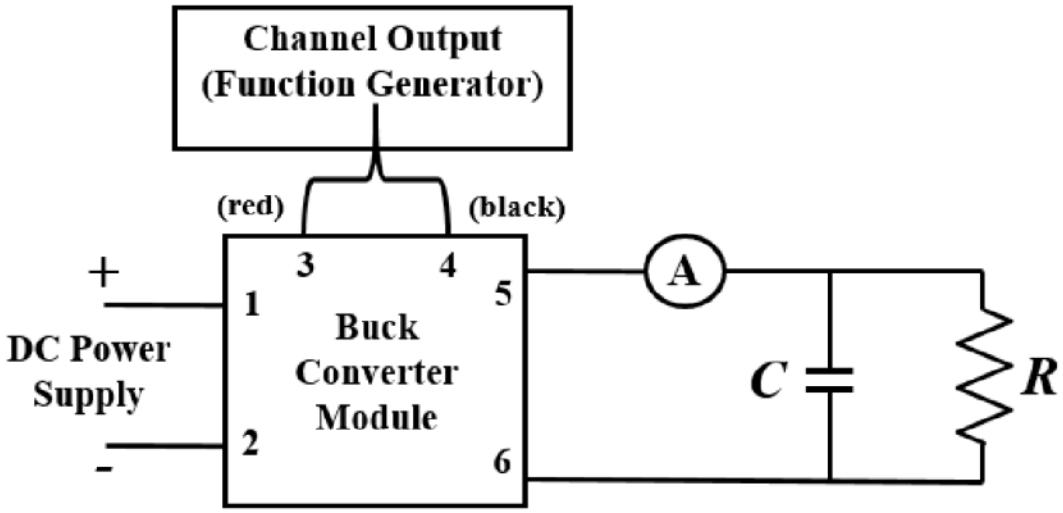
To-Do

Set the resistive load to 20 Ω.

Connect all three phases of the capacitive load in series.

Take the capacitance value for every Knob position using an LCR meter. The power must be off during taking the measurement.

For experimental setup, follow the connection scheme shown in Figure 5.



DC power supply is used for providing input voltage for the buck converter module.

Be careful about DC polarity.

The arbitrary function generator is used to provide PWM switching pulses of required frequency and duty cycle for the buck converter

Turn the DC power supply on and set the DC supply to 15 V.

Next, turn the arbitrary function generator on and select ‘Pulse’ in ‘Continuous ‘ mode with frequency of 1 kHz. Set the duty ratio as 30%, amplitude as 5 V and the offset as 2.5 V.

Repeat the exercise for each of the knob position of the capacitor load. Compare the calculated values with the theoretical values

Take reading of average output voltage and output voltage ripple (How to get ripple from CRO ?) for duty ratio of 50% and 70% for each of the knob position of the capacitor load

checked

EXPERIMENT 4

DC-DC Buck Converter

1. Experimental Setup [10 Marks]

(Draw the circuit of the buck converter (5 marks) and label the components (5 marks))

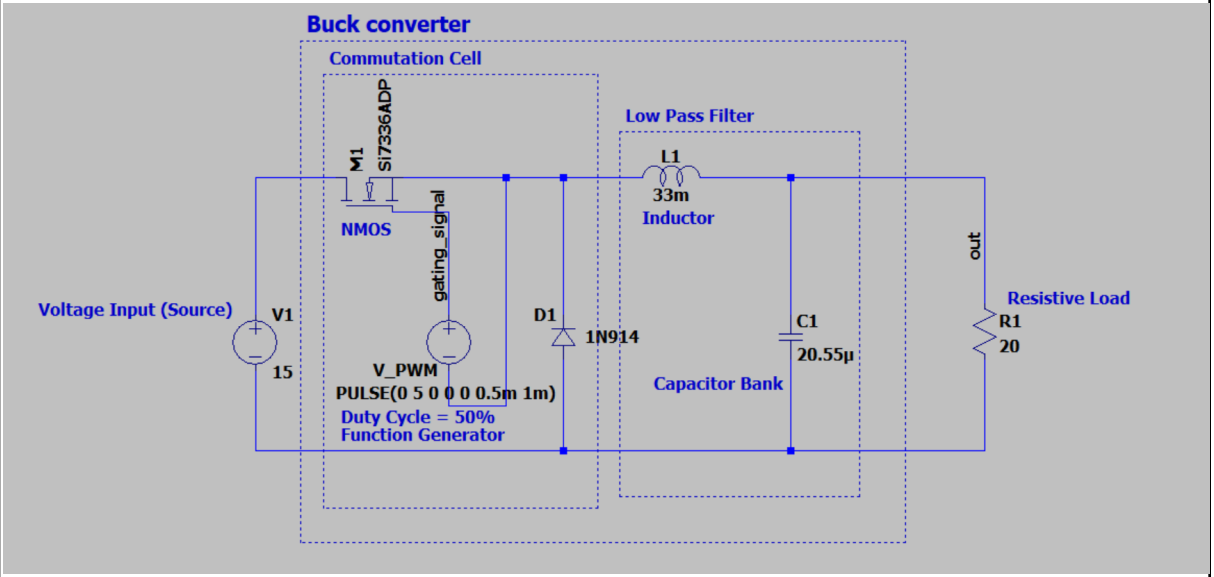


Figure 1. LTSPICE Schematic of Buck Converter

Investigation of voltage ripple

(1) Duty cycle of 30%

Calculate the output voltage ripple for each knob position [2 marks]

(Include your calculations for determining the output voltage ripple for each knob position.)

Output Voltage Ripple

$$\Delta v_0 = \frac{V - V_0}{16LC} D T_s^2$$

Constants
V = 15V
L = 33mH
Ts = 1ms
Fs = 1000Hz
D = 0.3

Knob 1
C =3.348uF
V0 = 3.1V

$$\Delta v_0 = \frac{V - V_0}{16(33m)C}(0.3)(1m)^2 = 2.0195\ V$$

checked

Knob 2
C = 6.734uF
V0 =3.37 V

$$\Delta v_0 = \frac{V - V_0}{16(33m)C}(0.3)(1m)^2 = 0.9812\ V$$

Knob 3
C = 10.068uF
V0 = 3.71V

$$\Delta v_0 = \frac{V - V_0}{16(33m)C}(0.3)(1m)^2 = 0.6371\ V$$

Knob 4
C = 13.408uF
V0 = 4.04V

$$\Delta v_0 = \frac{V - V_0}{16(33m)C}(0.3)(1m)^2 = 0.4644\ V$$

Knob 5
C = 16.755uF
V0 =4.03 V

$$\Delta v_0 = \frac{V - V_0}{16(33m)C}(0.3)(1m)^2 \Delta v_0 = 0.3720\ V$$

Knob 6
C = 20.11uF
V0 =4.03 V

$$\Delta v_0 = \frac{V - V_0}{16(33m)C}(0.3)(1m)^2 = 0.3099\ V$$

Theoretical Output Voltage

$$V_0 = DV = 0.3(15) = 4.5V$$

Table Results [3 marks]

Table I. Voltage Ripple and Capacitance Value with Duty Cycle = 30%

Knob position	*Capacitance value (F)*	*Average output voltage (V) (from multimeter)*	*Theoretical average output voltage (V) (calculation)*	*Output voltage ripple (V) (from oscilloscope)*		*Theoretical output voltage ripple (V) (calculation)*	*Simulation output voltage ripple (V)*
				Voltage ripple	*Peak-to-peak voltage*		
1	*3.348u*	*3.1*	*4.5*		*15.6*	*2.0195*	*0.8525*
2	*6.734u*	*3.37*	*4.5*		*13.2*	*0.9812*	*0.6825*
3	*10.068u*	*3.71*	*4.5*		*11.8*	*0.6371*	*0.5375*
4	*13.408u*	*4.04*	*4.5*		*10.2*	*0.4644*	*0.4250*
5	*16.755u*	*4.03*	*4.5*		*9.6*	*0.3720*	*0.3500*
6	*20.11u*	*4.03*	*4.5*		*7.8*	*0.3099*	*0.3000*

Show the output voltage ripple waveform (using CRO) for each knob position [3 marks]

(minus 1 mark)

checked

(Insert a picture of your output voltage ripple waveform (using CRO) for each knob position)

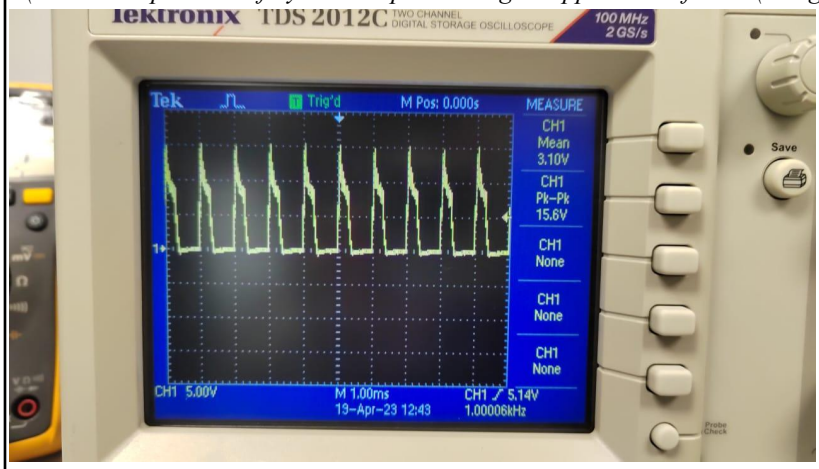


Figure 2 Output voltage waveform for C = 3.348uF and D = 0.3; y-axis is voltage (V) and x-axis is time (ms)

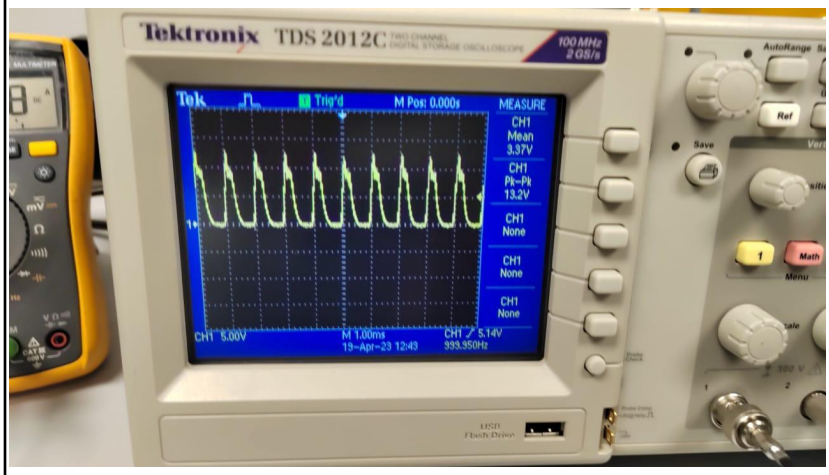


Figure 3 Output voltage waveform for C = 6.734uF and D = 0.3.; y-axis is voltage (V) and x-axis is time (ms)

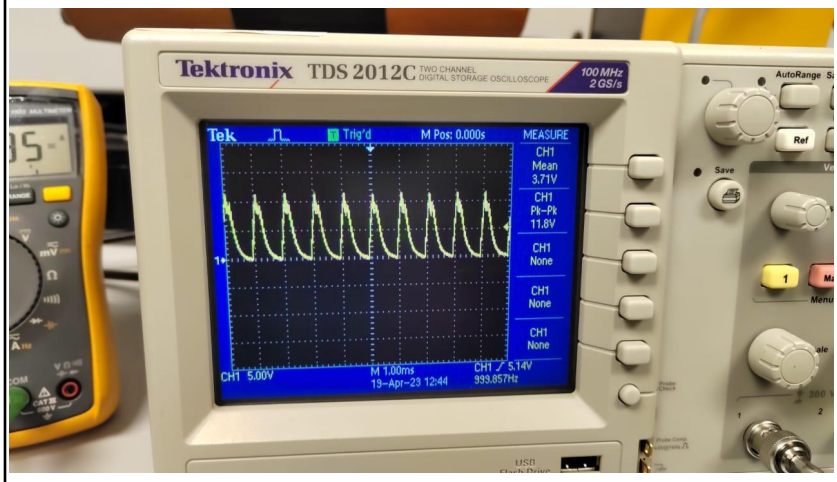


Figure 4 Output voltage waveform for C =10.068μF and D = 0.3.; y-axis is voltage (V) and x-axis is time (ms)

checked

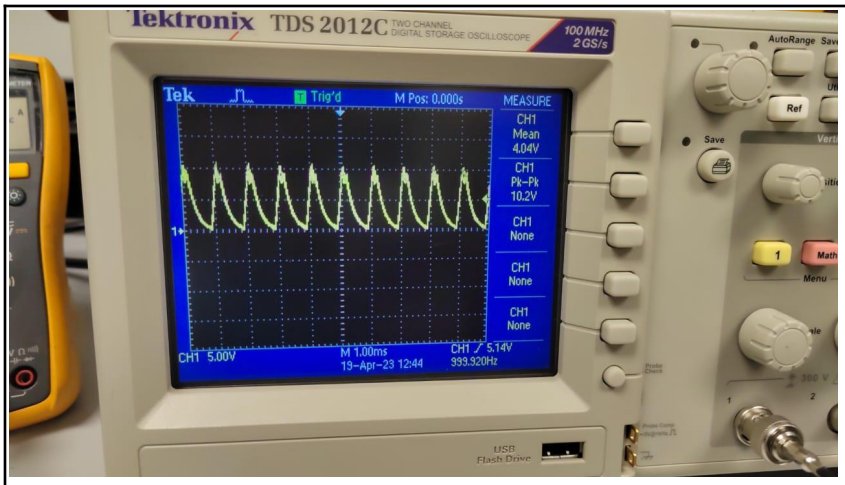


Figure 5 Output voltage waveform for C = 13.408*μF and D = 0.3.; y-axis is voltage (V) and x-axis is time (ms)*

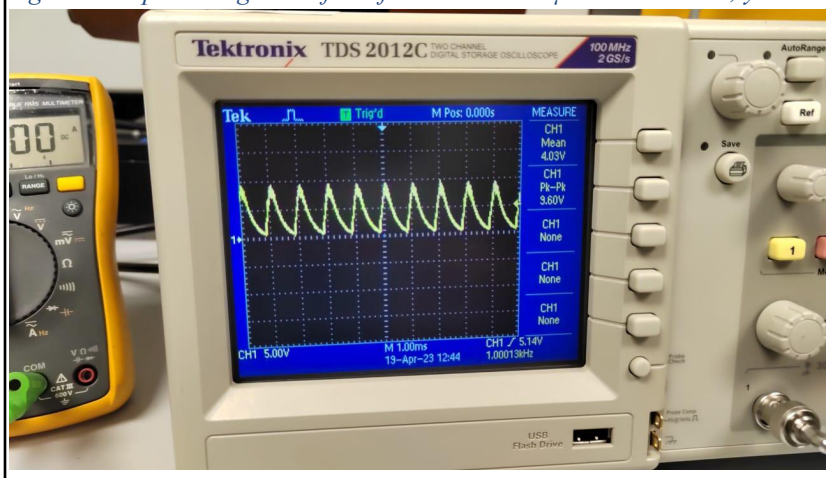


Figure 6 Output voltage waveform for C = 16.755*μF and D = 0.3.; y-axis is voltage (V) and x-axis is time (ms)*

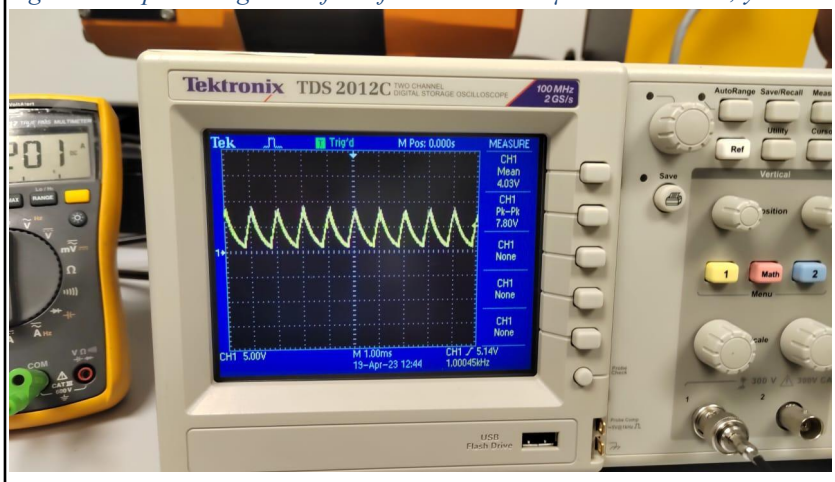


Figure 7 Output voltage waveform for C = 20.11*μF and D = 0.3.; y-axis is voltage (V) and x-axis is time (ms)*

Show the output voltage ripple waveform (from simulation) for each knob position [2 marks]

(Insert a picture of your output voltage ripple waveform (from simulation) for each knob position)

checked

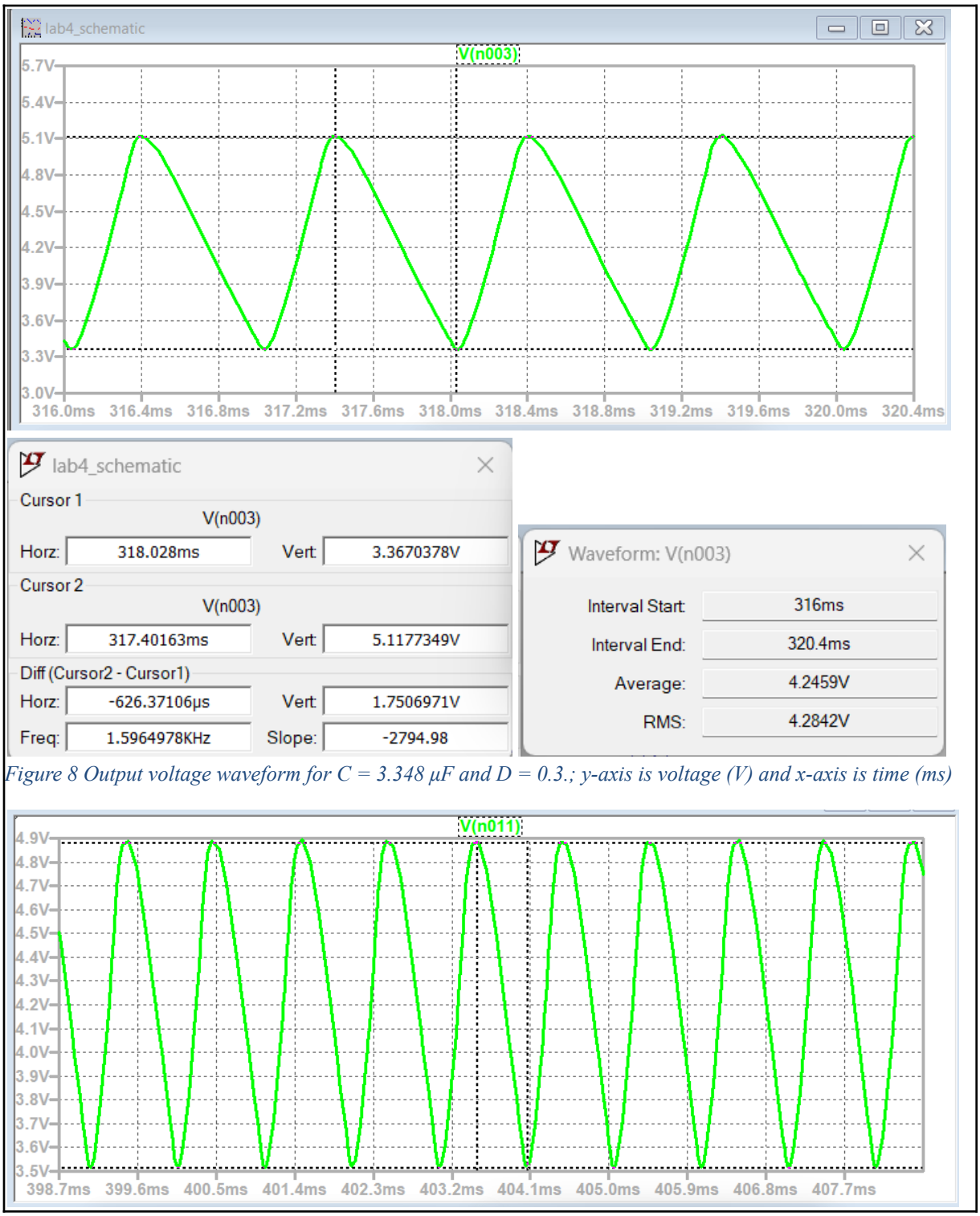


Figure 8 Output voltage waveform for C = 3.348 µF and D = 0.3.; y-axis is voltage (V) and x-axis is time (ms)

checked

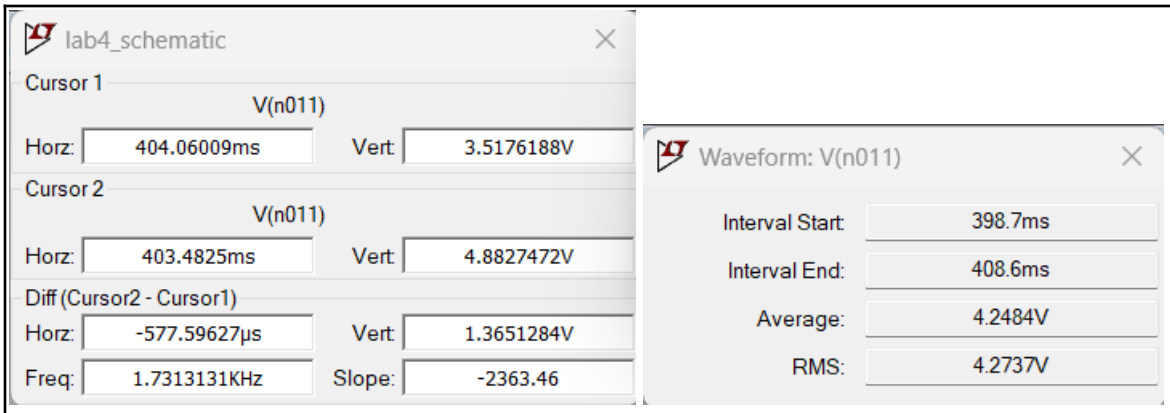


Figure 9 Output voltage waveform for C = 6.734 µF and D = 0.3.; y-axis is voltage (V) and x-axis is time (ms)

Figure 10 Output voltage waveform for C = 10.068 µF and D = 0.3.; y-axis is voltage (V) and x-axis is time (ms)

checked

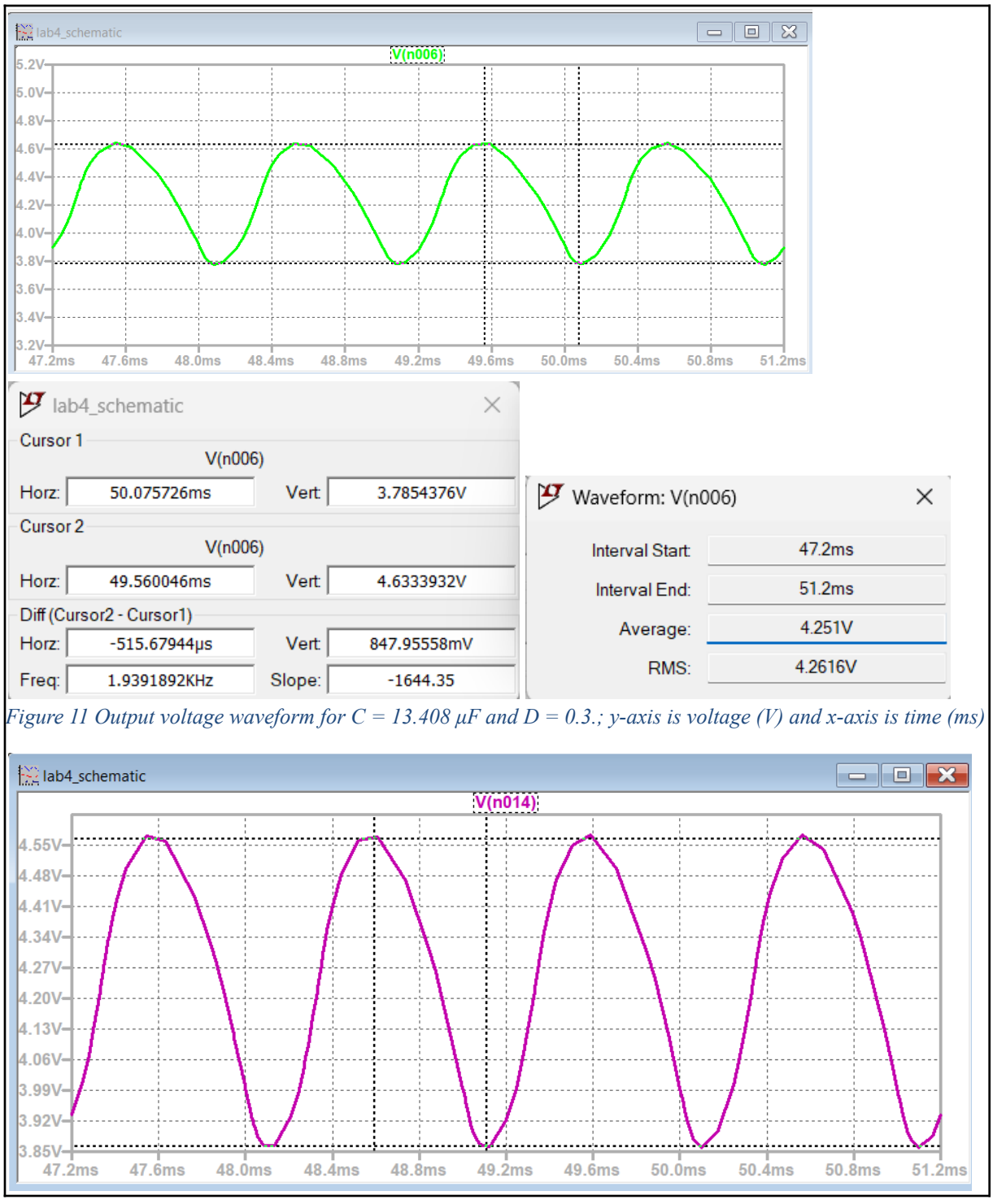


Figure 11 Output voltage waveform for C = 13.408 µF and D = 0.3.; y-axis is voltage (V) and x-axis is time (ms)

checked

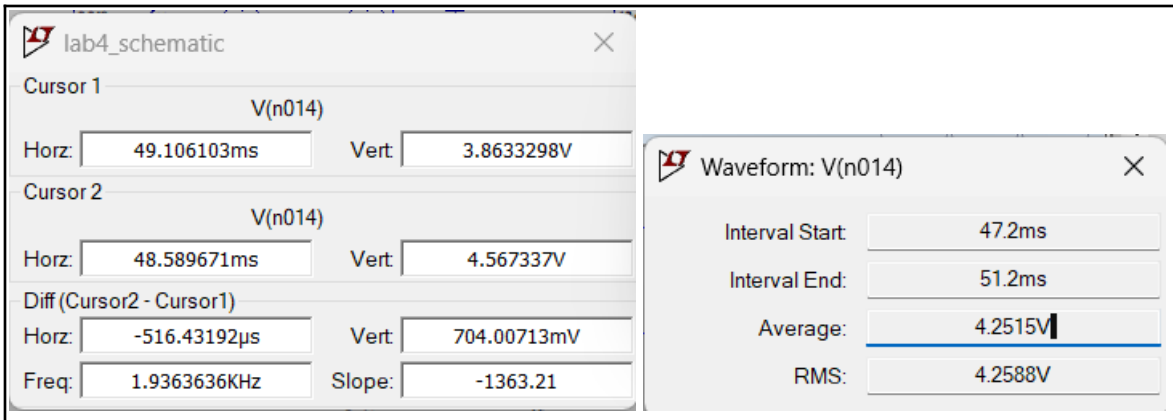


Figure 12 Output voltage waveform for C = 16.755µF and D = 0.3.; y-axis is voltage (V) and x-axis is time (ms)

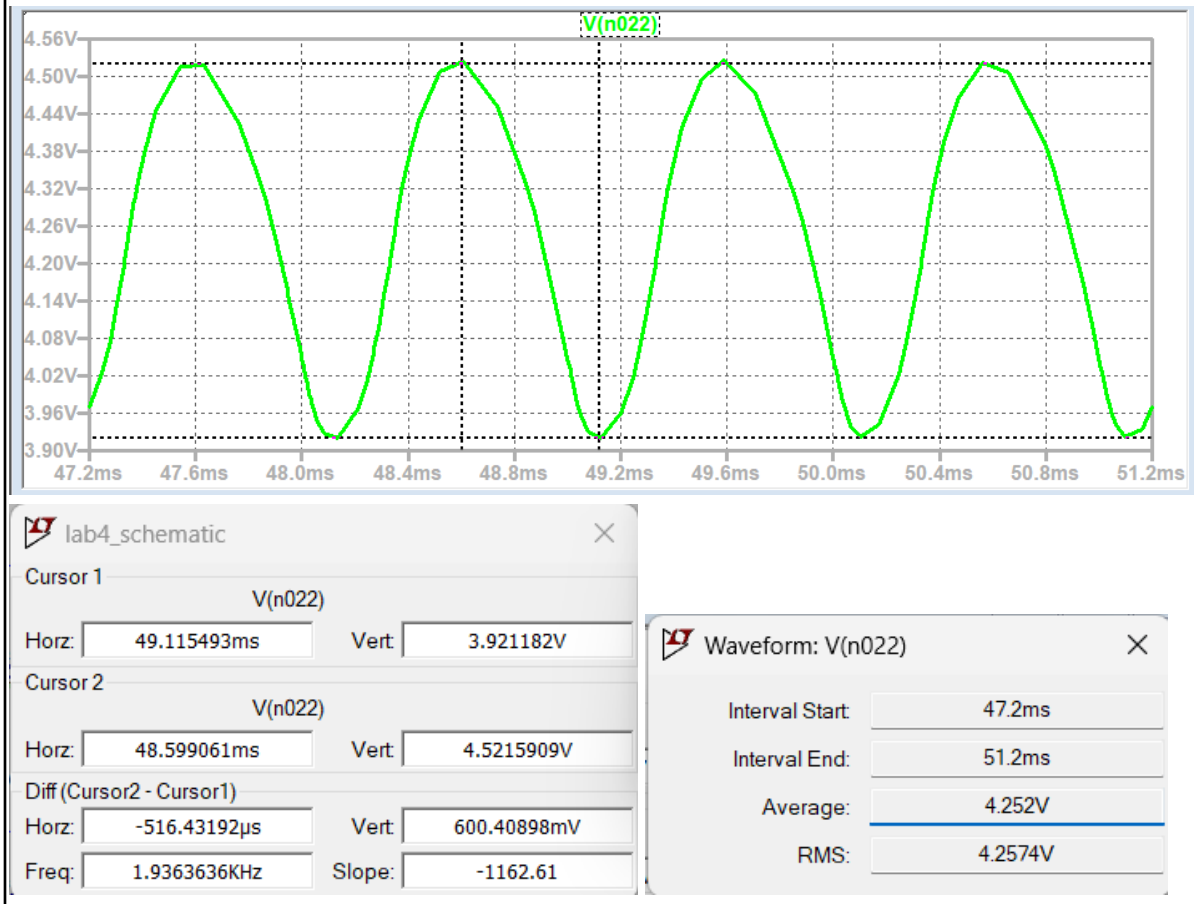


Figure 13 Output voltage waveform for C = 20.1 µF and D = 0.3.; y-axis is voltage (V) and x-axis is time (ms)

(2) Duty cycle of 50%

Calculate the output voltage ripple for each knob position [2 marks]

(Include your calculations for determining the output voltage ripple for each knob position.)

Output Voltage Ripple

$$\Delta v_0 = \frac{V - V_0}{16LC} D T_s^2$$

Constants
V = 15V
L = 33mH
Ts = 1ms

checked

Fs = 1000Hz
D = 0.5

Knob 1
C =3.348u F
V0 = 5.36V

$$\Delta v_0 = \frac{V - V_0}{16(33m)C}(0.5)(1m)^2 = 2.7549V$$

Knob 2
C =6.734u F
V0 =5.57 V

$$\Delta v_0 = \frac{V - V_0}{16(33m)C}(0.5)(1m)^2 = 1.326V$$

Knob 3
C =10.068u F
V0 = 5.94V

$$\Delta v_0 = \frac{V - V_0}{16(33m)C}(0.5)(1m)^2 = 0.8521V$$

Knob 4
C = 13.408uF
V0 = 6.23V

$$\Delta v_0 = \frac{V - V_0}{16(33m)C}(0.5)(1m)^2 = 0.6194V$$

Knob 5
C =16.755u F
V0 =6.49 V

$$\Delta v_0 = \frac{V - V_0}{16(33m)C}(0.5)(1m)^2 = 0.481V$$

Knob 6
C =20.11u F
V0 = 6.68V

$$\Delta v_0 = \frac{V - V_0}{16(33m)C}(0.5)(1m)^2 = 0.3918V$$

Theoretical Output Voltage

$$V_0 = DV = 0.5(15) = 7.5V$$

Table Results [3 Marks]

Table II. Voltage Ripple and Capacitance Value with Duty Cycle = 50%

Knob position	*Capacitance value (F)*	*Average output voltage (V) (from multimeter)*	*Theoretical average output voltage (V) (calculation)*	*Output voltage ripple (V) (from oscilloscope)*		*Theoretical output voltage ripple (V) (calculation)*	*Simulation output voltage ripple (V) (calculation)*
				Voltage ripple	*Peak-to-peak voltage*		
1	*3.348u*	*5.26*	*7.5*		*16.8*	*2.7549*	*1.0170*
2	*6.734u*	*5.57*	*7.5*	?	*14.0*	*1.326*	*0.7920*
3	*10.068u*	*5.94*	*7.5*		*12.8*	*0.8521*	*0.6115*
4	*13.408u*	*6.23*	*7.5*		*10.8*	*0.6194*	*0.4890*
5	*16.755u*	*6.49*	*7.5*		*9.4*	*0.4809*	*0.3960*
6	*20.11u*	*6.68*	*7.5*		*8.8*	*0.3917*	*0.3310*

Show the output voltage ripple waveform (using CRO) for each knob position [3 marks] checked

(Insert a picture of your output voltage ripple waveform (using CRO) for each knob position)

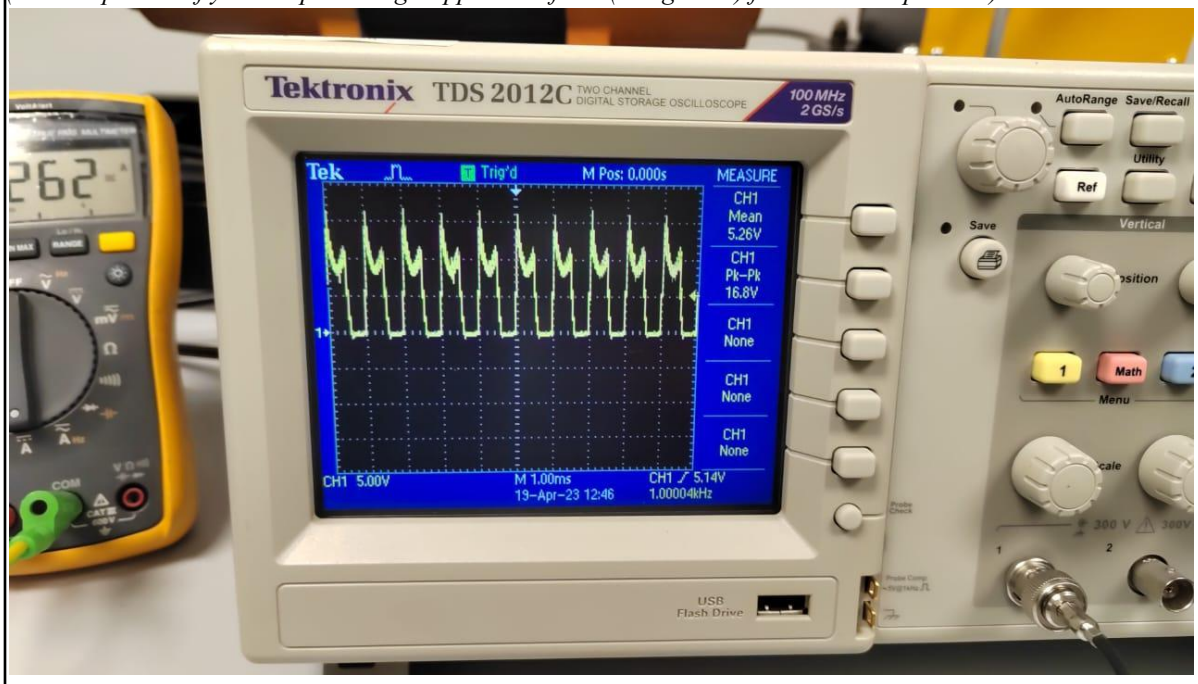


Figure 14 Output voltage waveform for C = 3.348μF and D = 0.5.; y-axis is voltage (V) and x-axis is time (ms)

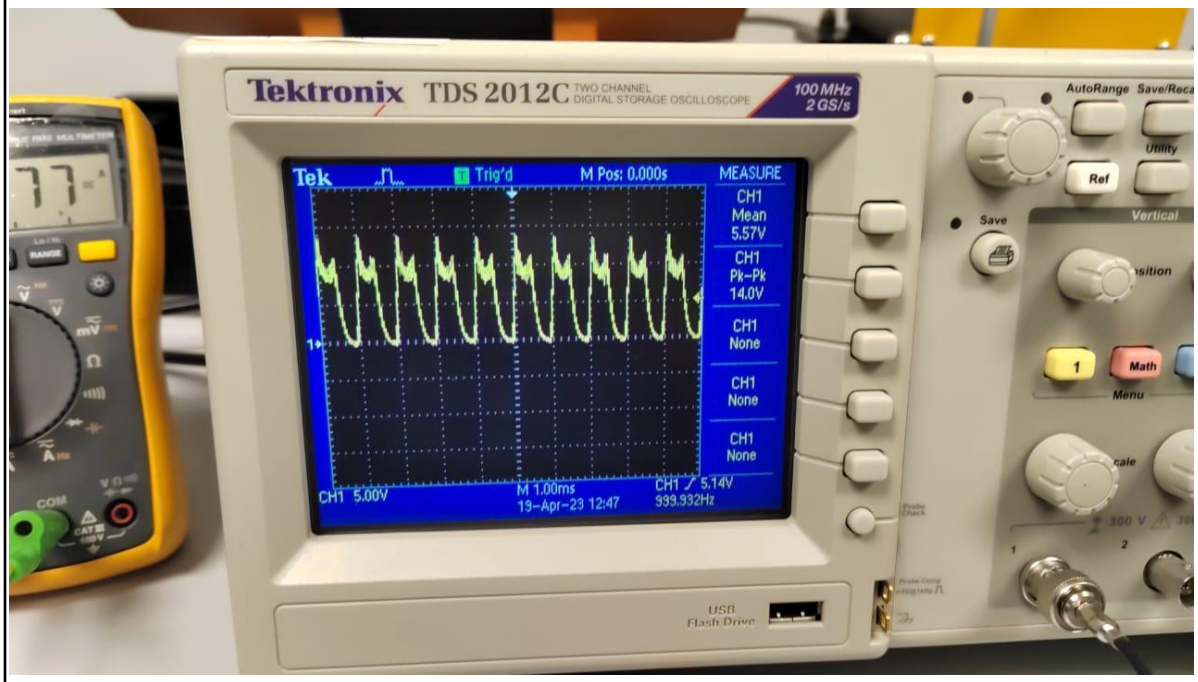


Figure 15 Output voltage waveform for C = 6.734μF and D = 0.53.; y-axis is voltage (V) and x-axis is time (ms)

checked

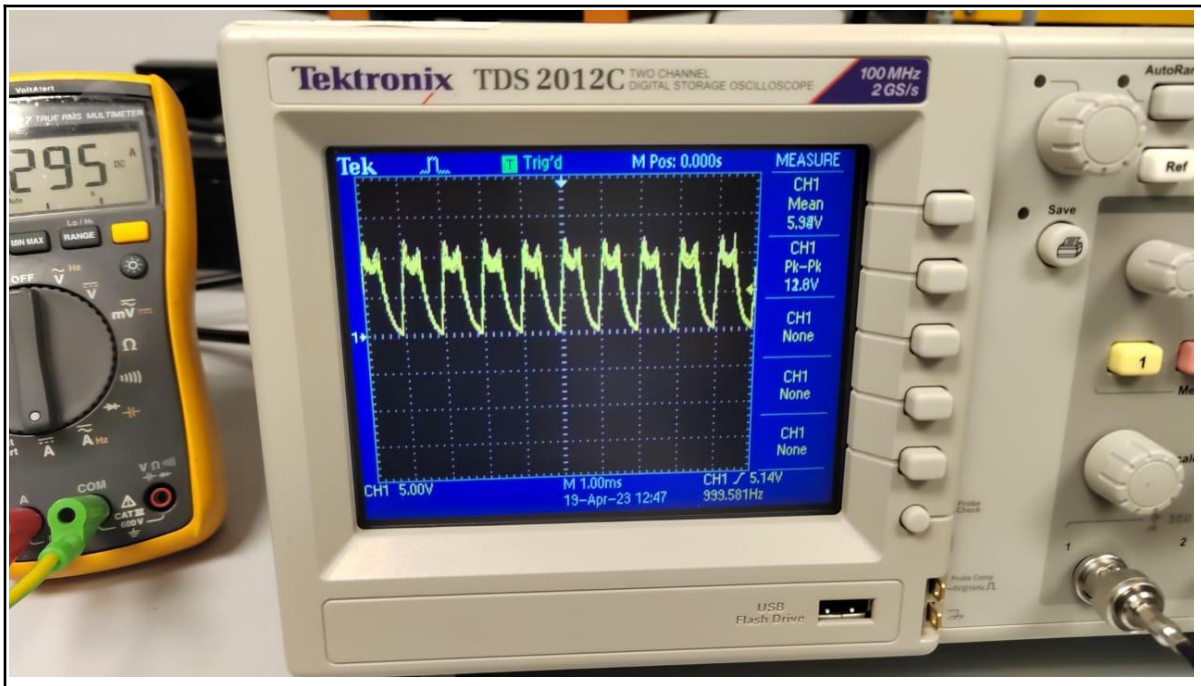


Figure 16 Output voltage waveform for C = 10.068μF and D = 0.5.; y-axis is voltage (V) and x-axis is time (ms)

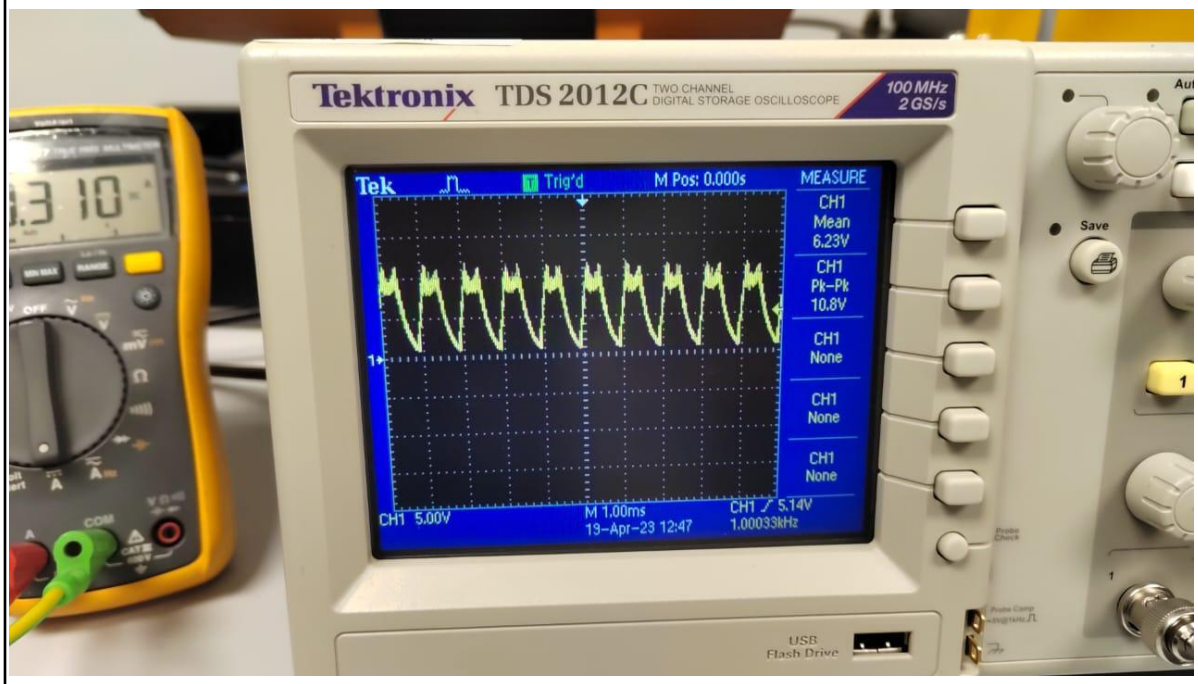


Figure 17 Output voltage waveform for C = 13.408μF and D = 0.5; y-axis is voltage (V) and x-axis is time (ms)

checked

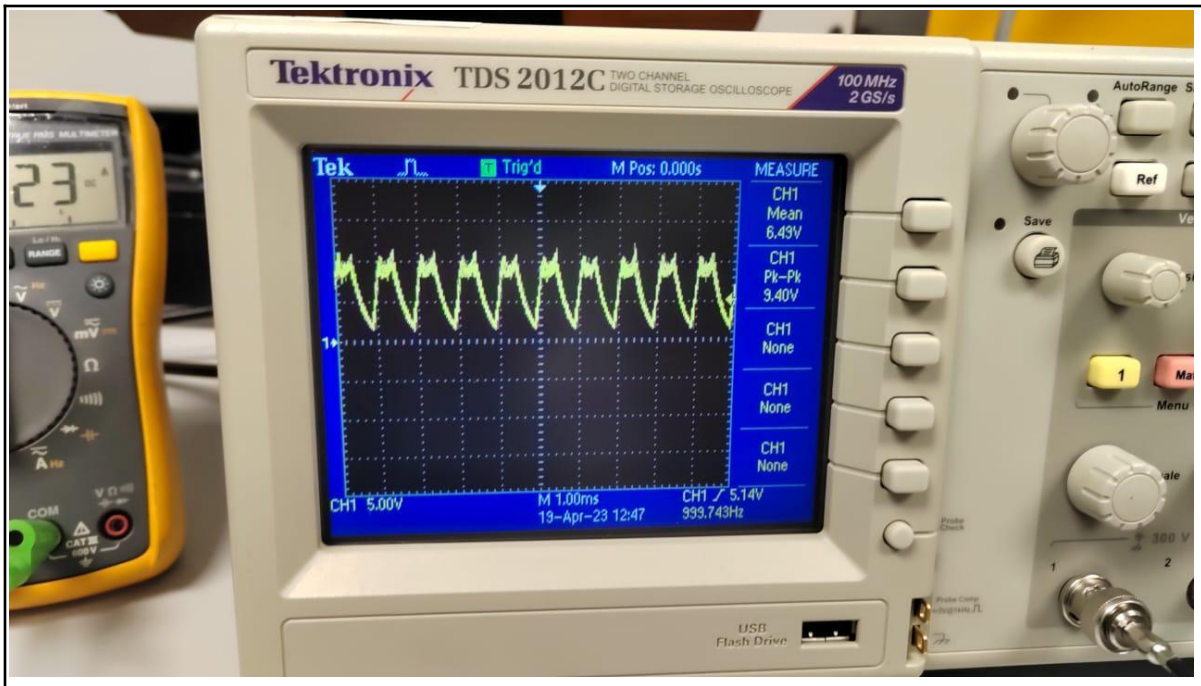


Figure 18 Output voltage waveform for C = 16.755*μF and D = 0.5; y-axis is voltage (V) and x-axis is time (ms)*

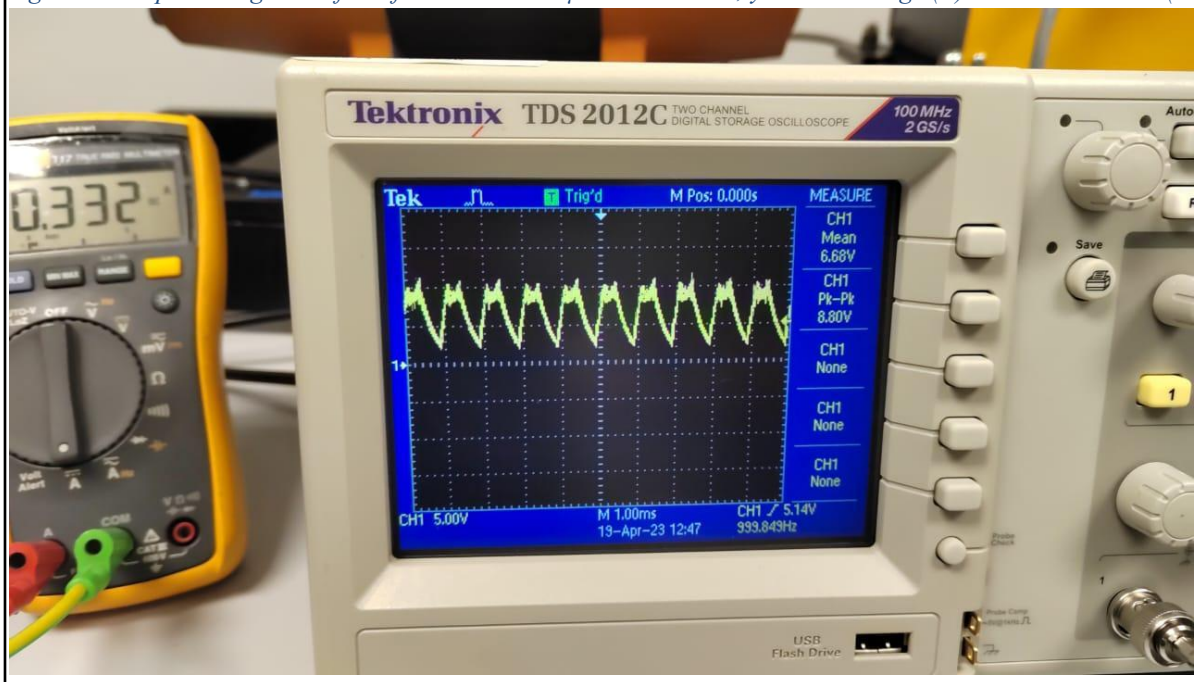


Figure 19 Output voltage waveform for C = 20.11*μF and D = 0.5; y-axis is voltage (V) and x-axis is time (ms)*

Show the output voltage ripple waveform (from simulation) for each knob position [2 marks]

(Insert a picture of your output voltage ripple waveform (from simulation) for each knob position)

checked

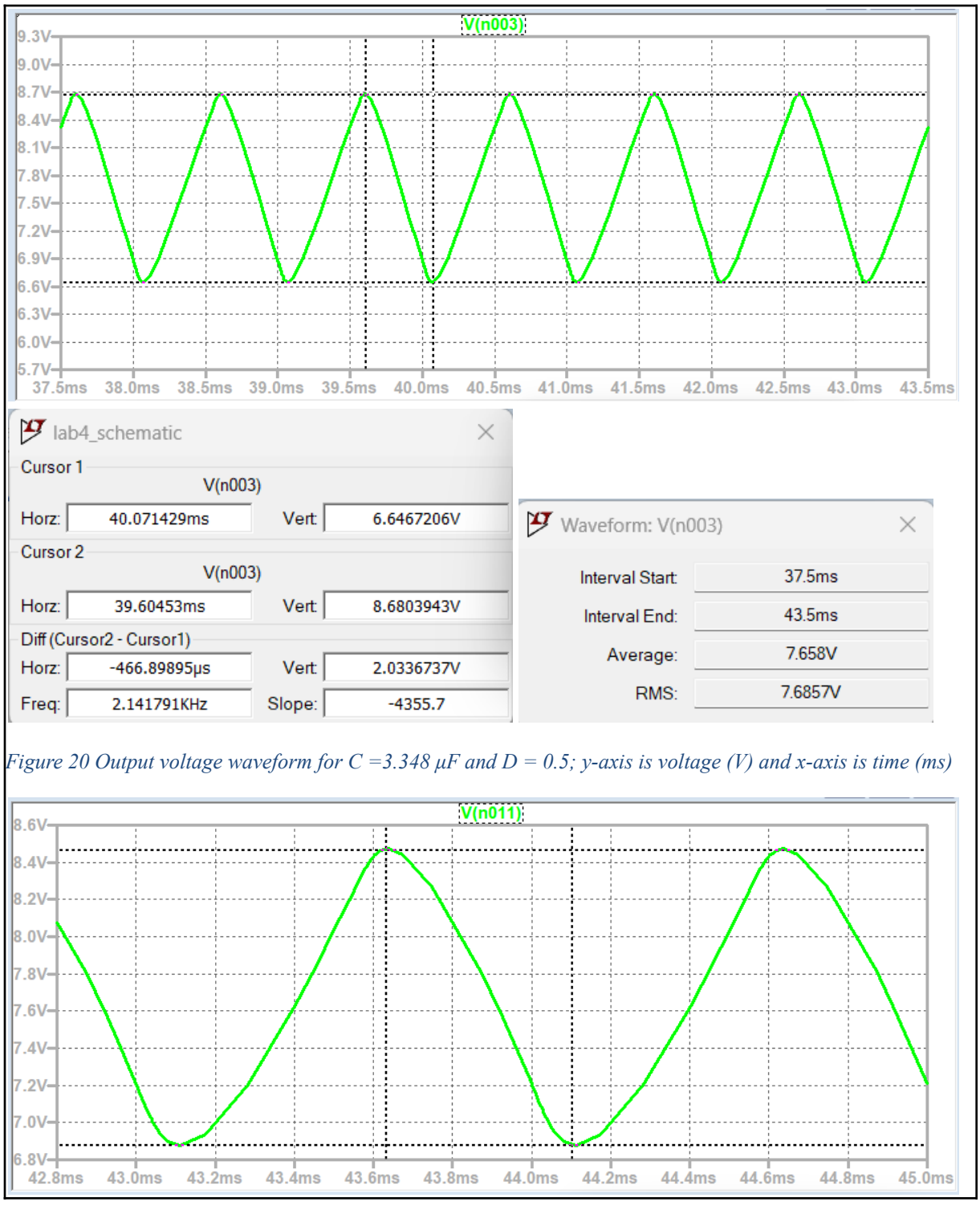


Figure 20 Output voltage waveform for C =3.348 µF and D = 0.5; y-axis is voltage (V) and x-axis is time (ms)

checked

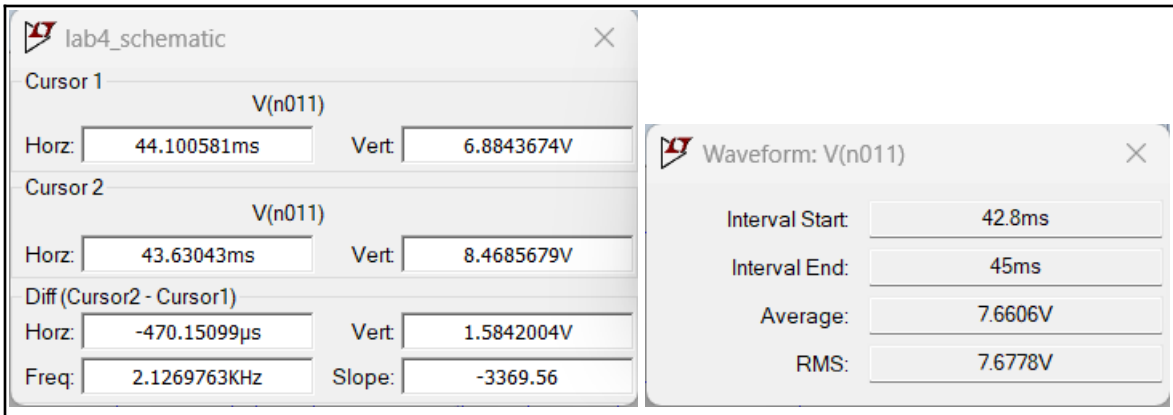


Figure 21 Output voltage waveform for C =6.734 µF and D = 0.5; y-axis is voltage (V) and x-axis is time (ms)

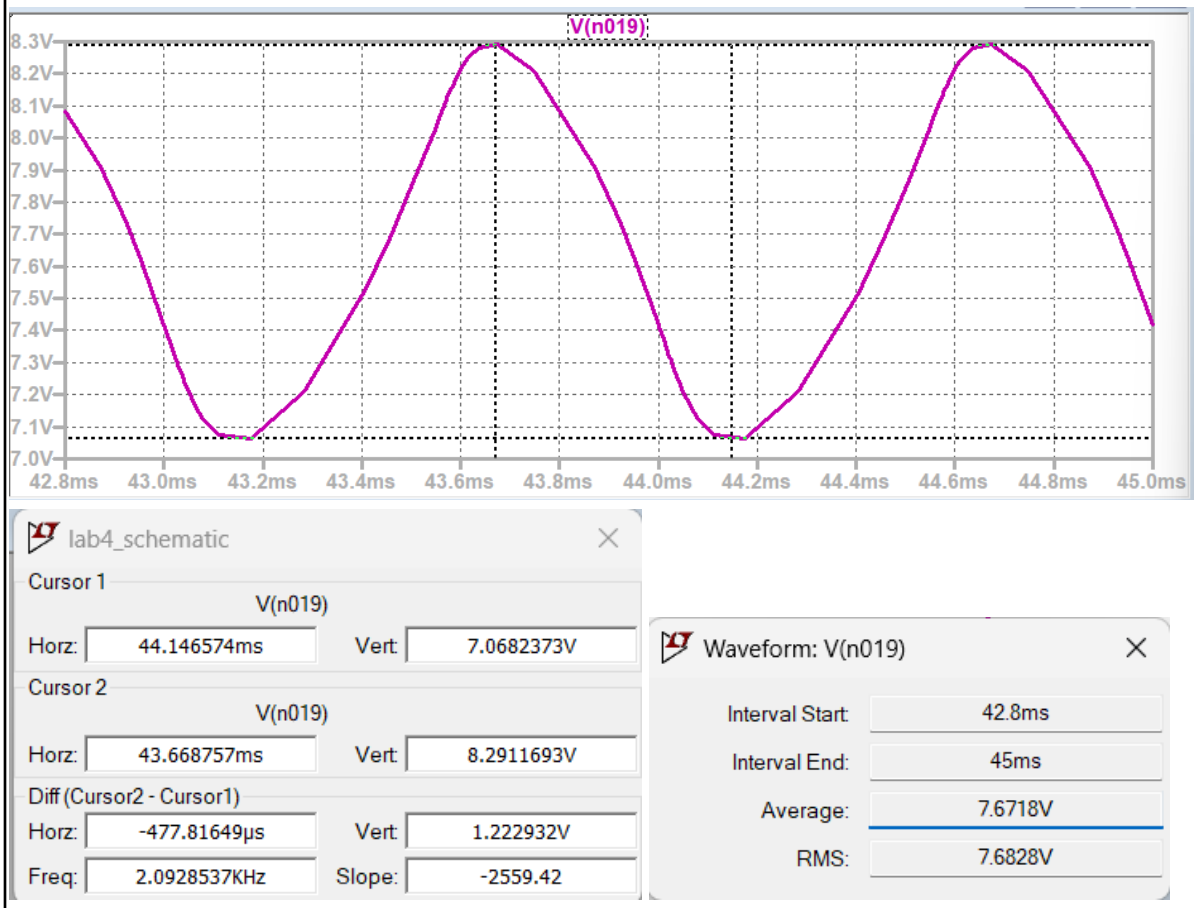


Figure 22 Output voltage waveform for C = 10.068µF and D = 0.5; y-axis is voltage (V) and x-axis is time (ms)

checked

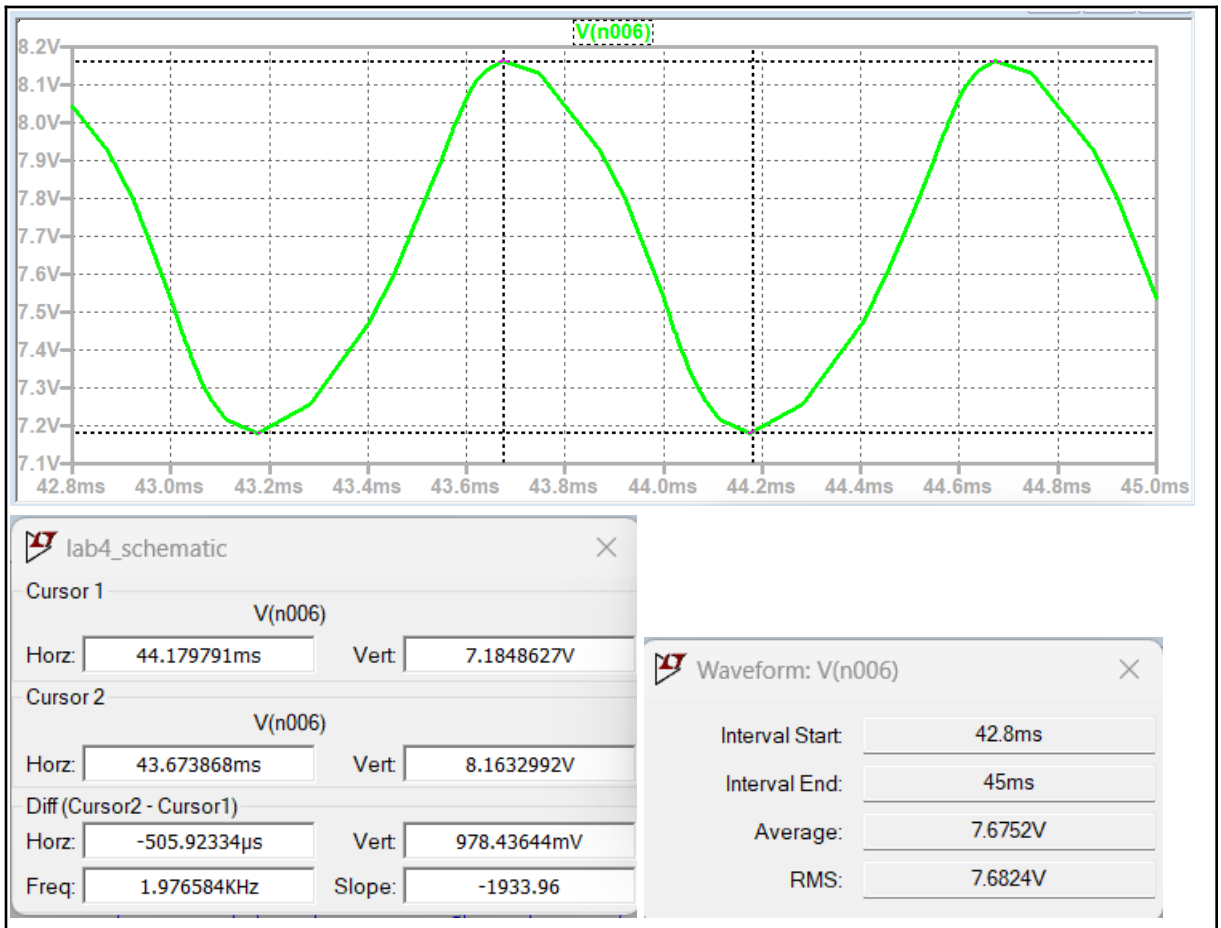
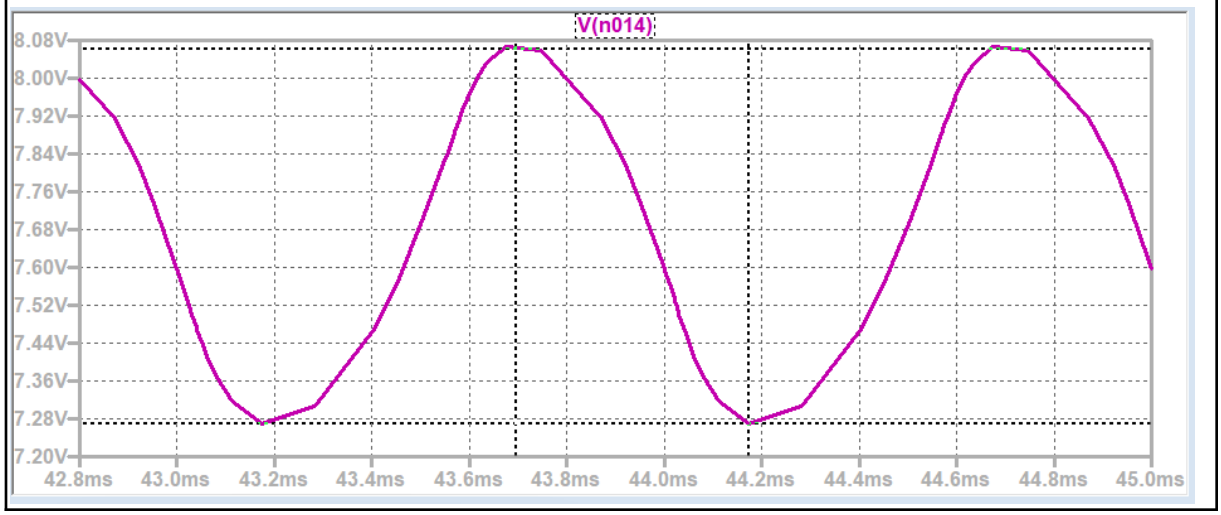


Figure 23 Output voltage waveform for C = 13.408µF and D = 0.5; y-axis is voltage (V) and x-axis is time (ms)



checked

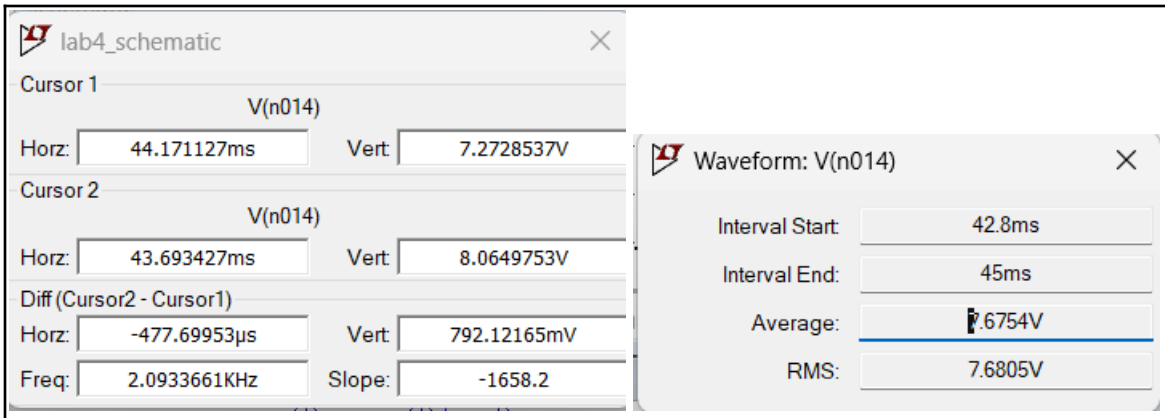


Figure 24 Output voltage waveform for C =16.755 µF and D = 0.5; y-axis is voltage (V) and x-axis is time (ms)

Figure 25 Output voltage waveform for C = 20.11µF and D = 0.5; y-axis is voltage (V) and x-axis is time (ms)

(3) Duty cycle of 70%

Calculate the output voltage ripple for each knob position [2 marks]

checked

(Include your calculations for determining the output voltage ripple for each knob position.)

Output Voltage Ripple

$$\Delta v_0 = \frac{V - V_0}{16LC} DT_s^2$$

Constants
V = 15V
L = 33mH
Ts = 1ms
Fs = 1000Hz
D = 0.5

Knob 1
C = `3.348u`*F*
V0 =8.16 V

$$\Delta v_0 = \frac{V - V_0}{16(33m)C}(0.7)(1m)^2 = 2.7085V$$

Knob 2
C =6.734u F
V0 = 8.52V

$$\Delta v_0 = \frac{V - V_0}{16(33m)C}(0.7)(1m)^2 = 1.2757V$$

Knob 3
C =10.068uF
V0 =8.88 V

$$\Delta v_0 = \frac{V - V_0}{16(33m)C}(0.7)(1m)^2 = 0.8058V$$

Knob 4
C = 13.408 uF
V0 = 9.15V

$$\Delta v_0 = \frac{V - V_0}{16(33m)C}(0.7)(1m)^2 = 0.5784V$$

Knob 5
C = 16.755 uF
V0 = 9.32V

$$\Delta v_0 = \frac{V - V_0}{16(33m)C}(0.7)(1m)^2 = 0.4494V$$

Knob 6
C =20.11 u F
V0 = 9.58V

$$\Delta v_0 = \frac{V - V_0}{16(33m)C}(0.7)(1m)^2 = 0.3573V$$

Theoretical Output Voltage

$$V_0 = DV = 0.7(15) = 10.5V$$

Table Results [3 marks]

Table III. Voltage Ripple and Capacitance Value with Duty Cycle = 70%

Knob position	*Capacitance value (F)*	*Average output voltage (V) (from multimeter)*	*Theoretical average output voltage (V) (calculation)*	*Output voltage ripple (V) (from oscilloscope)*		*Theoretical output voltage ripple (V) (calculation)*	*Simulation output voltage ripple (V) (calculation)*
				Voltage ripple	*Peak-to-peak voltage*		
1	*3.348u*	*8.16*	*10.5*		*17.4*	*2.7085*	*0.7974*

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2	*6.734u*	*8.52*	*10.5*		*14.0*	*1.2757*	*0.6226*
3	*10.068u*	*8.88*	*10.5*		*12.6*	*0.8058*	*0.4760*
4	*13.408u*	*9.15*	*10.5*		*11.2*	*0.5784*	*0.3840*
5	*16.755u*	*9.32*	*10.5*		*9.6*	*0.4494*	*0.3220*
6	*20.11u*	*9.58*	*10.5*		*8.6*	*0.3573*	*0.2715*

Show the output voltage ripple waveform (using CRO) for each knob position [3 marks]

(Insert a picture of your output voltage ripple waveform (using CRO) for each knob position)

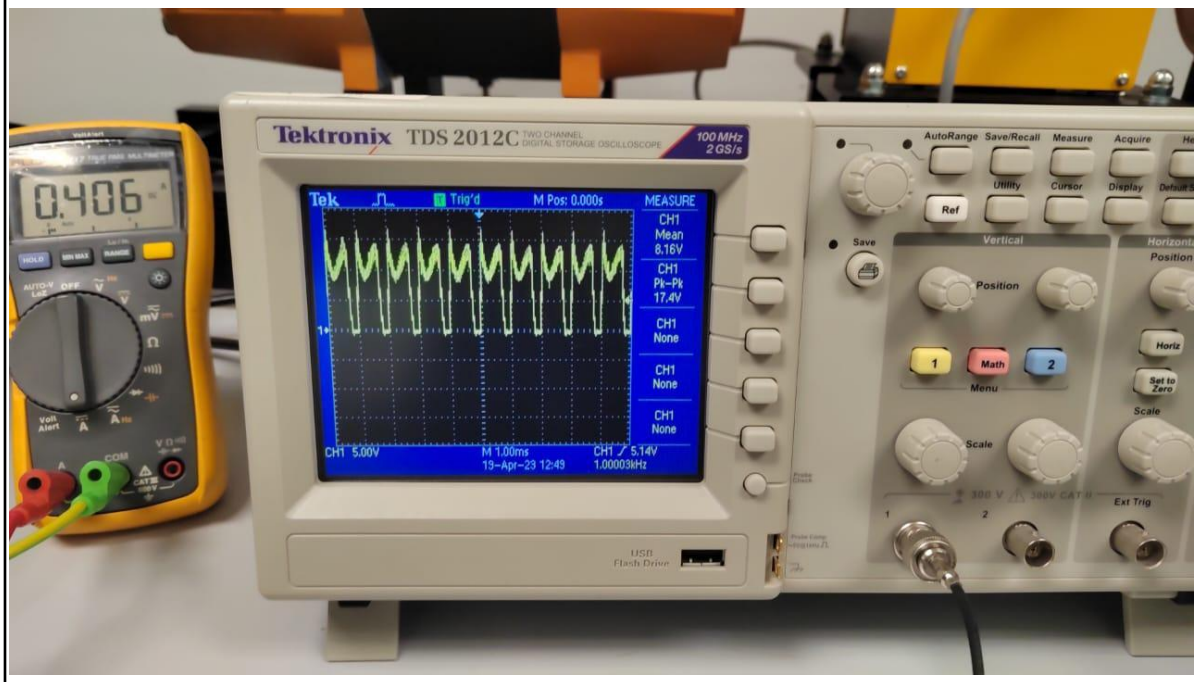

Figure 26 Output voltage waveform for C = 3.348µF and D = 0.7; y-axis is voltage (V) and x-axis is time (ms)

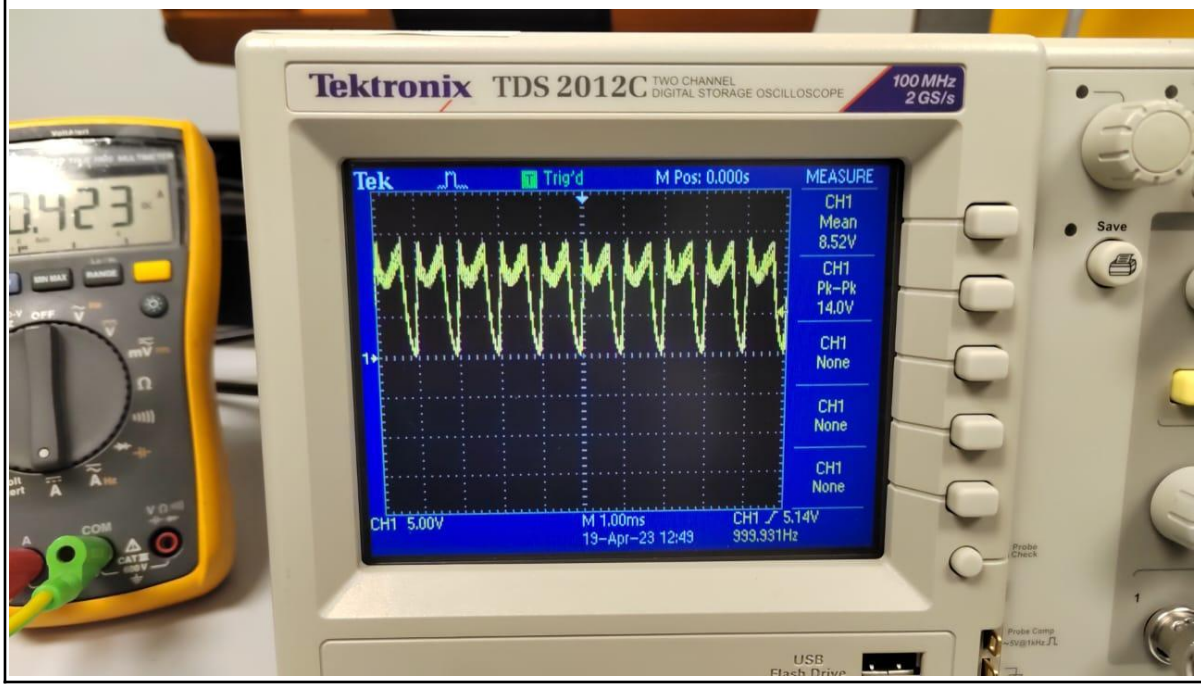

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Figure 27 Output voltage waveform for C = 6.734μF and D = 0.7; y-axis is voltage (V) and x-axis is time (ms)

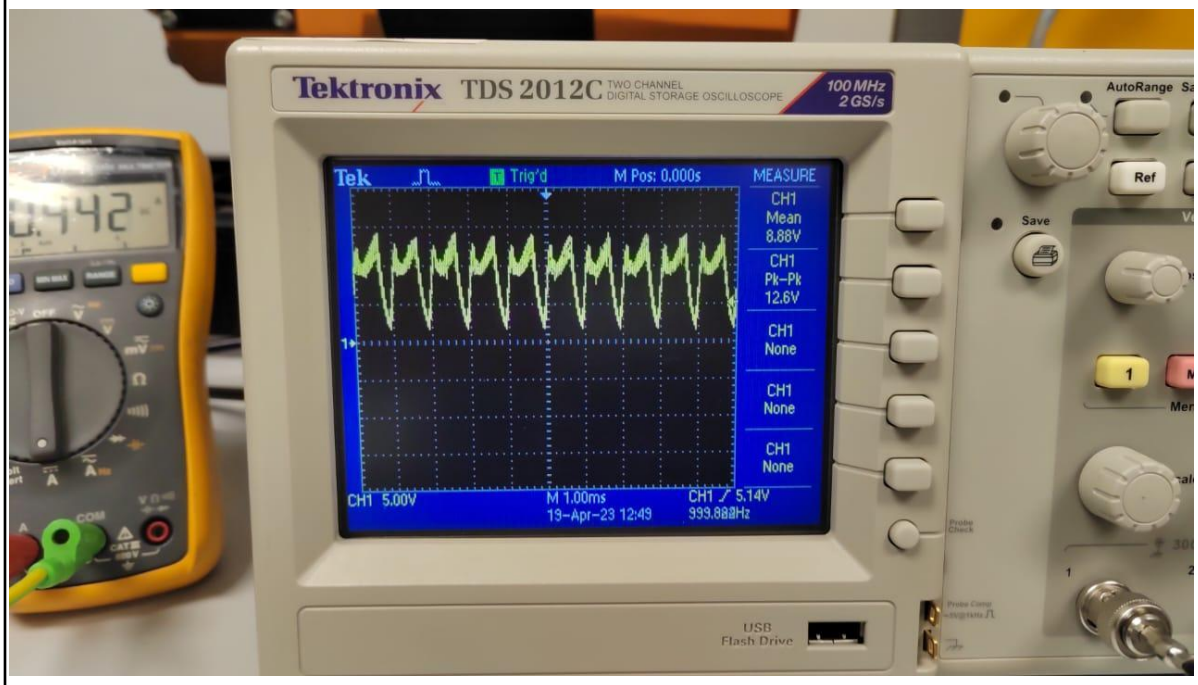

Figure 28 Output voltage waveform for C = 10.068μF and D = 0.7; y-axis is voltage (V) and x-axis is time (ms)

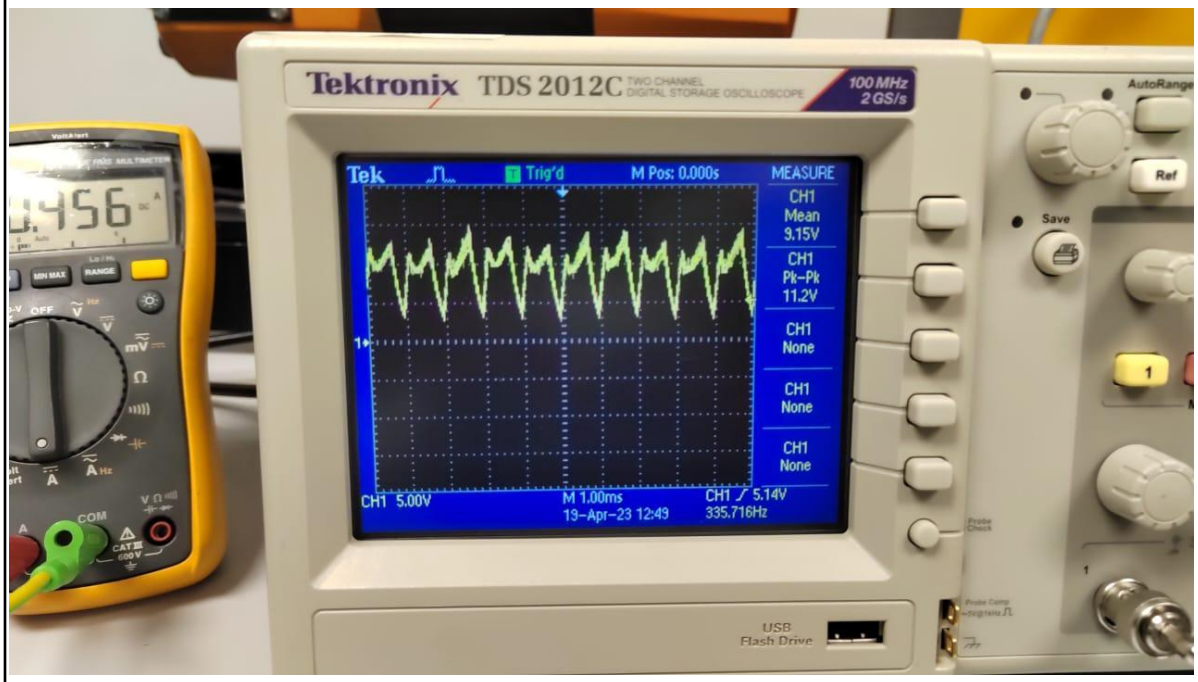

Figure 29 Output voltage waveform for C =13.408 μF and D = 0.7; y-axis is voltage (V) and x-axis is time (ms)

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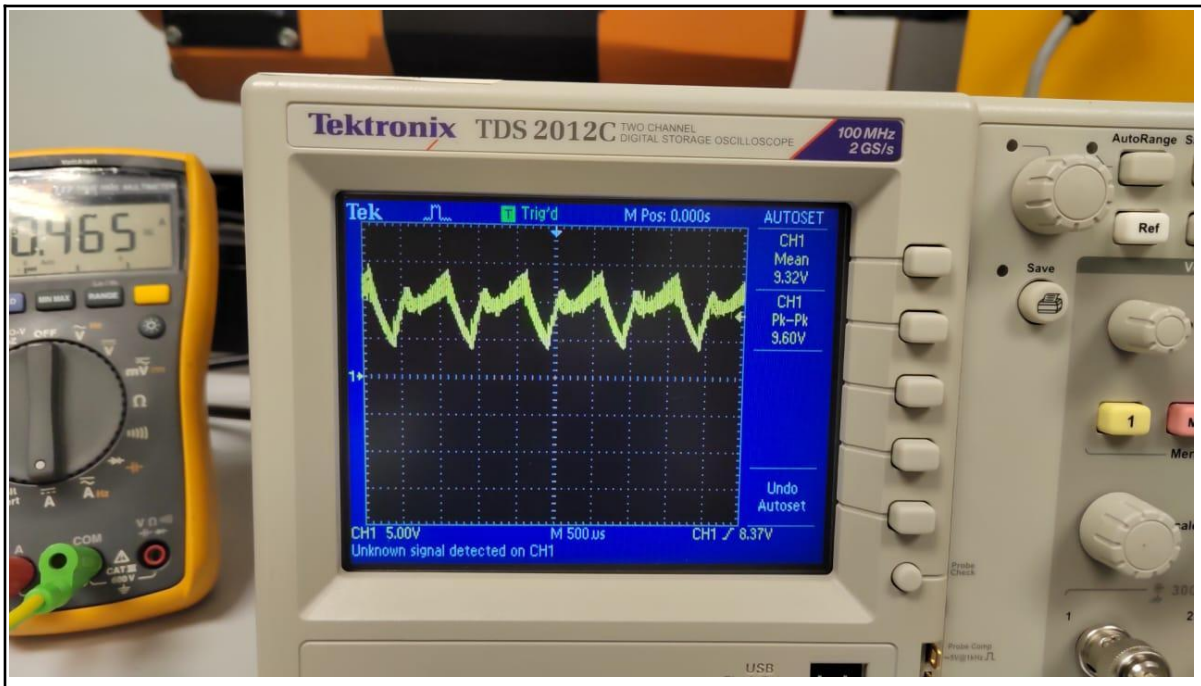

Figure 30 Output voltage waveform for C = 16.755µF and D = 0.7; y-axis is voltage (V) and x-axis is time (ms)

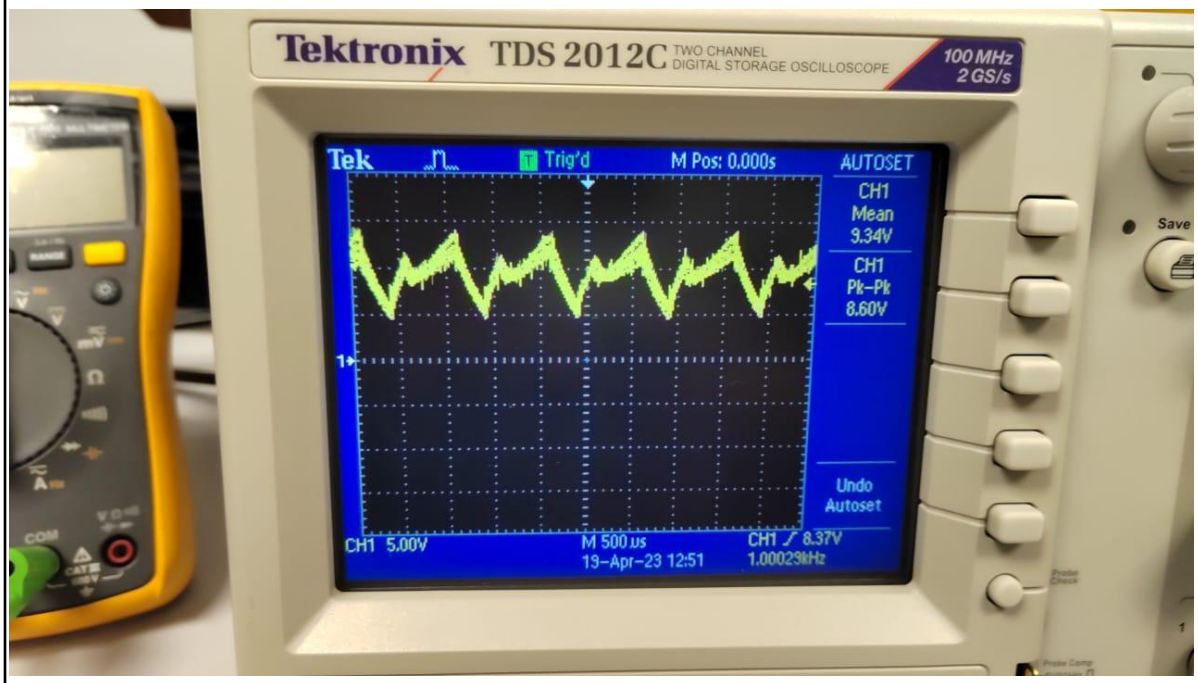

Figure 31 Output voltage waveform for C =20.11µF and D = 0.7; y-axis is voltage (V) and x-axis is time (ms)

Show the output voltage ripple waveform (from simulation) for each knob position [2 marks]

(Insert a picture of your output voltage ripple waveform (from simulation) for each knob position)

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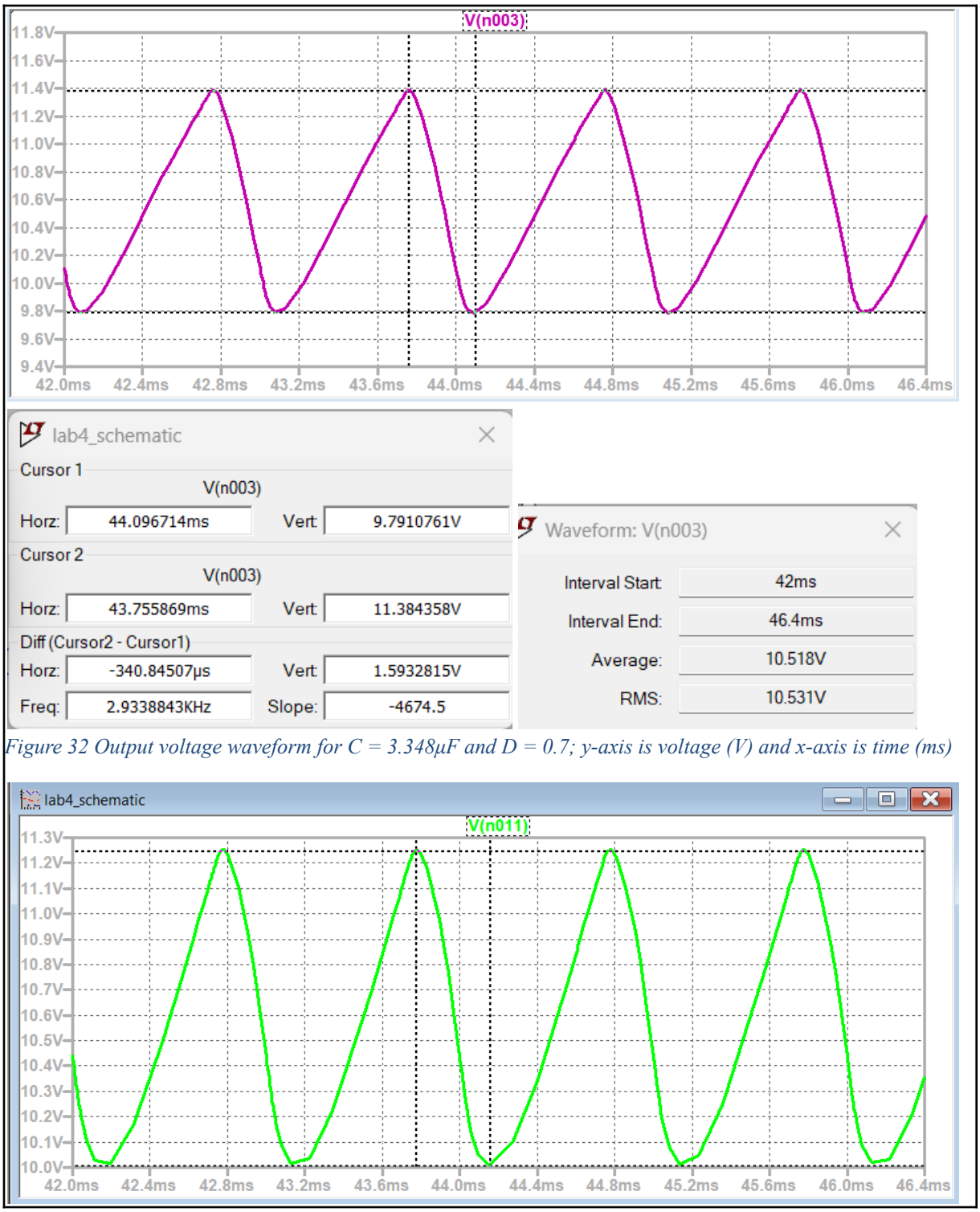

Figure 32 Output voltage waveform for C = 3.348µF and D = 0.7; y-axis is voltage (V) and x-axis is time (ms)

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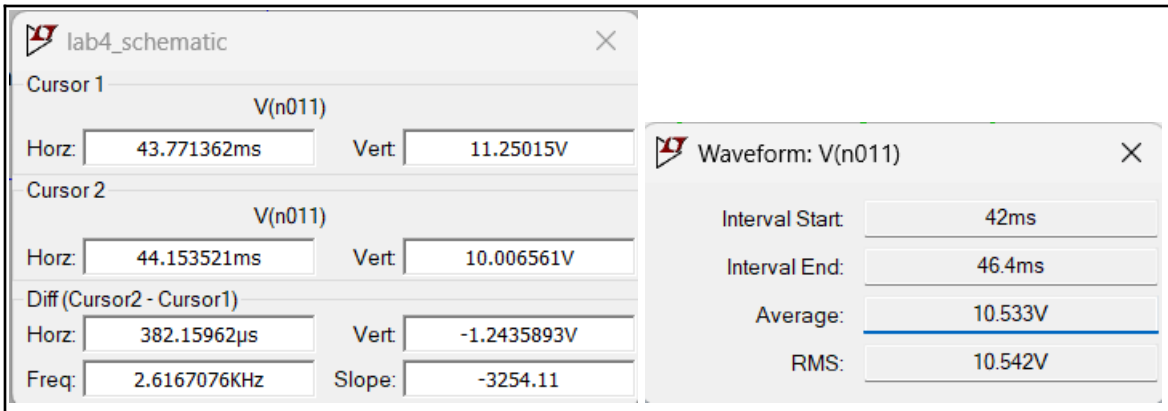

Figure 33 Output voltage waveform for C = 6.734µF and D = 0.7; y-axis is voltage (V) and x-axis is time (ms)

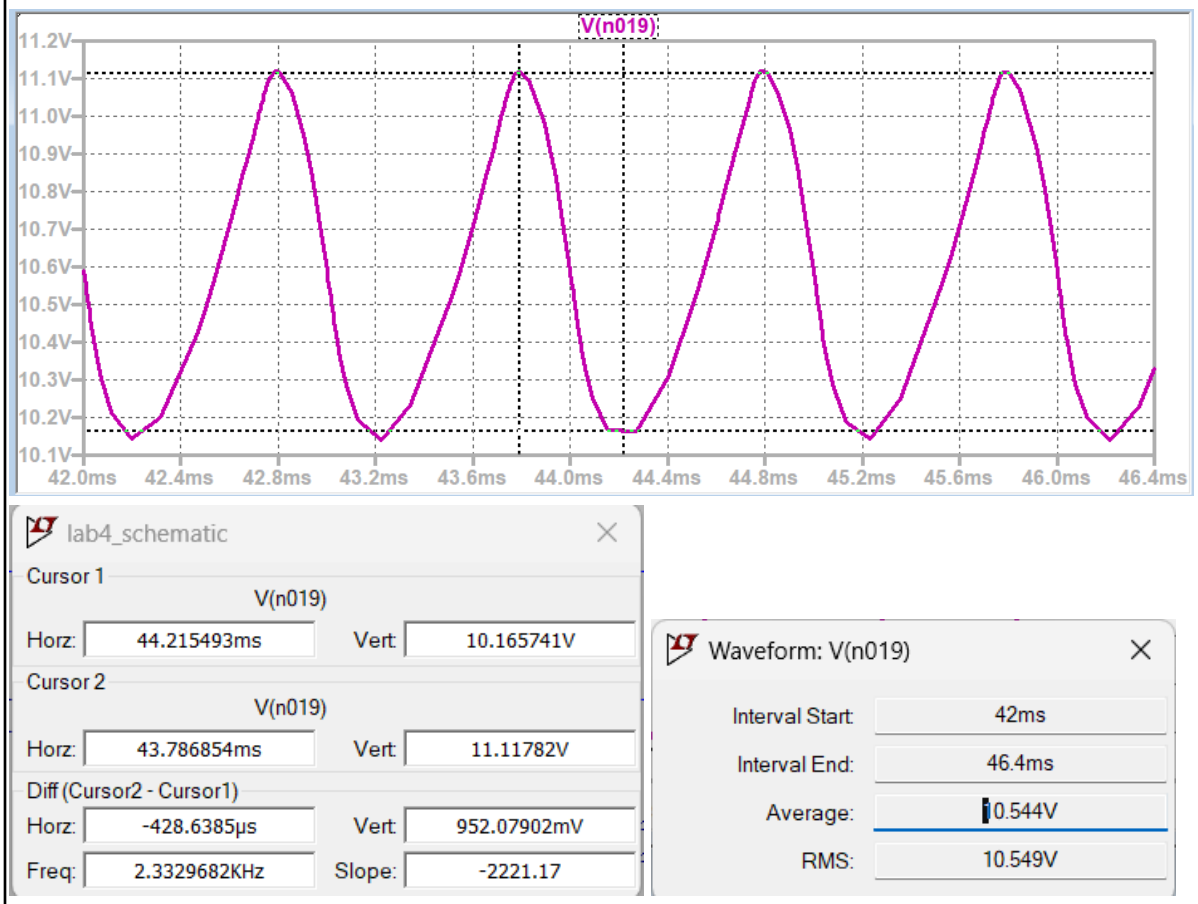

Figure 34 Output voltage waveform for C = 10.068µF and D = 0.7; y-axis is voltage (V) and x-axis is time (ms)

checked

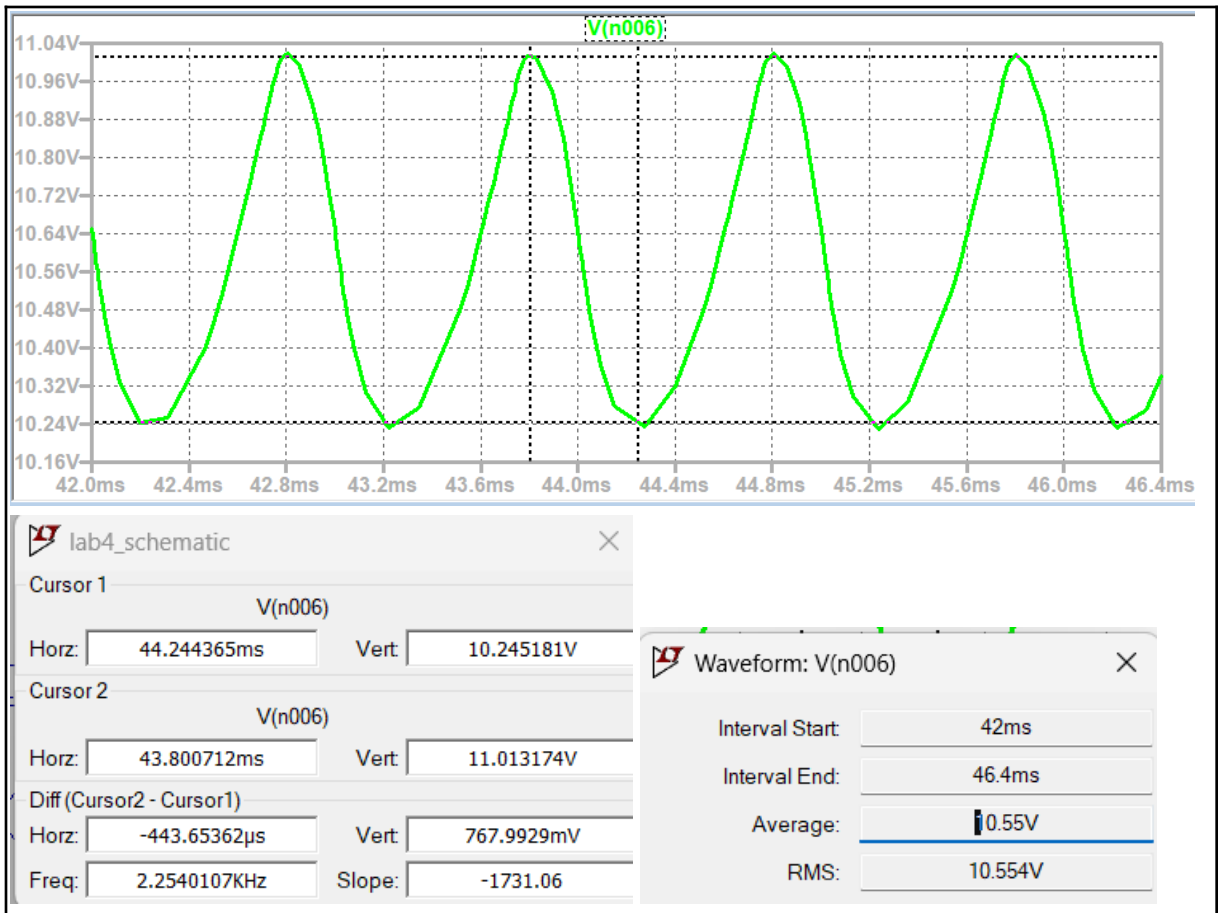

Figure 35 Output voltage waveform for C = 13.408µF and D = 0.7; y-axis is voltage (V) and x-axis is time (ms)

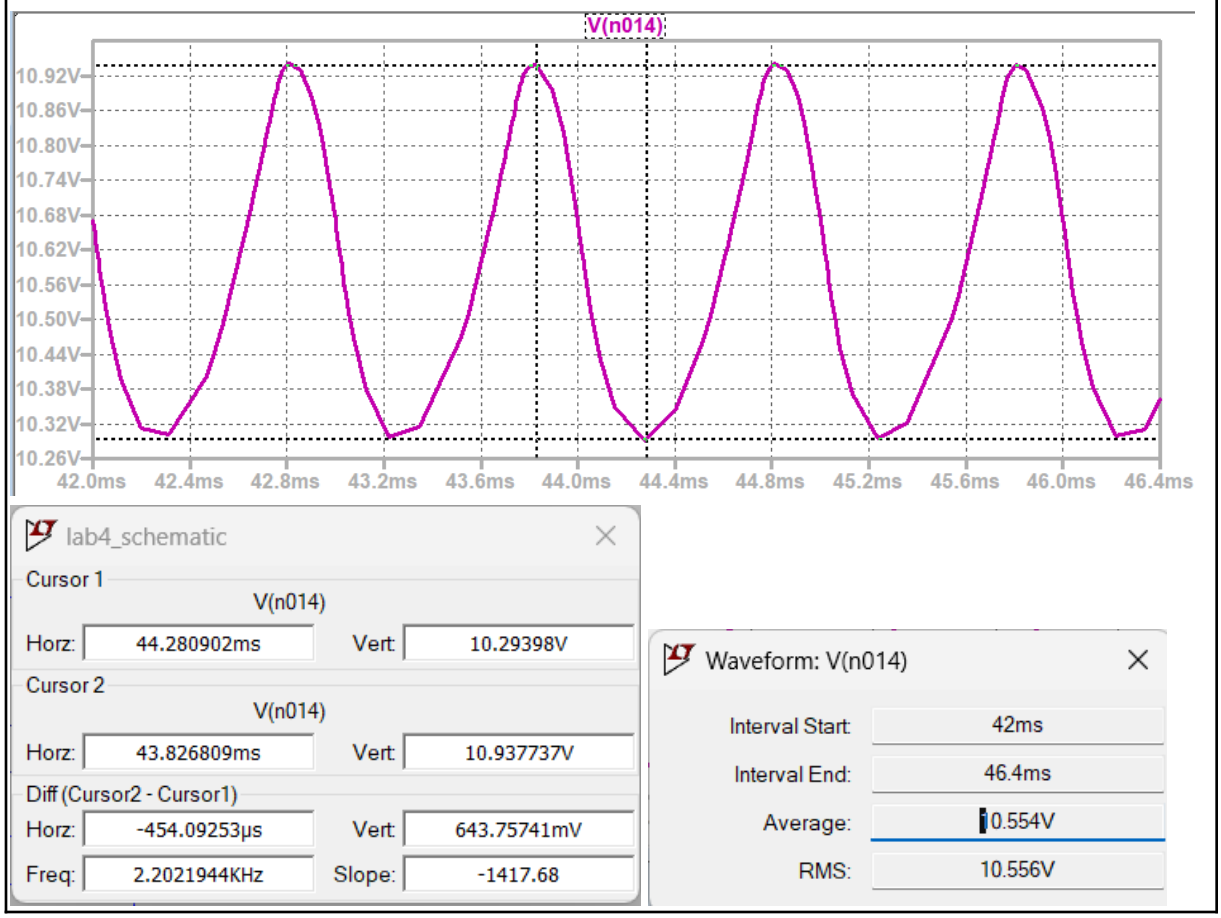

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Figure 36 Output voltage waveform for C = 16.755µF and D = 0.7

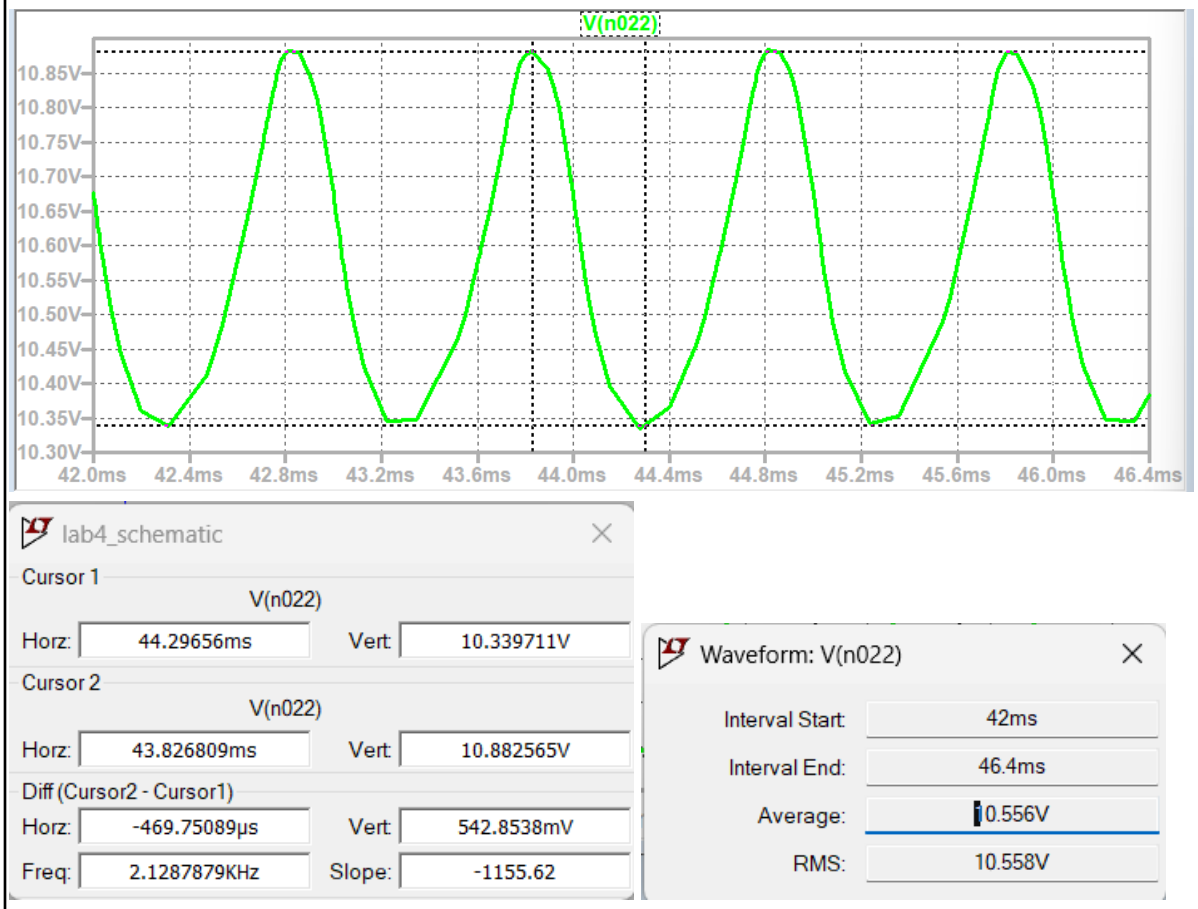

Figure 37 Output voltage waveform for C = 20.11µF and D = 0.7; y-axis is voltage (V) and x-axis is time (ms)

Analysis [20 Marks]

(Discuss the obtained results of average output voltage and output voltage ripple for duty ratio of 30%, 50% and 70% for each of the knob position of the capacitor load.)

Change in Duty Cycle and change in output average Value

For a duty cycle of 30%, our average output voltage starts from 3.1V and gradually increases up to saturation voltage of 4.03V as we increase the capacitance value. The simulated average output voltage remains constant at 4.25V.

For a duty cycle of 50%, our average output voltage starts from 5.26V and gradually increases up to saturation voltage of 6.9V as we increase the capacitance value. The simulated average output voltage remains constant at 7.66V.

For a duty cycle of 70%, our average output voltage starts from 8.16V and gradually increases up to saturation voltage of 9.58V as we increase the capacitance value. The simulated average output voltage remains constant at 10.556V.

Generally, the measured average output voltage is smaller than the theoretical value for each duty cycle. This can be justified as there will be internal voltage drop in the internal resistance of the wire connections, and the internal circuitry of the measurement equipment.

The simulated average output value is close to the theoretical average output voltage. The marginal differences can be attributed to the difference in buck converter circuitry on Spice and in the LMS module.

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There is a scenario that should be noted. The change in capacitance should not change the average output value. This is because taking the KVL of the buck-converter, the low pass filter and the load, it will be in this form

$$V_{out} = V_l + V_{load} V_{out} = L\frac{dI_l}{dt} + V_{load}$$

For an inductor circuit in steady state, the average output of the inductor would be equal to zero to prevent the build-up of voltage as shown in Figure 1.

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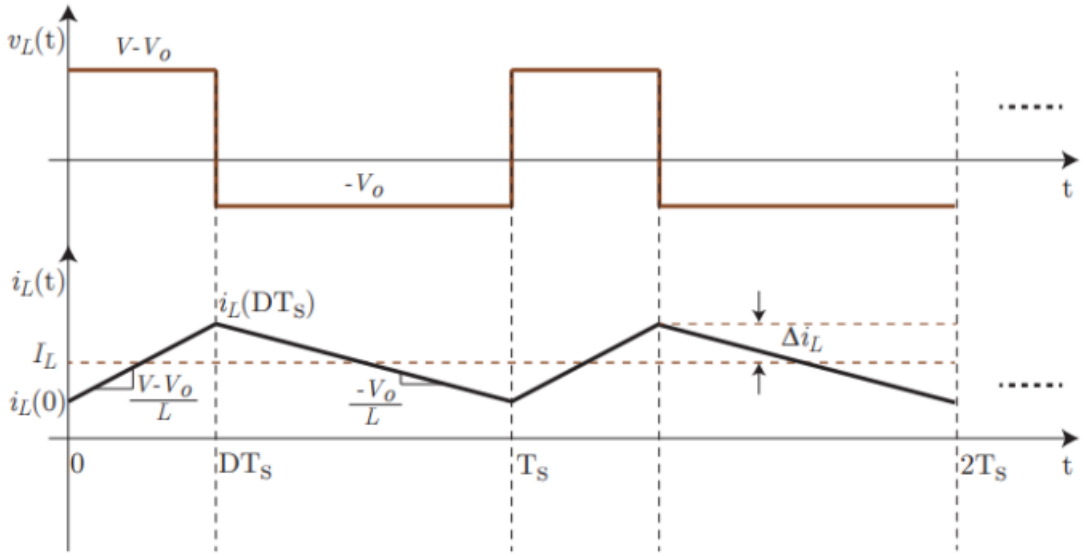

Figure 38 Graph of inductor voltage and inductor current

However, during the experiment, as the capacitance values changes, we notice that the capacitance starts off small, then increases closer to the theoretical values as we increase the capacitance value. This can be justified by assuming that the resistive has stray capacitance in series with it, which causes the additional voltage drop at low parallel capacitance, but becomes negligible as we increase the parallel capacitance value to it.

Change in Capacitance and change in output ripple voltage

As we increase the capacitance, the output ripple decreases for each duty cycle. This follows the inverse relationship that relates the output ripple voltage with the capacitance.

$$\Delta V_0 = \frac{(V-V_0)DT_s^2}{16LC}$$

The theoretical output ripple for a duty cycle of 30% ranges from 0.3099 – 2.0195 V. The theoretical output ripple for a duty cycle of 50% ranges from 0.3000– 0.8525V. The theoretical output ripple for a duty cycle of 30% ranges from 0.3573 – 2.709 V.

The simulated output ripple for a duty cycle of 30% ranges from *0.6 - 1.705 V*. The simulated output ripple for a duty cycle of 50% ranges from *0.3310- 1.0170V*. The simulated output ripple for a duty cycle of 70% ranges from *0.2715 – 0.7974V.*

The experimental output ripple for a duty cycle of 30% (obtained from the peak ranges from `7.8- 15.6`*V*. The simulated output ripple for a duty cycle of 50% ranges from `8.8 - 16.8`*V*. The simulated output ripple for a duty cycle of 70% ranges from `8.6- 17.4`*V.*

The simulated and theoretical does not defer much at low duty cycles, but as the duty cycle increases, the differences between them increases. This can be attributed to the differences in buck converter circuitry between the Spice model and the LMS model.

There is a special scenario that should be taken note. The theoretical value and the actual output ripple differ by a very large margin (500% - 2000%). There are 2 possible explanations to this.

Theory 1: The cut-off frequency of the low pass filter is insufficient to filter off external noise and the output voltage ripple effectively. This could happen if the noise has a lower frequency than the cutoff frequency of the low pass filter.

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Theory 2: The cutoff frequency of the low pass filter is much higher than the switching frequency. Meaning the harmonics of the signal might be in the passband as well.

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Discussion

1. Explain the relationship between duty cycle and the voltage ripple. [10 Marks]

Duty cycle is the ratio when the switch is ON to the total switching period. The voltage ripple is the fluctuation in output voltage due to the switching. It is given:

$$\Delta v_o = \frac{V - V_o}{16LC} DT_s^2$$

Substituting the equation for the average output voltage $V_0 = DV$,

$$\Delta v_o = \frac{V - DV}{16LC} DT_s^2$$

$$\Delta v_o = \frac{V(1 - D)}{16LC} DT_s^2$$

The relationship between the voltage ripple and the duty cycle is parabolic:

$$\Delta V_o \propto D(1 - D)$$

We will get the largest voltage ripple when D is 50%, and the voltage ripple decreases as the duty cycle increases / decreases from 50%.

2. List the difficulties encountered during the experiments. [3 Marks] Justify the differences between the measured and calculated values. [2 Marks] State whether the measured or calculated values are more accurate. [2 marks] For real practice, suggest procedures which can be carried out to prevent any measurement error(s). [3 Marks]

Difficulties encountered

- *A considerable amount of time was used to familiarize with the function generator. Our team struggled to generate the pulse in continuous mode with 1kHz frequency.*
- *The buck converter was pretty much a black-box in this experiment. We did not devise a way to measure the outputs of the buck converter to ensure it is correct. Therefore, we can only assume that the buck converter is functioning as expected and its output is 100% correct. However, there were great magnitude deviations in the CRO waveforms from the LTSpice waveforms, and we have no immediate explanation why this phenomenon occurred.*
- *The output voltage ripple value is not displayed in the CRO, and requires the value of the output voltage to calculate. This hinders us from performing instantaneous calculations and directly cross-checking the results.*

Justification of differences between measured and calculated values

- *The internal dynamics of the real-life buck converter circuit differs from the ideal model.*
- *The cut-off frequency of the low pass filter in the buck converter is higher than the frequency of the noise. The noise can introduce oscillations and offsets in the waveform, which is observed in our results.*
- *The cut-off frequency of the low pass filter is higher than the switching frequency and its harmonics. Similarly, this may introduce oscillations in the waveform, which is observed in our results.*
- *The inductance in the circuit is actually not known, we just assumed it to be 33mH.*

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- *Internal resistance and stray capacitance/inductance in real-life components are not accounted for in calculations.*
- *Thermal, Shot, and Flicker noise inherent in circuit design.*
- *Pulse frequency fed to the buck converter might need to be higher (eg. 1 MHz instead of 1 kHz)*

Which values are more accurate?

The calculated values are more accurate because:

- *The calculated values are analytical approaches, formulas derived from fundamental laws of physics. These equations model the actual phenomenon to a high level of accuracy.*
- *Some of the calculated values were obtained through simulation. LTSpice models the solution space and solves it with respect to time. The accuracy of performing such calculations repeatedly provides insight into the transient response of the system.*

Real-life practices to prevent measurement errors

- *Calibration of measurement devices to reduce the likelihood of systematic errors.*
- *Repeat the experiment and take the average to reduce the likelihood of human errors.*
- *Perform simulations beforehand and plot the expected output. During the experiment, we can then immediately compare the measured output to the theoretical output. This gives us assurance that the results are correct if the outputs are similar; and prompt us to re-check our experimental setup if they are not.*
- *Ensure the frequency input to the system is correct (ie. a system may behave differently for various frequencies, described by the frequency response of the system)*

***Conclusion and Findings** [14 Marks]*

The objective of this experiment is to comprehend the operation of a DC-DC buck converter. The two manipulated variables in this experiment are the duty cycle percentage of the commutation cell & the value of capacitance for the capacitor used in the buck converter. The arbitrary function generator controls the duty cycle ratio whilst the three-phase capacitor load bank supplies the capacitance needed. The capacitor load bank comprises a switch to turn the load on or off. Additionally, a capacitance-controlled knob is present to adjust the capacitance value of the load.

The duty cycle ratio is adjusted to obtain percentages of 30%, 50%, and 70%. The capacitance-controlled knob (variable capacitor) is rotated 6 times to alternate through 6 capacitance values: 3.348, 6.734, 10.068, 13.408, 16.775 and 20.110 (μF). The following steps were taken to conduct the experiment:

1) *The DC power supply was turned on and set to provide a voltage of 15 V*
2) *The arbitrary function generator was switched on with following settings:*
   Duty ratio: 30%, Waveform: Pulse, Mode: Continuous, Frequency: 1kHz, Amplitude: 5V, Offset: 2.5V
3) *The capacitive load was turned on, and the knob was set to '1' (3.348 μF)*
4) *The average output voltage was measured using a digital multimeter*
5) *The output ripple voltage was measured using a Cathode Ray Oscilloscope (CRO)*
6) *WIth the same settings, the capacitor-controlled knob was rotated 5 more times to cycle through increasing capacitance values.*
7) *Steps 2 to 6 were repeated using duty ratios of 50% and 70%*

The output voltage is given by:

$$V_o = DV$$

where V_o is output voltage, D is duty ratio, V is input voltage. V_o is directly proportional to D when V is constant. Thus, when duty cycle increases, the output voltage increases as well. Our measurements comply with this theoretical analysis. The output voltage ripple, Δv_o can also be approximated to $\Delta v_o = (D - D^2)$ when all other parameters are constant. The equation is visualized in the following graph:

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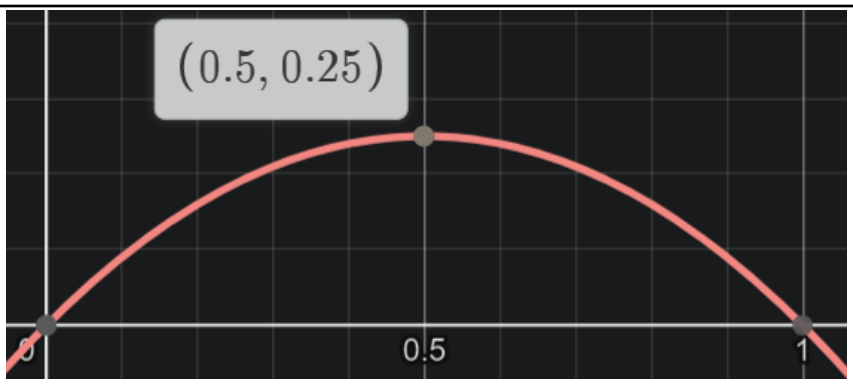

Figure 38 Illustration of voltage ripple generated using DESMOS Graph

As we can see observe, the relationship between Δv_o and D is a negative quadratic graph with a maximum point. The output ripple voltage peaks when the duty cycle ratio is exactly 50%. The ripple voltage measurements from the experiment complement this analysis. Finally, we observe that the output ripple voltage value diminishes as the capacitance value rises. This relationship can be made sense through the equation that follows:

$$\Delta v_o = \frac{(V - V_o)DT^2}{16LC}$$

whereby we can observe that the output ripple voltage is inversely proportional to capacitance. The 3 relationships analyzed theoretically align with the practical measurements.

We were able to investigate how various factors impact the output results of a DC-DC buck converter. The manipulated variables were the duty ratio and capacitance, whilst the responding variables were the output ripple voltage and average output voltage. The experiment has improved our knowledge of how each factor affects the functionality and efficacy of the DC-DC Buck Converter.

References *[6 Marks]*

(Include minimum 3 references here)

[1] B. Bahrani. (2022). ECE3051 – DC-DC Buck Converter [PDF]. Available: https://lms.monash.edu/course/view.php?id=133062&section=26

[2] Hart, Daniel W. (2011). Power Electronics International ed. McGraw-Hill.

[3] A. W. Cristri and R. F. Iskandar, "Analysis and Design of Dynamic Buck Converter with Change in Value of Load Impedance," Procedia Engineering, vol. 170, pp. 398–403, 2017, doi: https://doi.org/10.1016/j.proeng.2017.03.064.

[4] "What is Buck Converter? Operating Principle and Waveform Representation of Buck Converter," Electronics Coach, Sep. 15, 2021. https://electronicscoach.com/buck-converter.html

[5] P. Falkowski, "Analysis and design of high efficiency DC/DC buck converter," PRZEGLĄD ELEKTROTECHNICZNY, vol. 1, no. 5, pp. 158–163, May 2016, doi: https://doi.org/10.15199/48.2016.05.29.

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