Lab 3 BJT Curve Tracer 2 (Common Base)

1 LTspice simulations (pre-lab)

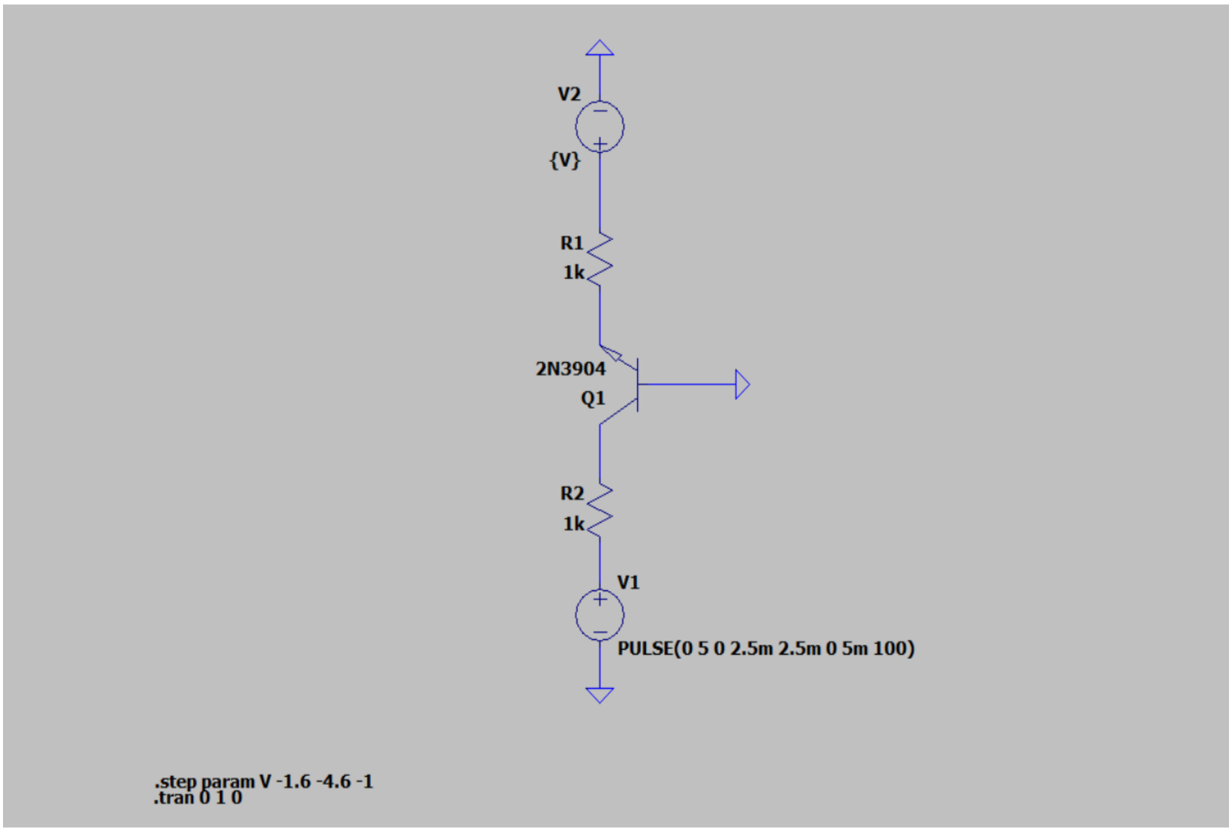
PART A: SIMULATION

Plot I_C vs V_{CB} using X-Y plot and export the plot to be included in your lab report. In your XY plot, X-Axis should be VCB, Y-Axis should be IC. Include a screenshot of the circuit schematic in your report. **(2 marks)**

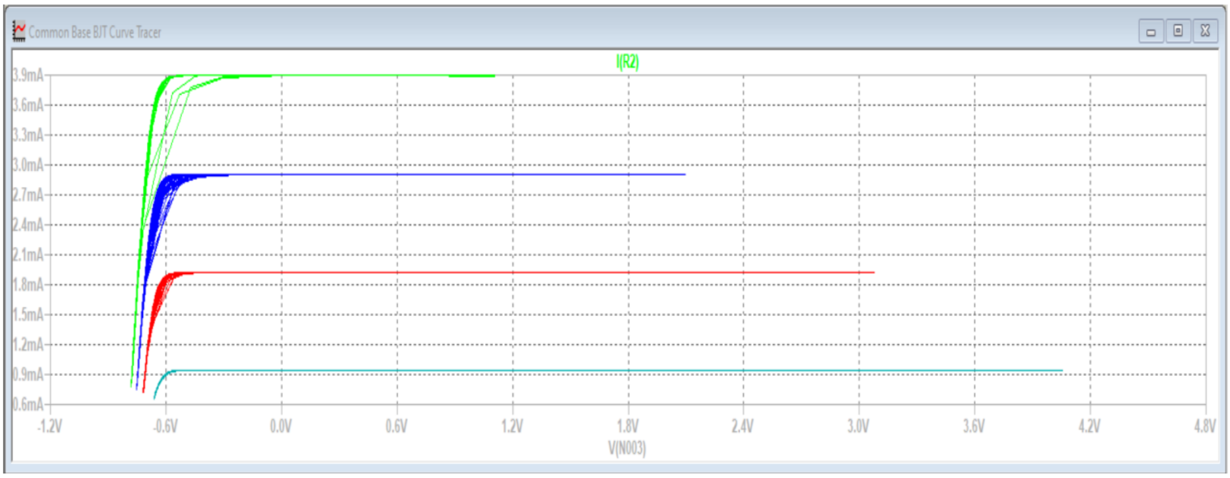
From your knowledge gained in the previous experiment (Lab 2), is it sensible that VCB can sometimes be negative? What region is the transistor operating in, in this case? **(1 mark)**

Find the I_C/I_E. Is it what you expect? Explain you reasoning. **(2 marks)**

Circuit Schematic



Ic vs Vcb Waveform



Explanation

When V_{cb} is negative, means V_{bc} >0 and the junction is in forward bias. This means that the collector is at a lower voltage than the base.

If the base-emitter junction is at reverse bias, then the transistor is operating in reverse active region.

The collector current (I_C) will be very small and is determined by the reverse saturation current ($I_{C,\ r\text{-}sat}$) of the transistor.

The collector current in reverse bias can be estimated using the reverse-bias saturation current equation:

$$I_c = I_{r-sat} * (e^{\frac{V_{cb}}{V_T}} - 1)$$

Where V_T is the thermal voltage ($\frac{kT}{q}$)

As V_{cb} becomes more negative, the collector current decreases more, and the transistor eventually enters the reverse-active region.

If the base-emitter junction is at forward bias, then the transistor is operating saturation mode.

Theoretical Calculations

We know that

$$I_e = I_c + I_b$$

Since

$$I_b = \frac{1}{300} I_c$$

We will obtain

$$I_e = I_c + \frac{1}{300} I_c$$

Which equates to

$$\frac{I_c}{I_e} = 0.997$$

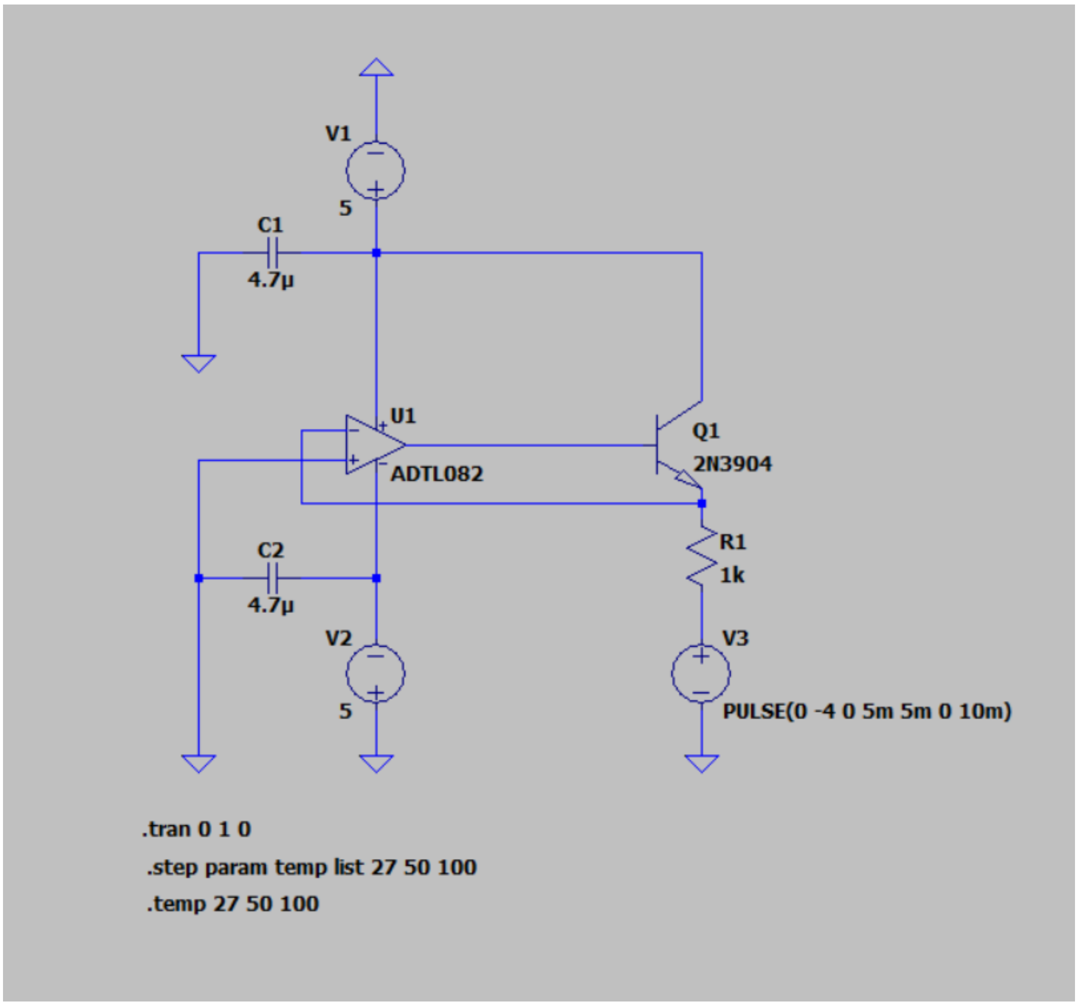
The value obtained is as expected. The values we have taken is in the forward active region and the measured current gain is equal to the theoretical gain.

PART B: SIMULATION

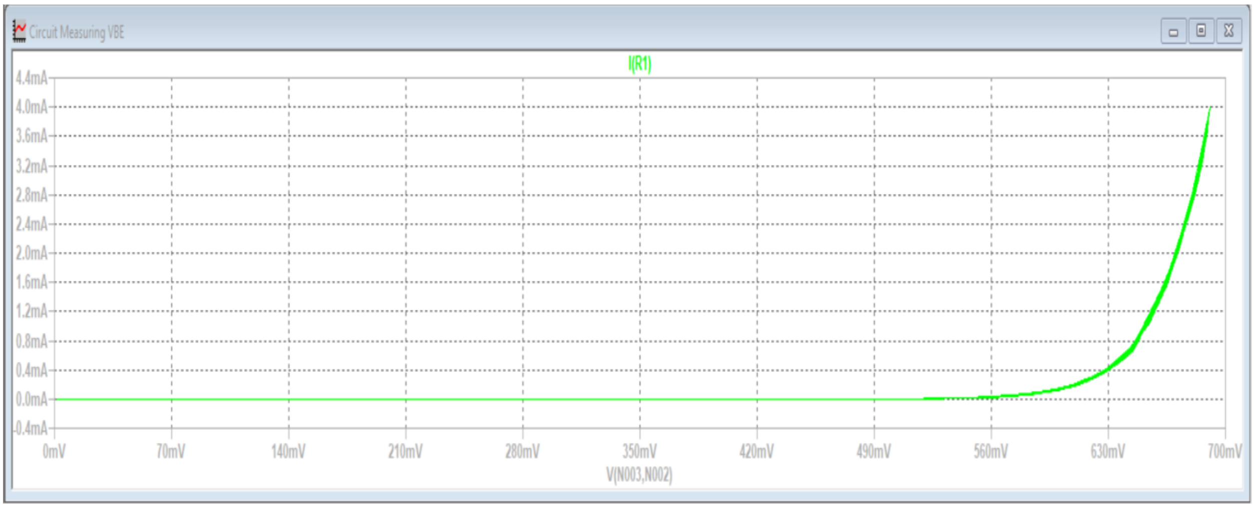
Report: (5 marks)

(a) Plot I_E vs V_{BE} using X-Y plot waveform, and export the plot to be included in your lab report. In your XY plot, X-Axis should be VBE, Y-Axis should be IE. Include a screenshot of the circuit schematic in your report. **(1 mark)**

Circuit Schematics



Ie vs Vbe

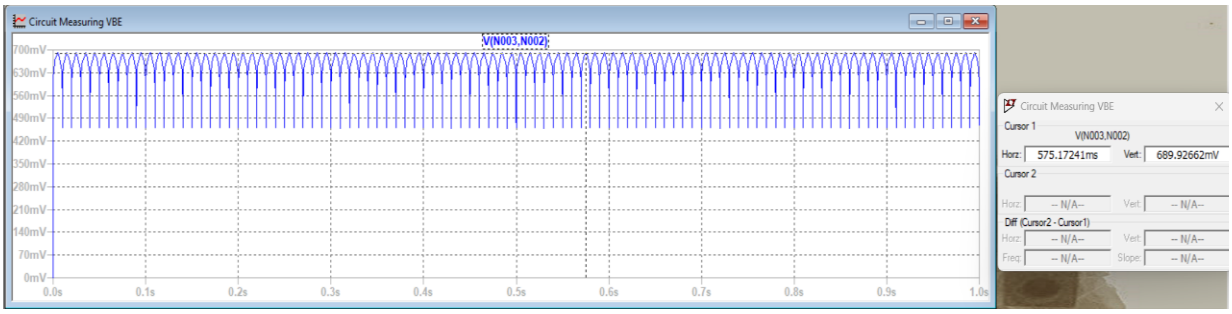


(b) Why are the capacitors necessary? What happens if you remove them? **(1 mark)**

As states in the lecture videos, the capacitors are known as bypass/decoupling capacitors. The bypass capacitors will provide low impedance path for high frequency noise and high frequency voltage fluctuations to be removed from the power supply, preventing them from affecting other components on the circuit. Basically, it will remove stray inductance

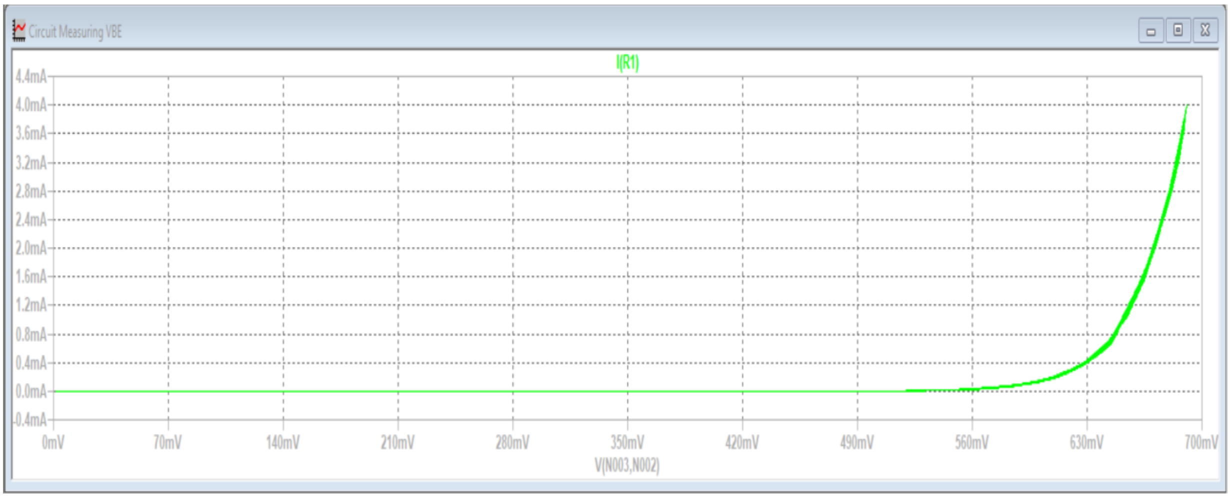
So by removing the bypass capacitors, there will be high frequency noise and high frequency voltage fluctuations which will affect other components on the circuit. This would also affect our measurement as the value of Vbe will fluctuate, reducing the accuracy of our result.

(c) What is your measured V_{BE}? How close is the measurement to the typically used value ~0.7 V? **(1 mark)**

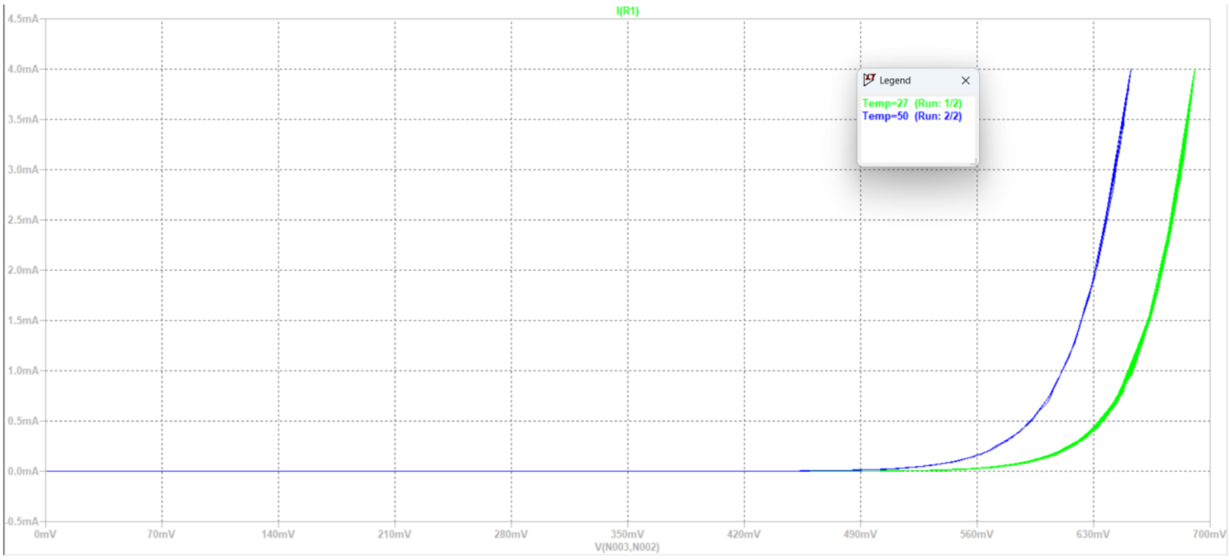


Based on LTSpice, the measured value is very close to having a value of 0.7V. The measured value obtained is 689.93 mV.

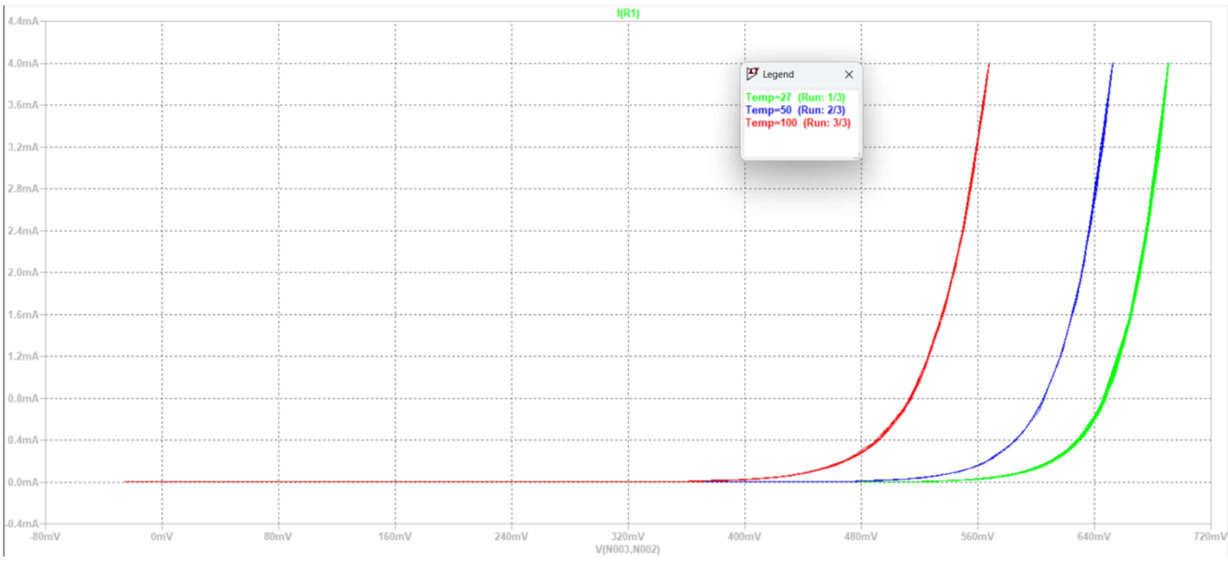
(d) How does temperature affect the IE vs VBE plot? Plot IE vs VBE characteristic for at least 3 different temperatures and include in the report. Does the simulation match your expectation? Explain your answer. **(2 marks)**



At room temperature (approximately 27 degrees – LTSpice default temperature), the BJT is operating within its normal temperature range, and the IE vs VBE plot shows a typical shape, with a linear region at low voltages and currents, and a saturation region at high voltages and currents.



At approximately 50 degrees, the current gain of the BJT has clearly decreased, resulting in a shallower slope and lower saturation current in the IE vs VBE plot. The BJT is also more prone to thermal runaway at high currents, due to the increased saturation current.



At approximately 100 degrees, the IE vs VBE plot shows a significant change in shape, with a reduced linear region and a flattened saturation region. This is due to the increased thermal effects on the BJT structure, leading to reduced carrier. The BJT is also more prone to breakdown and thermal damage at high voltages and currents.

2 Experimental Work (pre-lab and in-lab)

PART A: CURVE TRACER OF COMMON BASE BJT

Using the XY plot function in Scopy to plot I_C *vs.* V_{CB} waveform, and export the plot to be included in your lab report. In your XY plot, X-Axis should be CH 1, Y-Axis should be CH 2.

By measuring the voltage drops across the resistors with the oscilloscope, calculate the ratio of I_C/I_E. Is it what you expect? Explain you reasoning.

Click the Hyperlink [Scopy Oscilloscope]() if you are not sure about how to draw an XY plot.

W1 and W2 waveform

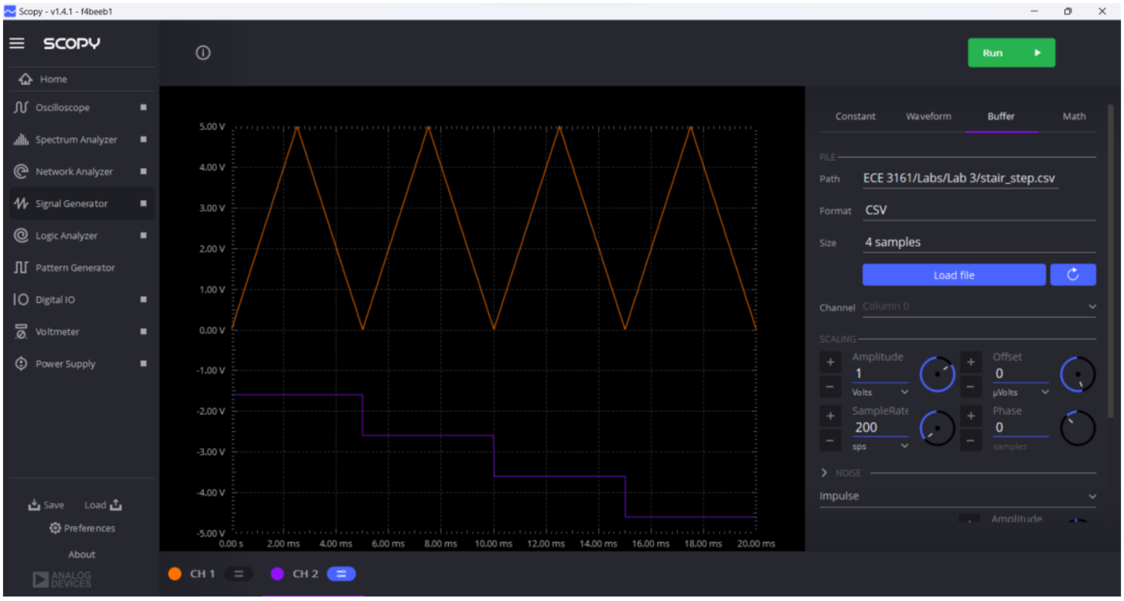


Fig. 1. W_1 wave form (orange) and W_2 waveform (blue), Voltage on the y-axis, and Time on the x-axis

Ic vs Vcb waveform

Fig. 2. $V_{1k\Omega}$-V_{CB} waveform (right), where $V_{1k\Omega}$ is on the y-axis and V_{CB} is on the x-axis

Explanation

$V_{1k\Omega}$ is the potential difference across the 1kΩ resistor, it is connected to the collector junction of the bipolar junction transistor. To obtain I_C, $V_{1k\Omega}$ needs to be divided by its resistor value 1kΩ

Yes, Vcb can sometime be negative. When $V_{CB} < 0V$, this means $V_{BC} > 0V$, the base-collector junction of an NPN transistor is in reversed-biased since the collector junction is at a higher potential than the base junction. Since $V_{BE} > 0.7$ V in this case, the base-emitter junction is in forward-biased. This means the transistor's operating mode is forward-active.

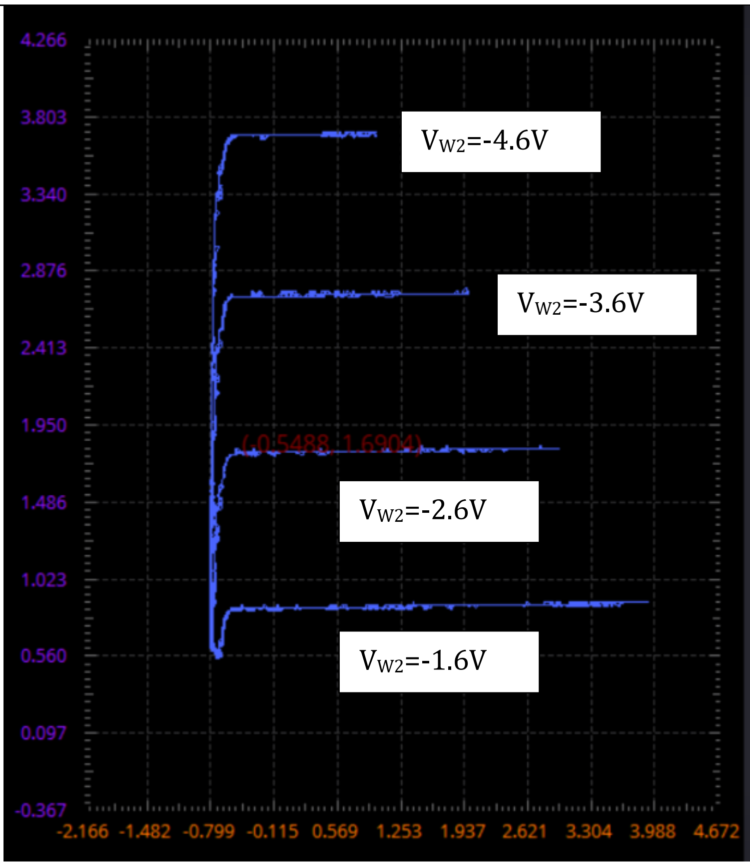


Fig. 3. $V_{1k\Omega}$-V_{CB} waveform, where $V_{1k\Omega}$ is on the y-axis and V_{CB} is on the x-axis

By measuring the voltage drops across the resistors with the oscilloscope, calculate the ratio of IC/IE. Is it what you expect? Explain you reasoning.

Theoretical Calculations

We know that the DC gain of 2N3904 BJT is $\beta \cong 300$, the expected ratio of I_c/I_E would be approximately 1, accurately speaking,

Applying KCL,

$$I_e = I_c + I_b$$

Since

$$I_b = \frac{1}{300} I_c$$

We will obtain

$$I_e = I_c + \frac{1}{300} Ic$$

Which equates to

$$\frac{I_c}{I_e} = 0.997$$

Measured

We can measure the ratio of I_c and I_e in the physical circuit by using our oscilloscope pins to measure the voltage going through both of the resistor.
The voltage going through the 1kΩ resistor at the collector and the voltage going through the 1kΩ resistor at the emitter is shown in the graph below. We are assuming that we are taking the voltage drop when the transistor is at the forward active region.

Fig. 3. $V_{1k\Omega}$ at emitter waveform, y-axis is voltage and x-axis is time

Fig. 4. $V_{1k\Omega}$ at emitter waveform, y-axis is voltage and x-axis is time (enlarged)

Based on the above graph, we can obtain the value of I_c by computing

$$I_C = \frac{V_{1k\Omega}}{1k\Omega} = \frac{3.674\text{V}}{1\text{k}\Omega} = 3.674 \text{ mA}$$

We know that

$$I_E = \frac{V_E - V_{W2}}{1k\Omega}$$

Using theoretical values of $V_{BE,}$ we have:
We assume that V_{BE}=0.7V, since V_B = 0V (grounded), we can deduce that $V_E = -0.7V$
Select V_{w2}= -4.6V

$$I_E = \frac{-0.7 - (-4.6)}{1k\Omega} = 3.9mA$$

Therefore, ratio of I_c/I_E is

$$\frac{I_c}{I_E} = 0.942$$

The error is

$$\frac{|0.942 - 0.997|}{0.997} * 100\% = 5.51\%$$

However, through direction measurement, based on figure 4, we have $V_{1k\Omega}$ = 3.706V at the emitter junction. The actual measured I_E=3.706/1k = 3.706 mA, and the ratio of I_C/I_E=3.674/3.706=0.991

The measured error is

$$\frac{|0.991 - 0.997|}{0.997} * 100\% = 0.60\%$$

The value obtained is as expected. The values we have taken is in the forward active region and the measured current gain is equal to the theoretical gain.

PART B: MEASURING TRANSISTOR VBE

Using the XY plot function in Scopy to plot I_E *vs.* V_{BE} waveform, and export the plot to be included in your lab report. In your XY plot, X-Axis should be CH 2, Y-Axis should be CH 1.

a. What is your measured V_{BE}? How close is the measurement to the typically used value ~0.7 V?

Fig. 5. $V_{1k\Omega}$ -V_{BE} plot (right), $V_{1k\Omega}$ on the y-axis, and V_{BE} on the x-axis

Fig. 6. Enlarged $V_{1k\Omega}$ -V_{BE} plot (right), $V_{1k\Omega}$ on the y-axis, and V_{BE} on the x-axis

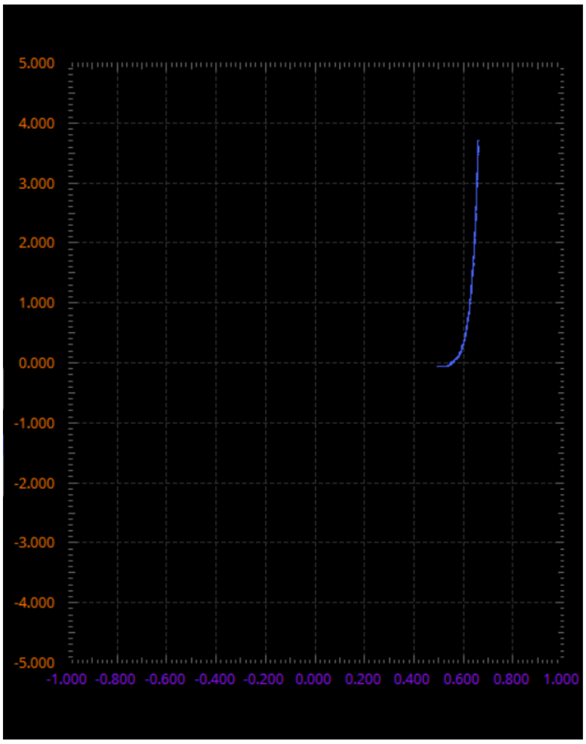


Fig. 7. Enlarged $V_{1k\Omega}$ -V_{BE} plot, $V_{1k\Omega}$ on the y-axis, and V_{BE} on the x-axis

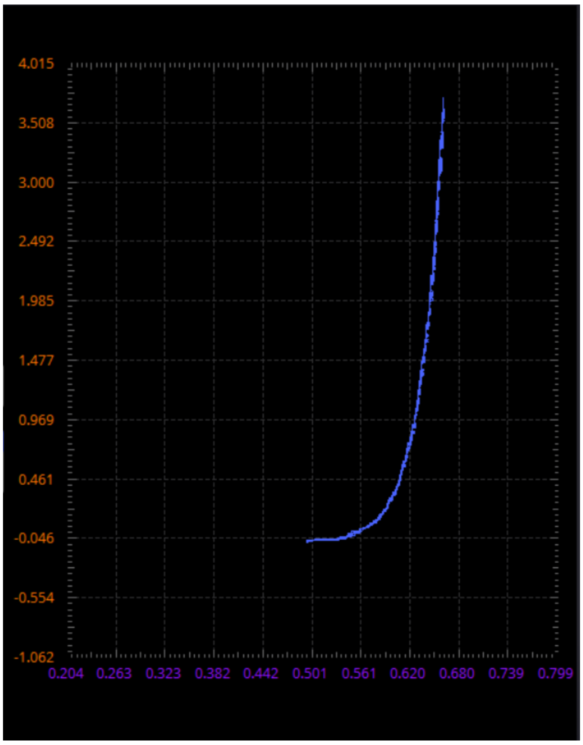


Fig. 8. Enlarged $V_{1k\Omega}$ -V_{BE} plot, $V_{1k\Omega}$ on the y-axis, and V_{BE} on the x-axis

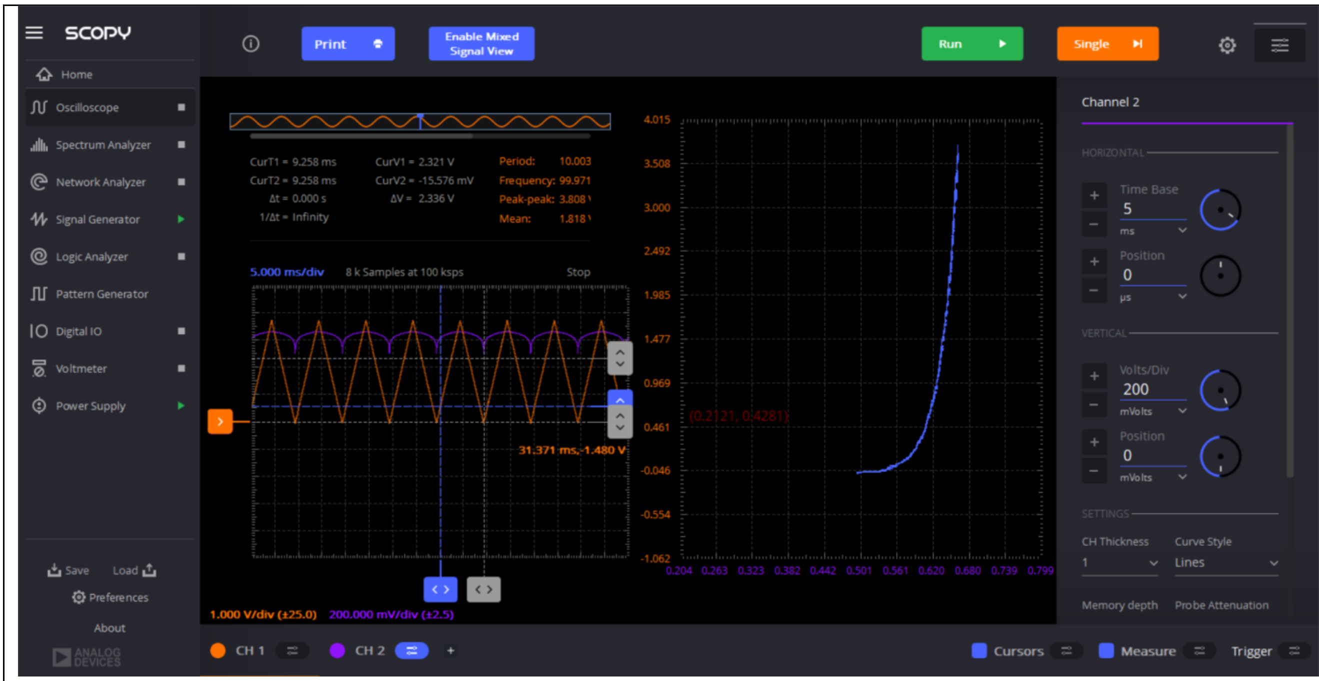


Fig. 9. Enlarged $V_{1k\Omega}$ -V_{BE} plot, $V_{1k\Omega}$ on the y-axis, and V_{BE} on the x-axis, label point 1

Fig. 10. Enlarged $V_{1k\Omega}$ -V_{BE} plot, $V_{1k\Omega}$ on the y-axis, and V_{BE} on the x-axis, label point 2

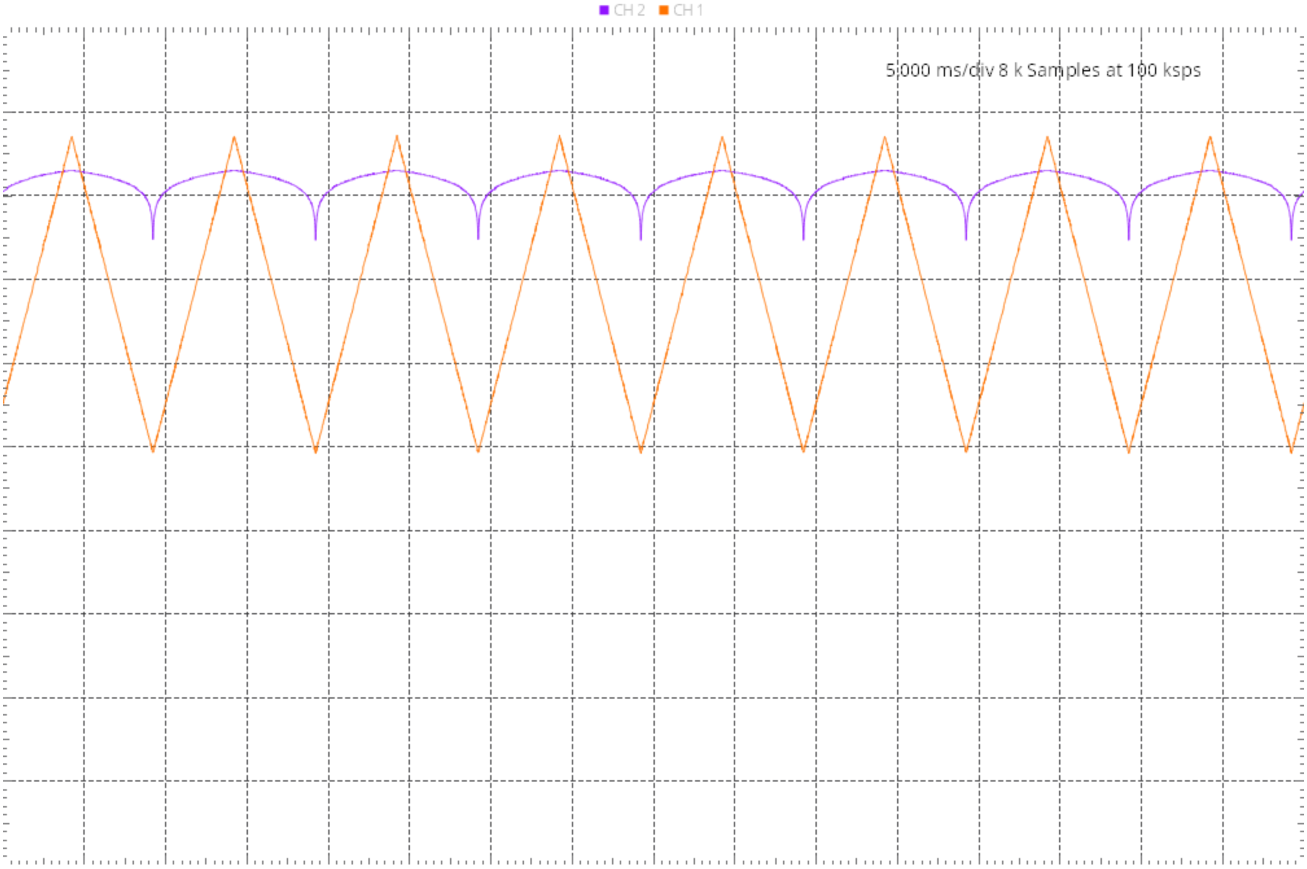
As we can see from the graph above, the measured value for Vbe is

$$V_{BE} = 690.744\ mV$$

There is a slight deviation from the nominal value V_{BE} = 0.7V.
The voltage drop between the base and emitter of a transistor) can vary depending on several factors, including temperature, manufacturing tolerances, and the specific properties of the materials used in the transistor.
The nominal value of V_{be} for a 2N3904 transistor is given as 0.7V, but in reality, the actual value can vary between 0.65V to 0.75V. It could be due to manufacturing variations, and materials used, internal

resistance which exist within the NPN Transistor itself. The difference could be due to the systematic error made during the measurement of the graph in Scopy.

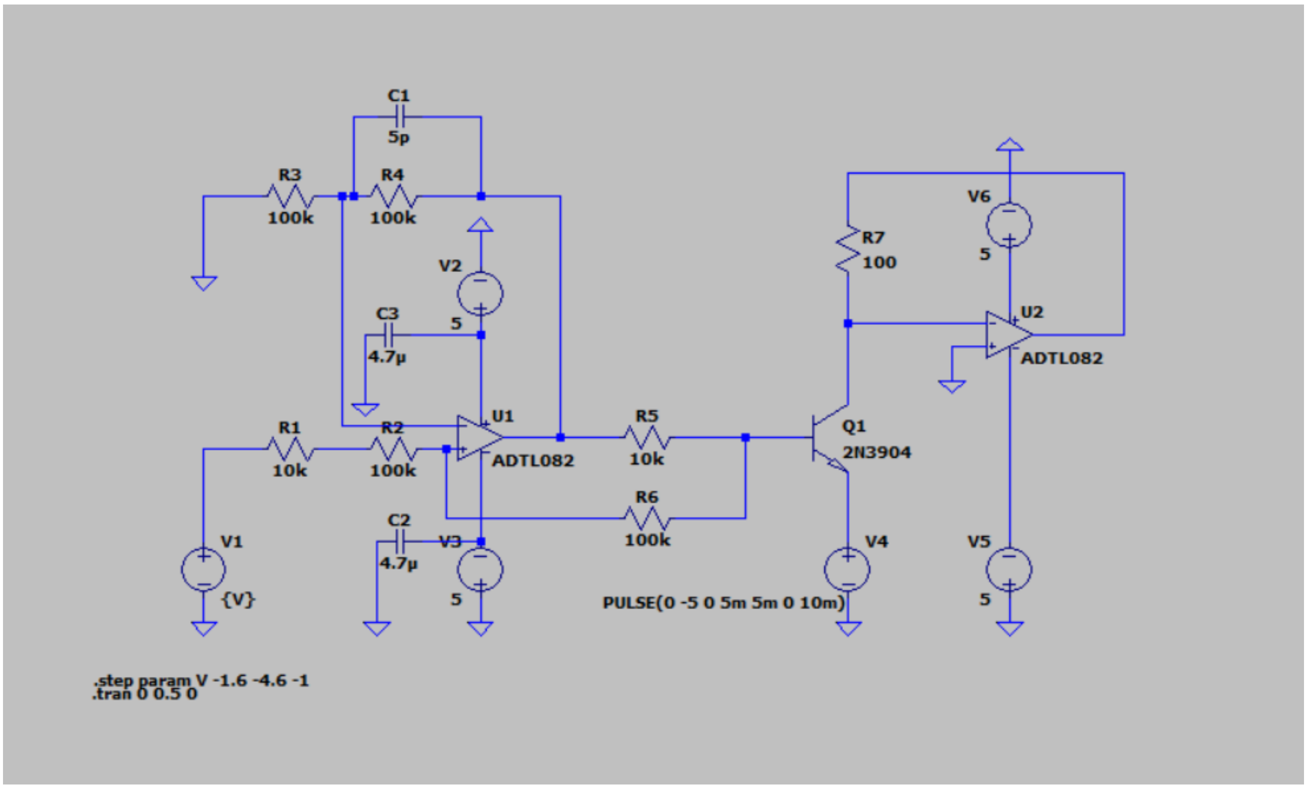
Exported Plot



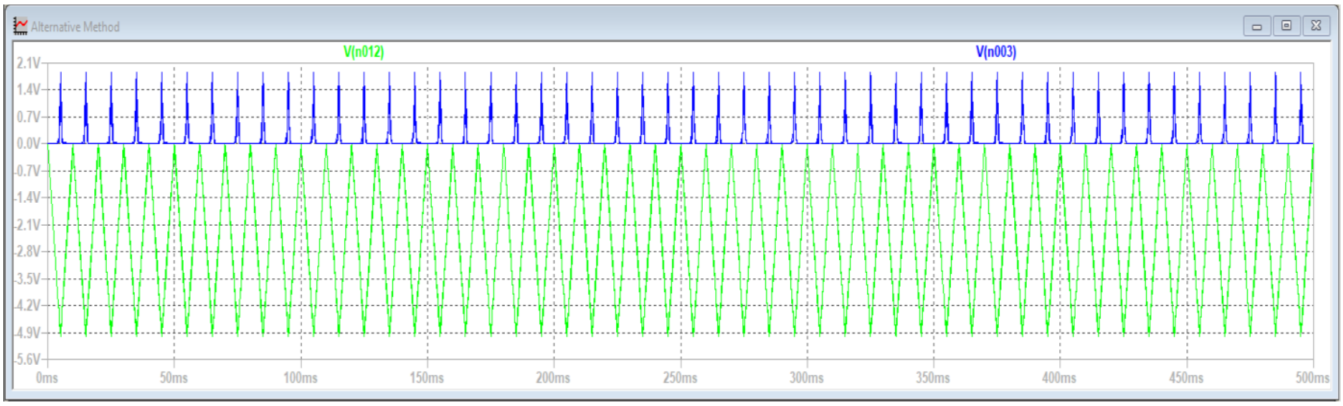
PART C: ALTERNATIVE METHOD (OPTIONAL)

Export the plot of Scope 1 and 2 waveforms to be included in your lab report.

Circuit Schematic



LTSpice Waveform



Acknowledgement

This labsheet is based on the Educational Programme of Analog Devices Inc. The original source can be found at https://wiki.analog.com/university/courses/electronics/electronics-lab-4 . Please browse their educational pages for supporting material on ADALM2000, Scopy and the devices used in this lab.

For extra information, please go to https://wiki.analog.com/university/tools/adalm2000/users .

ASSESSMENT

Student Statement:

I have read the university's statement on cheating and plagiarism, as described in the *Student Resource Guide*. This work is original and has not previously been submitted as part of another unit/subject/course. I have taken proper care safeguarding this work and made all reasonable effort to make sure it could not be copied. I understand the consequences for engaging in plagiarism as described in *Statue 4.1 Part III – Academic Misconduct*. **I certify that I have not plagiarized the work of others or engaged in collusion when preparing this submission.**

Student signature: Nigel Tan Jin Chun, Izaac Chong Yen Juin Date: 22 /03 /2023

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All components must be kept by you, for future use (including the miniproject).