MONASH University
MALAYSIA

SCHOOL OF ENGINEERING

ELECTRICAL AND COMPUTER SYSTEMS ENGINEERING

LABORATORY REPORT MARKING RUBRIC
ECE3051: ELECTRICAL ENERGY SYSTEMS

Experiment Number: 2

Title of Lab Sheet: Single Phase Diode Rectifiers

Group Number: 8

No.	Student ID	Name of Group Members	Total Marks
1	30720230	Loh Jia Quan	99.5/100
2	31106889	Agill Kumar Saravanan	99.5/100
3	30719305	Huan Meng Hui	99.5/100
4	32194471	Tan Jin Chun	99.5/100
5	32259417	Chong Yen juin	99.5/100

MARKS BREAKDOWN

Section	Total Score	Actual Marks	Scoring Band	Criteria	Comment
Results	40		30-40	Clear and completely labelled figures of the experiment/simulation results with justifications and tables. A detailed caption is provided for each figure with an in-text figure reference. The x-axis and y-axis are labelled with the unit in the bracket. The legend is provided whenever it is deemed to be required. If there is more than one line, the lines should be clearly distinguishable with the visible difference such as dotted line, dashed line and solid line, even in black and white.	39.5
			20-30	Some of the figures of the experiment/simulation setup are not clear, do not have any labelling/ caption/ in-text caption reference/ distinguishable multiple lines and are blurry. The table and justification have mistakes or errors.	
			0-20	Insufficient amounts of figures and labelling of the experiment/simulation layout setup, which is not correct and/or unclear. The table is not filled.	
Discussion	40		30-40	Complete data collection and presentation using tables/figures/ graphs with appropriate labels. Discussion of the results with prudent judgment. Have a comparison of the measured results with theoretical values and in-text citations from the peer-reviewed references. The comprehensive comparison, evaluation and justification of the results are given with clear explanation to demonstrate the understanding of the laboratory.	40
			20-30	The discussion shows little understanding of what the experiment/simulation is all about. Brief comparison, evaluation and justification of the results, with unclear/ incorrect explanation on the theoretical and experimental/ simulation results.	
			0-20	Only restatement of the results without commenting on the expected key points. Incorrect judgment/ arguments were used. No comparison, evaluation and justification of the results, with an unsatisfactory explanation on the theoretical and experimental/ simulation results.	
Conclusion, References and Appendix	20		15-20	Explained how the aims of the experiment have been achieved. The key features of the methods used, the most important results and the findings of the laboratory have been summarized. Complete references list to any book, articles and websites is provided with proper in-text citations in correct formatting. The appendix is provided in detail.	20

			10-15	A conclusion is drawn but is not supported by the experimental/ simulation evidence and a clear understanding of the findings. Incomplete references to the books or any other sources used in the report and the in-text citations are inappropriate or incorrect. The appendix is partially provided.	
			0-10	No sensible conclusion. The referencing is presented in the wrong format. No evidence, attachments, appendices are attached. Irrelevant referencing was used. Unclear understanding of the experiment without a summarized conclusion and the evidence of results. No appendix is provided.	
Total	100				99.5

Examiner/ Assessor of ECE3051: Electrical Energy Systems

Date: 15/4/2023

EXPERIMENT 2

SINGLE PHASE DIODE RECTIFIERS

Full Wave Diode Circuits

1. Resistive Load: 18.8 Ω

Experimental setup [2.5 Marks]

(Draw the circuit diagram. State the required measured values and waveforms.)

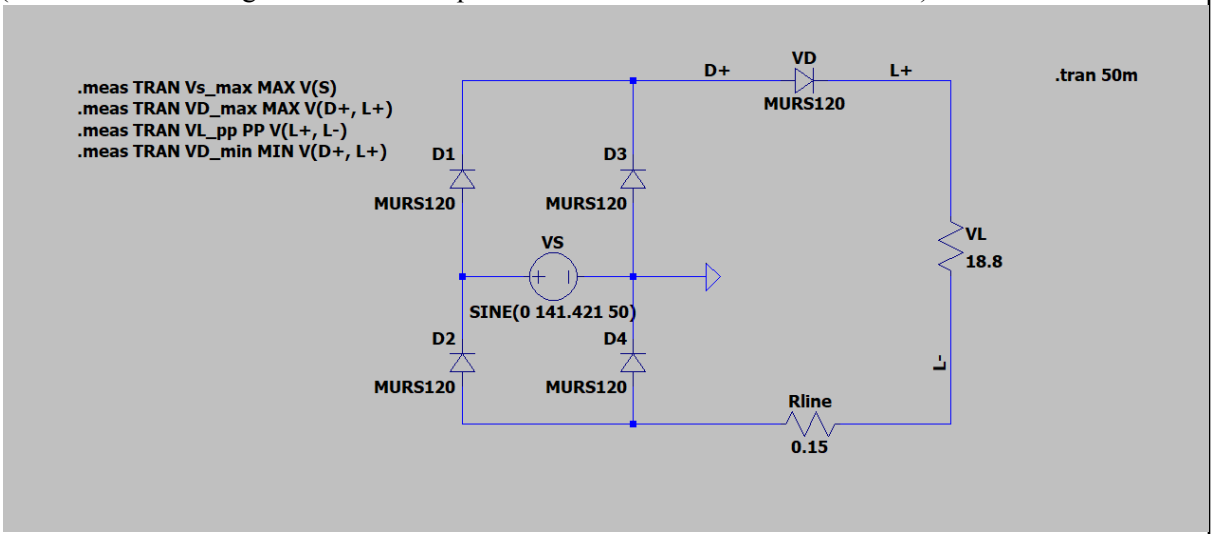

Fig.1 LTSpice Schematic of Resistive Load

The required measured values are

1. The peak value of V_S, the source voltage
2. The average value (mean) of V_L, the load resistor voltage
3. The voltage across the rectifying diode, V_D

```
SPICE Error Log: C:\Users\Chong Yen Juin\Desktop\Monash\ECE3051\Lab_2\Resistive_Load.log
Circuit: * C:\Users\Chong Yen Juin\Desktop\Monash\ECE3051\Lab_2\Resistive_Load.asc

.OP point found by inspection.

vs_max: MAX(v(s))=141.348 FROM 0 TO 0.05
vd_max: MAX(v(d+, l+))=1.02501 FROM 0 TO 0.05
vl_pp: PP(v(l+, l-))=137.171 FROM 0 TO 0.05
vd_min: MIN(v(d+, l+))=-8.61976e-06 FROM 0 TO 0.05


Date: Tue Mar 28 23:22:55 2023
Total elapsed time: 0.096 seconds.

tnom = 27
temp = 27
method = modified trap
totiter = 2711
traniter = 2711
tranpoints = 1245
accept = 1182
rejected = 63
matrix size = 11
fillins = 0
solver = Normal
Avg thread counts: 1.2/1.5/1.5/1.2
Matrix Compiler1: 504 bytes object code size  0.3/0.3/[0.2]
Matrix Compiler2: 787 bytes object code size  0.2/0.4/[0.1]
```

Fig.2 LTSpice Simulation Result of Resistive Load

checked

Calculation to get mean load voltage

$V_{L\ (peak\text{-}to\text{-}peak)} = 137.171\ V \rightarrow V_{L,mean} = \frac{2*137.171}{\pi} = 87.326V$

minus 0.5 mark

Required waveforms:
Waveform 1: V_s, V_L and V_D

Actual Measurements

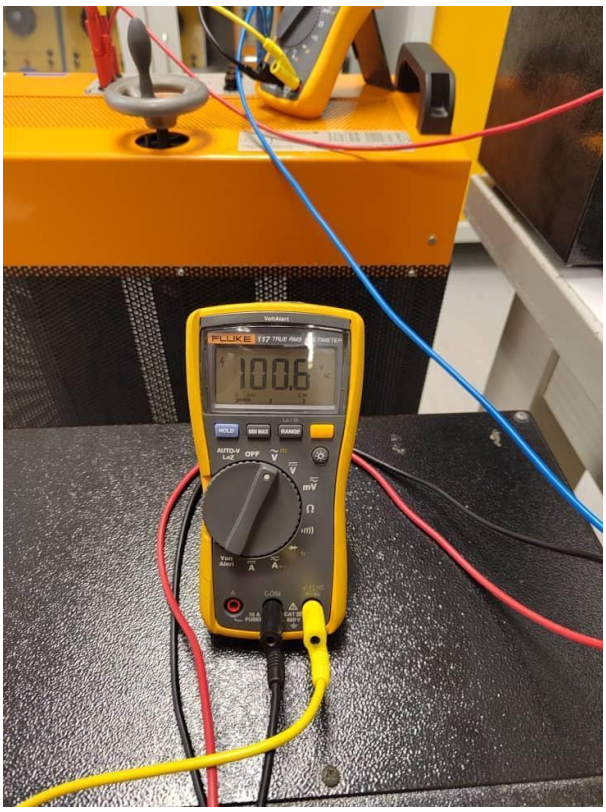

Fig 3. RMS value of source voltage, V_S measured by multimeter.

$$V_{s_{peak}} = 100\,V * \sqrt{2} = 142.27\,V$$

checked

Fig. 4 RMS value of load voltage V_L measured by multimeter.

$$V_{L_{mean}} \; in\, r.m.s. = 86.9\, V_{rms}$$

$$I_{L_{mean}} \; in\, r.m.s. = V_{L_{mean}} / R_{load} = 86.9/18.8 = 4.62A$$

Results [2.5 Marks]

Parameter	Measurement Value (Unit)
Measured Peak Source Voltage (V_S)	142.27 V
Measured Mean Load Voltage (V_L)	86.9 V_{rms}
Measured Mean Load Current (I_L)	4.62A_{RMS}

Calculation of Theoretical Value [2.5 Marks]

checked

(Include your calculation to obtain the theoretical value of Mean Load Voltage (V_L))
Mean
Since this is a full bridge rectifier, the period of the waveform can be assumed to be π.

Assumptions: Diode is ideal and does not require turn on- voltage

Mean Voltage transferred over to resistor components

$$V_{mean} = \frac{1}{T_{full\ bridge}} \int_0^{\pi} V_{ac,p-p} * sin(\omega t)\, d\omega t$$

$$V_{mean} = \frac{1}{\pi} \int_0^{\pi} V_{ac,p-p} sin(\omega t)\, d\omega t$$

$$V_{mean} = \frac{V_{ac,p-p}}{\pi} (-cos(\omega t)|_0^{\pi}$$

$$V_{mean} = \frac{100\sqrt{2}}{\pi} ((\pi) + cos(0))$$

$$V_{mean} = \frac{2*100\sqrt{2}}{\pi} = 90.03V$$

Mean Voltage transferred over to load

$$V_{mean,load} = V_{mean} * \left(\frac{18.8}{18.8+0.15}\right) = 90.03 * \frac{18.8}{18.95} V_{mean,load} = 89.32V$$

Mean Voltage transferred over to load

$$I_{mean}, load = \frac{89.32V}{18.8} = 4.75A$$

Waveforms of V_S, V_L, and V_D as one plot [2.5 Marks]

(Include the waveforms of your experimental results from CRO and simulation results from MATLAB/ Simulink or LTSpice)

CRO

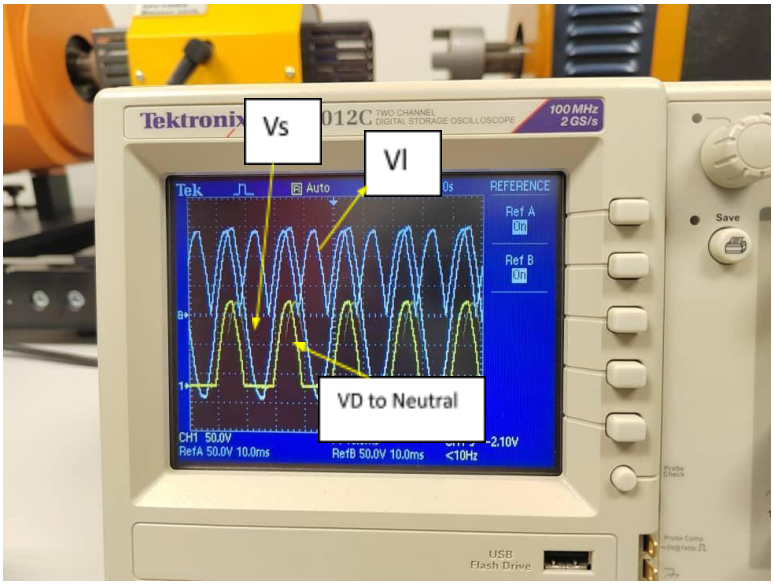

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Fig. 5. Experimental results from CRO, V_S (black), V_D (blue), V_L (Red); y-axis is voltage (V), x-axis is time (ms)

LTSpice

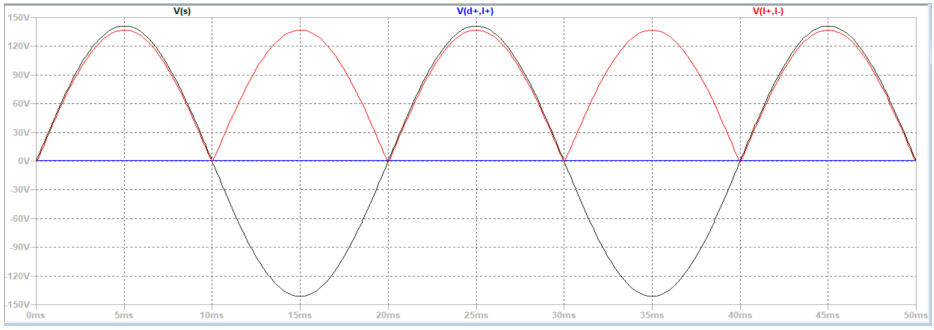

Fig. 6. Simulated waveforms in LTSpice, V_S (black), V_D (blue), V_L (Red); Y axis is voltage (V), X axis is time(ms)

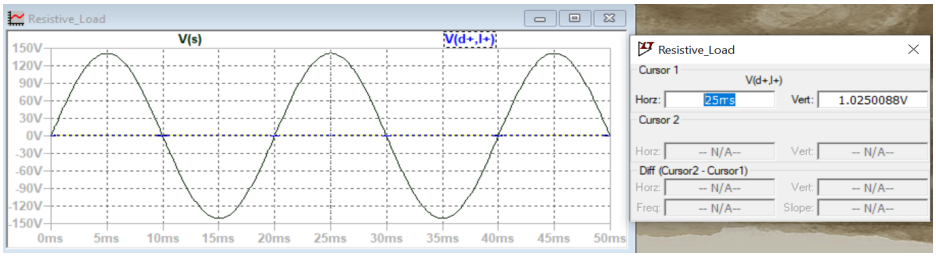

Fig. 7. Simulated waveforms in LTSpice, V_S (black), V_D (blue), with values; Y axis is voltage (V), X axis is time(ms)

Discussion [5 Marks]

(Discuss the waveforms obtained from your experimental and simulation results)

The waveforms displayed in Figure 5 measured by the CRO are analyzed after AC coupling and scaled down, offset on the screen appropriately for comparison purposes. The waveforms have no DC offset after AC coupling. The simulation result matches the experimental results.

The peak of experimental V_S is around 142.27 V, which is approximately the same as the results obtained from simulation, both are sine waves with no phase shift.

In simulation, the load voltage waveform is a fully-rectified sine wave, 137 V_{p-p}. Similarly, the mean voltage across the load, V_L is a fully-rectified sine wave 86.9 V_{RMS}.. The load voltage waveform is fully rectified because four diodes are employed to create a full-wave rectification. During the negative half-cycle of V_S, the current passes through D1 and D4, while during the other cycle the current passes through D2 and D3, effectively rendering the load voltage to take the absolute value of V_S, approximately.

The experimental waveform of V_D is the node V_{D+} to Neutral, this is to avoid the shorting of the diode. However, the simulation of the V_D waveform is very close to 0V, showing a voltage of 1.02V. But as we measured during the experiment, the V_D (experimental) is only 912 mV higher than the load voltage waveform during its peak, otherwise it would look like a straight line if it is not scaled up. The

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micro-voltage level difference is due to the turn-on voltage of the diode. V_D has shown no DC offset due to AC coupling as well.

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2. Resistive – Inductive Load: 18.8 Ω and 250 mH in series

Experimental setup [5 Marks]

(Draw the circuit diagram. State the required measured values and waveforms.)

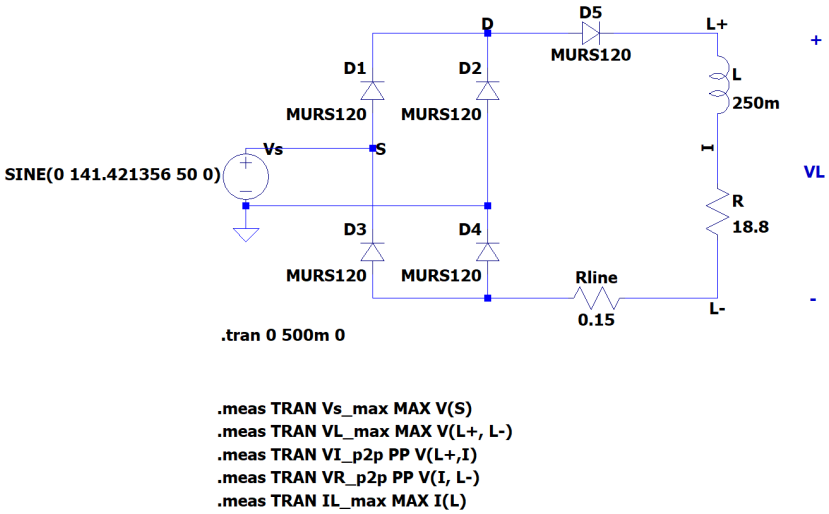

Fig.8 LTSpice Schematic of Resistive and Inductive Load

The required measured values are:
Vs_max - the peak of the source voltage
VL_max - the peak of the voltage across the inductor + 18.8Ω resistor
VI_p2p - the peak-to-peak voltage of the inductor only
VR_p2p - the peak-to-peak voltage of the 18.8Ω resistor only
IL_max - the peak current through the inductor.

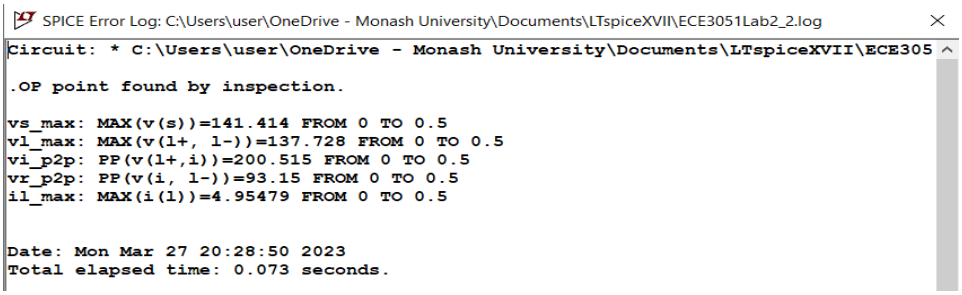

Fig.9 LTSpice Result of Resistive and Inductive Load

Required waveforms are:
Waveform 1: $V_{s,}$ $V_{L,}$ I_L
Waveform 2: $V_{L,}$ V_R and V_I

Waveforms of V_S, V_L and I_L; and V_L, V_R and V_I as one plot [5 Marks]

(Include the waveforms of your experimental results from CRO and simulation results from MATLAB/ Simulink or LTSpice.

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Project the waveforms of VS, VL, and IL in the CRO as one plot.

CRO

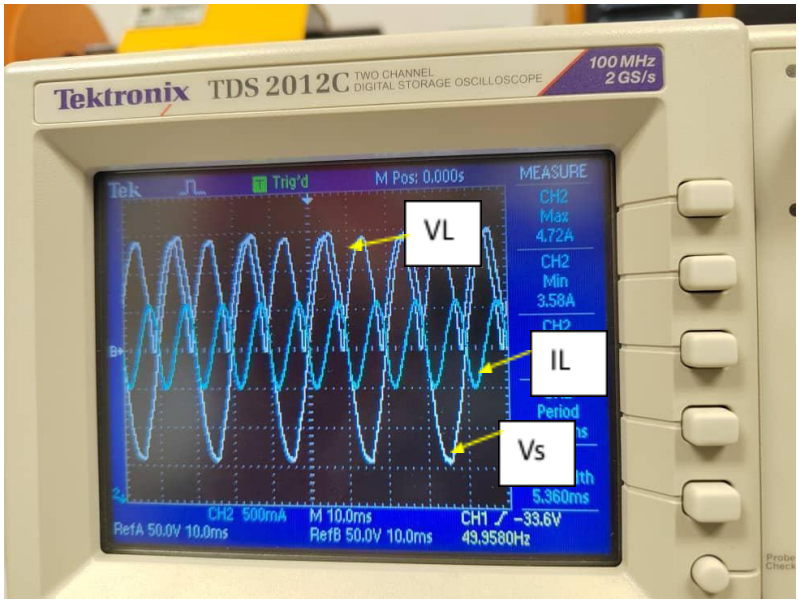

Fig. 10. Experimental results from CRO, V_L (black), V_S, I_L; y-axis is voltage (V) for V_L and V_S and current (A) for I_L, x-axis is time (ms)

LTSpice

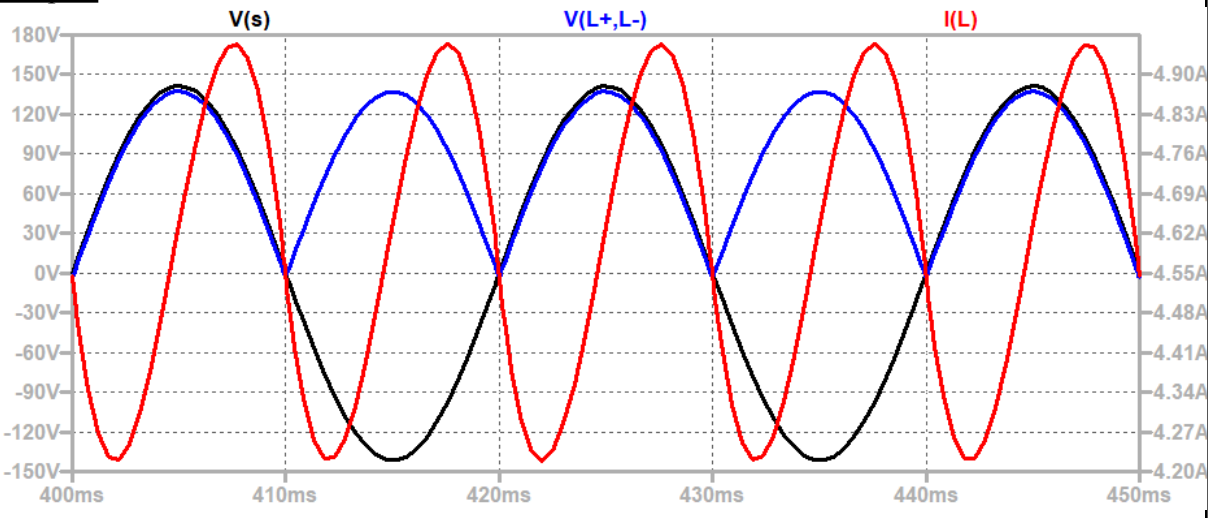

Fig. 11. LTSpice waveforms of V_S (black - voltage (V)), V_L (blue - voltage (V)), and I_L (red - current (A)); x-axis is time (ms)

Project the waveforms of VL, VR, and VI in the CRO as one plot.

CRO

checked

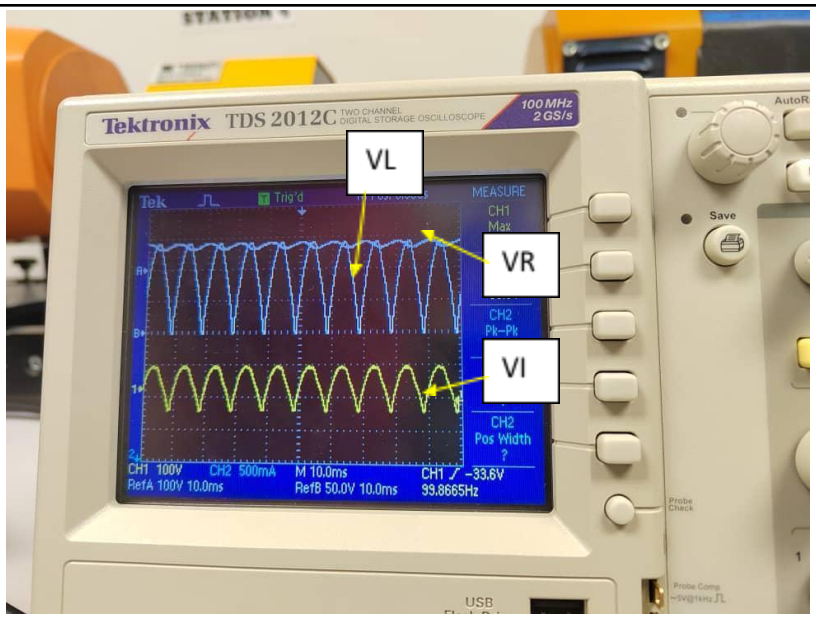

Fig. 12. Experimental results from CRO, V_L, V_S, V_R (yellow); y-axis is voltage (V), x-axis is time (ms)

LTSpice

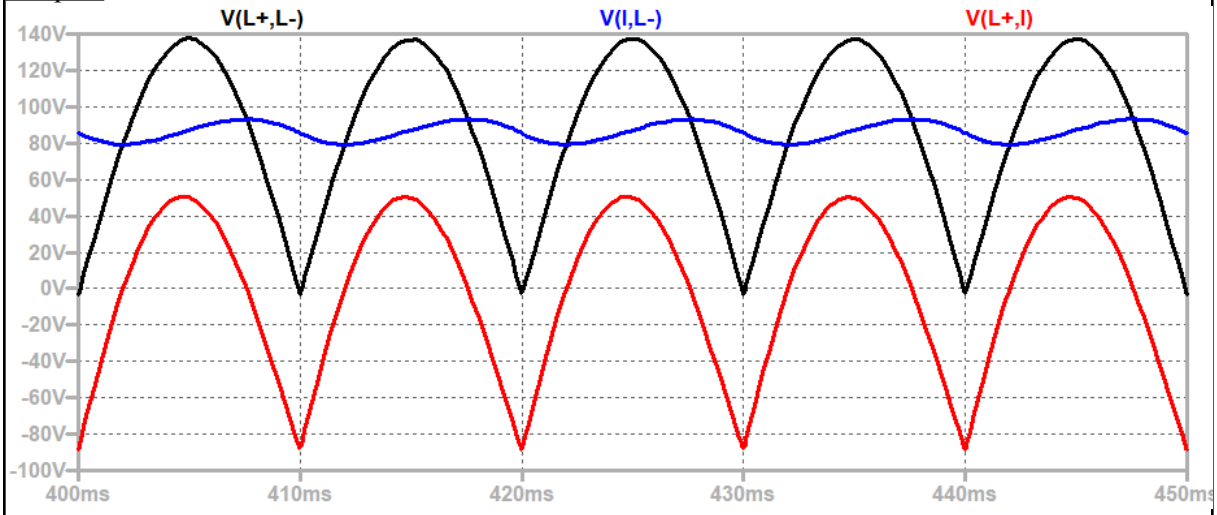

Fig. 13. LTSpice waveforms of V_L (black), V_R (blue), and V_I (red); y-axis is voltage (V), x-axis is time (ms)

Measure the conduction angle

$$conduction\ angle\ = \frac{t_C}{T_S} \times 360$$

Where t_C is the conduction time (ie. when I_L is positive), and T_S is the period of Vs. According to experimental and simulated results, current through the inductor is always positive, therefore the conduction time is equal to the period of Vs. Therefore, the conduction angle is 360 degrees.

Determine the relationship between V_R, and V_I waveforms at the point where di/dt = 0

di/dt = 0 occurs at the turning points of I_L (max or min), where the gradient is zero. In fig. x, V_L is shown to be very close to zero, while V_R is at its maximum when di/dt = 0. Note that in the

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experimental setup section above, the maximum value of various waveforms have been measured in LTSpice via the .meas function.

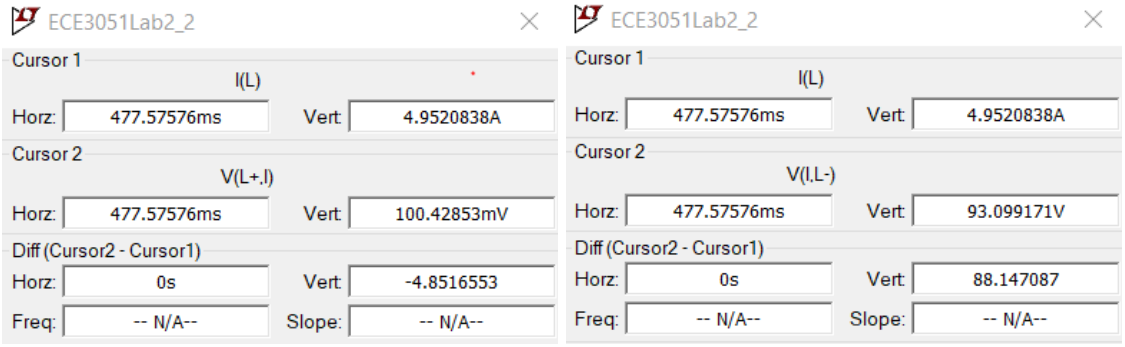

Fig. 14. LTSpice cursor measurements of V_I (Left) and V_R (right) when di/dt = 0

In fig. 15 below, the red dotted lines show where di/dt = 0.

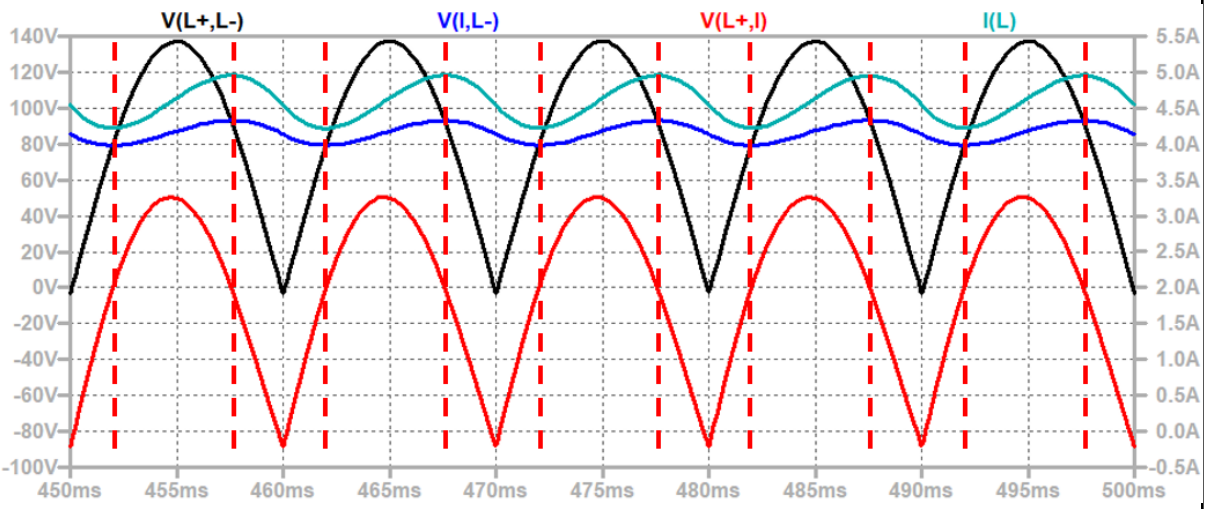

Fig. 15. V_L (black), V_I (red), V_R (blue) waveforms with red dashed lines at di/dt = 0; y-axis is voltage (V) except for I_L current (A), x-axis is time (ms)

The voltage drop across the load is the sum of the voltage drop across the inductor and resistor respectively, given by the equation below.

$$V_L = iR + L\, di/dt$$

When di/dt = 0, all the voltage is dropped across the resistor (ie $V_L = iR$). The voltage drop across the inductor ($V_I = L$ di/dt) is therefore 0V.

Discussion [5 Marks]

checked

(Discuss the waveforms obtained from your experimental and simulation results)

All waveforms captured by the CRO match the simulations. Note that the CRO waveforms are AC coupled (their DC offset has been removed), and are scaled for easier comparison with the simulation results.

Analysing the waveforms individually:

V_S (Source Voltage)

A sine wave is observed on the CRO. Although the amplitude was not explicitly measured in this question, the voltage reading on the multimeter was 99.1Vrms, which translates to 140.1V peak. Comparing with the ideal 141.42V in the simulation, there were some resistive losses that resulted in a slightly lower value.

V_L (Voltage across the load)

The voltage across the load is a fully rectified sine wave. This is expected since the circuit is a full wave rectifier.

I_L (Current through the load)

It is noticed that the current waveform has twice the frequency as the voltage waveform. This is because a full wave rectifier circuit utilizes both halves of the AC input signal to produce a unidirectional DC output signal. In other words, the output waveform has twice as many peaks as the input waveform, and the current flow in the circuit also changes direction twice as frequently as the input voltage.

V_R (Voltage across the resistor)

A sine wave is observed at the CRO which resembles the shape and magnitude of the simulated waveform. The magnitude is small in comparison with VI because the resistance value is small.

V_I (Voltage across the inductor

A rectified sine wave is observed at the CRO. It is phase shifted approximately 90 deg from VR, this is expected as since the current flowing through the resistor and the inductor is the same, the voltage of the inductor must lag the current waveform by 90 deg.

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3. Resistive – Inductive Load: 18.8 Ω and 250 mH in series with FWD

Experimental setup [5 Marks]

(Draw the circuit diagram. State the required measured values and waveforms)

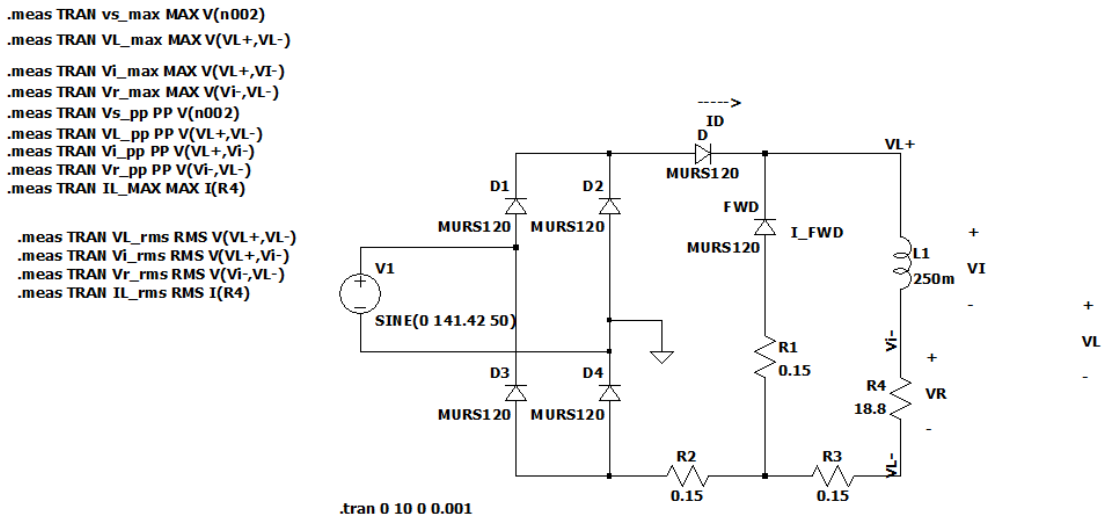

Fig.16. LTSpice Schematic of Resistive and Inductive Load in series with FWD

The measured values are

1. potential difference V_{L+} and V_{L-}, V_L
2. potential difference between the inductor L1, V_I and R4, V_R respectively
3. current across diode D, I_D and FWD, I_{FWD} and I_L

```
Circuit: * H:\My Drive\ECE3051\Lab 2\Q3.asc

.OP point found by inspection.

vs_max: MAX(v(n002))=141.42 FROM 0 TO 10
vl_max: MAX(v(vl+,vl-))=137.781 FROM 0 TO 10
vi_max: MAX(v(vl+,vi-))=111.959 FROM 0 TO 10
vr_max: MAX(v(vi-,vl-))=91.7434 FROM 0 TO 10

vs_pp: PP(v(n002))=282.84 FROM 0 TO 10
vl_pp: PP(v(vl+,vl-))=140.065 FROM 0 TO 10
vi_pp: PP(v(vl+,vi-))=198.799 FROM 0 TO 10
vr_pp: PP(v(vi-,vl-))=91.7434 FROM 0 TO 10

il_max: MAX(i(r4))=2.78265e-010 FROM 0 TO 10

vl_rms: RMS(v(vl+,vl-))=94.4307 FROM 0 TO 10
vi_rms: RMS(v(vl+,vi-))=42.7068 FROM 0 TO 10
vr_rms: RMS(v(vi-,vl-))=85.3548 FROM 0 TO 10
il_rms: RMS(i(r4))=4.54015 FROM 0 TO 10
```

Fig.17. LTSpice Results of Resistive and Inductive Load in series with FWD

Required waveforms are:
Waveform 1: V_L, V_I, V_R
Waveform 21: V_L, I_D, I_{FWD}
Waveform 3: I_D, I_{FWD}, I_L

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Waveforms of V_L, V_R and V_I; V_L, I_D and I_{FWD}; and I_D, I_{FWD} and I_L as one plot [5 Marks]

(Include the waveforms of your experimental results from CRO and simulation results from MATLAB/ Simulink or LTSpice. Determine how all three currents are related to each other.)

CRO

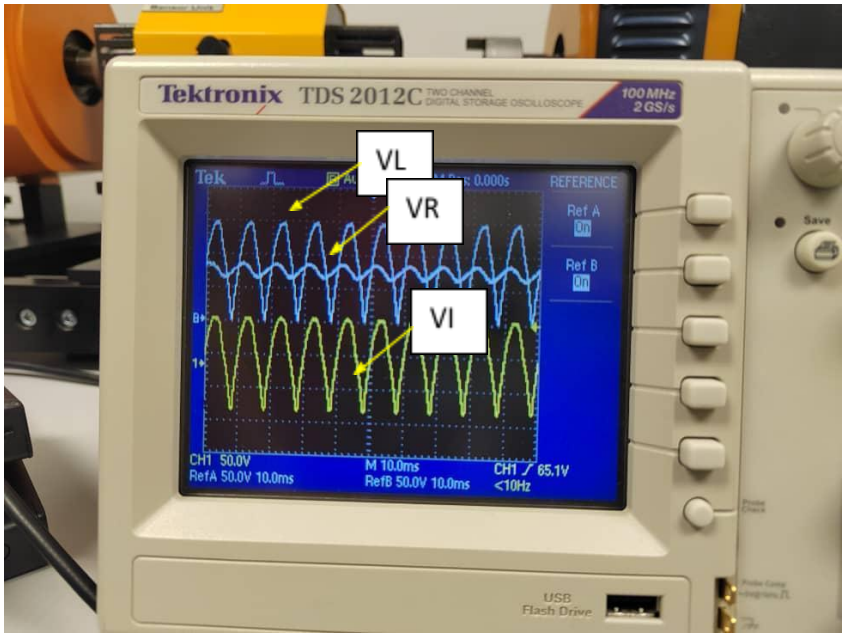

Fig. 18. Experimental results from CRO, V_L, V_S, V_I (yellow); y-axis is voltage (V), x-axis is time (ms)

LTSpice

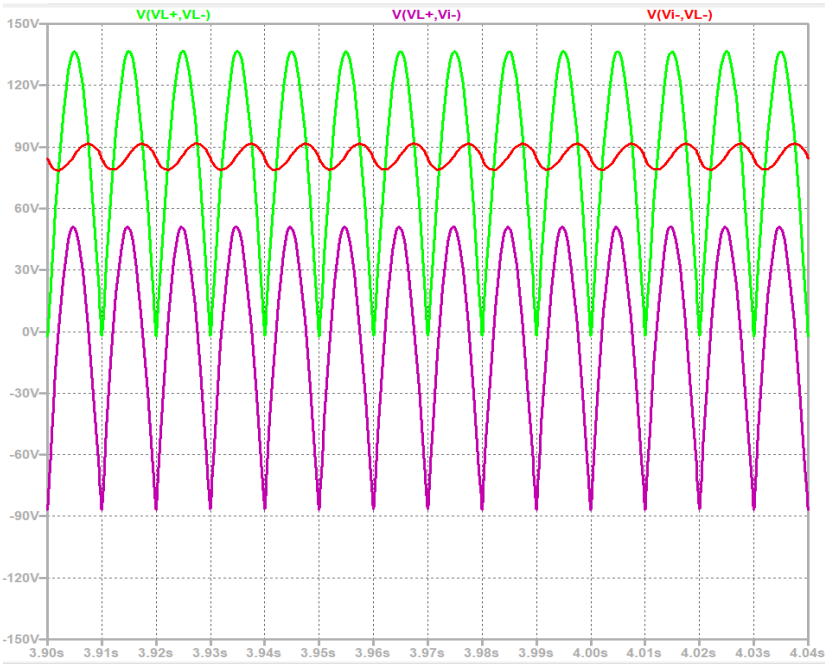

Fig. 19. LTSpice waveforms of $V_{L\ (Green)}$, $V_{I\ (Purple)}$, $V_{R\ (red)}$

CRO

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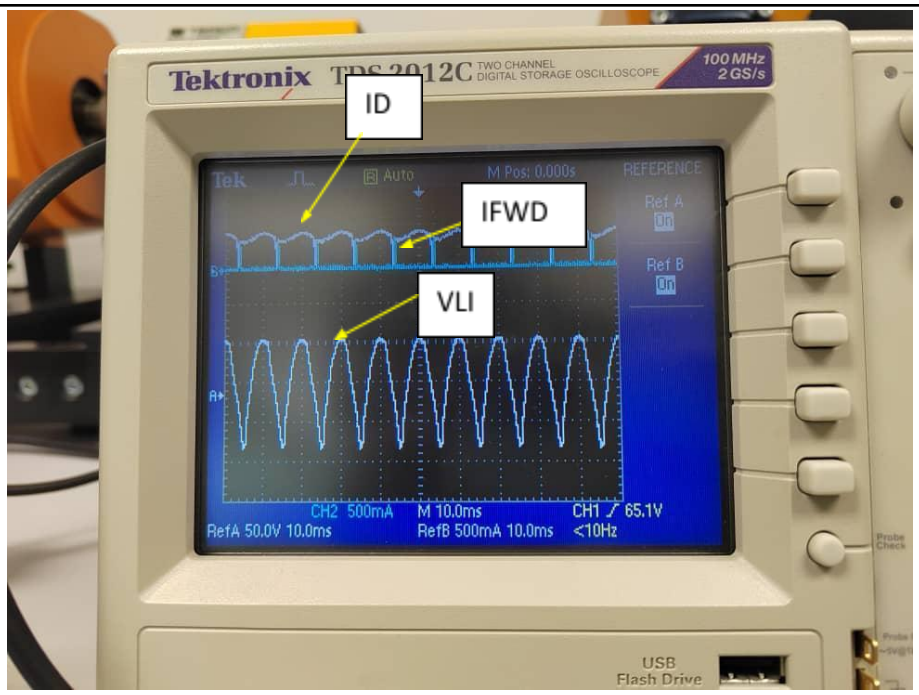

Fig. 18. Experimental results from CRO, I_D, I_{FWD}, V_{LI} ; y-axis is voltage (V_{LI}) and current (A) for I_D, I_{FWD}, x-axis is time (ms)

LTSpice

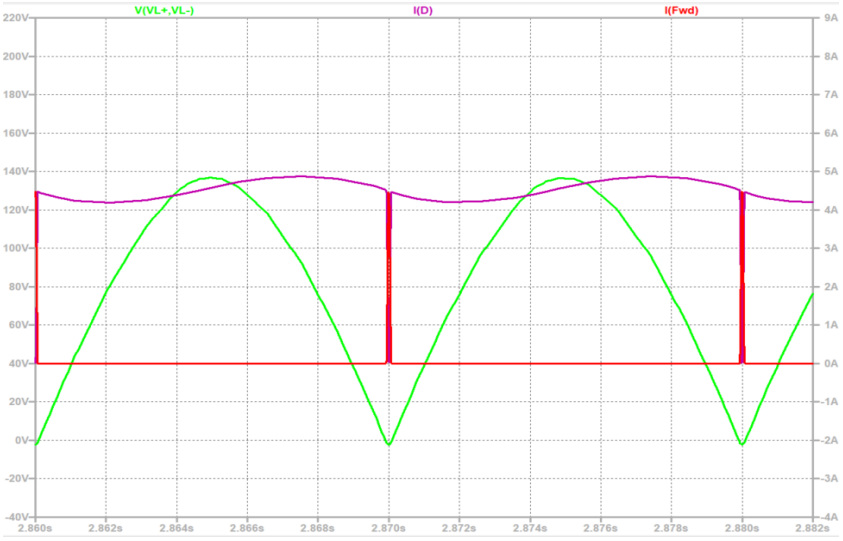

Fig. 19. LTSpice waveforms of $V_{L\ (Green)}$, $I_{D\ (Purple)}$, $I_{FWD\ (Red)}$, y-axis is voltage (V_{LI}) and current (A) for I_D, I_{FWD}, x-axis is time (ms)

checked

CRO

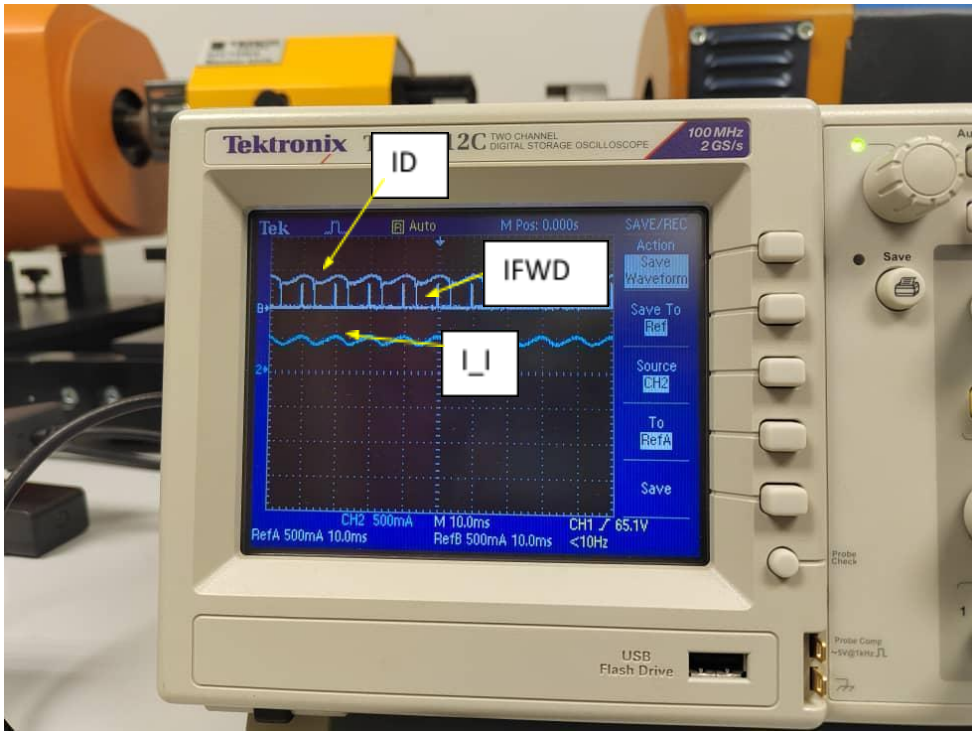

Fig. 20. Experimental results from CRO, I_D, I_{FWD}, I_I ; y-axis is current (A), x-axis is time (ms)

LTSpice

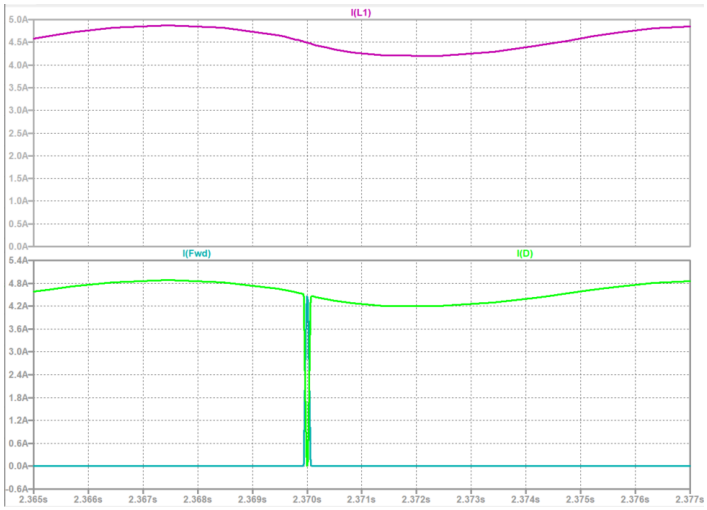

Fig. 21. LTSpice waveforms I_D, I_{FWD}, I_I ; y-axis is current (A), x-axis is time (ms)

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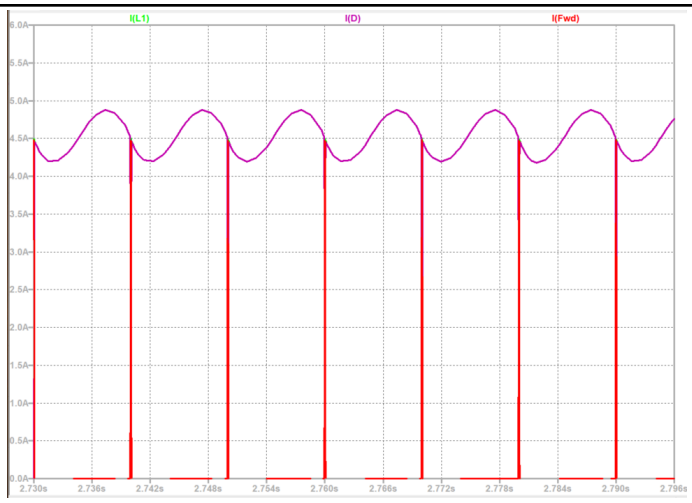

Fig. 22. LTSpice waveforms of $I_{D\ (Green)}$, $I_{FWD\ (Turquoise)}$, $I_{l\ (Purple)\ (Zoomed\ In)}$/ $I_{D\ (Purple)}$, $I_{FWD\ (Red)}$, $I_{L(Green)\ (Zoomed\ out)}$; y-axis is current (A), x-axis is time (ms)

Determine how all three currents are related to each other.
The currents are related by Kirchoff's Law on the Conservation of Current
We can see that $I_{FWD} + I_D = I_L$

Discussion [5 Marks]

(Discuss the waveforms obtained from your experimental and simulation results)

It can be observed that the resistor voltage is getting a small ripple voltage around 90V, whereas the inductor voltage follows the rectified voltage shape closely. If we were to add the inductor voltage and resistor voltage, we would obtain the exact voltage given by VL, which obeys Kirchhoff's Voltage Law. The presence of the inductor and the full bridge rectifier was able to regulate the load voltage at approximately 90V.

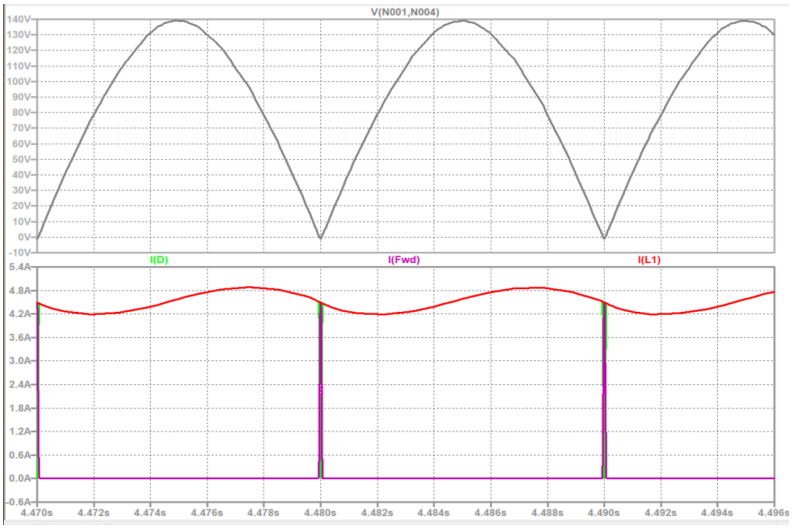

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Fig. 23. LTSpice waveforms of V_L (first waveform on top) y-axis is voltage (V), x-axis is time (ms), , $I_{D\ (Green)}$, $I_{L1\ (Red)}$, $I_{FWD\ (Blue)}$; y-axis is current (A), x-axis is time (ms)

For the current waveform, the explanations can be divided into when Diode D is forward biased and reverse biased. Diode D will be forward biased, when the supply voltage exceeds the turn-on voltage of the diode, and will be in reverse biased when the rectified supply voltage is below the turn on voltage of Diode D.

When Diode D is forward biased, the branch with the Free-Wheeling Diode can be disregarded as the FWD is now in reverse bias. The current waveform across the load resistor and inductor, I_L should follow the shape of the resistor voltage, based on Ohm's Law and the branch being in series. I_D should also be identical to I_L due to Kirchhoff's Current Law.

When Diode D is in reverse biased, the FWD will then become forward active, allowing current flow, which explains the drop in current across Diode D and the increase in current of the FWD, which is due to the energy supply from the inductor. However, as this is a Full Bridge Rectifier, Diode D will be in forward biased in the next half cycle. The spikes of the current flow in both the diode current and FWD current is due to the momentary switching of current flow.

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4. Resistive Load: 18.8 Ω with Output Capacitor

Experimental setup [5 Marks]

Draw the circuit diagram. State the required measured values and waveforms.)

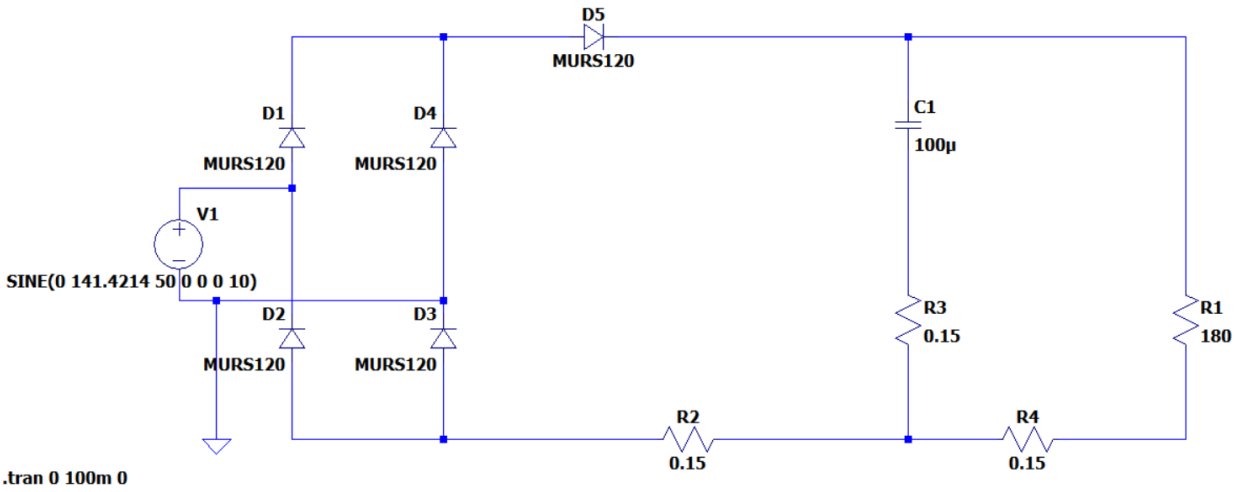

Fig.24. LTSpice Schematic of Resistive and Capacitive Load

The required measurements are

1. the source voltage waveform (Vs)
2. the load voltage waveform (V_L)
3. and the voltage across the rectifying diode (V_D).
4. We also need to determine the voltage ripple in the load voltage

The required waveform is

Waveform 1: Vs (The source voltage waveform), V_L (The load voltage waveform), V_D (the voltage across the rectifying diode).

Waveforms of V_S, V_L and V_D; V_S and V_L; as one plot [5 Marks]

(Include the waveforms of your experimental results from CRO and simulation results from MATLAB/ Simulink or LTSpice. Determine the voltage ripple in the load voltage. Set the resistance of the resistive load to the maximum value. Explain how this ripple voltage changes with the new load)

CRO

When RL = 18.8 Ohm

checked

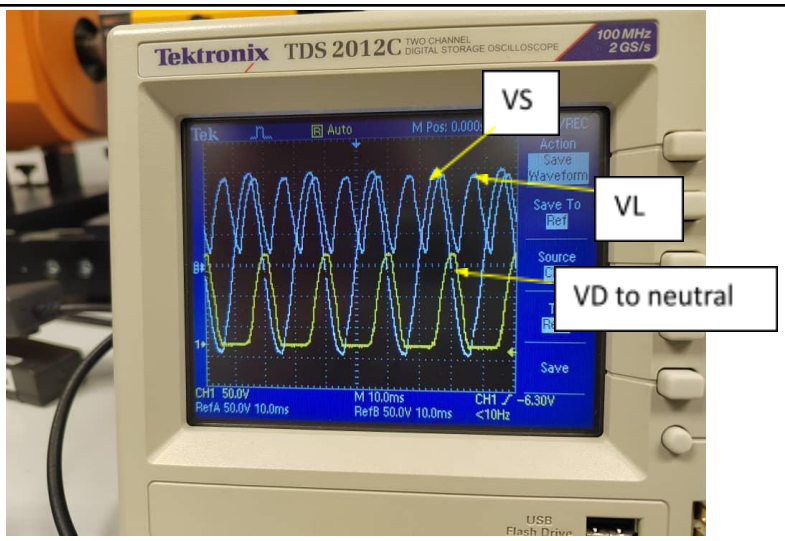

Fig. 25. Experimental results from CRO, V_S, V_L, V_D (to neutral to avoid short circuit) ; y-axis is Voltage (V), x-axis is time (ms)

LTSpice

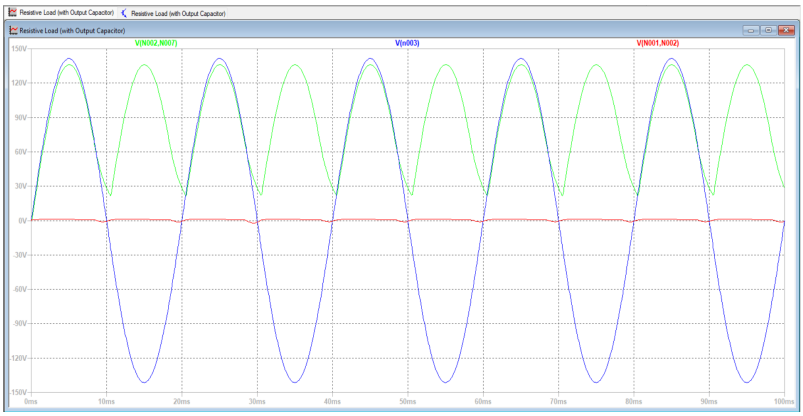

Fig. 26. LTSpice waveforms V_S (Blue), V_L (Green), V_D (Red) ; y-axis is voltage (V), x-axis is time (ms)

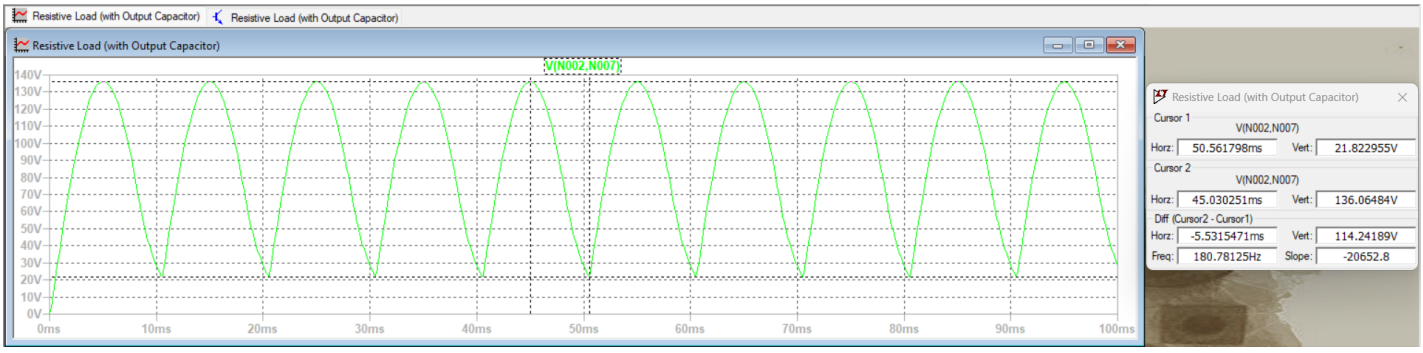

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Fig. 27. LTSpice waveforms V_S (Blue), V_L (Green), V_D (Red) ; y-axis is voltage (V), x-axis is time (ms); with measurements taken

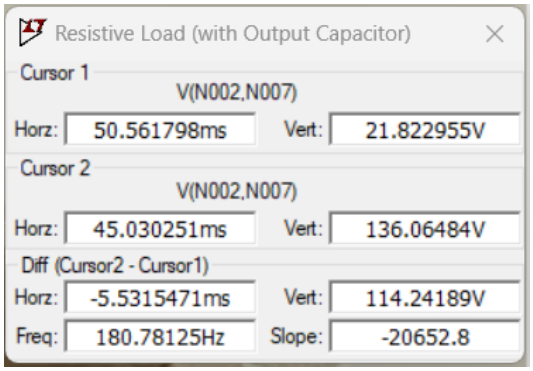

Fig. 28. LTSpice waveforms V_S (Blue), V_L (Green), V_D (Red) ; y-axis is voltage (V), x-axis is time (ms); with measurements taken (zoom in)

CRO

When RL = 180 Ohm

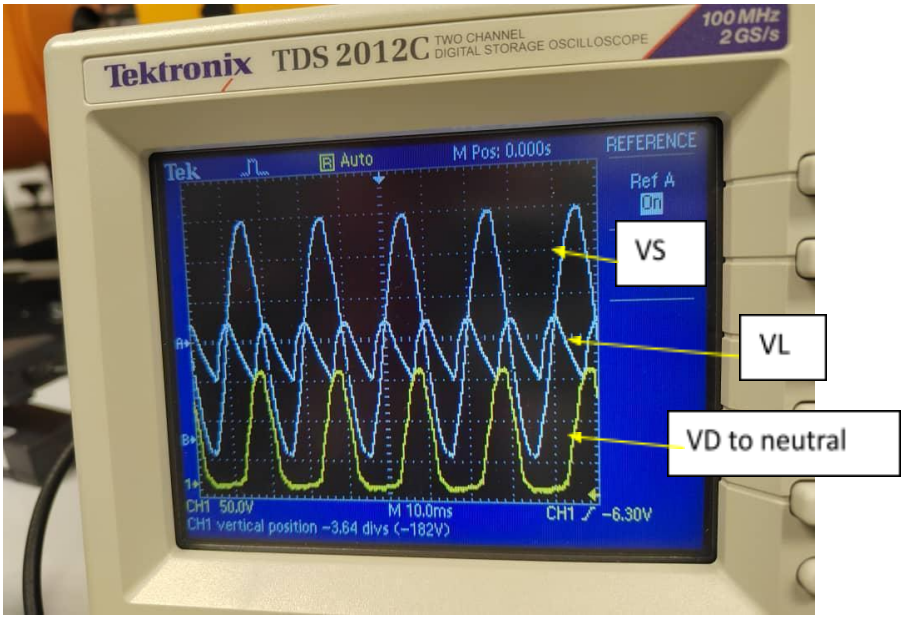

Fig. 29. Experimental results from CRO, V_S, V_L, V_D (to neutral to avoid short circuit) ; y-axis is Voltage (V), x-axis is time (ms); maximum resistance load

LTSpice

checked

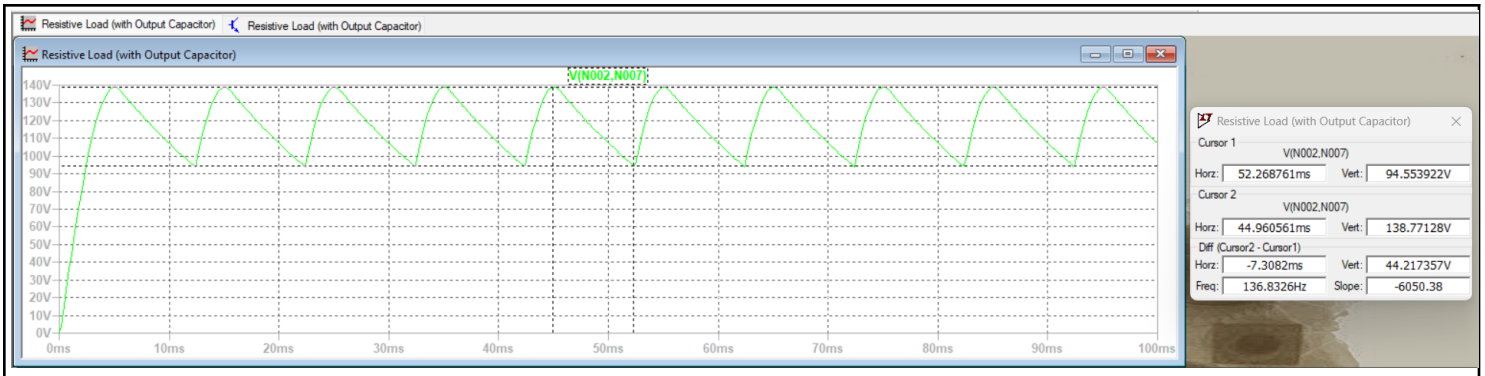

Fig. 30. LTSpice waveforms V_S (Blue), V_L (Green), V_D (Red) ; y-axis is voltage (V), x-axis is time (ms); with measurements taken; maximum resistance load

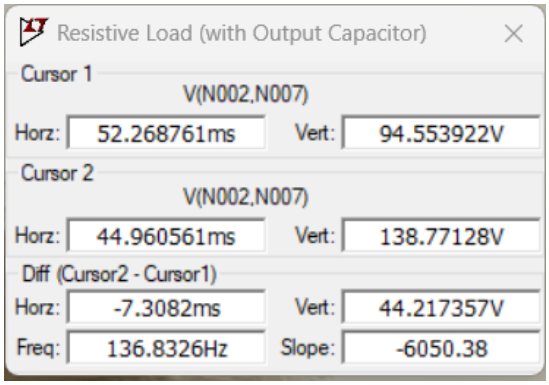

Fig. 31. LTSpice waveforms V_S (Blue), V_L (Green), V_D (Red) ; y-axis is voltage (V), x-axis is time (ms); with measurements taken; maximum resistance load (Zoom in)

Based on the measured simulated values, we can make our deduction about the voltage ripple in the load voltage

<u>When RL is 18.8Ω</u>

min(VL,18.8Ω) = 21.822955V
max(VL,18.8Ω) = 136.0648V
$VL, ripple$,18.8Ω = max(VL,18.8Ω) − min(VL,18.8Ω) = 114.241845V

<u>When RL is 180Ω</u>

min(VL,180Ω) = 94.553922V
max(VL,180Ω) = 138.77128V
$VL, ripple$,180Ω = max(VL,180Ω) − min(VL,180Ω) = 44.217358V

As we can see from the above calculated values, we can deduce that as the resistance of the load increases, the voltage ripple in the load voltage will decrease.

Discussion [5 Marks]

(Discuss the waveforms obtained from your experimental and simulation results)
The waveforms of VS, VD and VL from the experimental results and simulation results **should be similar**.

checked

As we can see from the above simulated and experimental graph, Vs is a full sine wave and VL is a fully rectified wave that has different rise and fall time. The reason for the waveform shape of VL is due to the discharge of the 100 µF capacitor. The discharge of the capacitor is an exponential decay which would result in the waveform shown above.

VD is also a rectified wave. The reason for the small voltage is because the voltage required for the diode to conduct is small. We can also deduce that as the load resistance increases, the voltage ripple decreases, but the maximum and minimum values of the load voltage increase. The voltage ripple becomes more apparent too.

We can explain this phenomenon by looking at the capacitor. As the capacitor starts to accumulate energy (electric field), the voltage at the positive terminal of the diode, D will become lower and the voltage at the negative terminal of the diode, D will increase when the source voltage, Vs starts to decrease from its maximum value. Diode D will become reverse biased and this would cut off (disconnect) the load from the source.

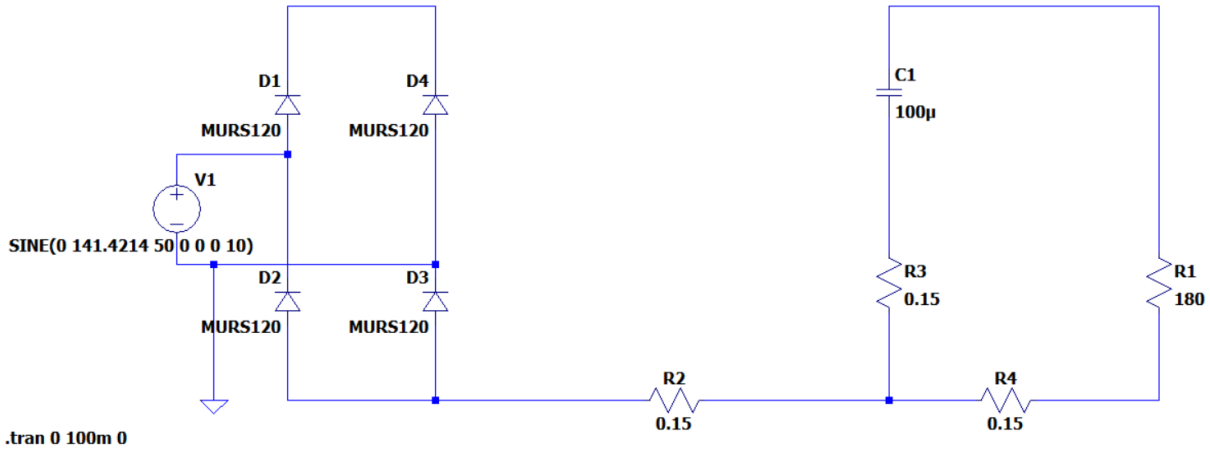

Fig. 32. LTSpice Schematic of Resistive and Capacitive Load, diode in reverse bias

When Vs starts to decrease from its maximum value to the value of the rectified voltage, the rectified voltage, Vrec, will be larger than the voltage across the load, VL. The capacitor will discharge and will act as the energy source of the load.

The current flowing through the diode D will be 0. This means that the current flowing through C1, R3 and R1 is zero as well.

$$-\frac{V_L}{R_L} = C\frac{dV_C}{dt}$$

$$V_L = -R_L C\frac{dV_C}{dt}$$

We can deduce from the above equation that the time constant is RLC and is directly proportional to RL which explains why the capacitor takes some time to discharge when the resistance of the load increases. This explains why as the resistance of the load increases, we will have a smaller ripple voltage.

checked

General Discussion

1. List four main differences between a full-wave and a half-wave diode rectifier circuit. State the difference in terms of efficiency for both the full-wave and half-wave diode rectifier circuit. [10 Marks]

Difference 1:
Full-wave rectification rectifies the negative component of the input voltage to a positive voltage (thus converting it into DC using a diode bridge configuration. This means the full bridge is bidirectional in nature as it allows current to flow in 2 directions in the supply (1 direction in the load)
Half-wave just removes the negative voltage component, thus only allowing current flow in one direction of the AC supply [1]
The waveforms of both configurations are shown below

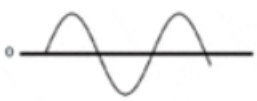

Fig. 33. Input waveform

Fig. 34. voltage waveform after rectification (full bridge)

Fig. 35. voltage waveform after rectification (half bridge)

Difference 2:
A full wave rectifier uses up to 2 (center tapped)-4(bridge) diodes to perform the full rectification. Conversely, a half wave rectifier only uses 1 diode to ensure current flows in one direction.

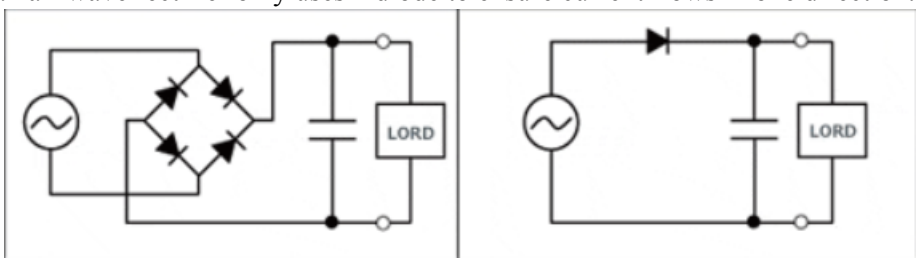

Fig. 36. (left) Full-wave rectification; (right) Half-wave rectification

Difference 3:
The output frequency of the full wave rectification is double of the supply voltage frequency due to the full rectification allowing it to be continuous. The output frequency of the half wave frequency is the same as the supply voltage frequency. [2]
Difference 4:
The peak inverse voltage for the half wave rectifier is equal to the maximum value of the input voltage. For the full wave rectifier, the peak inverse voltage is equal to the double of the maximum value of input voltage [2]

checked

Difference in efficiency
Efficiency of a rectifier circuit is determined as the ratio of DC output power to the AC input power. For a half-wave rectifier, rectifier efficiency is 40.6%. For a full-bridge rectifier, efficiency is 81.12% [3]

2. Explain why ripple voltage appears during half-wave and full-wave rectification. Suggest an effective method to reduce the ripple voltage in a rectifier circuit. [10 Marks]

Ripple is the residual periodic variation in the DC voltage that was rectified from an AC voltage supply. The ripple is due to incomplete suppression of the AC voltage after rectification through the use of voltage smoothing circuits like capacitor smoothing or free-wheeling diodes. [4]

Ripple may be undesirable due to the following issues:
Ripple will cause heating in DC circuits when applied to components with parasitic capacitance.
The presence of ripple can also reduce the resolution of digital circuits, causing logic circuits to give incorrect outputs

An effective method to reduce ripple voltage in a rectifier circuit is to a smoothing capacitor to the circuit.
Based on [5], the peak-to-peak voltage of the ripple voltage is given in the form

$$V_{pp} = \frac{I_{output}}{2*frequency*capacitance}$$

Thus, if we can add a high capacitance capacitor to the circuit, it will be able to smoothen the output voltage waveform and reduce the ripple voltage. However, there are some tradeoffs, such as increase in reactive power than could increase the apparent power consumption of the circuit. We can also employ a low-pass filter by calculating the frequency of the ripple and designing a low pass filter with the ripple voltage frequency as the cut off frequency. [5]

Conclusion and Findings [14 Marks]

(Include your analysis of the behavior of a single phase full-wave rectifier circuit. State the learning outcomes of this experiment.)

In a nutshell, the results obtained from the experiments have given us a better understanding in the workings of a full-wave rectifier and the implementation of the different types of loads and its effect on the result for both the simulation that we did in Simulink/LTspice and the experiment that we did in the lab. We also have to learn how to use multiple physical equipment in the laboratory such as the clamp meter and oscilloscope. The clamp meter is used to measure power, RMS current and voltage while the oscilloscope is used to plot the current and voltage waveform that we require.

Resistive Load:
As we can see from the above graphs from the LTspice simulation and oscilloscope, the waveforms plotted are very similar to each other. The measured value and the theoretical value will be slightly different from each other as the theoretical value does not take into account the resistivity of the wire. We can also see that there will be no phase shift for the input and output voltage (Vs and VL) as this is a resistive load (absence of capacitor and inductor).

checked

We can also observe that the full cycle of the voltage source will be rectified. During the positive half-cycle of Vs, the current will flow through diodes D1 and D4. During the negative half-cycle of Vs, the current will flow through diodes D2 and D3. We will obtain a simple rectifier circuit.

Resistive - Inductive Load:
As we can see from the above graphs from the LTspice simulation and oscilloscope, the waveforms plotted are also very similar to each other. The working principle of this rectifier circuit is also very similar to the circuit in Question 1. The only difference between the two rectifier circuits is the addition of an inductor in the rectifier circuit of Question 2. The inductor will smooth the output voltage as it stores energy (when the diode is forward-biased) and releases energy to the load (when the diode is reversed-biased).

We can also note that the waveform that we have obtained in the oscilloscope has an inductive flyback but the waveform in the simulation does not have it. The reasoning behind this observation is that the inductor is assumed to be ideal in the simulation. When power is removed from the inductor, it will be changed immediately (instantaneous). The VL value is also lower in the hands-on experiment. The voltage drop across the diode will cause the amplitude to be different when compared to the voltage source.

Resistive - Inductive Load with FWD:
As we can see from the above graphs from the LTspice simulation and oscilloscope, the waveforms plotted are also very similar to each other. A FWD (Free Wheeling Diode) has been introduced in this circuit in addition with two 0.15Ω resistor. The FWD will only allow the circuit to conduct when the magnitude of the rectified voltage is smaller than the turn-on voltage of the diode. This will cause the change in the load current to be smaller as the load current will only oscillate at a small amplitude. This will allow the load to operate consistently even at high frequencies as this would prevent large current oscillations from occurring which would protect the load.

When the load voltage is negative, the IFWD will be an upward spike and Id will have a downward spike. The inductor stores and releases energy, allowing the free-wheeling diode to start conducting current in a brief period of time while other diodes will stop conducting, resulting in the production of spikes. Since the sum of Id and IFWD will equate to the load current, IL, ID will become IL, with downward spikes whenever the load voltage is negative (Inductor Charging and Discharging). IFWD will add up to ID, eliminating load current spikes, resulting in a sinusoidal wave.

Resistive Load with Output Capacitor:
As we can see from the above graphs from the LTspice simulation and oscilloscope, the waveforms plotted are also very similar to each other. A capacitor will replace the FWD (Free Wheeling Diode) and the inductor in the circuit.The capacitor will smoothen the output voltage as it discharges when the diode D is in reverse-bias.VD and VL will be rectified waves due to the rectification made by the diodes. The 100μF capacitor will cause the exponential decay of the waveform for VL and VD. We can also conclude that when the load resistance increases, the voltage ripple will decrease and the maximum and minimum voltage increases.

In the general discussion section, we have briefly discussed the difference between a half-wave rectifier and a full-wave rectifier. The reasoning behind the existence of the ripple voltage and the methods to reduce the ripple voltage in the rectifier circuit has also been discussed.

In conclusion, we have learned a lot in this lab experiment such as how different rectifier circuit configurations functions and achieved the objectives of this lab which is to examine the behavior of single phase diode circuits.

checked

References (Minimum 3 References) [6 Marks]

[1] "Full-Wave Rectification and Half-Wave Rectification | Electronics Basics | ROHM," www.rohm.com. https://www.rohm.com/electronics-basics/ac-dc/rectification#:~:text=Full%2Dwave%20rectification%20rectifies%20the

[2] "Difference between Half Wave and Full Wave Rectifier," www.tutorialspoint.com. https://www.tutorialspoint.com/difference-between-half-wave-and-full-wave-rectifier

[3] "Diode As A Rectifier - Half Wave Rectifier & Full Wave Rectifier," BYJUS. https://byjus.com/physics/how-diodes-work-as-a-rectifier/#:~:text=The%20rectifier%20efficiency%20of%20a%20full%2Dwave%20rectifier%20is%2081.2%25. (accessed Mar. 25, 2023).

[4] "Ripple (electrical)," Wikipedia, Jun. 18, 2022. https://en.wikipedia.org/wiki/Ripple_(electrical)#:~:text=Ripple%20(specifically%20ripple%20voltage)%20in

[5] "How do you reduce voltage ripple?," Coil Technology Corporation, Jul. 02, 2020. https://www.powerctc.com/en/node/4569

******** THE END *******

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