ECE3073 – Computer Systems
Lab Exercise No. LAB3A
Monash University Malaysia
Lecturer: A/Prof. N. Ramakrishan
Date: March 18, 2023

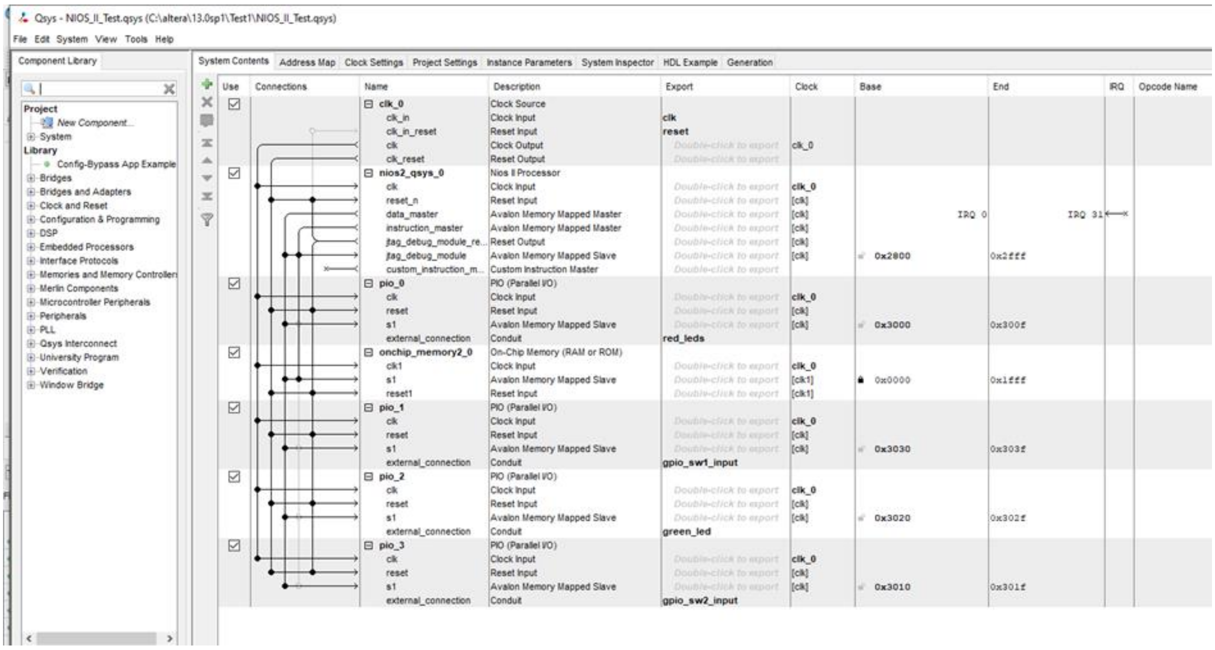
Interfacing multiple GPIO (Input) in Polling Loop – Code in Assembly and C

The aim of the exercise follows your Lab 3 exercise in two sections LAB3A and LAB3B. This is mainly to dilute this week work as for the first time you will be using labsland remote lab. For this week we will connect 2 GPIO pin as input to NIOS processor in a polling loop.

You need to refer to my Lab Demo video and Lab 3 sheets . (Keep them aside)

Step 1: Complete the QYSYS setup to build NIOS computer System

The NIOS Processor system – QYSYS setting should be made as below, note down the base addresses ensure you make the same.



Use	Name	Description	Export	Clock	Base	End	IRQ	Opcode Name
☑	⊟ clk_0	Clock Source						
	clk_in	Clock Input	clk					
	clk_in_reset	Reset Input	reset					
	clk	Clock Output	Double-click to export	clk_0				
	clk_reset	Reset Output	Double-click to export					
☑	⊟ nios2_qsys_0	Nios II Processor						
	clk	Clock Input	Double-click to export	clk_0				
	reset_n	Reset Input	Double-click to export	[clk]				
	data_master	Avalon Memory Mapped Master	Double-click to export	[clk]				
	instruction_master	Avalon Memory Mapped Master	Double-click to export	[clk]				
	jtag_debug_module_re...	Reset Output	Double-click to export	[clk]				
	jtag_debug_module	Avalon Memory Mapped Slave	Double-click to export	[clk]	0x2800	0x2fff		
	custom_instruction_m...	Custom Instruction Master	Double-click to export					
☑	⊟ pio_0	PIO (Parallel I/O)						
	clk	Clock Input	Double-click to export	clk_0				
	reset	Reset Input	Double-click to export	[clk]				
	s1	Avalon Memory Mapped Slave	Double-click to export	[clk]	0x3000	0x300f		
	external_connection	Conduit	red_leds					
☑	⊟ onchip_memory2_0	On-Chip Memory (RAM or ROM)						
	clk1	Clock Input	Double-click to export	clk_0				
	s1	Avalon Memory Mapped Slave	Double-click to export	[clk1]	0x0000	0x1fff		
	reset1	Reset Input	Double-click to export	[clk1]				
☑	⊟ pio_1	PIO (Parallel I/O)						
	clk	Clock Input	Double-click to export	clk_0				
	reset	Reset Input	Double-click to export	[clk]				
	s1	Avalon Memory Mapped Slave	Double-click to export	[clk]	0x3030	0x303f		
	external_connection	Conduit	gpio_sw1_input					
☑	⊟ pio_2	PIO (Parallel I/O)						
	clk	Clock Input	Double-click to export	clk_0				
	reset	Reset Input	Double-click to export	[clk]				
	s1	Avalon Memory Mapped Slave	Double-click to export	[clk]	0x3020	0x302f		
	external_connection	Conduit	green_led					
☑	⊟ pio_3	PIO (Parallel I/O)						
	clk	Clock Input	Double-click to export	clk_0				
	reset	Reset Input	Double-click to export	[clk]				
	s1	Avalon Memory Mapped Slave	Double-click to export	[clk]	0x3010	0x301f		
	external_connection	Conduit	gpio_sw2_input					

Following table shows the details

Devices interfaced with NIOS	No of bits	Direction	Size/Base Address
RAM size	NA	NA	8192 bytes
PIO_1 ((8 RED LEDs)	8 bits	Output	Base address 0x3000
PIO_2 (GPIO_SW[1]_Input)	1 bit	Input	Base address 0x3030
PIO_3_(GREEN LED)	1 bit	Output	Base address 0x3020
PIO_4_(GPIO_SW[2]_input)	1 bit	input	Base address 0x3010

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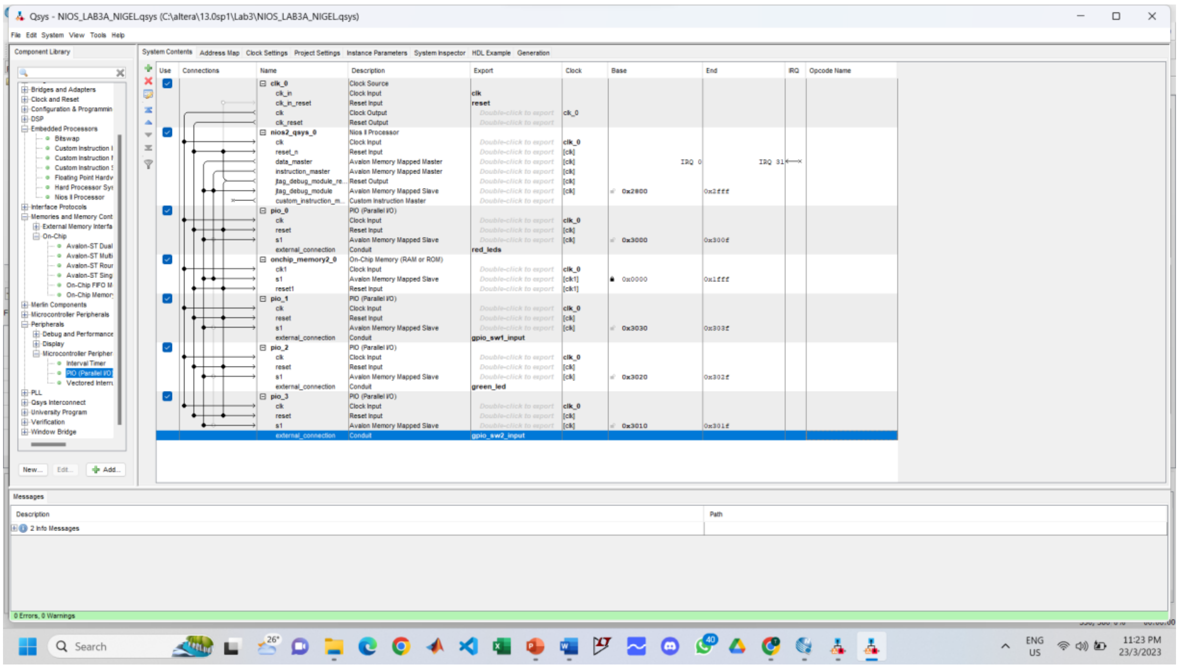
(i) Paste screen shot of your QYSYS below with timestamp from your PC (2 marks)



Qsys - NIOS_LAB3A_NIGEL.qsys (C:\altera\13.0sp1\Lab3\NIOS_LAB3A_NIGEL.qsys)

Use	Connections	Name	Description	Export	Clock	Base	End	IRQ	Opcode Name
☑		⊟ clk_0	Clock Source						
		clk_in	Clock Input	clk					
		clk_in_reset	Reset Input	reset					
		clk	Clock Output	Double-click to export	clk_0				
		clk_reset	Reset Output	Double-click to export					
☑		⊟ nios2_qsys_0	Nios II Processor						
		clk	Clock Input	Double-click to export	clk_0				
		reset_n	Reset Input	Double-click to export	[clk]				
		data_master	Avalon Memory Mapped Master	Double-click to export	[clk]	IRQ 0	IRQ 31		
		instruction_master	Avalon Memory Mapped Master	Double-click to export	[clk]				
		jtag_debug_module_re...	Reset Output	Double-click to export	[clk]				
		jtag_debug_module	Avalon Memory Mapped Slave	Double-click to export	[clk]	0x2800	0x2fff		
		custom_instruction_m...	Custom Instruction Master	Double-click to export					
☑		⊟ pio_0	PIO (Parallel I/O)						
		clk	Clock Input	Double-click to export	clk_0				
		reset	Reset Input	Double-click to export	[clk]				
		s1	Avalon Memory Mapped Slave	Double-click to export	[clk]	0x3000	0x300f		
		external_connection	Conduit	red_leds					
☑		⊟ onchip_memory2_0	On-Chip Memory (RAM or ROM)						
		clk1	Clock Input	Double-click to export	clk_0				
		s1	Avalon Memory Mapped Slave	Double-click to export	[clk1]	0x0000	0x1fff		
		reset1	Reset Input	Double-click to export	[clk1]				
☑		⊟ pio_1	PIO (Parallel I/O)						
		clk	Clock Input	Double-click to export	clk_0				
		reset	Reset Input	Double-click to export	[clk]				
		s1	Avalon Memory Mapped Slave	Double-click to export	[clk]	0x3030	0x303f		
		external_connection	Conduit	gpio_sw1_input					
☑		⊟ pio_2	PIO (Parallel I/O)						
		clk	Clock Input	Double-click to export	clk_0				
		reset	Reset Input	Double-click to export	[clk]				
		s1	Avalon Memory Mapped Slave	Double-click to export	[clk]	0x3020	0x302f		
		external_connection	Conduit	green_led					
☑		⊟ pio_3	PIO (Parallel I/O)						
		clk	Clock Input	Double-click to export	clk_0				
		reset	Reset Input	Double-click to export	[clk]				
		s1	Avalon Memory Mapped Slave	Double-click to export	[clk]	0x3010	0x301f		
		external_connection	Conduit	gpio_sw2_input					

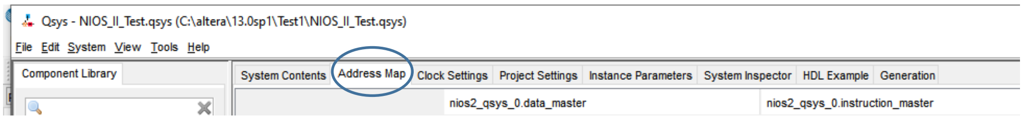
Messages

Description	Path
2 Info Messages	

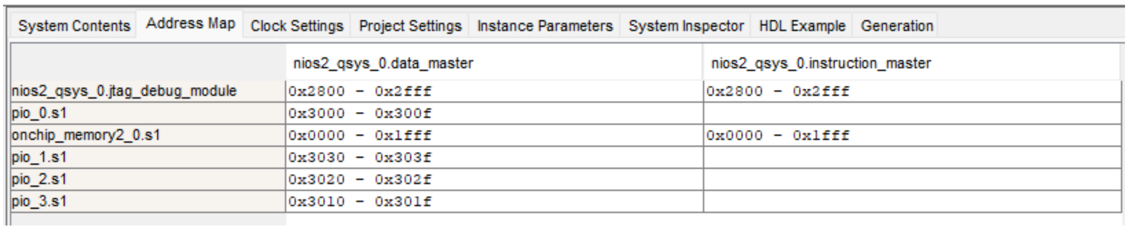
0 Errors, 0 Warnings

11:23 PM
23/3/2023

(ii) Paste the "address map" tab screen shot below such that all the address details of the PIO's are visible. (2 marks)



Qsys - NIOS_II_Test.qsys (C:\altera\13.0sp1\Test1\NIOS_II_Test.qsys)



	nios2_qsys_0.data_master	nios2_qsys_0.instruction_master
nios2_qsys_0.jtag_debug_module	0x2800 – 0x2fff	0x2800 – 0x2fff
pio_0.s1	0x3000 – 0x300f	
onchip_memory2_0.s1	0x0000 – 0x1fff	0x0000 – 0x1fff
pio_1.s1	0x3030 – 0x303f	
pio_2.s1	0x3020 – 0x302f	
pio_3.s1	0x3010 – 0x301f	

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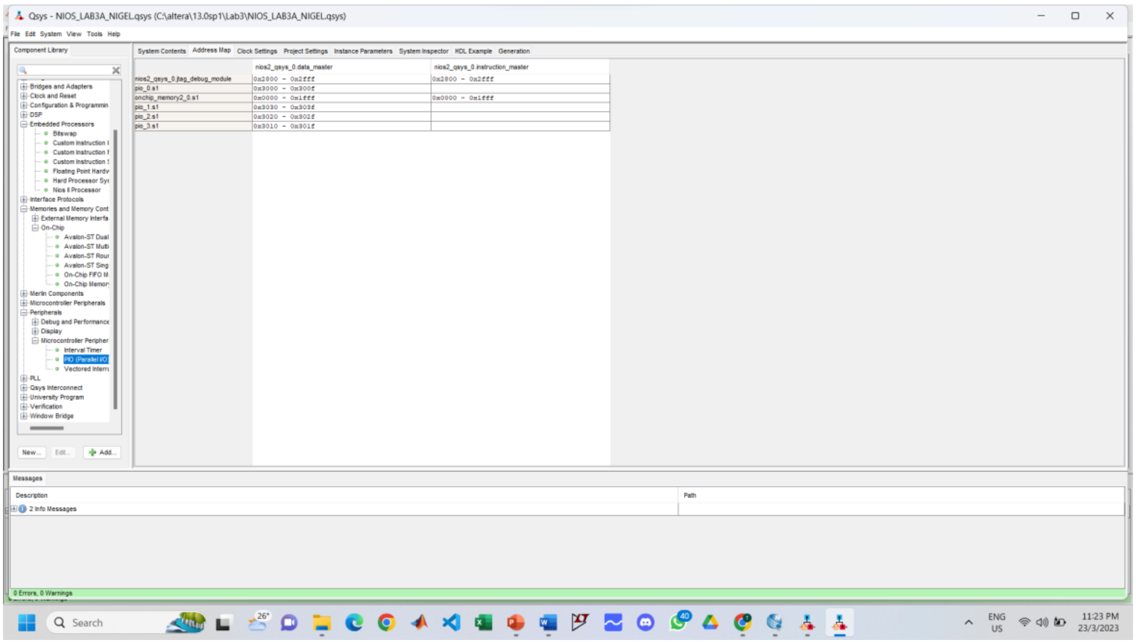

Qsys - NIOS_LAB3A_NIGEL.qsys (C:\altera\13.0sp1\Lab3\NIOS_LAB3A_NIGEL.qsys)

	nios2_qsys_0.data_master	nios2_qsys_0.instruction_master
nios2_qsys_0.jtag_debug_module	0x2800 - 0x2fff	0x2800 - 0x2fff
pio_0.s1	0x3000 - 0x300f	
onchip_memory2_0.s1	0x0000 - 0x1fff	0x0000 - 0x1fff
pio_1.s1	0x3030 - 0x303f	
pio_2.s1	0x3020 - 0x302f	
pio_3.s1	0x3010 - 0x301f	

2 Info Messages

0 Errors, 0 Warnings

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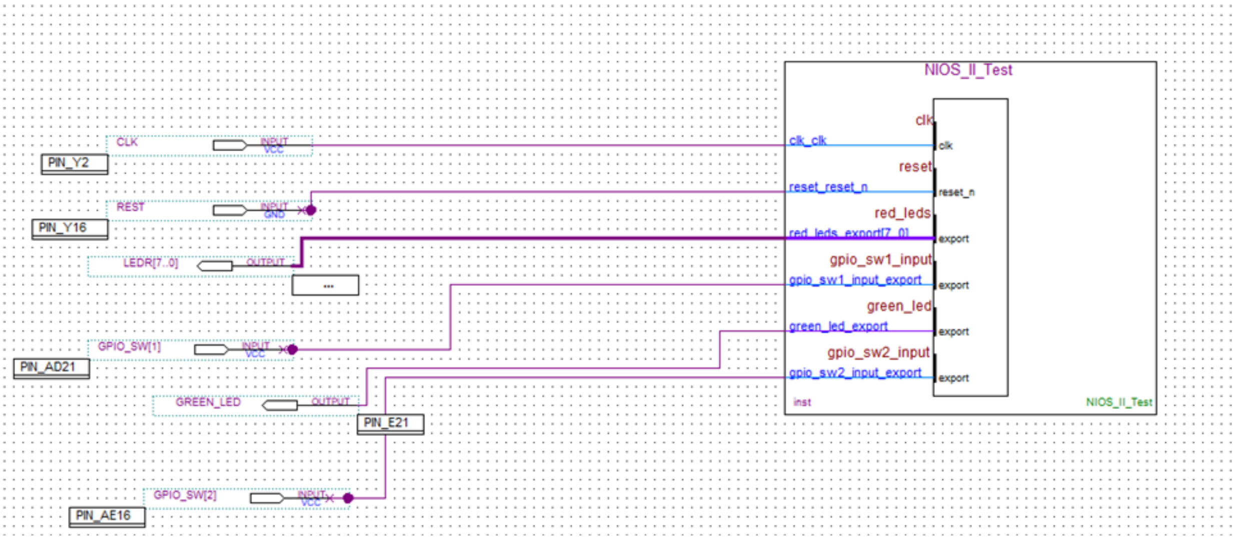
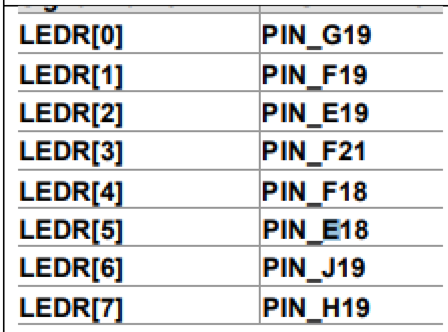
Step 2: Building the schematics of the NIOS system using quartus

(iii) Now complete the quartus schematic or Verilog code to build the computer system to interface the devices like as shown below



Please note the following pin plan

PIN Number (Label) of DE2-115	Assignment
PIN_Y2	Clock 50 MHz
PIN_Y16	GPIO [5] – Ensure this is HIGH always- you will notice the switch in LabsLand portal is made ON- so no worries
 LEDR[0] PIN_G19 LEDR[1] PIN_F19 LEDR[2] PIN_E19 LEDR[3] PIN_F21 LEDR[4] PIN_F18 LEDR[5] PIN_E18 LEDR[6] PIN_J19 LEDR[7] PIN_H19	LED 7 to LED 0 (8 RED LEDS of DE2-115)
PIN_AD21	GPIO[6] which is SW[1] of LabsLand
PIN_E21	Green LED LEDG[0]
PIN_AE16	GPIO [7] which is SW[2] of LabsLand

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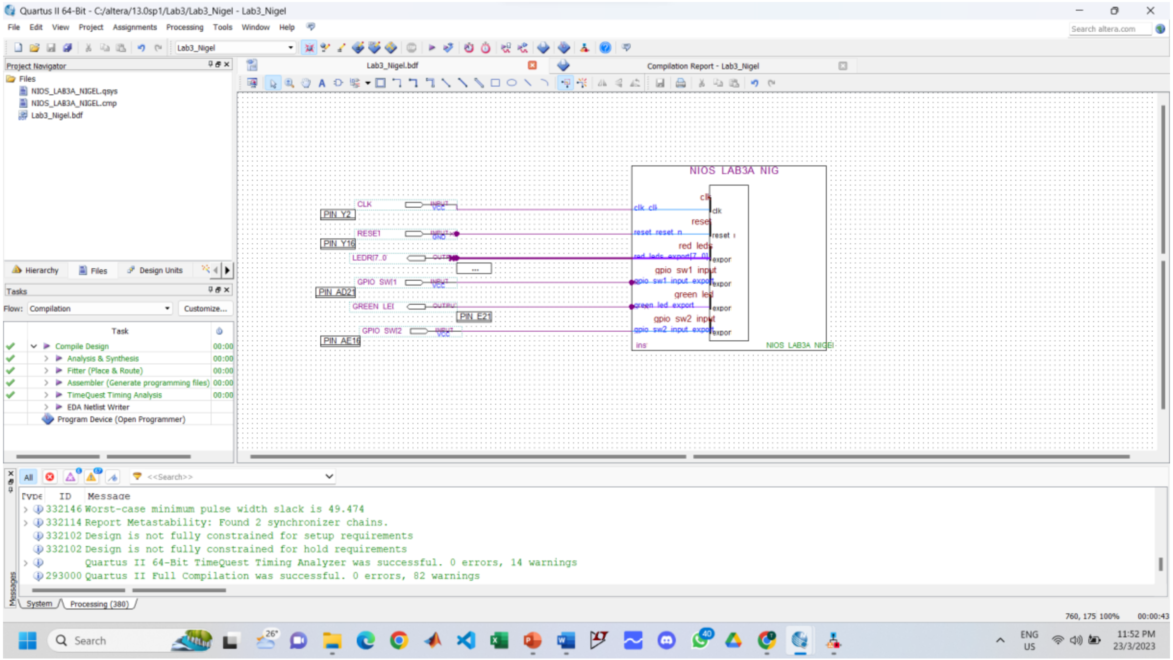
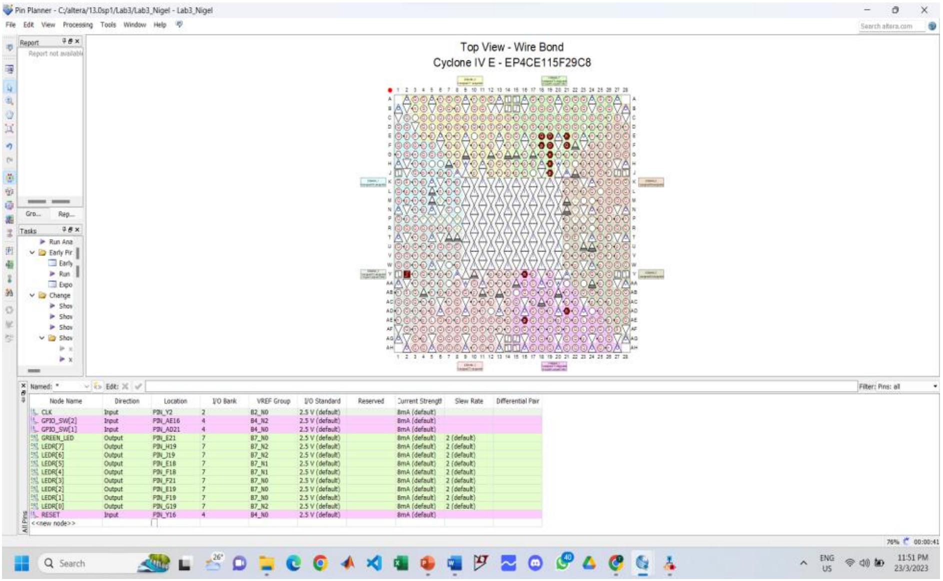
(i) Paste screen shot of your schematics showing error free compilation (3 marks)



```
Type  ID     Message
  332146 Worst-case minimum pulse width slack is 49.474
  332114 Report Metastability: Found 2 synchronizer chains.
  332102 Design is not fully constrained for setup requirements
  332102 Design is not fully constrained for hold requirements
         Quartus II 64-Bit TimeQuest Timing Analyzer was successful. 0 errors, 14 warnings
  293000 Quartus II Full Compilation was successful. 0 errors, 82 warnings
```

(ii) Paste the pinplanner screen shot indicating you made right pin connections exactly to the same PIN Labels as per table/schematics above (2 marks)


Pin Planner - C:/altera/13.0sp1/Lab3/Lab3_Nigel - Lab3_Nigel
File Edit View Processing Tools Window Help
Top View - Wire Bond
Cyclone IV E - EP4CE115F29C8
Report
Report not available
Tasks
Named: *
Edit:
Filter: Pins: all
All Pins
Search
ENG US
11:51 PM 23/3/2023

Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair
CLK	Input	PIN_Y2	2	B2_N0	2.5 V (default)		8mA (default)		
GPIO_SW[2]	Input	PIN_AE16	4	B4_N2	2.5 V (default)		8mA (default)		
GPIO_SW[1]	Input	PIN_AD21	4	B4_N0	2.5 V (default)		8mA (default)		
GREEN_LED	Output	PIN_E21	7	B7_N0	2.5 V (default)		8mA (default)	2 (default)	
LEDR[7]	Output	PIN_H19	7	B7_N2	2.5 V (default)		8mA (default)	2 (default)	
LEDR[6]	Output	PIN_J19	7	B7_N2	2.5 V (default)		8mA (default)	2 (default)	
LEDR[5]	Output	PIN_E18	7	B7_N1	2.5 V (default)		8mA (default)	2 (default)	
LEDR[4]	Output	PIN_F18	7	B7_N1	2.5 V (default)		8mA (default)	2 (default)	
LEDR[3]	Output	PIN_F21	7	B7_N0	2.5 V (default)		8mA (default)	2 (default)	
LEDR[2]	Output	PIN_E19	7	B7_N0	2.5 V (default)		8mA (default)	2 (default)	
LEDR[1]	Output	PIN_F19	7	B7_N0	2.5 V (default)		8mA (default)	2 (default)	
LEDR[0]	Output	PIN_G19	7	B7_N2	2.5 V (default)		8mA (default)	2 (default)	
RESET	Input	PIN_Y16	4	B4_N0	2.5 V (default)		8mA (default)		
<<new node>>									

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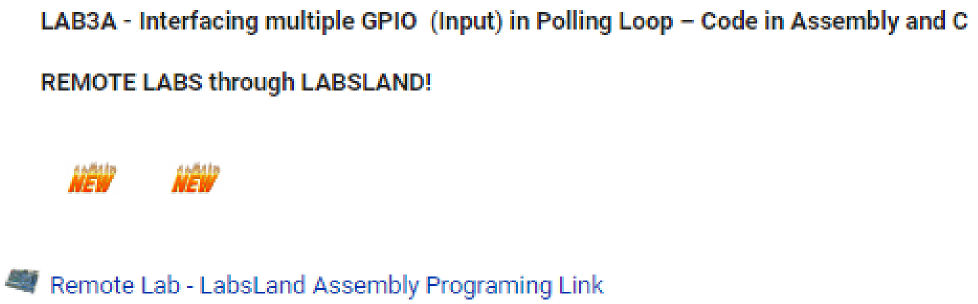
Step 3: NIOS assembly code and testing the result in LabsLand portal

Write suitable NIOS assembly code to demonstrate when GPIO_SW[1]_Input is HIGH the 8 RED LEDs goes HIGH (turn ON) , if GPIO_SW[2]_input goes HIGH , GREEN LED goes HIGH (turn ON), and vice versa. Basically SW[1] and SW[2] will be switch to control RED and Green LEDs. To summarize program the condition is explained in table below in assembly.

GPIO_SW[1]	RED LEDs (8 of them)
When GPIO_SW[1] = 0x01	0xFF (all red led lights up)
When GPIO_SW[1] = 0x00	0x00 (all red led lights OFF)

GPIO_SW[2]	GREEN LED
When GPIO_SW[2] = 0x01	0x01 (Green led lights up)
When GPIO_SW[2] = 0x00	0x00 (Green led lights OFF)

To access LabsLand Remote Lab



LAB3A - Interfacing multiple GPIO (Input) in Polling Loop – Code in Assembly and C

REMOTE LABS through LABSLAND!

Remote Lab - LabsLand Assembly Programing Link

Click above link one for Assembly another for C (choose assembly for this step)

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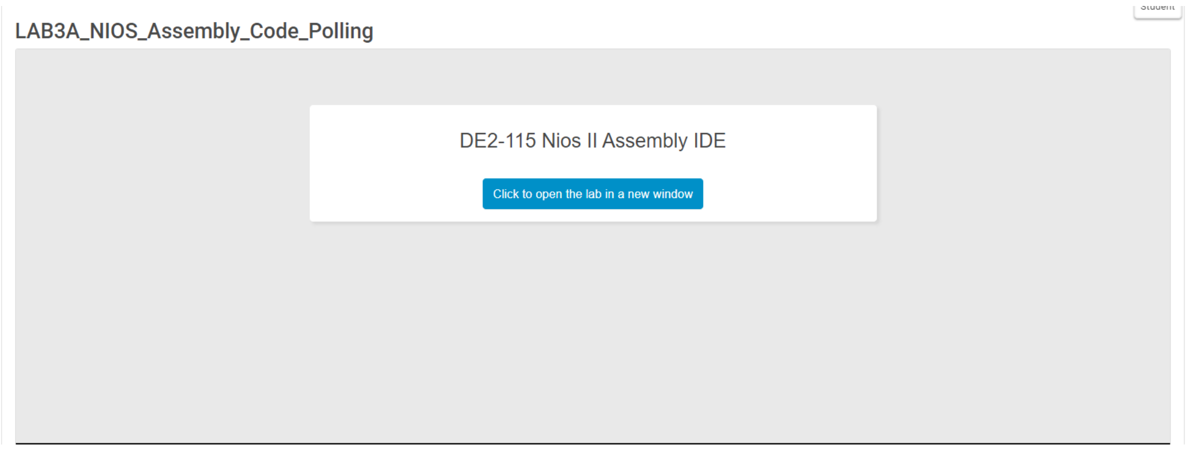
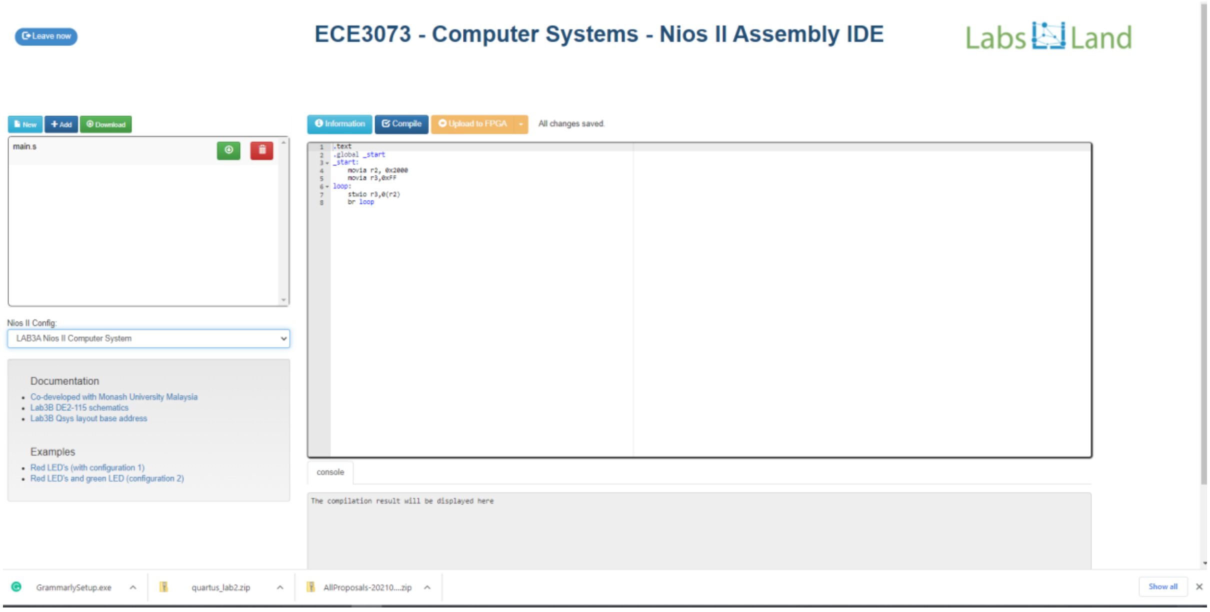


LAB3A_NIOS_Assembly_Code_Polling

DE2-115 Nios II Assembly IDE

Then you will see this



ECE3073 - Computer Systems - Nios II Assembly IDE

```
.text
.global _start
_start:
    movia r2, 0x2000
    movia r3,0xFF
loop:
    stwio r3,0(r2)
    br loop
```

Nios II Config: LAB3A Nios II Computer System

Documentation

- Co-developed with Monash University Malaysia
- Lab3B DE2-115 schematics
- Lab3B Qsys layout base address

Examples

- Red LED's (with configuration 1)
- Red LED's and green LED (configuration 2)

```
The compilation result will be displayed here
```

Edit your suitable code , ensure the first 3 lines .text to _start is untouched.

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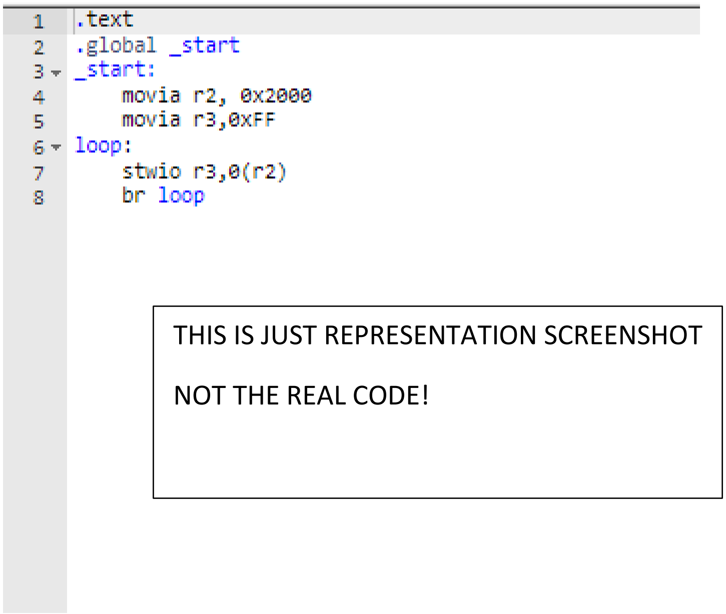


```
.text
.global _start
_start:
    movia r2, 0x2000
    movia r3,0xFF
loop:
    stwio r3,0(r2)
    br loop
```

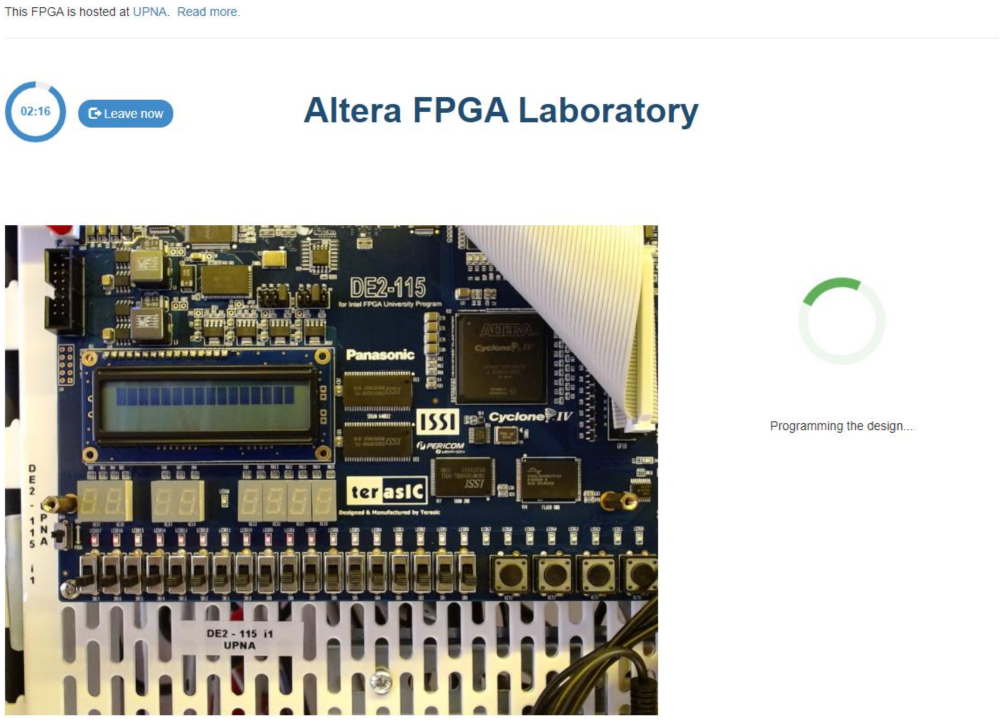
THIS IS JUST REPRESENTATION SCREENSHOT

NOT THE REAL CODE!

Click “compile” when done

Then upload to FPGA board

You will then see



This FPGA is hosted at UPNA. Read more.

Altera FPGA Laboratory

Programming the design...

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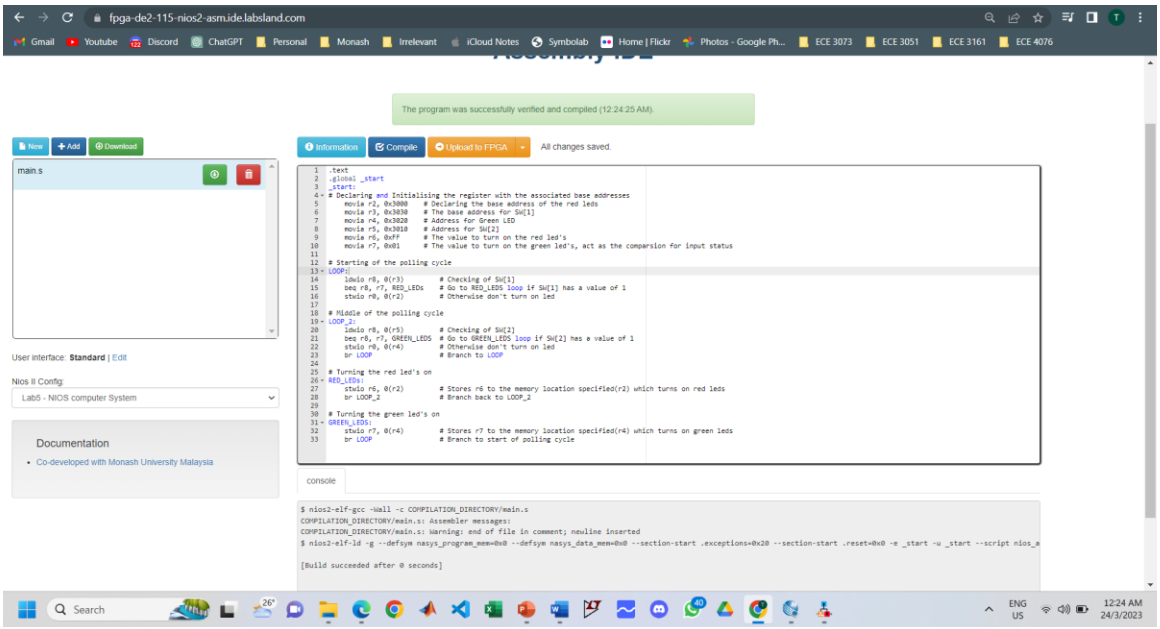
Now complete the following:

(i) Paste your labsland page with your assembly code screen below (2 marks)

Compiled NIOS II Assembly Code Screenshot in Labsland



The program was successfully verified and compiled (12:24:25 AM).

All changes saved.

User interface: **Standard** | Edit

Nios II Config:
Lab5 - NIOS computer System

Documentation

- Co-developed with Monash University Malaysia

```
.text
.global _start
_start:
# Declaring and Initialising the register with the associated base addresses
    movia r2, 0x3000    # Declaring the base address of the red leds
    movia r3, 0x3030    # The base address for SW[1]
    movia r4, 0x3020    # Address for Green LED
    movia r5, 0x3010    # Address for SW[2]
    movia r6, 0xFF      # The value to turn on the red led's
    movia r7, 0x01      # The value to turn on the green led's, act as the comparsion for input status

# Starting of the polling cycle
LOOP:
    ldwio r8, 0(r3)         # Checking of SW[1]
    beq r8, r7, RED_LEDs    # Go to RED_LEDS loop if SW[1] has a value of 1
    stwio r0, 0(r2)         # Otherwise don't turn on led

# Middle of the polling cycle
LOOP_2:
    ldwio r8, 0(r5)         # Checking of SW[2]
    beq r8, r7, GREEN_LEDS  # Go to GREEN_LEDS loop if SW[2] has a value of 1
    stwio r0, 0(r4)         # Otherwise don't turn on led
    br LOOP                 # Branch to LOOP

# Turning the red led's on
RED_LEDs:
    stwio r6, 0(r2)         # Stores r6 to the memory location specified(r2) which turns on red leds
    br LOOP_2               # Branch back to LOOP_2

# Turning the green led's on
GREEN_LEDS:
    stwio r7, 0(r4)         # Stores r7 to the memory location specified(r4) which turns on green leds
    br LOOP                 # Branch to start of polling cycle
```

```
$ nios2-elf-gcc -Wall -c COMPILATION_DIRECTORY/main.s
COMPILATION_DIRECTORY/main.s: Assembler messages:
COMPILATION_DIRECTORY/main.s: Warning: end of file in comment; newline inserted
$ nios2-elf-ld -g --defsym nasys_program_mem=0x0 --defsym nasys_data_mem=0x0 --section-start .exceptions=0x20 --section-start .reset=0x0 -e _start -u _start --script nios_a

[Build succeeded after 0 seconds]
```

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Assembly Code

```
.text
.global _start
_start:
# Declaring and Initialising the register with the associated base addresses
   movia r2, 0x3000    # Declaring the base address of the red leds
   movia r3, 0x3030    # The base address for SW[1]
   movia r4, 0x3020    # Address for Green LED
   movia r5, 0x3010    # Address for SW[2]
   movia r6, 0xFF      # The value to turn on the red led's
   movia r7, 0x01      # The value to turn on the green led's, act as the comparsion for input status

# Starting of the polling cycle
LOOP:
   ldwio r8, 0(r3)        # Checking of SW[1]
   beq r8, r7, RED_LEDs    # Go to RED_LEDS loop if SW[1] has a value of 1
   stwio r0, 0(r2)        # Otherwise don't turn on led

# Middle of the polling cycle
LOOP_2:
   ldwio r8, 0(r5)        # Checking of SW[2]
   beq r8, r7, GREEN_LEDS  # Go to GREEN_LEDS loop if SW[2] has a value of 1
   stwio r0, 0(r4)        # Otherwise don't turn on led
   br LOOP               # Branch to LOOP

# Turning the red led's on
RED_LEDs:
   stwio r6, 0(r2)        # Stores r6 to the memory location specified(r2) which turns on red leds
   br LOOP_2              # Branch back to LOOP_2

# Turning the green led's on
GREEN_LEDS:
   stwio r7, 0(r4)        # Stores r7 to the memory location specified(r4) which turns on green leds
   br LOOP               # Branch to start of polling cycle
```

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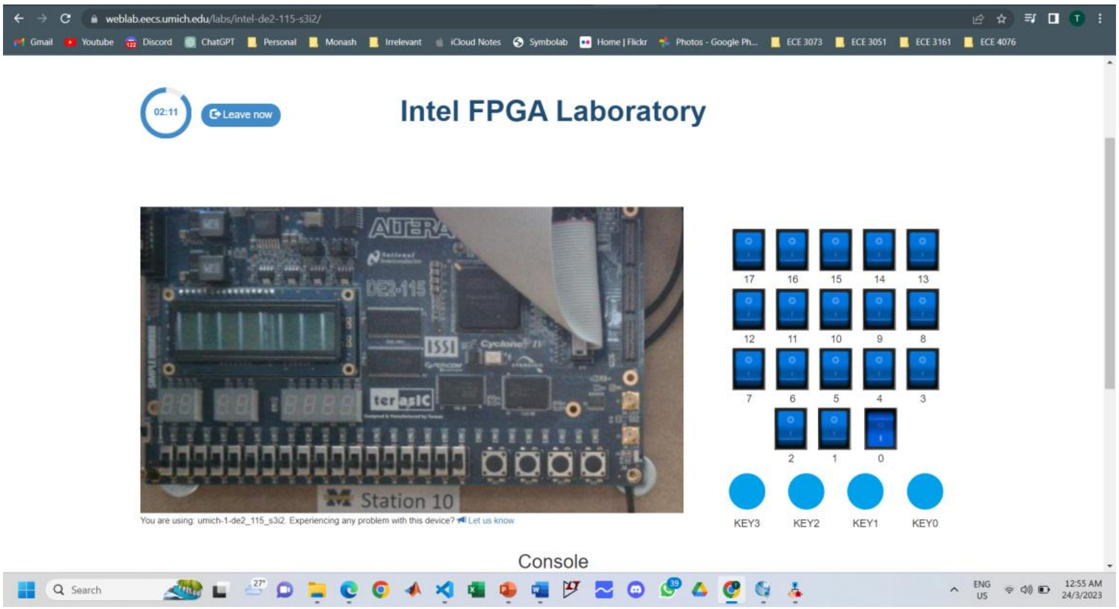
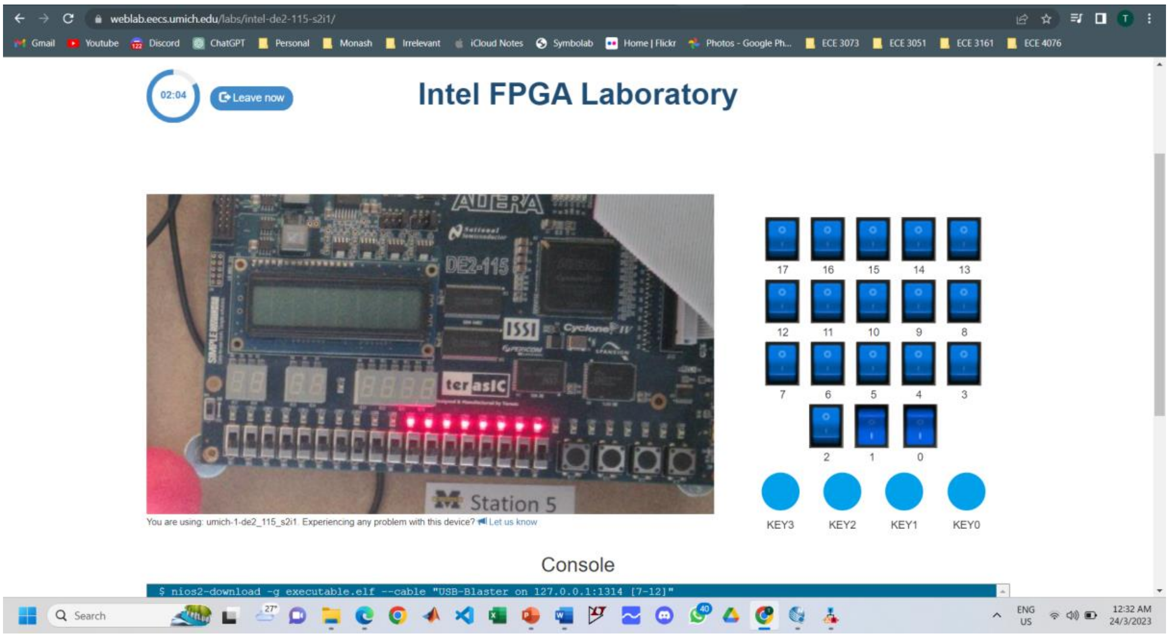
(ii) Screen shot showing the RED and Green LED ON with relevant switches in ON position (3 Marks)

When SW [1] = 0 and SW [2] = 0



You are using: umich-1-de2_115_s3i2. Experiencing any problem with this device? Let us know

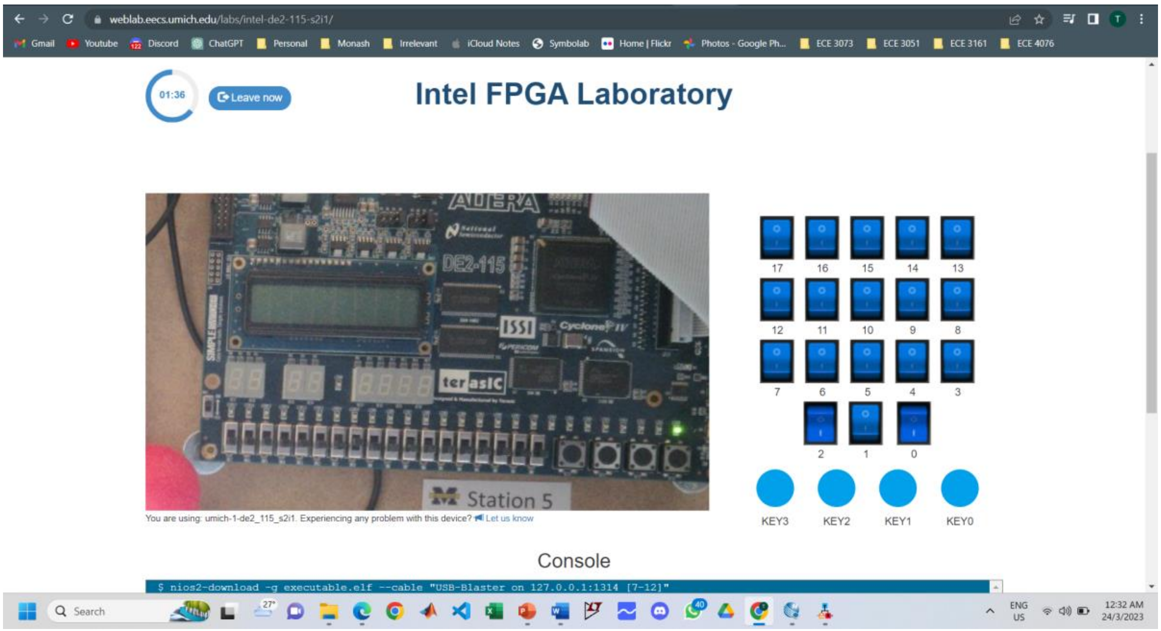
When SW [1] = 1 and SW [2] = 0 (RED LED ON ONLY)



You are using: umich-1-de2_115_s2i1. Experiencing any problem with this device? Let us know

```
$ nios2-download -g executable.elf --cable "USB-Blaster on 127.0.0.1:1314 [7-12]"
```

When SW [1] = 0 and SW [2] = 1 (GREEN LED ON ONLY)



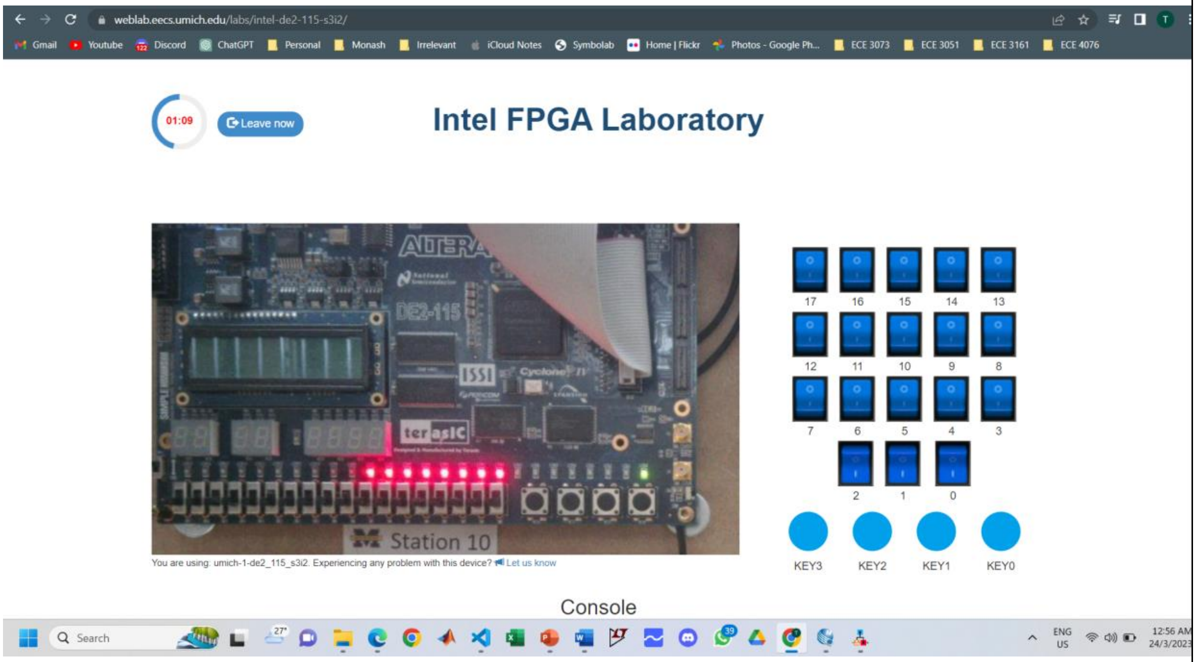
Intel FPGA Laboratory

You are using: umich-1-de2_115_s2i1. Experiencing any problem with this device? Let us know

Console

```
$ nios2-download -g executable.elf --cable "USB-Blaster on 127.0.0.1:1314 [7-12]"
```

When SW [1] = 1 and SW [2] = 1 (BOTH RED LED AND GREEN LED ON)



Intel FPGA Laboratory

You are using: umich-1-de2_115_s3i2. Experiencing any problem with this device? Let us know

Console

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Monash University Malaysia
Lecturer: A/Prof. N. Ramakrishan
Date: March 18, 2023

Step 4: NIOS - C code and testing the result in LabsLand portal

Write suitable C code (refer Lab 3 sheet and Lab 3 demo video) to demonstrate when GPIO_SW[1]_Input is HIGH the 8 RED LEDs goes HIGH (turn ON) , if GPIO_SW[2]_input goes HIGH , GREEN LED goes HIGH (turn ON), and vice versa. Basically SW[1] and SW[2] will be switch to control RED and Green LEDs. To summarize program the condition is explained in table below in assembly.

GPIO_SW[1]	RED LEDs (8 of them)
When GPIO_SW[1] = 0x01	0xFF (all red led lights up)
When GPIO_SW[1] = 0x00	0x00 (all red led lights OFF)

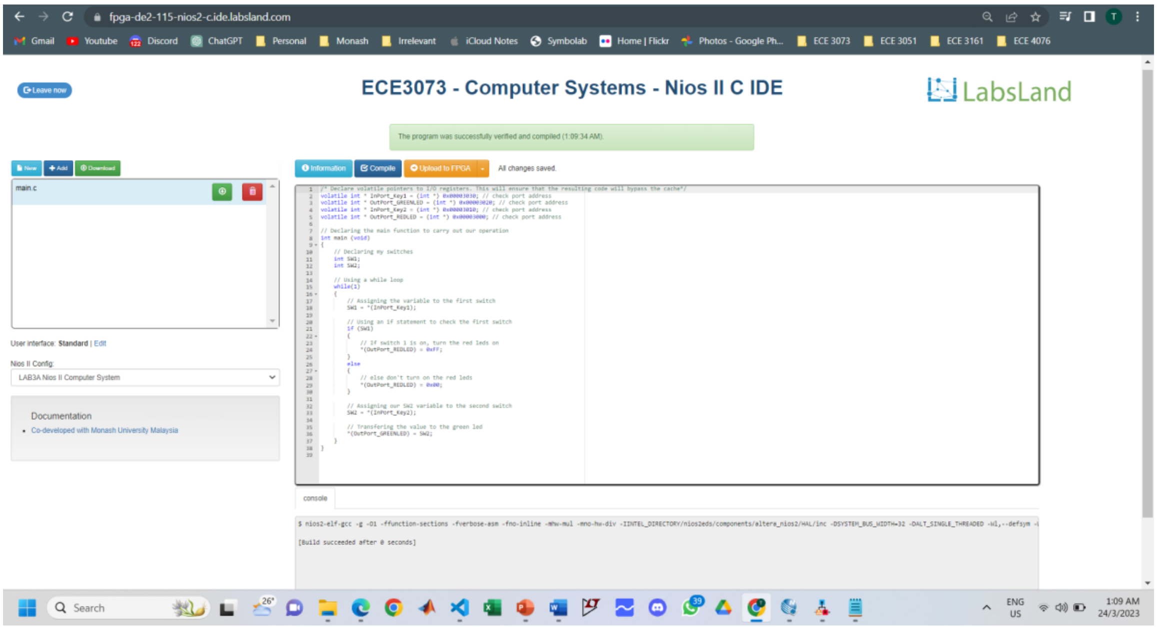
GPIO_SW[2]	GREEN LED
When GPIO_SW[2] = 0x01	0x01 (Green led lights up)
When GPIO_SW[2] = 0x00	0x00 (Green led lights OFF)

For this step same – but choose

Remote Lab - LabsLand C Programming Link

(i) Paste your labsland page with your C code screen below (5 marks)

Compiled C Code Screenshot in Labsland



The program was successfully verified and compiled (1:09:34 AM).

```c
/* Declare volatile pointers to I/O registers. This will ensure that the resulting code will bypass the cache*/
volatile int * InPort_Key1 = (int *) 0x00003030; // check port address
volatile int * OutPort_GREENLED = (int *) 0x00003020; // check port address
volatile int * InPort_Key2 = (int *) 0x00003010; // check port address
volatile int * OutPort_REDLED = (int *) 0x00003000; // check port address

// Declaring the main function to carry out our operation
int main (void)
{
    // Declaring my switches
    int SW1;
    int SW2;

    // Using a while loop
    while(1)
    {
        // Assigning the variable to the first switch
        SW1 = *(InPort_Key1);

        // Using an if statement to check the first switch
        if (SW1)
        {
            // If switch 1 is on, turn the red leds on
            *(OutPort_REDLED) = 0xFF;
        }
        else
        {
            // else don't turn on the red leds
            *(OutPort_REDLED) = 0x00;
        }

        // Assigning our SW2 variable to the second switch
        SW2 = *(InPort_Key2);

        // Transfering the value to the green led
        *(OutPort_GREENLED) = SW2;
    }
}

```

```
$ nios2-elf-gcc -g -O1 -ffunction-sections -fverbose-asm -fno-inline -mhw-mul -mno-hw-div -IINTEL_DIRECTORY/nios2eds/components/altera_nios2/HAL/inc -DSYSTEM_BUS_WIDTH=32 -DALT_SINGLE_THREADED -Wl,--defsym -

[Build succeeded after 0 seconds]
```

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C Code

```
/* Declare volatile pointers to I/O registers. This will ensure that the
resulting code will bypass the cache*/
volatile int * InPort_Key1 = (int *) 0x00003030; // check port address
volatile int * OutPort_GREENLED = (int *) 0x00003020; // check port address
volatile int * InPort_Key2 = (int *) 0x00003010; // check port address
volatile int * OutPort_REDLED = (int *) 0x00003000; // check port address

// Declaring the main function to carry out our operation
int main (void)
{
    // Declaring my switches
    int SW1;
    int SW2;

    // Using a while loop
    while(1)
    {
        // Assigning the variable to the first switch
        SW1 = *(InPort_Key1);

        // Using an if statement to check the first switch
        if (SW1)
        {
            // If switch 1 is on, turn the red leds on
            *(OutPort_REDLED) = 0xFF;
        }
        else
        {
            // else don't turn on the red leds
            *(OutPort_REDLED) = 0x00;
        }

        // Assigning our SW2 variable to the second switch
        SW2 = *(InPort_Key2);

        // Transfering the value to the green led
        *(OutPort_GREENLED) = SW2;
    }
}
```

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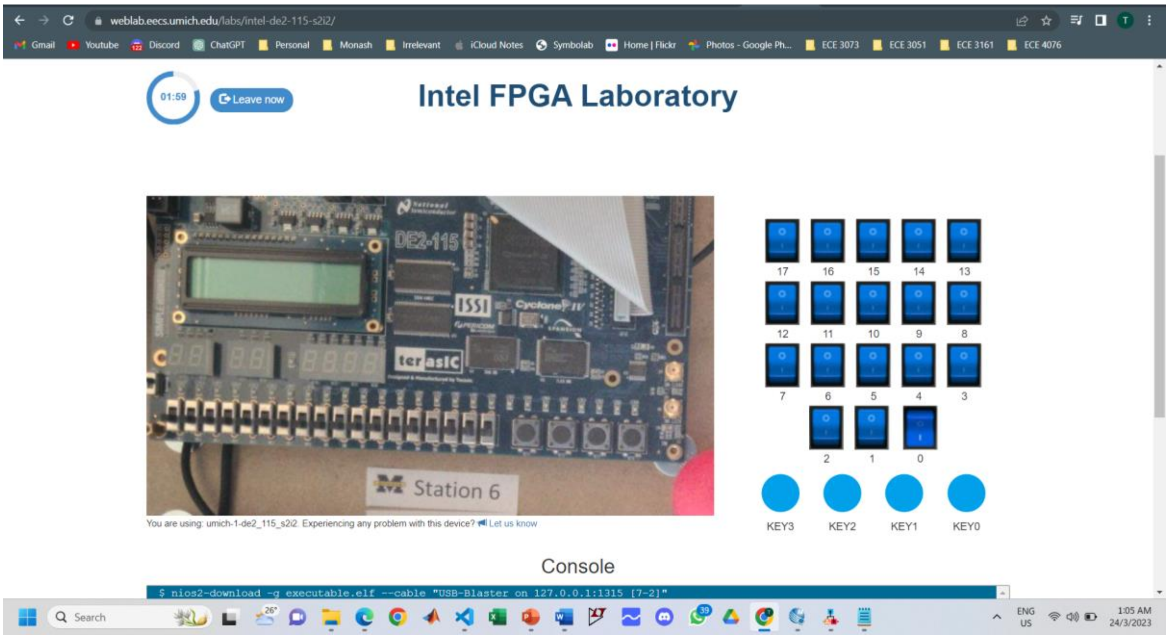
(ii) Screen shot showing the RED and Green LED ON with relevant switches in ON position (5 Marks)

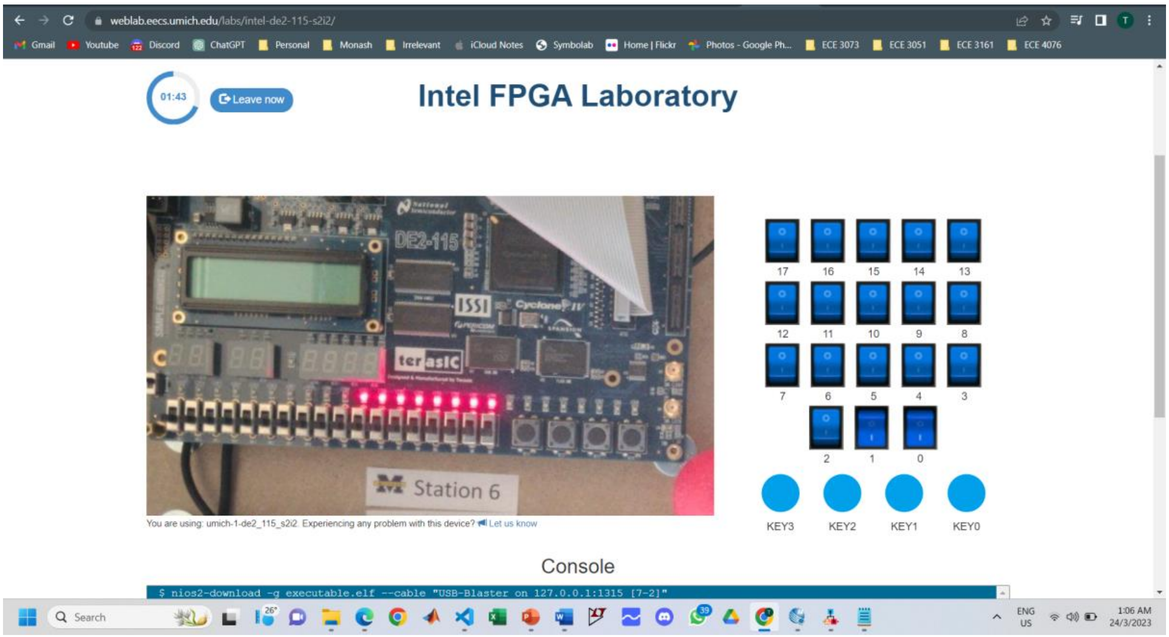
When SW [1] = 0 and SW [2] = 0



You are using: umich-1-de2_115_s2i2. Experiencing any problem with this device? Let us know

```
$ nios2-download -g executable.elf --cable "USB-Blaster on 127.0.0.1:1315 [7-2]"
```

When SW [1] = 1 and SW [2] = 0 (RED LEDs ON ONLY)



You are using: umich-1-de2_115_s2i2. Experiencing any problem with this device? Let us know

```
$ nios2-download -g executable.elf --cable "USB-Blaster on 127.0.0.1:1315 [7-2]"
```

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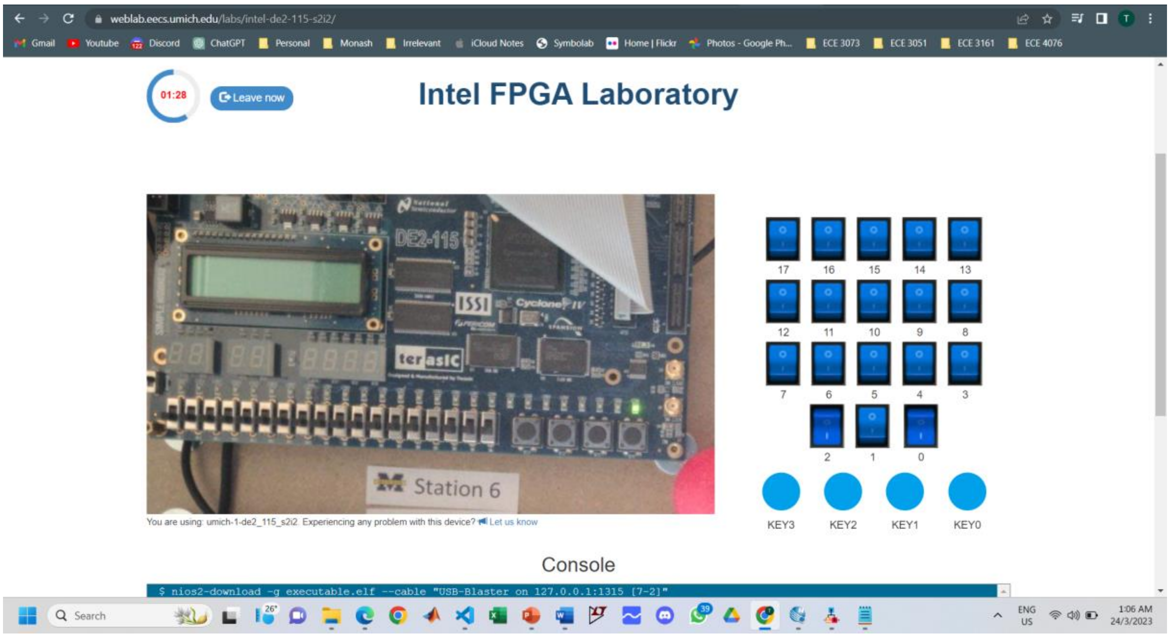
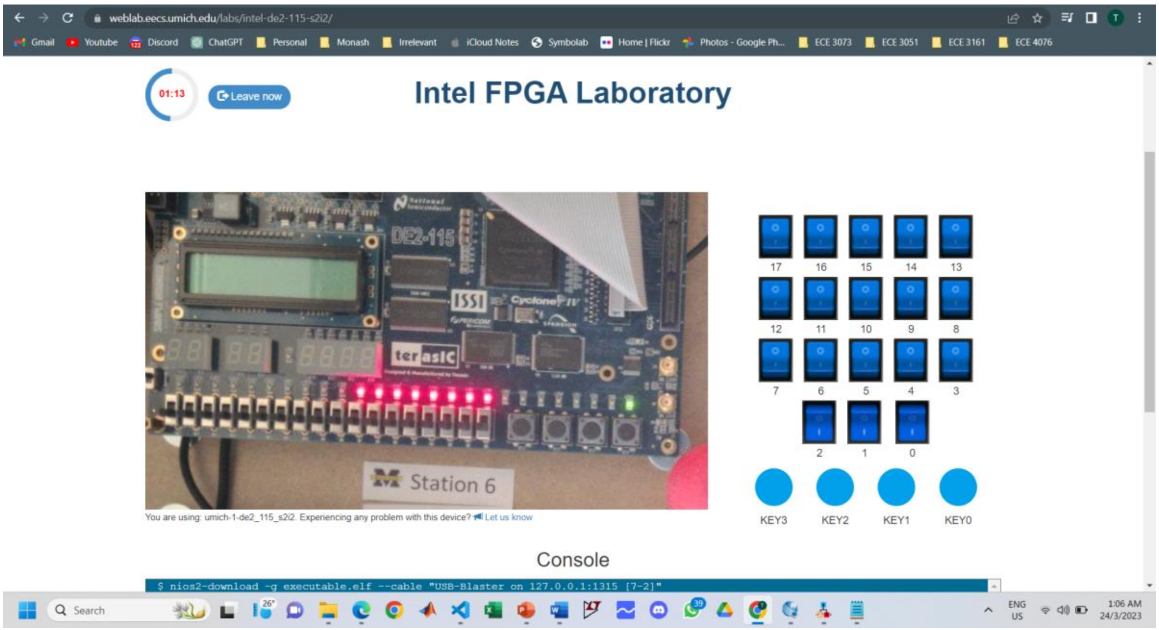
When SW [1] = 0 and SW [2] = 1 (GREEN LED ON ONLY)


weblab.eecs.umich.edu/labs/intel-de2-115-s2i2/
Gmail Youtube Discord ChatGPT Personal Monash Irrelevant iCloud Notes Symbolab Home | Flickr Photos - Google Ph... ECE 3073 ECE 3051 ECE 3161 ECE 4076
01:28
Leave now
Intel FPGA Laboratory
Station 6
17 16 15 14 13
12 11 10 9 8
7 6 5 4 3
2 1 0
KEY3 KEY2 KEY1 KEY0
Console
Search
ENG US
1:06 AM
24/3/2023

You are using: umich-1-de2_115_s2i2. Experiencing any problem with this device? Let us know

```
$ nios2-download -g executable.elf --cable "USB-Blaster on 127.0.0.1:1315 [7-2]"
```

When SW [1] = 1 and SW [2] = 1 (BOTH RED LED AND GREEN LED ON)


weblab.eecs.umich.edu/labs/intel-de2-115-s2i2/
Gmail Youtube Discord ChatGPT Personal Monash Irrelevant iCloud Notes Symbolab Home | Flickr Photos - Google Ph... ECE 3073 ECE 3051 ECE 3161 ECE 4076
01:13
Leave now
Intel FPGA Laboratory
Station 6
17 16 15 14 13
12 11 10 9 8
7 6 5 4 3
2 1 0
KEY3 KEY2 KEY1 KEY0
Console
Search
ENG US
1:06 AM
24/3/2023

You are using: umich-1-de2_115_s2i2. Experiencing any problem with this device? Let us know

```
$ nios2-download -g executable.elf --cable "USB-Blaster on 127.0.0.1:1315 [7-2]"
```