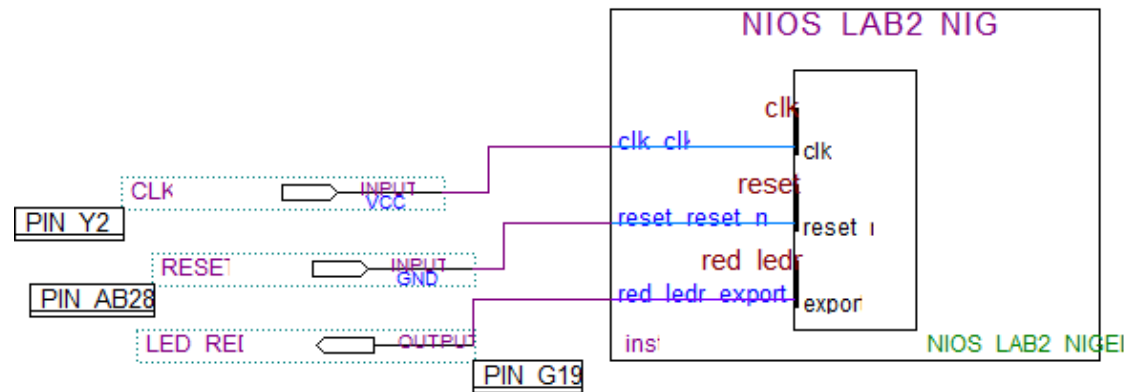


Student ID: 32194471  
Name: Nigel Tan Jin Chun  
Date: 14/3/2023  
Lab 2, ECE3073

**Lab 2 – Monash University Malaysia, Sem 1 2021 – Sheet**

1. Screen shot of the NIOS – II microcomputer system with one LED interface, with no errors and labels of pin numbers are visible and paste the assembly code to light the LED ON. (4 marks)



Student ID: 32194471  
Name: Nigel Tan Jin Chun  
Date: 14/3/2023  
Lab 2, ECE3073

Quartus II 64-Bit - C:/altera/13.0sp1/Lab2/Lab2\_Part1\_Nigel - Lab2\_Part1\_Nigel

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator

Files

- NIOS\_LAB2\_NIGEL.qsys
- NIOS\_LAB2\_NIGEL.cmp
- Lab2\_Part1\_Nigel.bdf

Hierarchy Files Design Units

Tasks

Flow: Compilation Customize...

Task	Time
Compile Design	00:00
Analysis & Synthesis	00:00
Fitter (Place & Route)	00:00
Assembler (Generate programming files)	00:00
TimeQuest Timing Analysis	00:00
EDA Netlist Writer	00:00
Program Device (Open Programmer)	

Messages

Type ID Message

- 332146 Worst-case minimum pulse width slack is 49.472
- 332114 Report Metastability: Found 2 synchronizer chains.
- 332102 Design is not fully constrained for setup requirements
- 332102 Design is not fully constrained for hold requirements
- Quartus II 64-Bit TimeQuest Timing Analyzer was successful. 0 errors, 14 warnings
- 293000 Quartus II Full Compilation was successful. 0 errors, 43 warnings

System (2) / Processing (323)

256, 383, 100% 00:00:45

ENG US 11:26 AM 14/3/2023

Student ID: 32194471

Name: Nigel Tan Jin Chun

Date: 14/3/2023

Lab 2, ECE3073

# **CODE**

```
.global _start
```

```
_start:
```

```
movia r3, 0x2000
```

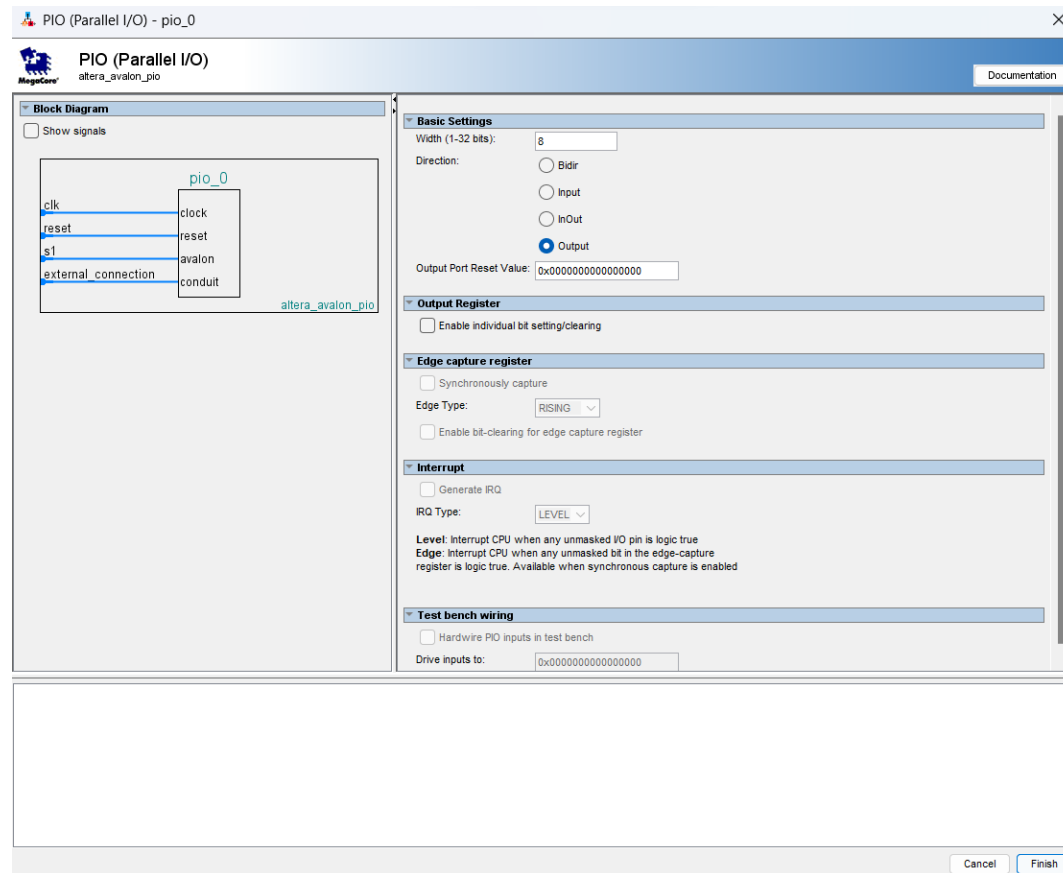
```
loop:  movia r4, 0x01
```

```
        stwio r4, 0(r3)
```

```
        br loop
```

Student ID: 32194471  
Name: Nigel Tan Jin Chun  
Date: 14/3/2023  
Lab 2, ECE3073

2. Qsys screen shot showing PIO for 8- LEDs, and screen shot of the schematics, type the code for lighting up 8 red LEDs. ( 3 marks)



Student ID: 32194471  
Name: Nigel Tan Jin Chun  
Date: 14/3/2023  
Lab 2, ECE3073

Qsys - NIOS\_LAB2\_NIGEL.qsys\* (C:\altera\13.0sp1\Lab2\NIOS\_LAB2\_NIGEL.qsys)

File Edit System View Tools Help

Component Library

Project

- New Component...
- System
- Library
  - Config-Bypass App Exe
  - Bridges
  - Bridges and Adapters
  - Clock and Reset
  - Configuration & Programmin
  - DSP
  - Embedded Processors
  - Interface Protocols
  - Memories and Memory Cont
  - Merlin Components
  - Microcontroller Peripherals
  - Peripherals
    - Debug and Performance
    - Display
    - Microcontroller Peripher
      - Interval Timer
      - PIO (Parallel I/O)
      - Vectored Interr
  - PLL
  - Qsys Interconnect
  - University Program
  - Verification

New... Edit... Add...

System Contents Address Map Clock Settings Project Settings Instance Parameters System Inspector HDL Example Generation

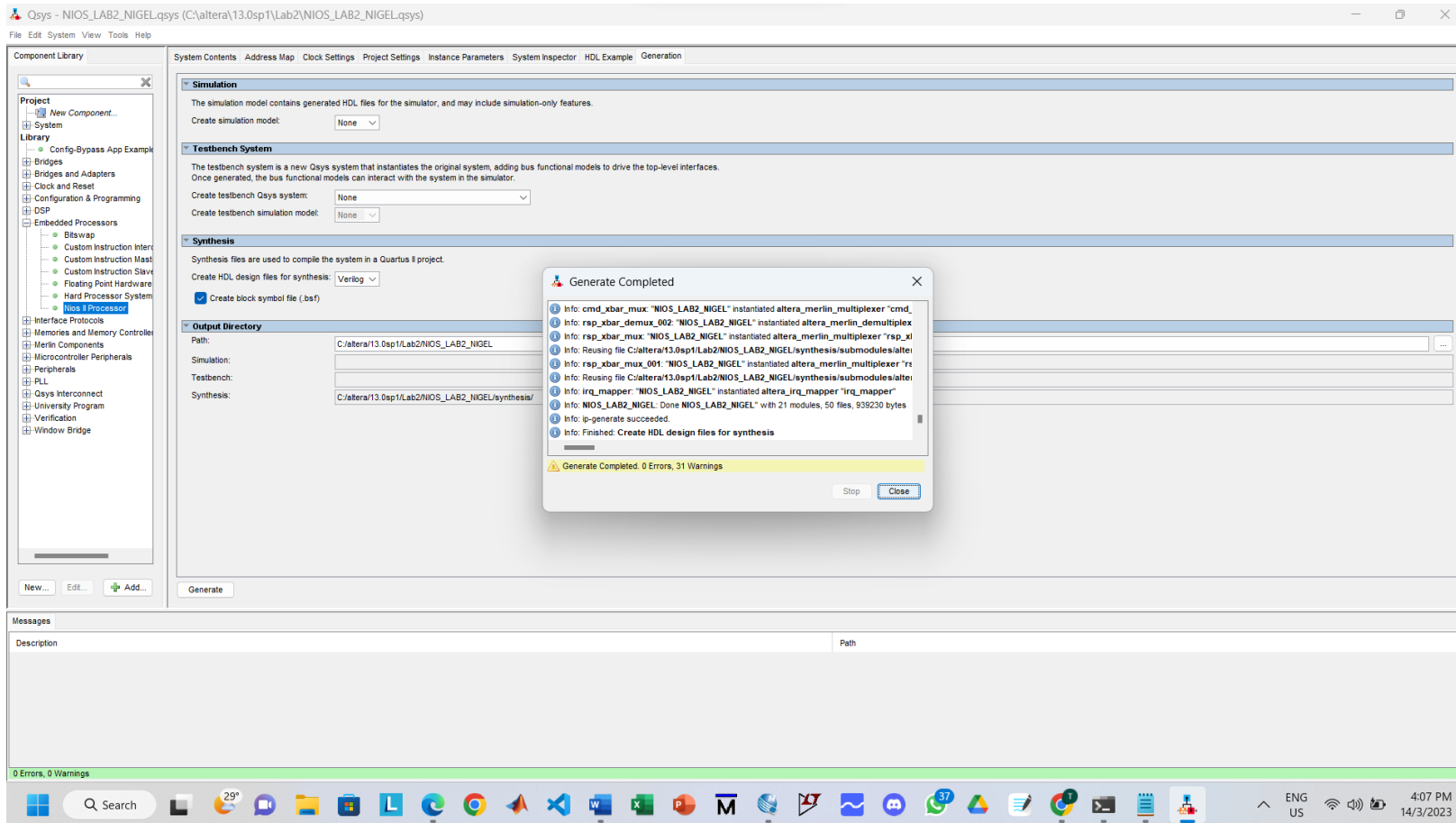
Use Connections Name Description Export Clock Base End

Use	Connections	Name	Description	Export	Clock	Base	End
✓		clk_0	Clock Source	clk	clk_0		
✓		clk_in	Clock Input	reset			
✓		clk_in_reset	Reset Input	Double-click to export			
✓		clk	Clock Output	Double-click to export			
✓		clk_reset	Reset Output	Double-click to export			
✓		nios2_qsys_0	Nios II Processor				
✓		clk	Clock Input	Double-click to export	clk_0		
✓		reset_n	Reset Input	Double-click to export	[clk]		
✓		data_master	Avalon Memory Mapped Master	Double-click to export	[clk]		IRQ 0
✓		instruction_master	Avalon Memory Mapped Master	Double-click to export	[clk]		IRQ 31
✓		jtag_debug_module_re...	Reset Output	Double-click to export	[clk]		
✓		jtag_debug_module	Avalon Memory Mapped Slave	Double-click to export	[clk]	0x1800	0x1fff
✓		custom_instruction_m...	Custom Instruction Master	Double-click to export			
✓		onchip_memory2_0	On-Chip Memory (RAM or ROM)				
✓		clk1	Clock Input	Double-click to export	clk_0		
✓		s1	Avalon Memory Mapped Slave	Double-click to export	[clk1]	0x0000	0x0fff
✓		reset1	Reset Input	Double-click to export	[clk1]		
✓		pio_0	PIO (Parallel I/O)				
✓		clk	Clock Input	Double-click to export	clk_0		
✓		reset	Reset Input	Double-click to export	[clk]		
✓		s1	Avalon Memory Mapped Slave	Double-click to export	[clk]	0x2000	0x200f
✓		external_connection	Conduit	red_ledr			

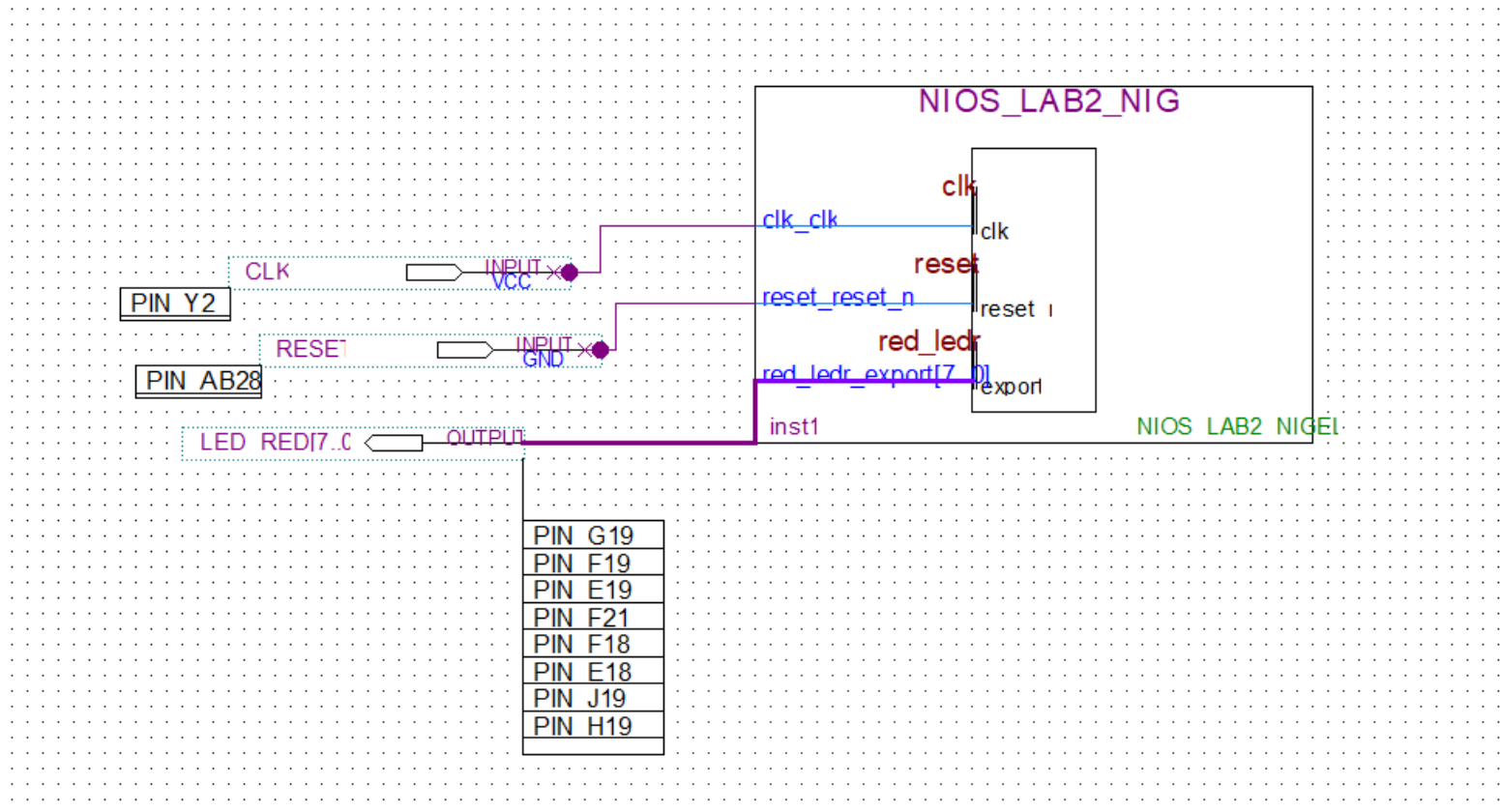
Messages

Description	Path
0 Errors, 0 Warnings	

Student ID: 32194471  
Name: Nigel Tan Jin Chun  
Date: 14/3/2023  
Lab 2, ECE3073



Student ID: 32194471  
Name: Nigel Tan Jin Chun  
Date: 14/3/2023  
Lab 2, ECE3073



Student ID: 32194471  
Name: Nigel Tan Jin Chun  
Date: 14/3/2023  
Lab 2, ECE3073

Quartus II 64-Bit - C:/altera/13.0sp1/Lab2/Lab2\_Part1\_Nigel - Lab2\_Part1\_Nigel

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Lab2\_Part1\_Nigel

Project Navigator

Files

- NIOS\_LAB2\_NIGEL.qsys
- NIOS\_LAB2\_NIGEL.cmp
- Lab2\_Part1\_Nigel.bdf

Lab2\_Part1\_Nigel.bdf

Compilation Report - Lab2\_Part1\_Nigel

Hierarchy Files Design Units

Tasks

Flow: Compilation Customize...

Task	Time
Compile Design	00:00
> Analysis & Synthesis	00:00
> Fitter (Place & Route)	00:00
> Assembler (Generate programming files)	00:00
> TimeQuest Timing Analysis	00:00
> EDA Netlist Writer	00:00
Program Device (Open Programmer)	

NIOS\_LAB2\_NIG

clk\_clk

reset\_reset\_n

red\_led

red\_ledr\_export[7]

inst1

NIOS LAB2 NIGEL

CLK

PIN Y2

RESE

PIN AB28

LED RED[7\_C]

OUTPUT

PIN G19

PIN F19

PIN E19

PIN F21

PIN F18

PIN E18

PIN J19

PIN H19

Messages

Type	ID	Message
>	332146	Worst-case minimum pulse width slack is 49.474
>	332114	Report Metastability: Found 2 synchronizer chains.
>	332102	Design is not fully constrained for setup requirements
>	332102	Design is not fully constrained for hold requirements
>		Quartus II 64-Bit TimeQuest Timing Analyzer was successful. 0 errors, 14 warnings
>	293000	Quartus II Full Compilation was successful. 0 errors, 61 warnings

System / Processing (339) /

758,464 100% 00:00:28

ENG US 4:28 PM 14/3/2023



Student ID: 32194471

Name: Nigel Tan Jin Chun

Date: 14/3/2023

Lab 2, ECE3073

# **CODE**

```
.global _start
```

```
_start:
```

```
movia r3, 0x2000
```

```
loop:  movia r4, 0xFF
```

```
        stwio r4, 0(r3)
```

```
        br loop
```

Student ID: 32194471

Name: Nigel Tan Jin Chun

Date: 14/3/2023

Lab 2, ECE3073

3. Screen shot of CPU simulator : <https://cpulator.01xz.net/?sys=nios-de2-115> showing 8 LEDs are HIGH ( 1 mark)

The screenshot displays the Nios II CPU simulator interface. The top bar is green and contains the status 'Running' and several control buttons: 'Step Into' (F2), 'Step Over' (Ctrl-F2), 'Step Out' (Shift-F2), 'Continue' (F3), 'Stop' (F4), 'Restart' (Ctrl-R), 'Reload' (Ctrl-Shift-L), 'File', and 'Help'. Below this, the interface is divided into several panels:

- Registers:** A list of registers (pc, r0-r16) with their current values. The 'pc' register is highlighted with a red background and shows the value 00000014.
- Editor (Ctrl-E):** A code editor showing assembly code. The code is as follows:

```
1 .global _start
2 _start:
3
4 movia r3, 0x10000000
5 movia r4, 0xFF
6
7 loop: stwio r4, 0(r3)
8       br loop
9
10
```
- Devices:** A panel on the right showing various hardware components:
  - LEDs:** Two rows of 8 LEDs each. The top row is labeled '10000000' and the bottom row is labeled '10000010'. Both rows show 8 red LEDs, indicating they are HIGH.
  - Switches:** A row of 17 switches labeled 17 down to 0. The 'All' checkbox is checked.
  - Push buttons:** A row of 4 buttons labeled 3 down to 0. The 'All' checkbox is checked.
  - Seven-segment displays:** A row of 8 displays labeled 7 down to 0. The 'All' checkbox is checked.
  - JTAG UART:** A section for JTAG and UART communication, showing 'Read FIFO: 0' and 'Write FIFO: 0'.
  - Interval Timer:** A section for interval timer, showing '6249999 Once Stop TO=0'.
  - VGA pixel buffer:** A section for VGA output, showing a noisy, multi-colored pixel buffer.
- Messages:** A panel at the bottom left showing compilation and linking messages. The messages indicate that the code was successfully compiled and linked into an ELF executable.

The Windows taskbar is visible at the bottom of the screen, showing the time as 11:57 AM on 14/3/2023.

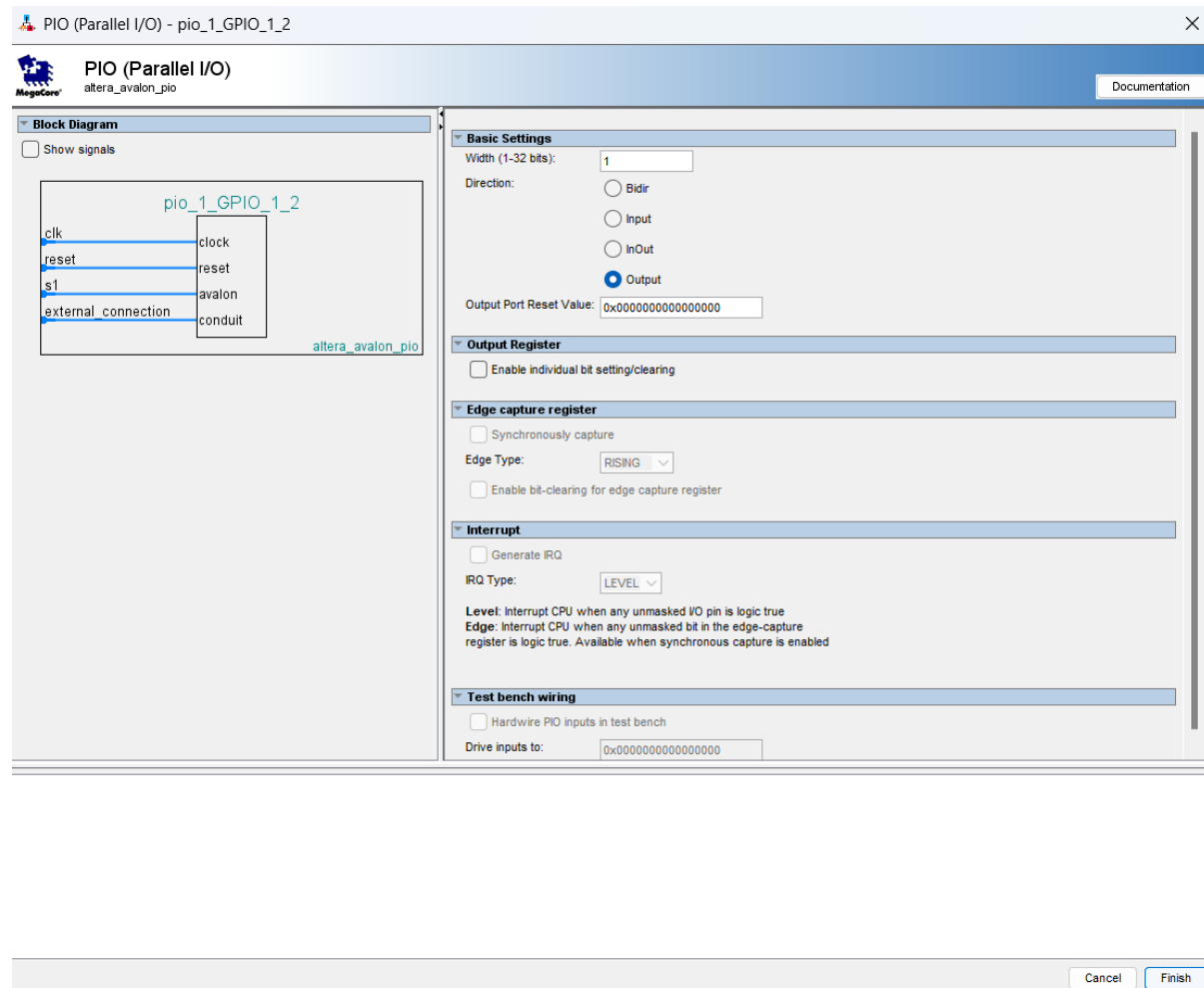
Student ID: 32194471

Name: Nigel Tan Jin Chun

Date: 14/3/2023

Lab 2, ECE3073

4. Screen shot of QSYS and Schematics that also include a 1-bit GPIO pin ( 3 marks)



Student ID: 32194471  
 Name: Nigel Tan Jin Chun  
 Date: 14/3/2023  
 Lab 2, ECE3073

Qsys - NIOS\_LAB2\_NIGEL.qsys\* (C:\altera\13.0sp1\Lab2\NIOS\_LAB2\_NIGEL.qsys)

File Edit System View Tools Help

Component Library

Library

- System
  - Config-Bypass App Exe
  - Bridges
  - Bridges and Adapters
  - Clock and Reset
  - Configuration & Programmin
  - DSP
  - Embedded Processors
    - Bitswap
    - Custom Instruction I
    - Custom Instruction I
    - Custom Instruction :
    - Floating Point Hardw
    - Hard Processor Sys
    - Nios II Processor
  - Interface Protocols
  - Memories and Memory Cont
  - Merlin Components
  - Microcontroller Peripherals
  - Peripherals
  - PLL
  - Qsys Interconnect
  - University Program
  - Verification
  - Window Bridge

New... Edit... Add...

System Contents Address Map Clock Settings Project Settings Instance Parameters System Inspector HDL Example Generation

Use	Connections	Name	Description	Export	Clock	Base	End
<input checked="" type="checkbox"/>		clk_0	Clock Source				
<input checked="" type="checkbox"/>		clk_in	Clock Input	clk	clk_0		
<input checked="" type="checkbox"/>		clk_in_reset	Reset Input	reset			
<input checked="" type="checkbox"/>		clk	Clock Output	clk	clk_0		
<input checked="" type="checkbox"/>		clk_reset	Reset Output	reset			
<input checked="" type="checkbox"/>		nios2_qsys_0	Nios II Processor				
<input checked="" type="checkbox"/>		clk	Clock Input	clk	clk_0		
<input checked="" type="checkbox"/>		reset_n	Reset Input	reset			
<input checked="" type="checkbox"/>		data_master	Avalon Memory Mapped Master	data_master	clk		
<input checked="" type="checkbox"/>		instruction_master	Avalon Memory Mapped Master	instruction_master	clk		
<input checked="" type="checkbox"/>		jtag_debug_module_re...	Reset Output	jtag_debug_module_re...	clk		
<input checked="" type="checkbox"/>		jtag_debug_module	Avalon Memory Mapped Slave	jtag_debug_module	clk		
<input checked="" type="checkbox"/>		custom_instruction_m...	Custom Instruction Master	custom_instruction_m...	clk	0x1800	0x1fff
<input checked="" type="checkbox"/>		onchip_memory2_0	On-Chip Memory (RAM or ROM)				
<input checked="" type="checkbox"/>		clk1	Clock Input	clk1	clk_0		
<input checked="" type="checkbox"/>		s1	Avalon Memory Mapped Slave	s1	clk1	0x0000	0x0fff
<input checked="" type="checkbox"/>		reset1	Reset Input	reset1			
<input checked="" type="checkbox"/>		pio_8_LED	PIO (Parallel IO)				
<input checked="" type="checkbox"/>		clk	Clock Input	clk	clk_0		
<input checked="" type="checkbox"/>		reset	Reset Input	reset			
<input checked="" type="checkbox"/>		s1	Avalon Memory Mapped Slave	s1	clk	0x2010	0x201f
<input checked="" type="checkbox"/>		external_connection	Conduit	external_connection			
<input checked="" type="checkbox"/>		pio_1_GPIO_1_2	PIO (Parallel IO)				
<input checked="" type="checkbox"/>		clk	Clock Input	clk	clk_0		
<input checked="" type="checkbox"/>		reset	Reset Input	reset			
<input checked="" type="checkbox"/>		s1	Avalon Memory Mapped Slave	s1	clk	0x2000	0x200f
<input checked="" type="checkbox"/>		external_connection	Conduit	external_connection			

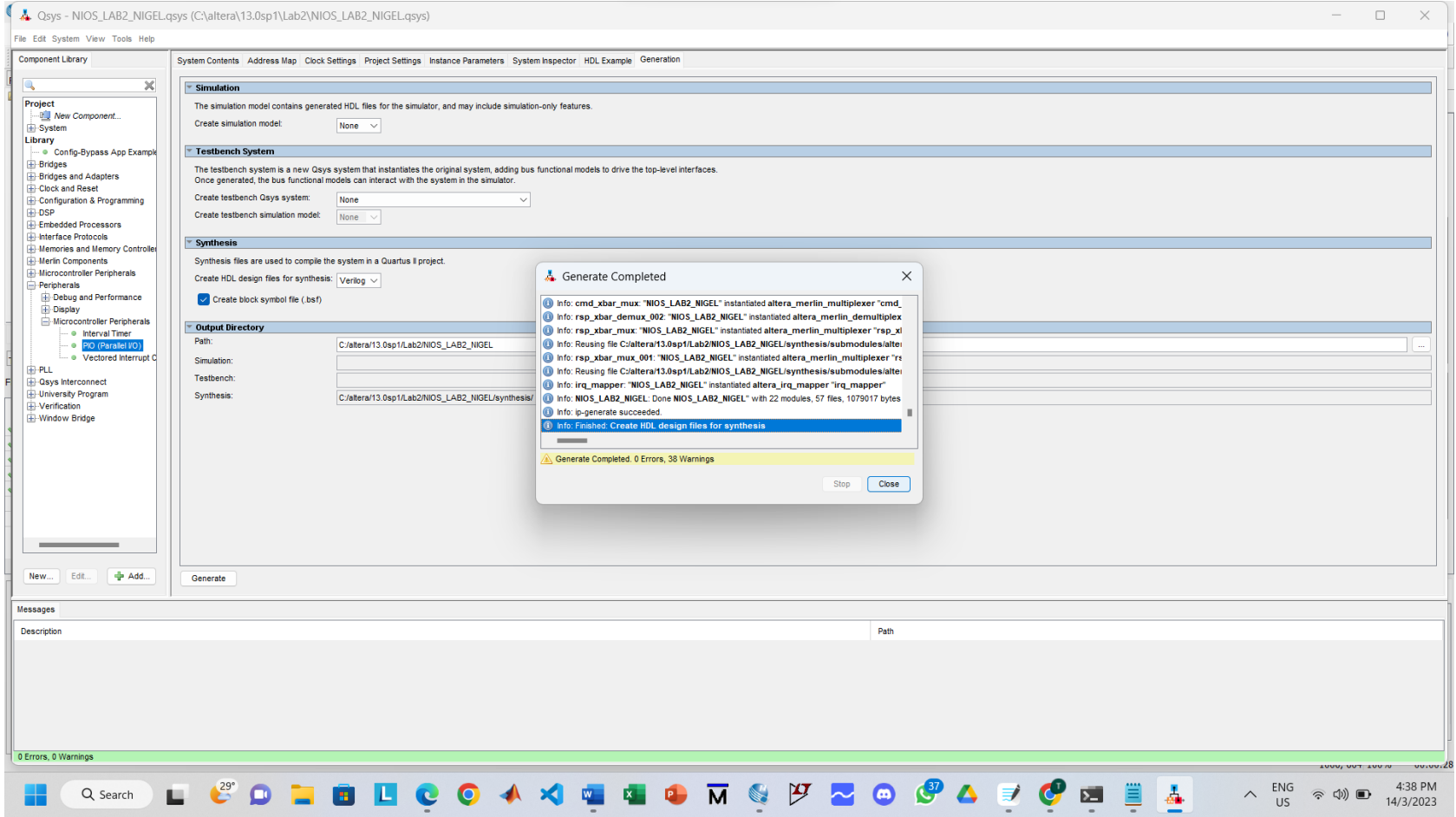
0 Errors, 0 Warnings

Student ID: 32194471

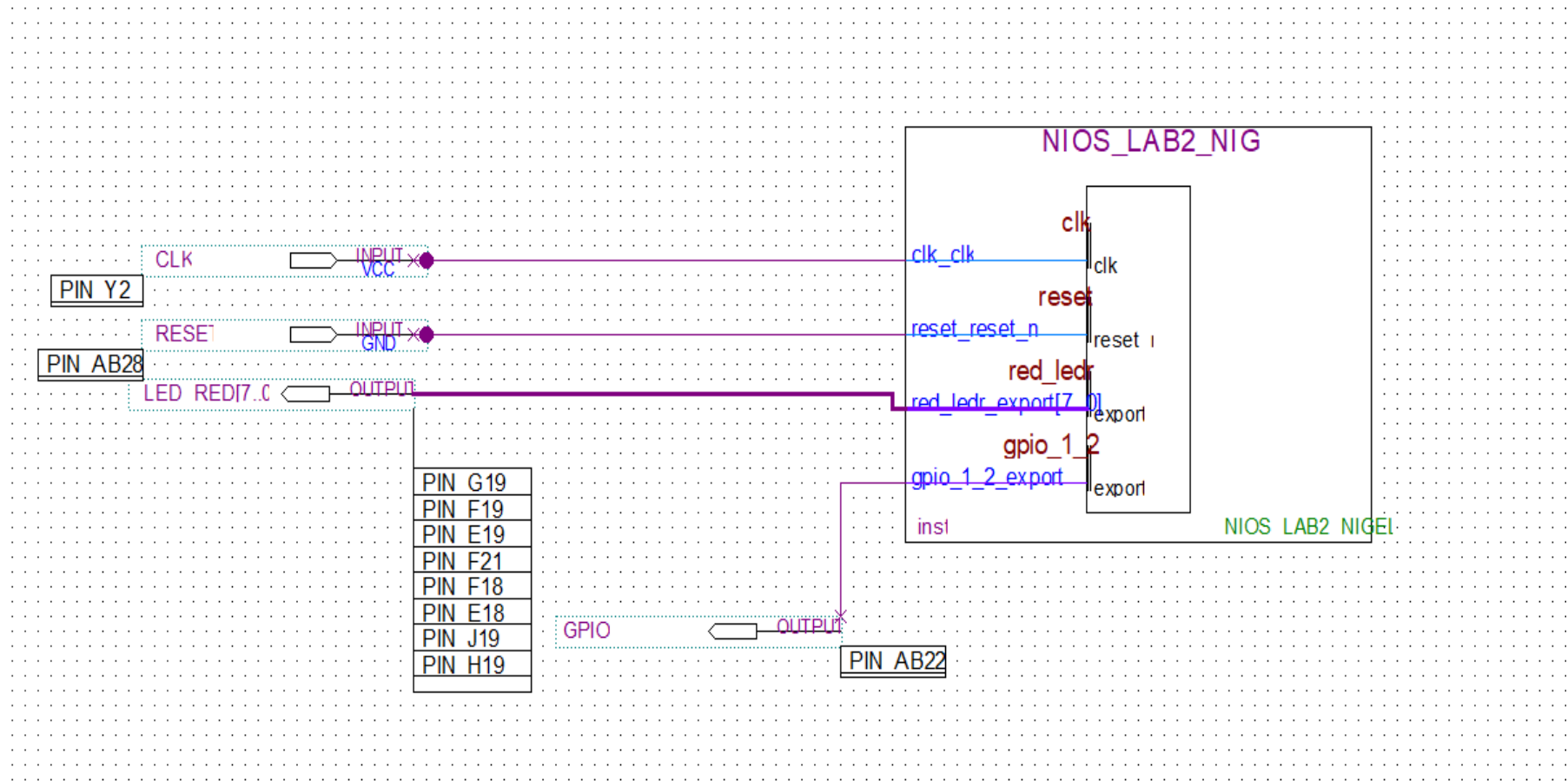
Name: Nigel Tan Jin Chun

Date: 14/3/2023

Lab 2, ECE3073



Student ID: 32194471  
Name: Nigel Tan Jin Chun  
Date: 14/3/2023  
Lab 2, ECE3073



Student ID: 32194471  
Name: Nigel Tan Jin Chun  
Date: 14/3/2023  
Lab 2, ECE3073

Quartus II 64-Bit - C:/altera/13.0sp1/Lab2/Lab2\_Part1\_Nigel - Lab2\_Part1\_Nigel

File Edit View Project Assignments Processing Tools Window Help

Lab2\_Part1\_Nigel

Project Navigator

Files

- NIOS\_LAB2\_NIGEL.qsys
- NIOS\_LAB2\_NIGEL.cmp
- Lab2\_Part1\_Nigel.bdf

Hierarchy Files Design Units

Tasks

Flow: Compilation Customize...

Task	Time
Compile Design	00:00
Analysis & Synthesis	00:00
Fitter (Place & Route)	00:00
Assembler (Generate programming files)	00:00
TimeQuest Timing Analysis	00:00
EDA Netlist Writer	00:00
Program Device (Open Programmer)	

Messages

Type ID Message

- 332146 Worst-case minimum pulse width slack is 49.473
- 332114 Report Metastability: Found 2 synchronizer chains.
- 332102 Design is not fully constrained for setup requirements
- 332102 Design is not fully constrained for hold requirements
- Quartus II 64-Bit TimeQuest Timing Analyzer was successful. 0 errors, 14 warnings
- 293000 Quartus II Full Compilation was successful. 0 errors, 71 warnings

System Processing (356)

727,598 100% 00:00:43

ENG US 4:56 PM 14/3/2023

Student ID: 32194471  
Name: Nigel Tan Jin Chun  
Date: 14/3/2023  
Lab 2, ECE3073

5. The assembly code that makes GPIO pin ON and immediately next instruction as OFF, such that by connecting GPIO pin to oscilloscope one can measure execution time. (2 marks)

**CODE**

```
.global _start
_start:

# r5 is set to the GPIO Base Address and r6 is set to be the value of GPIO
movia r5, 0x2000
movia r6, 0x01

# Loop to turn on and off the GPIO
loop:  stwio r6, 0(r5) # Turn on the GPIO
      stwio r0, 0(r5) # Turn off the GPIO
      br loop
```



Student ID: 32194471  
Name: Nigel Tan Jin Chun  
Date: 14/3/2023  
Lab 2, ECE3073

6. Complete the assembly codes to solve section f questions in Lab 2 sheet. Execution time of r, j type and l type (3 marks)

**CODE**

```
global _start
_start:

# initializing the base addresses of the PIO's
# register r3 is the LED base address, r4 is the flag bit base address, r5 stores the address of the LED Pattern
movia r3, 0x2010
movia r4, 0x2000
movia r5, 0x01
movia r6, 0x33
ldw r7, 0(r6)

# Looping
loop:
    stwio r7, 0(r3) # write to red LEDs
    stwio r5, 0(r4) # flag goes high
    stwio r0, 0(r4) # flag goes low
br loop
```

Student ID: 32194471  
Name: Nigel Tan Jin Chun  
Date: 14/3/2023  
Lab 2, ECE3073

7. Theoretically estimate the execution time of a R –type, J Type, I- Type ( 4 marks)

Type of instruction and example	Execution time and number of cycles of cpu
R – Type instruction ( Ex: add r8,r9,r10)	$1/50\text{MHz} = 20\text{ns}$ , $20\text{ns}/\text{cycle} * 6 \text{ cycle} = 120\text{ns}$ and 6 cycles of CPU
I Type instruction ( andi ...)	$1/50\text{MHz} = 20\text{ns}$ , $20\text{ns}/\text{cycle} * 6 \text{ cycle} = 120\text{ns}$ and 6 cycles of CPU
J – Type instruction(jmp or call)	$1/50\text{MHz} = 20\text{ns}$ , $20\text{ns}/\text{cycle} * 6 \text{ cycle} = 120\text{ns}$ and 6 cycles of CPU

To solve this question, you need to refer the instruction set manual, pls refer polling lecture video 😊

8. Practically measure the execution time using Altera University Program and Oscilloscope in the Lab ( Not Remote Lab)

Type of instruction and example	Execution time and number of cycles of cpu
R – Type instruction ( Ex: add r8,r9,r10)	
I Type instruction ( andi ...)	
J – Type instruction(jmp or call)	