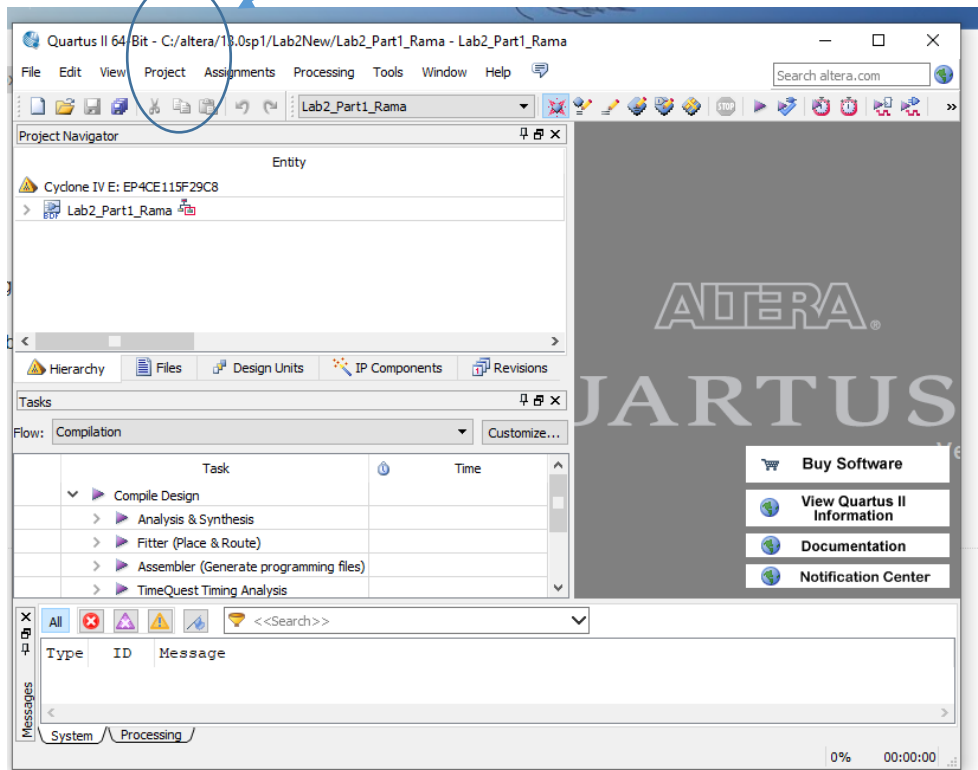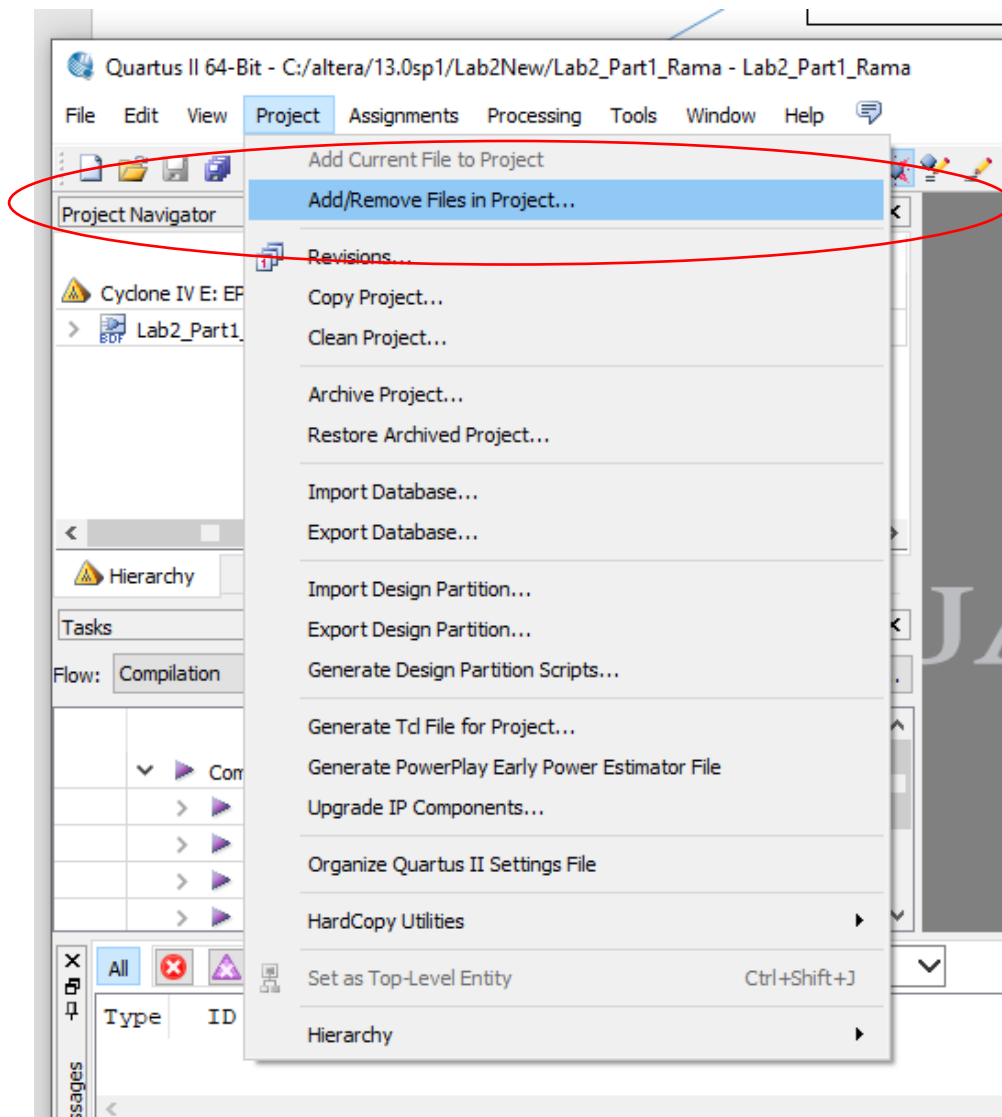1

Click add all to ensure two files with extension .qsys and .cmp are included.

Settings - Lab2_Part1_Rama

Category:

- General
- **Files**
- Libraries
- ∨ Operating Settings and Conditions
  - Voltage
  - Temperature
- ∨ Compilation Process Settings
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  - Incremental Compilation
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- TimeQuest Timing Analyzer
- Assembler
- Design Assistant
- SignalTap II Logic Analyzer
- Logic Analyzer Interface
- PowerPlay Power Analyzer Settings
- SSN Analyzer

Device...

Files

Select the design files you want to include in the project. Click Add All to add all design files in the project directory to the project.

File name: [   ] [...] Add

File Name	Type	Library	Design Entry/Synthesis Tool	H
NIOS_LAB2_RAMA.qsys	Qsys System File		<None>	
NIOS_LAB2_RAMA.cmp	Other		<None>	
Lab2_Part1_Rama.bdf	Block Diagram/Schematic File		<None>	

Add All
Remove
Up
Down
Properties

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